A Cross-Coupled Master–Slave Interleaving Method for Boundary Conduction Mode (BCM) PFC Converters

Hangseok Choi, *Senior Member, IEEE*, and Laszlo Balogh, *Member, IEEE*

***Abstract*—This paper proposes a cross-coupled master–slave interleaving control method for boundary conduction mode (BCM) power factor correction (PFC) converters. The natural period of every switching cycle of each channel is measured and compared to adaptively determine the master and slave converters, where a converter with a longer natural period becomes master operating in BCM, while a converter with a shorter natural period becomes slave operating in discontinuous conduction mode. The proposed method compensates disturbances within one switching cycle, guaranteeing stable 180° out-of-phase interleaving operation against any transient and disturbance. The proposed method has been implemented and tested on a 400 W interleaved BCM boost PFC prototype converter with a dedicated control IC.**

***Index Terms*—Interleaved boost, power factor correction (PFC), variable frequency.**

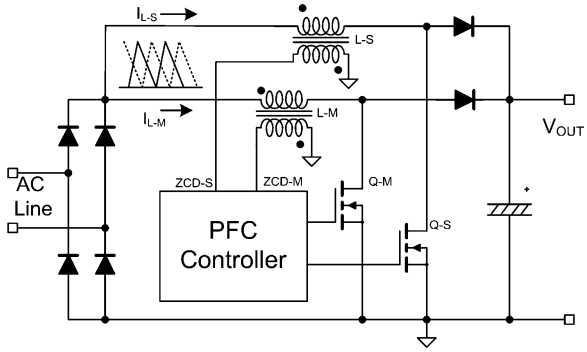

Fig. 1. Simplified circuit diagram of interleaved BCM boost PFC.

I. Introduction

THE boundary conduction mode (BCM) boost power factor correction (PFC) converter has been the most attractive topology for low-power levels because it can achieve better efficiency with lower cost than continuous conduction mode (CCM) boost PFC converter [1]–[3]. These benefits result from the elimination of the reverse-recovery losses of the boost diode and zero-voltage switching (ZVS) or near ZVS (also called valley switching) of boost switch. However, a BCM approach exhibits a relatively large peak inductor current which is twice of its average value and inevitably requires a larger differential mode electromagnetic interference (EMI) filter in the input side than that of a CCM approach. This offsets the benefits of the BCM approach and the applicable practical power level has been limited below 300 W. Another shortcoming of BCM operation is that its switching frequency varies with the instantaneous line voltage and output load condition. The switching frequency becomes extremely high especially for high-line and light-load condition, which deteriorates the efficiency severely in that condition.

Recently, interleaved BCM PFC circuits as illustrated in Fig. 1 have become more popular because of their ability to reduce the input current ripple and, consequently, the size of EMI filter extending their applicable practical power level above 300 W [4]–[20]. In addition, the output current ripple can also be significantly reduced by the ripple cancellation of interleaving, which allows longer life time of the output capacitor. Another benefit of the interleaved approach is that the light load efficiency can be improved by shutting down one channel of the interleaved converters at light-load condition, which is known as phase management. By shutting down one channel, the power that the other channel should handle becomes twice making the switching frequency half. This technique is very effective in improving the light load efficiency at high-line condition.

Interleaving technique itself has been widely used for constant frequency operation where the interleaving is relatively easy to implement since the turn-on instant is predetermined by the fixed switching frequency [20]–[23]. However, the interleaving BCM PFC is challenging since the switching frequency continuously varies with the instantaneous line voltage and output load condition. Especially, the startup and the operation around the line zero crossing are the most challenging conditions for interleaving because of the abrupt change of the switching frequency of each channel during transient.

In general, the interleaving techniques can be classified into two categories: open-loop master–slave method [4]–[10] and phase-locked loop (PLL)-based closed-loop method [11]–[16]. In the open-loop master–slave method [4]–[10], the master converter runs in standalone BCM, whereas the slave converter is phase shifted by a time delay equal to half of the switching

Manuscript received November 8, 2011; revised January 10, 2012 and January 17, 2012; accepted March 3, 2012. Date of current version May 31, 2012. This paper is an extended version of "Novel adaptive master–slave method for interleaved boundary conduction mode (BCM) PFC converters" presented at the IEEE Application Power Electronics Conference 2010. Recommended for publication by Associate Editor K. Ngo.

The authors are with the Power Conversion Group, Fairchild semiconductor, Bedford, NH 03110 USA (e-mail: hangseok.choi@fairchildsemi.com; laszlo.balogh@fairchildsemi.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2012.2190426

period of the master determined from its previous switching cycle. The half-switching cycle phase shift (PS) can be applied to the turn-on instant or turn-off instant. For both cases, either voltage mode control or current mode control can be applied. Since this method is based on the assumption that the master and slave converters are identical, it has a difficulty in guaranteeing stable BCM operation for both converters against mismatch of components and switching timing. A complete analysis of the behavior of the open-loop master–slave interleaving method has been presented in [8], which shows that among the open-loop interleaving methods, only the current mode control with a PS applied to the turn-on instant can provide stable operation against disturbance.

The closed-loop method measures the phase difference between the two converters and adjusts the phase difference by using a PLL approach [11]–[16]. For BCM operation, changing the ON-time of the boost switch also changes the switching period and the phase difference between two converters. This method can guarantee BCM operation for both channels regardless of the mismatch of components and switching timing. The dynamic behavior of closed-loop method has been well analyzed in [16]. Since a low-pass filtering is required to obtain the phase difference, the closed-loop method responds to the PS disturbance relatively slowly and it takes several tens of switching cycles to correct the disturbance. Another limitation of the closed-loop method is that it works only when both channels are in BCM, where the change of the ON-time results in the change of switching period. Once BCM is lost and the converter runs with its minimum frequency, which always occurs during startup of boost converter, the interleaving is lost and the PLL circuit causes severe current imbalance between the two converters. Same problem occurs when the switch of one channel is prematurely turned OFF by pulse-by-pulse current limit due to the mismatch of the sensing resistor or inductor.

In this paper, a cross-coupled master–slave method for interleaved BCM PFC converters is presented [18], [19]. The natural period of every switching cycle of each converter is measured and compared, which adaptively determines which converter should be a master converter. This method can be applied to either voltage mode or current mode control. Especially for voltage mode control, the proposed method can solve the problem of the open-loop master–slave method with a voltage mode control discussed in [8]. The proposed method can also solve the current imbalance problem of the closed-loop PLL method in CCM during startup or mismatched pulse-by-pulse current limit. The proposed method responds to the PS disturbance very fast and synchronization is achieved within one switching cycle, guaranteeing a stable interleaving operation during any transient and disturbance. The proposed scheme was implemented with a dedicated control IC and verified on a 400 W interleaved BCM boost PFC prototype converter.

II. Review of an Open-Loop Master–Slave Method

Fig. 2 shows the circuit diagram of the conventional open-loop master–slave interleaving method with a voltage mode and turn-on instant synchronization. To obtain the inductor current zero crossing detection (ZCD) signal, the auxiliary winding of an inductor is used as illustrated in Fig. 1. For an open-loop master–slave method, the ZCD signal for the slave is generally not used. The turn-on instant of master channel is determined by its own ZCD signal, which allows the master to operate in standalone BCM, whereas the turn-on instant of slave channel is determined by the PS signal, which is shifted from the turn-on instant of master by a time delay equal to half the switching period of the master determined from its previous switching cycle. The turn-off instants of master and slave are determined by their own pulsewidth modulation (PWM) comparators. The two PWM comparators share the error amplifier output voltage $V_{\rm EA}$ for their inverting inputs such that the ON-times should be same for both channels. The advantage of voltage mode method is that its BCM operation is not perturbed by the mismatch of boost inductors of master and slave. However, once the ON-time or turn-on instant of slave converter is perturbed such that the ON-time is increased or turn-on instant is delayed, the slave enters into CCM operation as shown in Figs. 3 and 4, respectively. Once the slave enters into CCM, it is not recovered to BCM operation even after the perturbation is removed. In the opposite cases, when the perturbed ON-time is shorter than the unperturbed ON-time and when the perturbed turn-on instant takes place earlier than the unperturbed turn-on instant, it returns to the normal BCM operation after the perturbation is removed. From a control circuit point of view, the perturbation of ON-time can easily occur by the switching noise on the error amplifier output voltage $V_{\rm EA}$ as shown in Fig. 3. And the mismatch between the two timing capacitors $C_{\rm TM}$ and $C_{\rm TS}$ in Fig. 2 can easily result in the mismatch of ON-times of master and slave. The PS signal can also be disturbed by the switching noise. Since the perturbation of ON-time and turn-on instant can cause CCM operation deteriorating the power factor, open-loop master–slave method itself is difficult to be used for actual application.

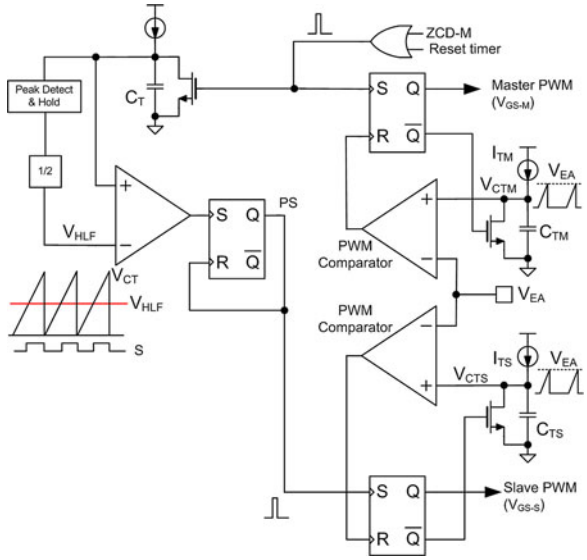

Fig. 2. Circuit diagram of the open-loop master–slave method with voltage mode and turn-on instant synchronization.

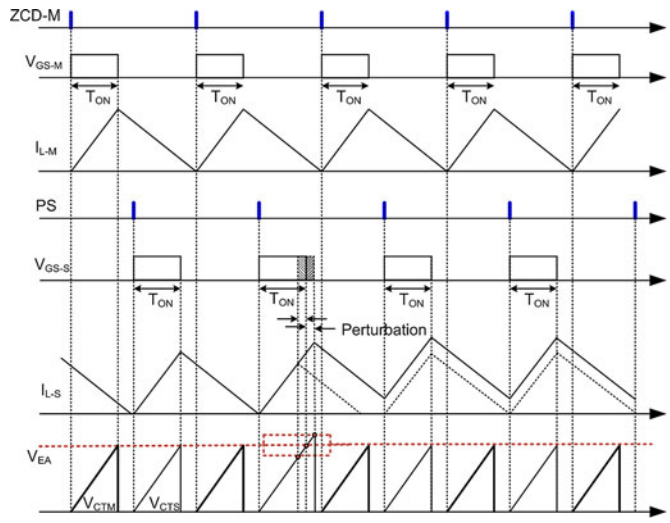

Fig. 3. Effect of ON-time perturbation on the open-loop master–slave method with voltage mode and turn-on instant synchronization.

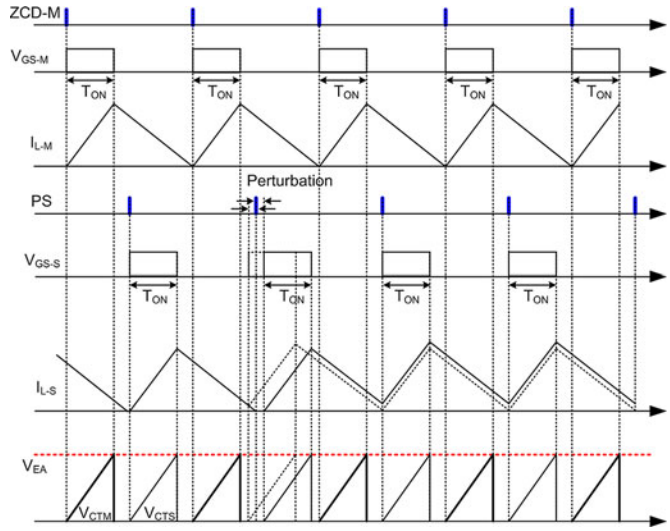

Fig. 4. Effect of turn-on instant perturbation on the open-loop master–slave method with voltage mode and turn-on instant synchronization.

III. Review of a Closed-Loop PLL Method

Fig. 5 shows the circuit diagram of the closed-loop PLL interleaving method. The phase angle between master and slave is obtained by averaging the output of a positive edge-triggered SR flip-flop which is set by the master gate drive signal and reset by the slave gate drive signal. The phase angle $\phi_{\rm PM}$ between master and slave is given as

$$\phi_{\rm PM} = \frac{V_{\rm AVG}}{V_{\rm DD}} \cdot 360^{\rm o} \tag{1}$$

where $V_{\rm AGV}$ is the output of the low-pass filter and $V_{\rm DD}$ is the supply voltage of the flip-flop.

The phase angle is 180° when the duty cycle of the output of SR flip-flop is 50%, which causes $V_{\rm AVG}$ to be half of $V_{\rm DD}$. The basic idea of the PLL method is that the change of ON-time results in the change of phase angle in BCM operation. The PLL circuit adjusts the ON-time of slave by changing the charging current of timing capacitor to maintain 180^o phase angle. Adjusting the charging current of timing capacitor can also be applied to both master and slave, which is called democratic method [15], [16]. The closed-loop PLL method guarantees BCM operation for both master and slave regardless of the mismatches of ON-times and power stage components. However, the closed-loop method cannot change the phase angle in a constant frequency operation. For most of BCM PFC controllers, internal reset timers are typically used to trigger PWM signal when ZCD signal is missing. When the output voltage is too close to the input voltage during startup, there is not enough voltage across the inductor to discharge the inductor current while the boost switch is turned OFF. Then, the ZCD signal is lost and the converter operates in CCM with a constant switching frequency determined by the reset timer, where the closed-loop PLL method cannot change the phase angle by changing the ON-time. Another problem is that a runaway of slave inductor current occurs in CCM as shown in Fig. 6. When the phase angle between the master and slave is less than 180°, the PLL circuit increases the ON-time of slave to increase the phase angle. However, this just increases the inductor current of slave without changing the phase angle. In actual application, the current runaway often results in the damage of the boost diode combined with its severe reverse-recovery current. To prevent the inductor current runaway, special synchronization circuit is required for the closed-loop PLL method.

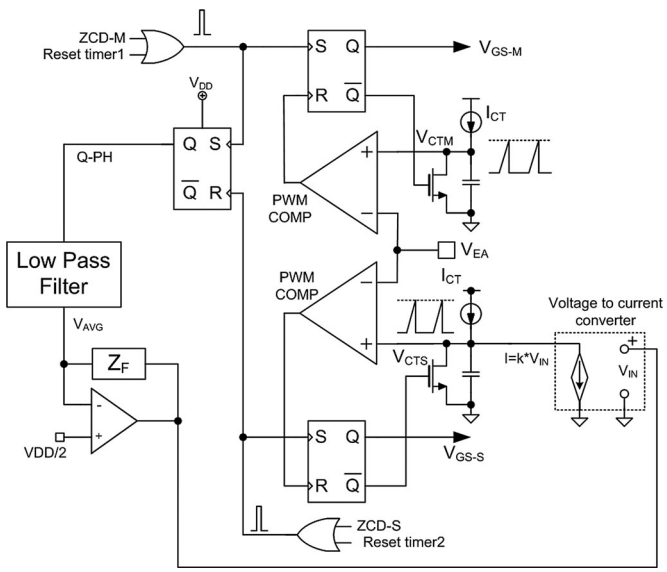

Fig. 5. Circuit diagram of the closed-loop PLL method with a turn-on instant synchronization.

IV. Operation Principle of the Proposed Method

Fig. 7 shows the simplified block diagram of the proposed interleaving method. For every switching cycle, the natural period is measured, which is defined as the time duration from the turn-on instant to the zero current detection (ZCD). Using the natural period of previous cycle, the PS signals (PS1 and PS2) that are delayed by half of the natural period of the previous

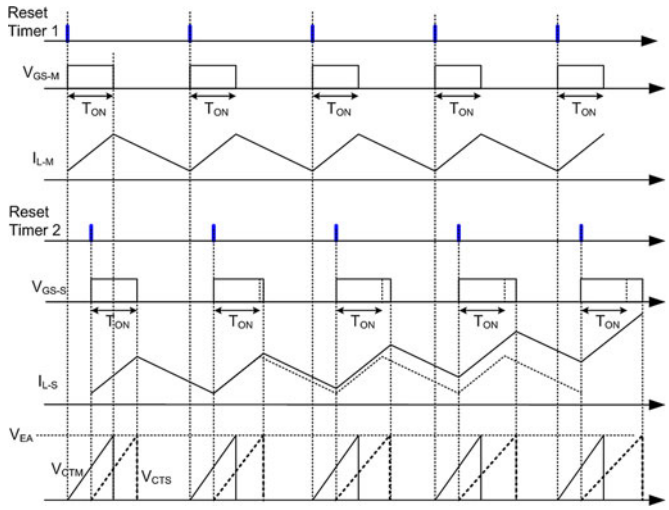

Fig. 6. Inductor current runaway in CCM operation of a closed-loop PLL method.

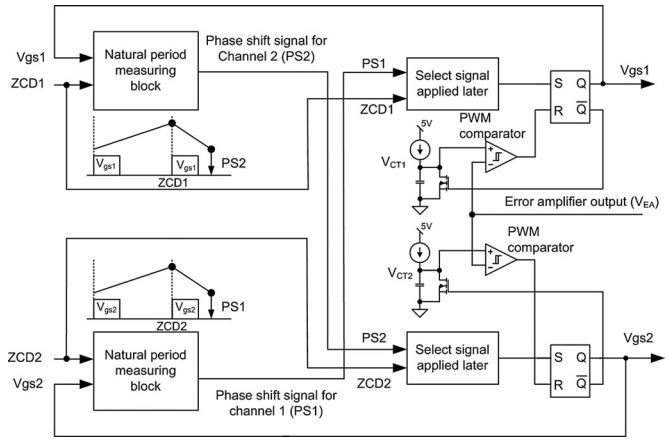

Fig. 7. Simplified block diagram of the proposed interleaving method.

cycle with respect to the turn-on instant are provided to other channels. Among ZCD signal and PS signal, the signal applied later determines the turn-on instant of boost switch. Meanwhile, the turn-off instants of master and slave are determined by their own PWM comparators. The two PWM comparators share the error amplifier output voltage $V_{\rm EA}$ for their inverting inputs such that the ON-times can be same for both channels. In the conventional open-loop master–slave method, the master and slave are predetermined. However, in the proposed method, any channel can be master or slave depending on which signal is introduced later among PS signal and ZCD signal. When the ZCD signal is introduced later than the PS signal, the converter operates in BCM (master) triggered by its own ZCD signal. When the PS signal is applied later than its own ZCD signal, the converter operates in discontinuous conduction mode (DCM) (slave).

To simplify the analysis of the proposed circuit operation, it is assumed that the two converters are identical, which allows perfect BCM operation with 180° out of phase when the perturbation is not introduced. Fig. 8 shows how the proposed scheme responds to the perturbation (increase of ON-time). Before the perturbation is introduced, ZCD2(n) and PS2(n) occur simultaneously, being delayed from ZCD1(n) by half of natural period as

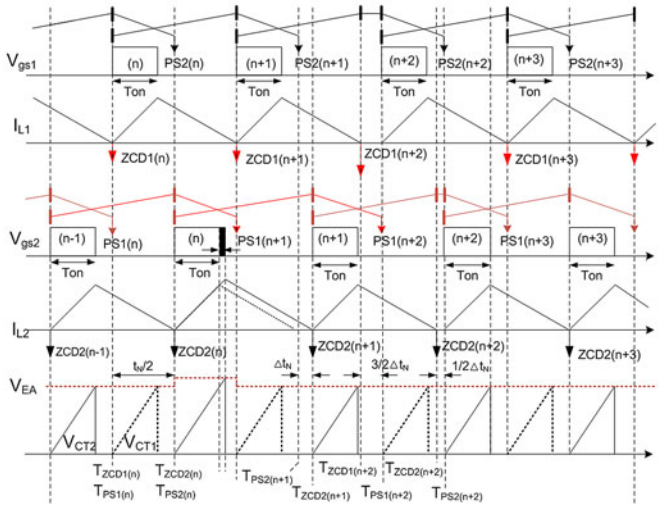

Fig. 8. Effect of ON-time perturbation on the proposed interleaving operation (ON time increase).

$$T_{\rm ZCD2(n)} = T_{\rm PS2(n)} = T_{\rm ZCD1(n)} + \frac{t_N}{2} \tag{2}$$

where t_N is the unperturbed natural period.

For the nth gate drive signal of channel 2, the ON-time is increased by the perturbation on the error amplifier output voltage $V_{\rm EA}$. Then, the natural period of channel 2 in the nth switching cycle is larger than the unperturbed natural period by Δt_N causing the ZCD2(n+1) to occur later than PS2(n+1) as

$$T_{\rm ZCD2(n+1)} = T_{\rm PS2(n+1)} + \Delta t_N. \tag{3}$$

Then, channel 2 is turned ON by ZCD2(n+1) and maintains its BCM operation. Since the natural period of channel 2 is increased by Δt_N, PS1(n+2) occurs later than ZCD1(n+2) as

$$T_{\rm PS1(n+2)} = T_{\rm ZCD1(n+2)} + \frac{3}{2}\Delta t_N \tag{4}$$

where $3/2{\cdot}\Delta t_N$ is caused by the increased natural period Δt_N and the PS signal that is delayed by half of the increased natural period $(1/2{\cdot}\Delta t_N)$.

Then, channel 1 is turned ON by PS1(n+2) signal and operates in DCM.

After the perturbation is removed, the natural period is reduced to the unperturbed natural period. Then, ZCD2(n+2) occurs at

$$T_{\rm ZCD2(n+2)} = T_{\rm ZCD2(n+1)} + t_N = T_{\rm PS2(n+1)} + \Delta t_N + t_N \tag{5}$$

while PS2(n+2) occurs at

$$T_{\rm PS2(n+2)} = T_{\rm PS1(n+2)} + \frac{t_N}{2} = T_{\rm ZCD1(n+1)} + \frac{3}{2}\Delta t_N + \frac{t_N}{2}. \tag{6}$$

Combining (2), (5), and (6) yields

$$T_{\rm PS2(n+2)} = T_{\rm ZCD2(n+2)} + \frac{1}{2}\Delta t_N. \tag{7}$$

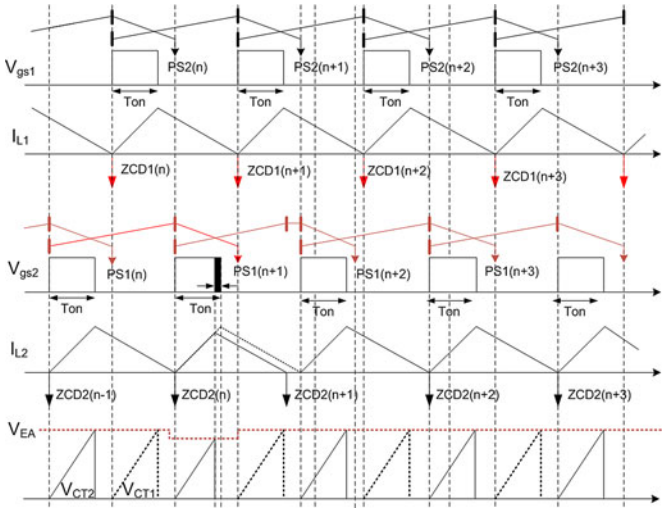

Fig. 9. Effect of ON-time perturbation on the proposed interleaving operation (ON time decrease).

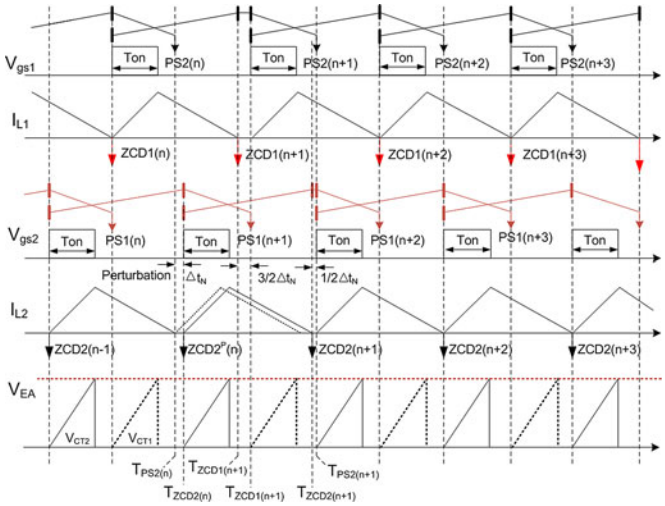

Fig. 10. Effect of turn-on instant perturbation on the proposed interleaving operation (ZCD later).

It can be seen that the $(n+2)$th turn-on of channel 2 is delayed by $1/2{\cdot}\Delta t_N$ compensating the perturbation perfectly. After the transition, the interleaved BCM operation is recovered.

Fig. 9 shows how the proposed control method responds to the decrease of ON-time by the perturbation introduced to V_{EA}. The perturbation makes the natural period of channel 2 smaller than the unperturbed natural period, forcing ZCD2$(n+1)$ to occur earlier than PS2$(n+1)$. This forces channel 2 to operate in DCM and PS1$(n+2)$ to occur earlier than ZCD1$(n+2)$. Since channel 1 is triggered by ZCD1$(n+2)$ that occurs later, the BCM operation of channel 1 is not disturbed. Channel 2 also returns to BCM operation after perturbation is removed.

Figs. 10 and 11 show how the proposed method operates when the turn-on instant is perturbed and delayed. The delayed turn-on can be caused by the disturbance of PS signal or ZCD signal.

The turn-on instant is perturbed by $\mathrm{ZCD2}^P(n)$ in Fig. 10 where $\mathrm{ZCD2}^P(n)$ is delayed by Δt_N . Since $\mathrm{ZCD2}^P(n)$ occurs

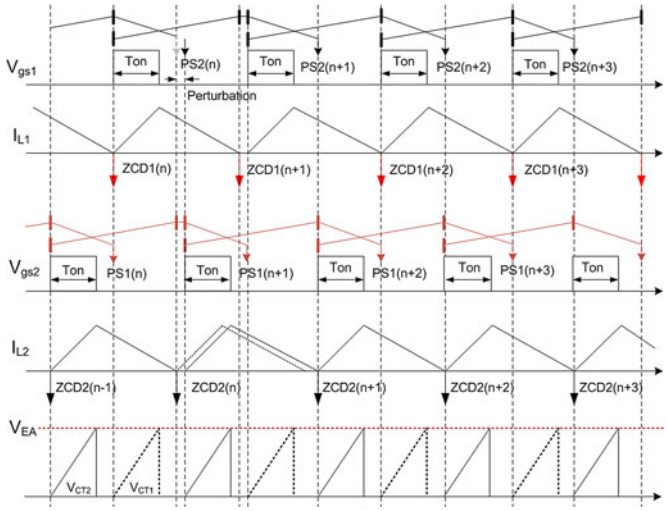

Fig. 11. Effect of turn-on instant perturbation on the proposed interleaving operation (PS occurs later).

later than PS2(n), the turn-on instant of channel 2 for the nth switching cycle is given as

$$T_{\mathrm{ZCD2}(n)} = T_{\mathrm{PS2}(n)} + \Delta t_N. \tag{8}$$

Since $\mathrm{ZCD2}^P(n)$ is delayed by Δt_N, the natural period of channel 2 is also increased by Δt_N. Then, the turn-on instant of channel 1 for the $(n+1)$th cycle is delayed by $3/2{\cdot}\Delta t_N$ as

$$T_{\mathrm{PS1}(n+1)} = T_{\mathrm{ZCD1}(n+1)} + \frac{3}{2}\Delta t_N \tag{9}$$

where $3/2{\cdot}\Delta t_N$ is caused by the increased natural period Δt_N and the PS signal that is delayed by half of the perturbation $(1/2{\cdot}\Delta t_N)$.

After the perturbation is removed, the natural period of channel 2 is reduced to the unperturbed natural period. Then, the turn-on instant of channel 2 for $(n+1)$th cycle is given as

$$T_{\mathrm{PS2}(n+1)} = T_{\mathrm{ZCD2}(n+1)} + \frac{1}{2}\Delta t_N. \tag{10}$$

This compensates the perturbation perfectly and the BCM operation with interleaving is recovered after the transition.

The turn-on instant is perturbed by PS2(n) in Fig. 11 where PS2(n) is delayed by Δt_N. Since the disturbance of PS signal does not affect the natural period of any channel, the perturbation just introduces turn-on delay for both channels and the interleaving is recovered after the perturbation is removed.

Fig. 12 shows how the proposed control scheme operates when the ZCD occurs earlier by perturbation. As can be seen, the perturbation does not disturb the interleaving operation since only the signal that occurs later among PS signal and ZCD signal determines the turn-on instant. In the same way, the system is not disturbed when the PS signal occurs earlier as well.

Fig. 13 shows the circuit diagram of the proposed method. The block to detect the signal occurring later among phase signal and ZCD signal is implemented using three edge-triggered SR flip-flops and one AND gate. A natural period detection circuit is implemented using sample and hold circuit.

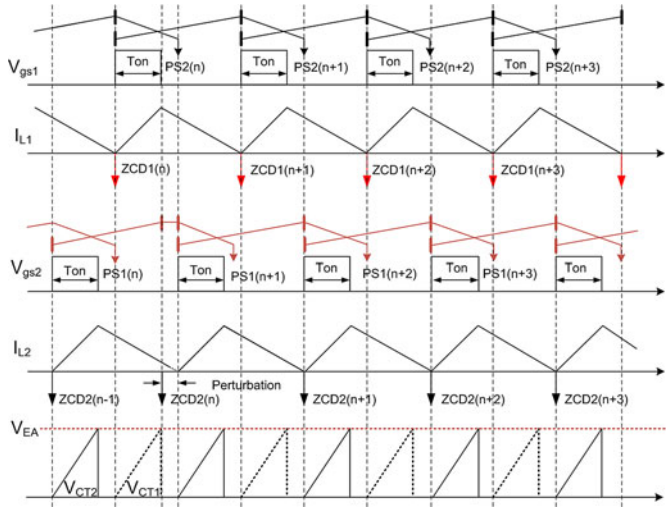

Fig. 12. Effect of ZCD instant perturbation on the proposed interleaving operation (ZCD occurs earlier).

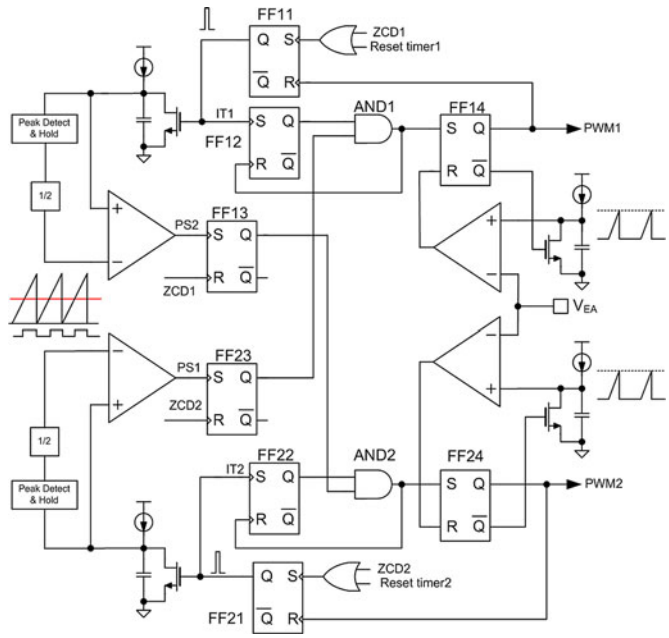

Fig. 13. Circuit diagram of the proposed interleaving method.

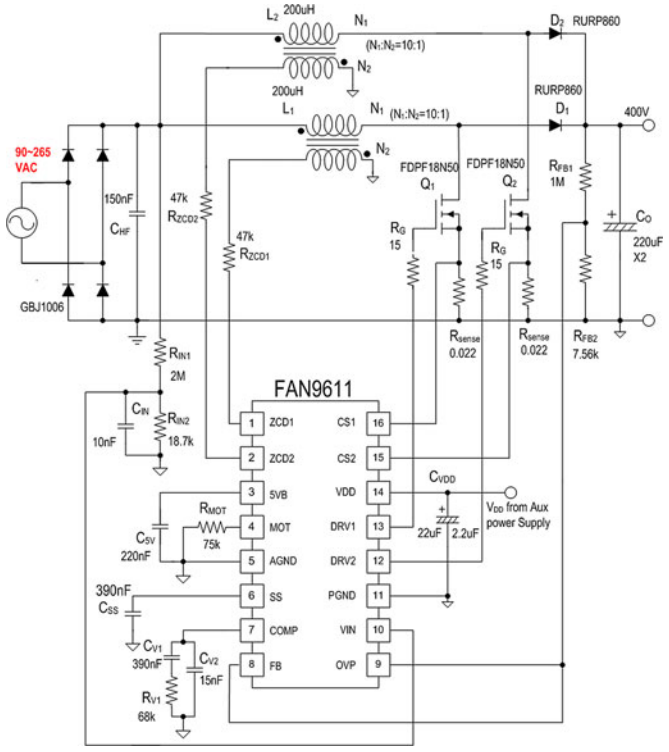

Fig. 14. Schematic of 400 W interleaved BCM boost PFC converter with a proposed interleaving method.

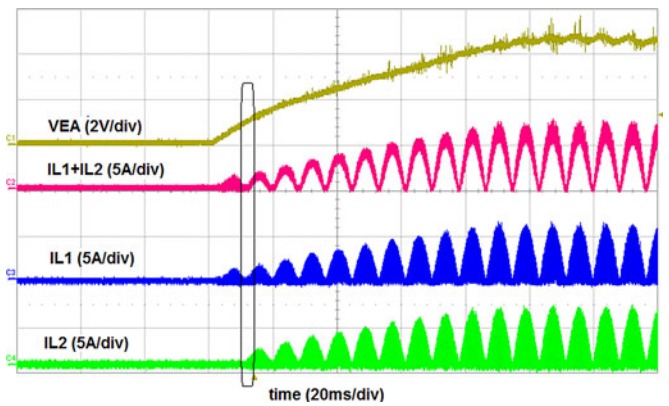

Fig. 15. Waveforms of the proposed method for load transient (115 V_{ac}, 0 W→400 W).

V. Experimental Results

In order to show the validity of the proposed control method, an interleaved BCM boost PFC prototype converter has been built as shown in Fig. 14. The proposed interleaving method has been implemented in an IC with 16 pins in small-outline integrated circuit (SOIC) package. The control IC (FAN9611) has two pins to detect the zero crossing instant of inductor current. The minimum switching frequency determined by an internal reset timer is set as 16.5 kHz to avoid audible noise. Since the switching frequency tends to be extremely high to maintain BCM at light-load condition, the maximum switching frequency is limited by the controller at 525 kHz. To improve the light load efficiency, phase management is also included in the control IC which sheds one channel at light-load condition.

Figs. 15 and 16 show the waveforms of the proposed control method when output load changes from no load to full load at low-line condition. Once the load is applied, the error amplifier output voltage $V_{\rm EA}$ rises enabling the gate drive signal of $Q1$ first. When the error amplifier output voltage increases more, the gate drive signal of $Q2$ is recovered from the phase management operation. As can be seen in the zoomed waveform in Fig. 16, the phase management introduces perturbation to the ON time of the gate drive signal of $Q1$ since the ON time is halved before the gate drive signal for $Q2$ is recovered from phase management. The proposed method maintains the interleaving from the very

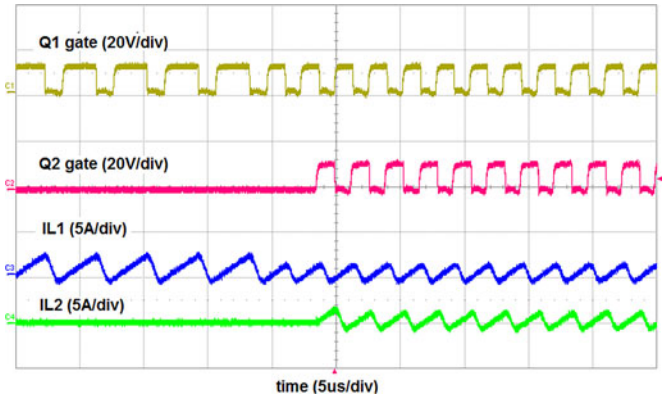

Fig. 16. Zoomed waveforms of the proposed method for load transient (115 V_{ac}, 0 W→400 W).

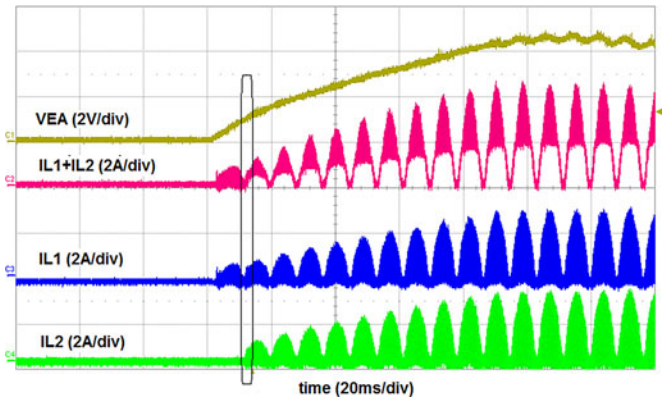

Fig. 17. Waveforms of the proposed method for load transient (230 V_{ac}, 0 W→400 W).

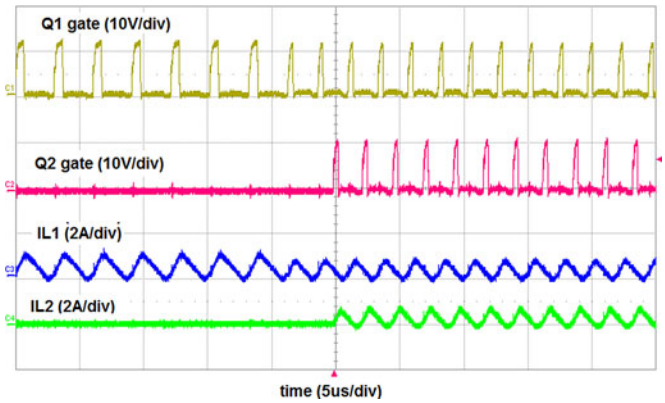

Fig. 18. Zoomed waveforms of the proposed method for load transient (230 V_{ac}, 0 W→400 W).

first drive signal of $Q2$ when channel 2 is recovered from phase-management operation. Figs. 17 and 18 show how interleaving is maintained when output load changes from no load to full load at high-line condition.

Figs. 19 and 20 show another example of ON-time perturbation by pulse-by-pulse current limit. The current sensing resistor for $Q2$ is replaced with larger one to set the pulse-by-pulse current limit at 4 A where the pulse-by-pulse current limit of $Q1$ is 10 A. This situation often occurs in real application during

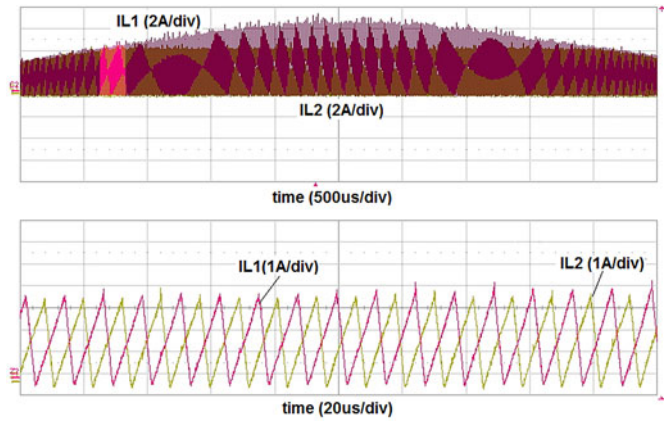

Fig. 19. Waveforms of the proposed method with before ON time is disturbed (115 V_{ac}, 300 W).

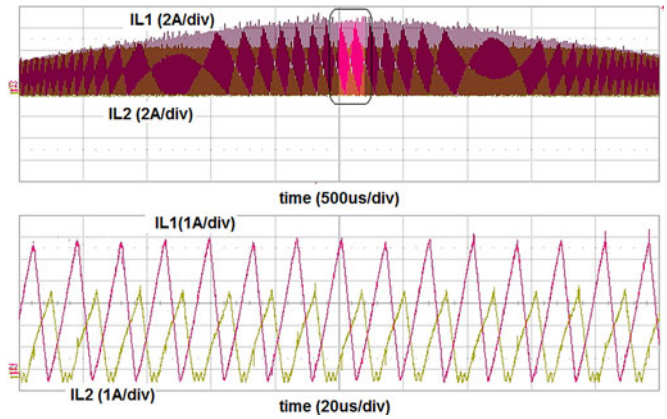

Fig. 20. Waveforms of the proposed method when ON time is disturbed (115 V_{ac}, 300 W).

overload or load transient due to the tolerances of inductor and current sensing resistor. The mismatch is exaggerated here to show the effect of the mismatch clearly. As can be observed, the proposed control method maintains the interleaving operation even with the persistent perturbation to the ON time.

Fig. 21 shows how the proposed control method maintains the interleaving of two channels around the ac line zero crossing for 115-V_{ac} line voltage and full-load condition. Around the line zero crossing, the inductor current is very small and the ZCD using the inductor auxiliary winding is lost. Thus, each channel runs with its own minimum frequency given by its reset timer (16.5 kHz), which introduces a perturbation to the turn-on instant. The proposed control method can maintain the interleaving around the line zero crossing regardless of sudden change of the switching frequency.

Figs. 22 and 23 show how the proposed method maintains the interleaving operation when the converter enters into CCM during startup. During startup, the output voltage is too close to the input voltage and there is not enough voltage across the inductor to discharge the inductor current while the boost switch is turned OFF. Therefore, the ZCD signal is lost and the converter operates with a constant switching frequency triggered by the reset timer (16.5 kHz), which also introduces a perturbation to

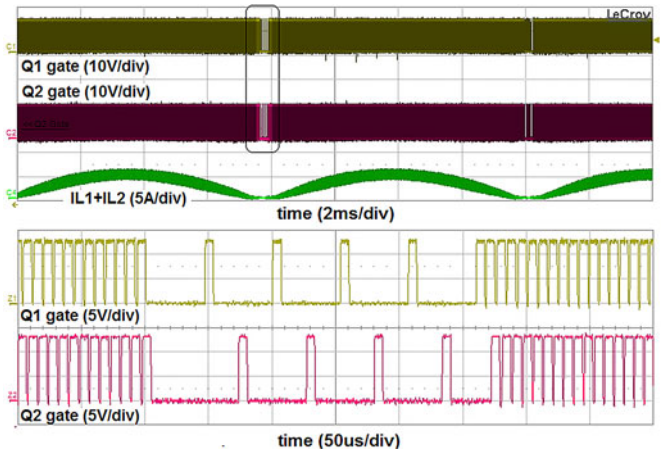

Fig. 21. Waveforms of the proposed method around line zero crossing (115 V_{ac}, 400 W).

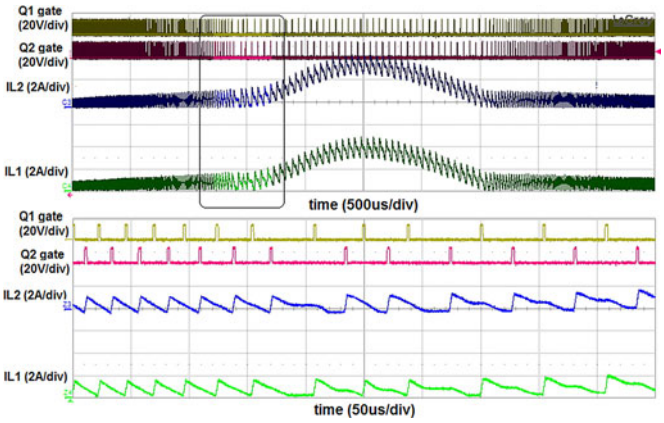

Fig. 22. Waveforms of the proposed method when the converters enter into CCM during startup (115 V_{ac}, 400 W).

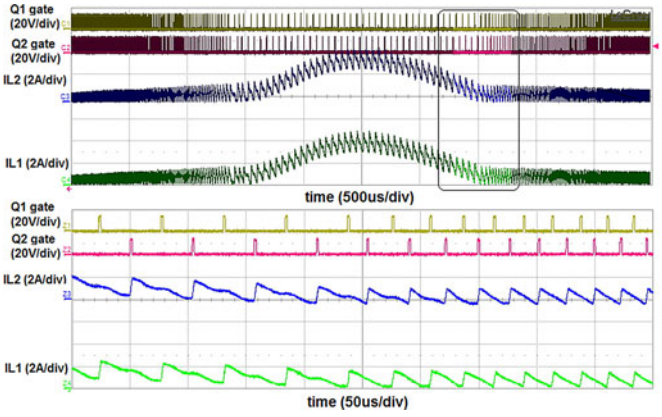

Fig. 23. Waveforms of the proposed method when the converters come out of CCM during startup (115 V_{ac}, 400 W).

the turn-on instant. The proposed control method can maintain the interleaving around the line zero crossing regardless of the abrupt change of switching frequency.

Figs. 24 and 25 show steady-state operation waveforms at full load with 115- and 230-V_{ac} line input voltages, respectively. As can be observed, the ripple of input current is reduced by the

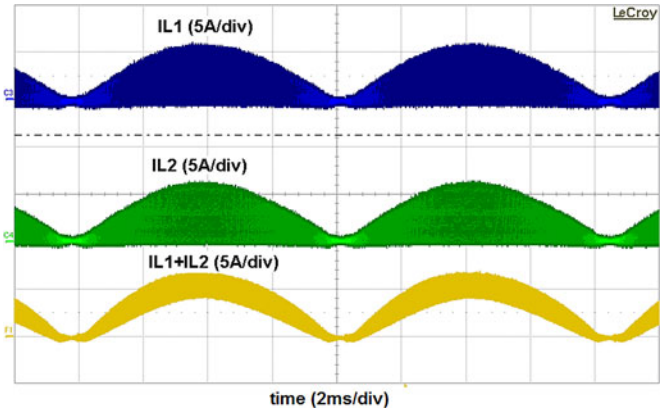

Fig. 24. Ripple cancellation with a proposed interleaving operation (low line, 115 V_{ac}, 400 W).

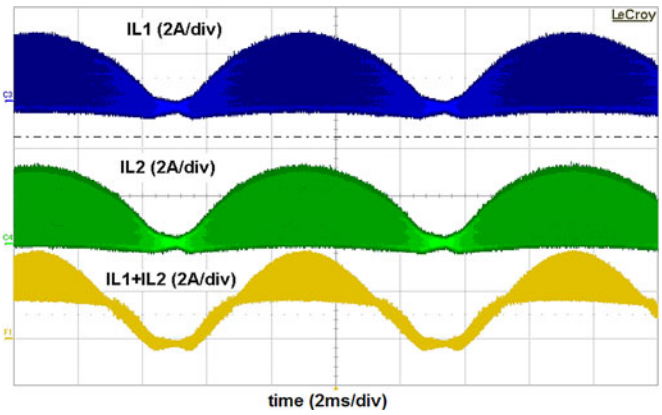

Fig. 25. Ripple cancellation with a proposed interleaving operation (high line, 230 V_{ac}, 400 W).

interleaving operation. Theoretically, perfect ripple cancellation is achieved when the duty cycle is 50%, which occurs when the instantaneous line input voltage is half of the output voltage. As can be observed in Fig. 25, the sum of two inductor currents exhibits zero ripple around phase angle of 40° and 140°.

Fig. 26 shows the measured harmonic current together with EN6100 class D regulation. It can be seen that the regulation can be met with enough margin with the proposed method. Fig. 27 shows the measured power factor at low line and high line, which shows that high power factor around 99% is achieved with the proposed method. The power factor drops severely at light-load condition especially for high-line condition (265 V_{ac}). This is because the boost converter operates in DCM at light-load condition due to the maximum frequency limit (525 kHz), which distorts the input current from sinusoidal shape [24].

Fig. 28 shows the measured efficiency of the prototype converter. At high line, higher than 98% efficiency is obtained at full-load condition. At low line, the maximum efficiency is 96.7%. Since the phase management sheds one channel when load drops below 25% of its nominal value, the light load efficiency is kept above 95% down to 10% load condition.

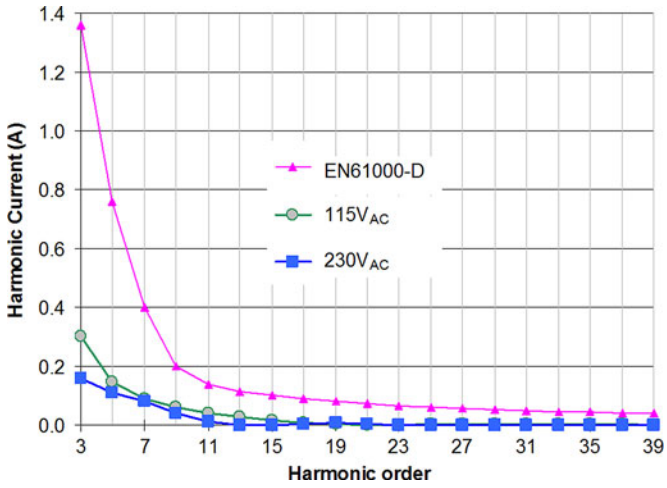

Fig. 26. Measured harmonic current and EN61000 Class D regulation.

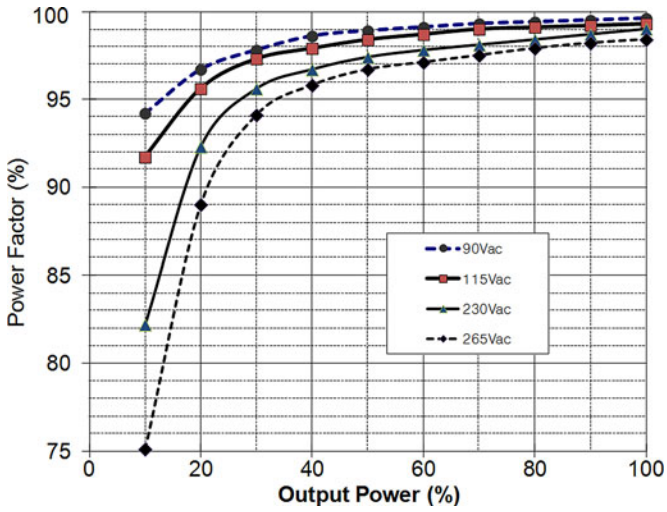

Fig. 27. Measured power factor.

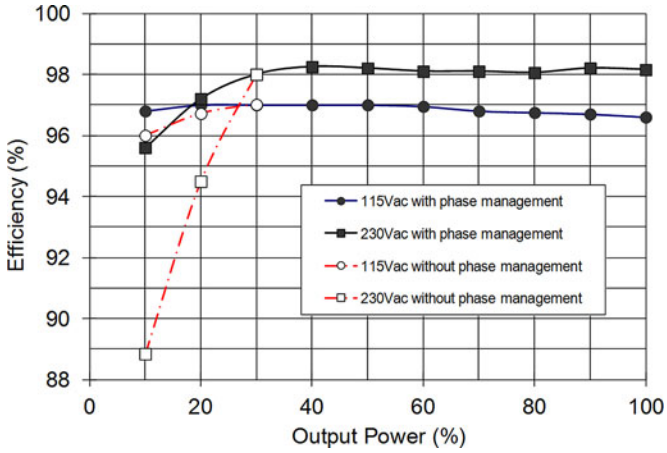

Fig. 28. Measured efficiency.

VI. Conclusion

A cross-coupled master–slave method for interleaved BCM PFC converters is presented, where the turn-on instant of master is determined by its own ZCD signal while the turn-on instant of slave is determined by the PS signal from the master in the same way as the conventional master–slave method does. However, the proposed method adaptively switches the master and slave converters based on the natural period of every switching cycle of each converter, which allows a stable 180° out-of-phase interleaving operation regardless of the mismatches of switching timing and power stage components. The proposed method responds to the disturbance on the PS very fast by compensating the disturbance within one switching cycle. The proposed method can overcome the limitation of the open-loop master–slave method that brings about CCM operation in slave when perturbed. The proposed method can also solve the current imbalance problem of the closed-loop PLL method when entering into CCM during startup. The experimental results from a 400 W interleaved BCM boost PFC converter with a dedicated control IC have verified that the proposed method guarantees stable interleaving operation during any transient and disturbance.

References

[1] C. Adragna, L. Huber, B. T. Irving, and M. M. Jovanovic, "Analysis and performance evaluation of interleaved DCM/CCM boundary boost PFC converters around zero-crossing of line voltage," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2009, pp. 1151–1157.

[2] J. S. Lai and D. Chen, "Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 1993, pp. 267–273.

[3] J. W. Kim, S. M. Choi, and K. T. Kim, "Variable on-time control of the critical conduction mode boost power factor correction converter to improve zero-crossing distortion," in *Proc. IEEE Power Electron. Drive Syst. Conf.*, Nov. 2005, pp. 1542–1546.

[4] T. Ishii and Y. Mizutani, "Power factor correction using interleaving technique for critical mode switching converters," in *Proc. IEEE Power Electron. Spec. Conf.*, May 1998, pp. 905–910.

[5] T. Ishii and Y. Mizutani, "Variable frequency switching of synchronized interleaved switching converters," U.S. Patent 5 905 369, May 18, 1999.

[6] B. T. Irving, Y. Jang, and M. M. Jovanović, "A comparative study of soft-switched CCM boost rectifiers and interleaved variable-frequency DCM boost rectifier," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb., 2000, pp. 171–177.

[7] T. F. Wu, J. R. Tsai, Y. M. Chen, and Z. H. Tsai, "Integrated circuits of a PFC controller for interleaved critical-mode boost converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2007, pp. 1347–1350.

[8] L. Huber, B. T. Irving, and M. M. Jovanović, "Open-loop control methods for interleaved DCM/CCM boundary boost PFC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1649–1657, Jul. 2008.

[9] L. Huber, B. T. Irving, C. Adragna, and M. M. Jovanović, "Implementation of open-loop control for interleaved DCM/CCM boundary boost PFC converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2008, pp. 1010–1016.

[10] C. Ku, D. Chen, C. Huang, and C. Liu, "A novel SFVM-M control scheme for interleaved CCM/DCM boundary-mode boost converter in PFC applications," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2295–2303, Aug. 2011.

[11] M. S. Elmore, "Input current ripple cancellation in synchronized, parallel connected critically continuous boost converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 1996, pp. 152–158.

[12] M. S. Elmore and K. A. Wallace, "Zero voltage switching supplies connected in parallel," U.S. Patent 5 793 191, Aug. 11, 1998.

[13] B. Lu, "A novel control method for interleaved transition mode PFC," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2008, pp. 697–701.

[14] X. Xu and A. Huang, "A novel closed loop interleaving strategy of multiphase critical mode boost PFC converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2008, pp. 1033–1038.

[15] L. Huber, B. T. Irving, and M. M. Jovanović, "Closed-loop control methods for interleaved DCM/CCM boundary boost PFC converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2009, pp. 991–997.

[16] L. Huber, B. T. Irving, and M. M. Jovanović, "Review and stability analysis of PLL-based interleaving control of DCM/CCM boundary boost PFC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1992–1999, Aug. 2009.
[17] H. Choi, "Design consideration for interleaved boundary conduction mode PFC using FAN9611," Fairchild Semiconductor, Bedford, NH, Application Note AN6086, Jun. 2008.
[18] H. Choi, "Novel adaptive master-slave method for interleaved boundary conduction mode (BCM) PFC converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Feb. 2010, pp. 36–41.
[19] C. Bridge and L. Balogh, "Synchronizing frequency and phase of multiple variable frequency power converters," U.S. Patent 7 933 132, Apr. 26, 2011.
[20] F. Yang, X. Ruan, Y. Yang, and Z. Ye, "Interleaved critical current mode boost PFC converter with coupled inductor," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2404–2413, Sep. 2011.
[21] T. Hsia, H. Tsai, D. Chen, M. Lee, and C. Huang, "Interleaved active-clamping converter with ZVS/ZCS features," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 29–37, Jan. 2011.
[22] S. Dwari and L. Parsa, "An efficient high-step-up interleaved DC–DC converter with a common active clamp," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 66–78, Jan. 2011.
[23] Y. Hsieh, M. Chen, and H. Cheng, "An interleaved flyback converter featured with zero-voltage transition," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 79–84, Jan. 2011.
[24] K. H. Liu and Y. L. Lin, "Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converter," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 1989, pp. 825–829.

Hangseok Choi (S'99–M'02–SM'12) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1996, 1999, and 2002, respectively.

From 2002 to 2007, he was a System and Application Engineer at Fairchild Semiconductor, Seoul. Since 2008, he has been a Principal System and Application Engineer in the Power Conversion Group, Fairchild Semiconductor, Bedford, NH, where he is currently involved in the development of high-performance power management ICs. He has authored or coauthored more than 50 technical papers and holds 20 U.S. patents. His research interests include analysis, simulation, and design of high-frequency, high-power-density power converters.

Laszlo Balogh (M'87) received the M.S.E.E. degree from the Technical University of Budapest, Budapest, Hungary, in 1983.

After doing research for several years designing power supplies for space, telecom, and industrial applications, he joined Unitrode (now Texas Instruments) in 1994. In 2005, he joined Fairchild Semiconductor, Bedford, NH, where he is currently a Technical Fellow, System Engineer, and Team Leader, in the Strategic R&D Team, Power Conversion, Industrial and Automotive Product Group. He is responsible for the development of various analog and digital pulsewidth modulation controllers, power supply support integrated circuits, and their application support. In his more than 28-year-long career in power management, he has authored many conference papers and application notes, has numerous granted and pending patents, and participates in organizing and presenting the Fairchild Power Supply Design Seminar worldwide.