A Current-Driving Synchronous Rectifier for an *LLC* Resonant Converter With Voltage-Doubler Rectifier Structure

Junming Zhang, *Member, IEEE*, Jiawen Liao, Jianfeng Wang, and Zhaoming Qian, *Senior Member, IEEE*

***Abstract*—This paper proposes a current-driving scheme for a synchronous rectifier (SR) in an *LLC* resonant converter with a voltage-doubler rectifier. In the proposed scheme, only one current transformer (CT) with one secondary winding is used to drive two SRs in the voltage-doubler rectifier. Also, the sensed current from the CT can be fed to the output with an energy-recovery circuit. Compared to the conventional center-tapped rectifier, the CT count for the SR drive circuit is reduced, which saves both cost and space. Although the current rating of the SR in the voltage-doubler rectifier is doubled, the voltage rating is well reduced and a lower voltage rating device with lower ON-state resistance can be used to compensate the increased current rating. Furthermore, the SR voltage stress is well clamped to the output voltage under any condition which improves the reliability of the circuit. A prototype with 16 V/5.6 A output was built to verify the theoretical analysis.**

***Index Terms*—Current driving, *LLC* resonant converter, synchronous rectifier (SR), voltage doubler.**

I. Introduction

THE trend toward high power density and efficiency on power supplies has stimulated a lot of research effort over the past few decades. To achieve high power density, a high switching frequency operation with high efficiency is necessary. In recent years, the *LLC* resonant converter has been widely adopted in isolated dc/dc application due to its high efficiency and simple structure [1]–[6]. Many research works have been published on the *LLC* resonant converter, such as those on optimal design methodology and protection [7]–[10].

To further improve efficiency, the synchronous rectifier (SR) has been widely adopted in low output voltage applications to reduce the conduction loss of the output rectifier. Since the *LLC* resonant converter is a current-fed topology and has no output inductor, the voltage stress of the output rectifier is much lower than in conventional voltage-fed topologies. Low-voltage rating MOSFET can be used as an SR to achieve high efficiency. However, the driving methods for SRs in an *LLC* resonant converter are much more complex than for the conventional voltage-fed topologies [11], [12].

Generally, there are two ways to drive an SR, the self-driven and the external-driven methods. The external-driven method utilizes the primary-side gate drive signal to generate the SR gate drive signal, which is typically complex and costly. An extra isolation circuit is required to transfer the gate drive signal between the primary side and the secondary side. Also, with the external-driven method, the *LLC* converter can only be operated under the Continuous Current Mode (CCM) condition, which is not preferred for efficiency optimization [13], [14].

The self-driven method can be further categorized into the voltage- and current-driven methods. The voltage-driven method is attractive for its simplicity and low cost. The SR-driving signal is derived from transformer secondary winding or inductor coupled winding with few extra components. However, they are topology dependent and usually only suitable for voltage-fed topologies with an inductive output filter. Since the *LLC* converter is a current-fed topology, the voltage on the transformer secondary winding can only be changed when SR is switched, which makes these voltage-driven methods not suitable for the *LLC* converter [24]. In order to adopt the voltage-driven methods in the *LLC* converter, a large leakage inductance needs to be presented in the transformer's secondary side, which results in high voltage spike across the SRs [15], [24].

The current-driven method senses the current flowing through the SR to turn ON or OFF the SR properly. Its main advantage is topology independence. A current-driven SR (CDSR) can directly replace a diode in any topology. The most convenient way to sense the current is by using a current transformer (CT). Numerous CDSR methods with CT have been proposed [16]–[23]. Generally, each SR needs a CT to detect its current and generate the proper driving signals [16]–[19]. In a high-current applications, the center-tapped structure is popular to reduce for reducing the conduction loss. Usually, two CTs are required to control two SRs in the center-tapped rectifier as shown in Fig. 1, which will cause high current loss in traces and windings of CTs; also, the cost is high. In order to reduce the power loss and the cost, the required CT count need to be minimized. In [21] and [22], the primary-side-current-sensing method is proposed. Thus, only one CT is required to drive two SRs in the secondary side. However, in the *LLC* resonant converter, the primary-side current differs from the secondary-side current due to the magnetizing current; a magnetizing current-compensation winding is required in [22] to derive the actual secondary-side SR current. In [20], the driving method with one CT in the secondary side for two

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J. Zhang, J. Wang, and Z. Qian are with the College of Electrical Engineering, Zhejiang University, Hangzhou, Zhejiang 310027, China (e-mail: zhangjm@zju.edu.cn; 20910100@zju.edu.cn; qian@cee.zju.edu.cn).

J. Liao is with the Electric Power Research Institute, Chongqing Electric Power Corporation, Chongqing 400000, China (e-mail: qwerpaul@zju.edu.cn).

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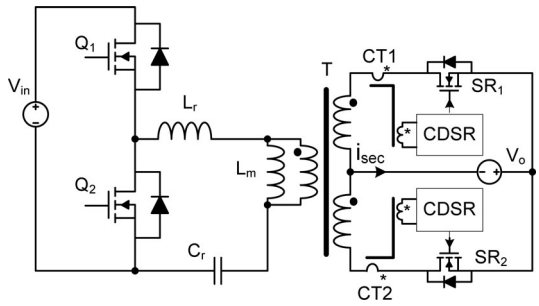

Fig. 1. Conventional center-tapper rectifier with CDSR.

SRs in the center-tapped rectifier is proposed. The sensed energy from CT is used to drive the SRs; therefore, the turns ratio of CT is quite big in order to minimize the related power loss, which is not suitable for a high-frequency application. Also, the gate-driving voltage varies with the load current. An SR-driving method for a voltage-doubler rectifier was proposed in [23], but the CT needs two secondary windings.

Another current-detecting method is to utilize the drain-to-source voltage drop $V_{\rm ds}$ when SR is ON. Several SR-driven methods based on $V_{\rm ds}$ detection with an IC or discrete circuit have been proposed [24]–[28]. Some commercial ICs are also available, such as IR1167/8, TEA1761, and MP6922. However, the accuracy and reliability of these driving methods are highly affected by the SR package, printed circuit board (PCB) layout, ON resistance $R_{\rm ON}$ of SR, and even by the temperature. The threshold for current detecting is usually around several millivolts, which makes the IC implementation difficult and costly. Due to the inevitable package and circuit inductance, the sensed $V_{\rm ds}$ is the sum of the $R_{\rm ON}$ voltage drop and the inductive voltage drop, which leads to duty cycle loss in a high-frequency operation. A capacitive network to compensate the inductive voltage drop is proposed in [24]; the parameters design and turning are still complex [28]. Furthermore, the variation of the parasitic parameters and $R_{\rm ON}$ will deteriorate the performance of the circuit. A digital implementation method is proposed in [28], the SR turns ON based on the primary-side switch turn-ON signal and the SR turn-OFF point is smartly adjusted based on the sensed SR $V_{\rm ds}$ signal. An extra isolation circuit for the turn-ON signal is required, which complicates the whole circuit.

Another issue related to the center-tapper rectifier in the *LLC* converter is the high voltage stress of SR due to the leakage inductance, which is always higher than 2 $V_{\rm out}$ [5]. An extra *RC* snubber circuit is usually required in practical applications to suppress this voltage spike and electromagnetic interference noise. Also, the transformer has two secondary windings, which decreases the utilization of transformer window area and makes transformer optimization difficult, especially for planar transformer. The low-voltage clamp rectifier structure proposed in [29] can effectively suppress the voltage spike, but the transformer structure is complex. Also, the current through the SRs in a center-tapped rectifier may not be equal due to the difference of the secondary-side current path and primary-side duty cycle, which further increases the conduction loss.

In this paper, an SR-driving method for a voltage-doubler rectifier in the *LLC* converter is proposed as shown in Fig. 2. With the trapezoid voltage-doubler structure, only one CT with one secondary winding is required to drive two SRs in the rectifier. The sensed energy from the CT can be fed to the output side and the power loss of the current-sensing circuit is minimized. The reduced CT count and simplified CT structure can further save PCB space, manufacturing effort, and the cost. Although the voltage-doubler rectifier has higher current stress compared to the center-tapped rectifier structure, the voltage stress of SR is well limited to the output voltage, which means that lower voltage rating device with lower ON resistance can be adopted to compensate for the increased current rating. The detailed operation principle is illustrated in Section II. The design considerations are discussed in Section III. In Section IV, detailed experimental results are presented.

II. Principle of Operation

As shown in Fig. 2, the trapezoid-type voltage-doubler rectifier is used. The gate drive voltage is clamped to the capacitor voltage $V_{\rm CO2}$ via D_5 and D_6, which theoretically equals half of the output voltage. It is suitable for some applications with relative high output voltage (usually above 12 V), such as laptop adapter (with typical 16–19 V output), and no extra voltage limit circuit is required. As shown in Fig. 2(b), two clamp circuits that consist of $R_a/D_a/Q_a$ and $R_b/D_b/Q_b$ are used to clamp the gate voltage to zero under the Discontinuous Current Mode (DCM) operation and provide a current freewheeling path for the magnetizing current of the CT. D_a/D_b is used to prevent Q_a/Q_b into deep saturation and fasten the ON/OFF speed. The capacitor C_1 is used to prevent any potential dc bias of the CT. The PMOS Q_7 is used as a level shifter and prevents the turning ON of $\rm SR_2$ when $\rm SR_1$ is ON since the undotted terminal of CT's secondary winding is clamped to V_o. Transistor pairs Q_2/Q_3 and Q_5/Q_6 are used as the push–pull stage to increase the driving capability. Transistor Q_8 provides a freewheeling path for the magnetizing current of CT under DCM operation when both SRs are OFF.

The detailed operation of the SR-driving circuit is presented later in the text. For simplicity, the output is simply modeled as a voltage source. Also, it is assumed that all of the switching devices and diodes are ideal, and the CT is modeled as a perfectly coupled transformer with magnetizing inductance $L_{m\_\rm CT}$. The steady-state operation waveforms and related equivalent circuits are shown in Figs. 3 and 4, respectively. The voltage across $C_{\rm O2}$ is modeled as a voltage sources $V_{\rm CO2}$ in the equivalent circuit. Before t_0, both $\rm SR_1$ and $\rm SR_2$ are OFF.

Mode 1 (t_0–t_1): At t_0, the transformer secondary side current $i_{\rm sec}$ increases from zero, and the body diode of $\rm SR_1$ begins to conduct. The clamp transistor Q_a turns OFF as soon as the body diode of $\rm SR_1$ turns ON. And the gate voltage of $\rm SR_1$ $V_{\rm gs\_SR1}$ is charged up by the reflected current $i_{\rm CTS1}$ through $N_{\rm CTS1}$ and the magnetizing current of CT $i_{{\rm CT}m}$. As mentioned earlier, transistor Q_2 is used to increase the driving capability with its current gain. The gate voltage $V_{\rm gs\_SR1}$ is given as

$$v_{\rm gs\_SR1}(t) = \frac{\beta}{C_{\rm gs}\cdot N_{\rm CT}}\cdot\int_{t0}^{t} i_{\rm sec}(t)\cdot dt \qquad (1)$$

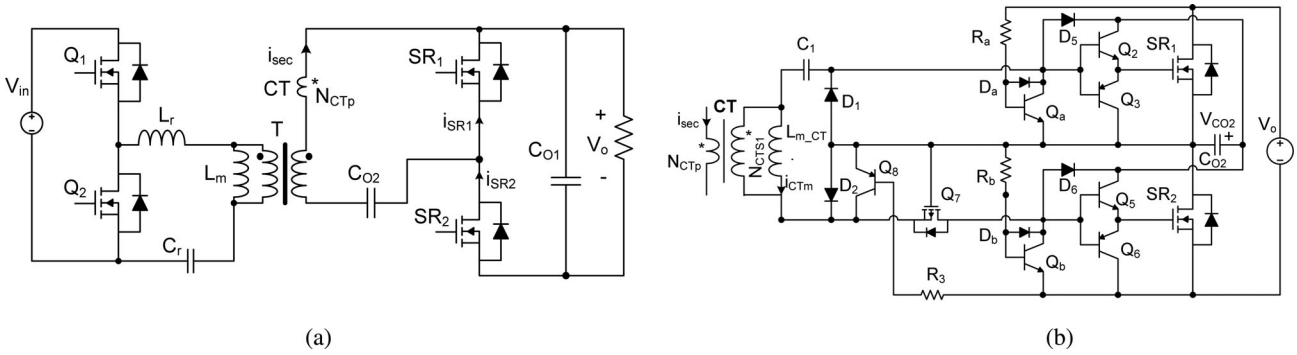

Fig. 2. Proposed SR-driving method for the trapezoid voltage-doubler rectifier. (a) Trapezoid voltage-doubler rectifier. (b) Proposed SR-driving method.

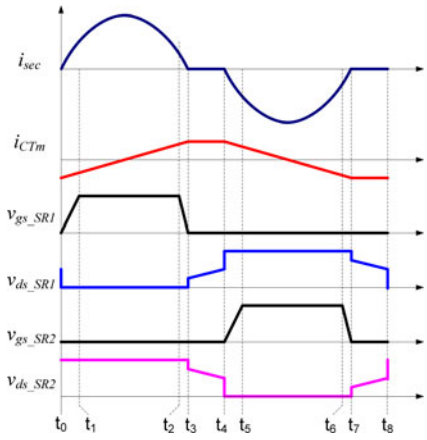

Fig. 3. Steady-state operation waveforms.

where $C_{\rm gs}$ is the gate capacitance of $\rm SR_1$; $N_{\rm CT}$ is the turns ratio of the CT, i.e., $N_{\rm CT} = N_{\rm CTS}/N_{\rm CTp}$; and β is the current gain of transistor Q_2.

In this mode, when the $\rm SR_1$ gate voltage $V_{\rm gs\_SR1}$ reaches the turn-ON threshold voltage, the current flows through $\rm SR_1$ instead of the body diode. When the $V_{\rm gs\_SR1}$ reaches the output voltage V_o, the clamp diodes D_5 turns ON, $V_{\rm gs\_SR1}$ is clamped to $V_{\rm CO2}$, and this mode ends.

Mode 2 (t_1–t_2): In this mode, $\rm SR_1$ is kept ON and the magnetizing current $i_{{\rm CT}m}$ increases linearly. Since the clamp diodes D_5 is ON, the sensed energy from the CT is fed to the capacitor $C_{\rm O2}$ and, then, fed to the output when $\rm SR_2$ is ON. Therefore, a small turns ratio of CT can be used to reduce the size and the turn-ON delay time as indicated in (1). The magnetizing current of CT can be expressed as

$$i_{{\rm CT}m}(t) = \frac{V_{\rm clamp} + 2 \cdot V_D}{L_{m\_{\rm CT}}} \cdot (t - t_1) - I_{\rm CT\_max} \qquad (2)$$

where $L_{m\_{\rm CT}}$ is the magnetizing inductance of CT; $I_{\rm CT\_max}$ is the peak magnetizing current of the CT; and $V_{\rm clamp}$ is the clamp voltage for the gate drive signal, which is equal to $V_o/2$ here. V_D is the forward-voltage drop of the clamp diode.

Mode 3 (t_2–t_3): When the transformer's secondary-side current decreases to a certain level, the CT's secondary-side current $i_{\rm CTS1}$ is smaller than the magnetizing current $i_{{\rm CT}m}$, the current difference flows through Q_8 to turn ON Q_3, and $V_{\rm gs\_SR1}$ is discharged to zero quickly. As soon as $\rm SR_1$ turns OFF and its drain–source voltage $V_{\rm ds\_SR1}$ increases from zero, the clamp transistor Q_a turns ON and the gate voltage $V_{\rm gs\_SR1}$ is clamped to zero until next switch cycle.

Mode 4 (t_3–t_4): This mode only exists in the DCM mode and both $\rm SR_1$ and $\rm SR_2$ are OFF. For CCM and critical DCM operations, this mode no longer exists. The magnetizing current of CT $i_{{\rm CT}m}$ freewheels through Q_8 and D_1. It should be noted that the transistor Q_8 can also handle the current from collector to emitter since the structure of the transistor is symmetrical, though the current gain is a little bit different.

Mode 5 (t_4–t_5): In this mode, the current flows through $\rm SR_2$. Although the operation of this mode is similar to that of Mode 1, the turn ON of PMOS Q_7 should be clarified here. As soon as the body diode of $\rm SR_2$ turns ON, the clamp transistor Q_b and Q_8 are OFF. The sensed current from CT charges up the gate–source capacitor of Q_7, and Q_7 turns ON. Also, the sensed current from CT charges up the gate voltage of $\rm SR_2$. The gate–source voltage of Q_7 is the same as $V_{\rm gs\_SR2}$ except the polarity since $\rm SR_2$ is ON. As soon as $V_{\rm gs\_SR2}$ reaches $V_{\rm CO2}$, the clamp diode D_6 turns ON and this mode ends.

The other operating modes during [t_5–t_8] are easy to understand since they are similar to Modes 2, 3, and 4, as described earlier, and they are thus not repeated here. The only difference is that the gate voltage of $\rm SR_2$, i.e., $V_{\rm gs\_SR2}$, is clamped to $V_{\rm CO2}$ through D_6. In Mode 8, the magnetizing current of CT freewheels through Q_a and Q_8/D_2 when both SRs are OFF.

III. Design Considerations

The detailed design of the *LLC* resonant converter is already well known and thus will not be elaborated upon here. Only the design considerations of the output capacitors will be briefly described. For simplicity, the transformer secondary winding current $i_{\rm sec}$ can be simply treated as a sinusoidal waveform with amplitude being equal to $I_{\rm sec\_pk}$, which is given in (3). In practical applications, the secondary-side current $i_{\rm sec}$ is slightly different from the sinusoidal waveform and depends on the amplitude of the transformer magnetizing current. The peak amplitude $I_{\rm sec\_pk}$ can be estimated as

$$i_{\rm sec}(t) = I_{\rm sec\_pk} \cdot \sin(2 \cdot \pi \cdot f_r \cdot t) \qquad (3)$$

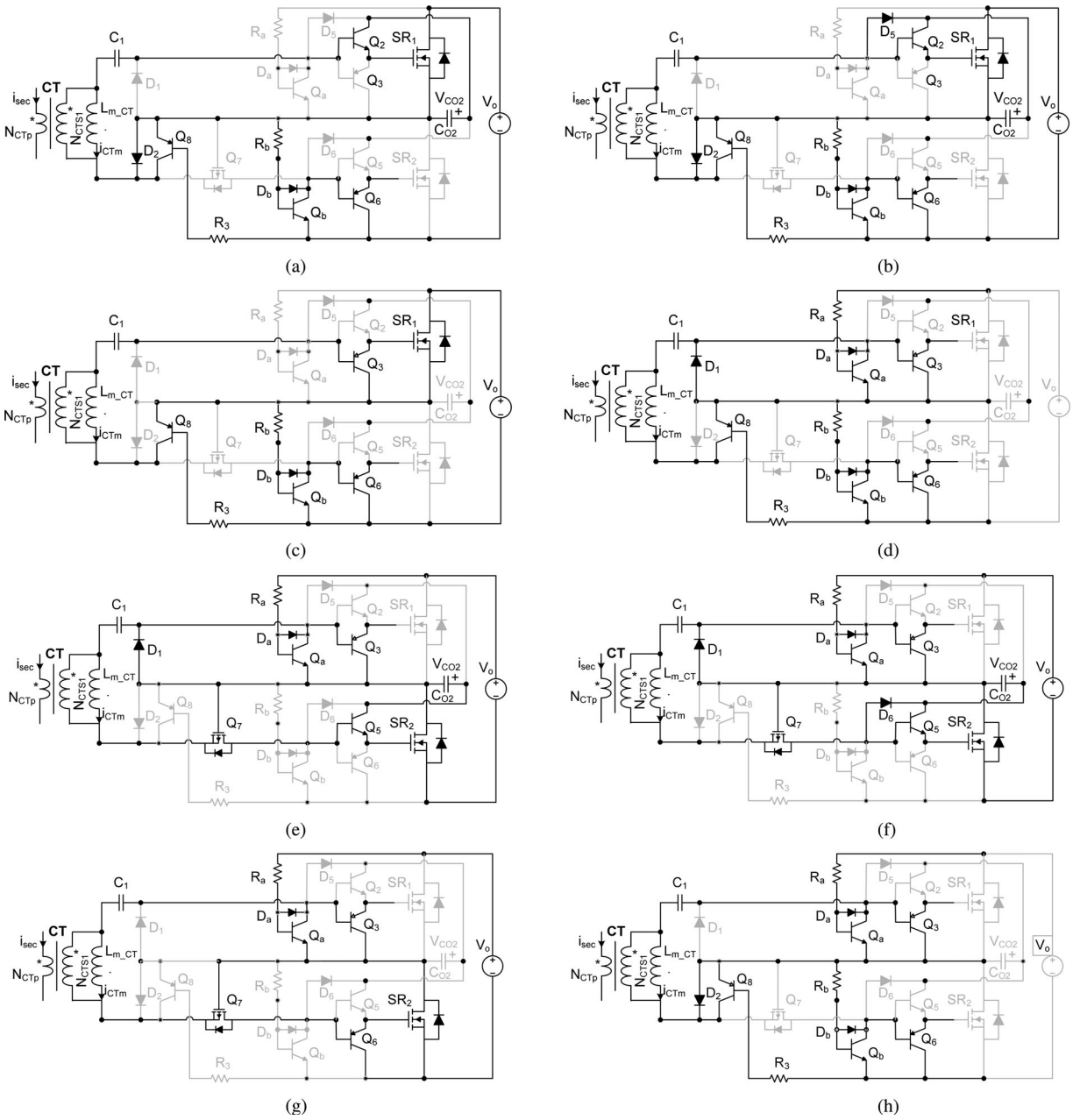

Fig. 4. Equivalent circuits for each operation mode. (a) Mode 1 (t_0–t_1). (b) Mode 2 (t_1–t_2). (c) Mode 3 (t_2–t_3). (d) Mode 4 (t_3–t_4). (e) Mode 5 (t_4–t_5). (f) Mode 6 (t_5–t_6). (g) Mode 7 (t_6–t_7). (h) Mode 8 (t_7–t_8).

$$I_{\mathrm{sec\_pk}} = \frac{\pi \cdot I_o \cdot f_r}{f_s} \cdot \frac{1-\cos(\pi \cdot f_r / f_{\mathrm{eq}})}{2} \tag{4}$$

$$f_{\mathrm{eq}} = \max(f_r, f_s) \tag{5}$$

where f_s is the switching frequency; f_r is the resonant frequency by the resonant inductor L_r and resonant capacitor C_r in the *LLC* converter; I_o is the average output current; f_{eq} is the maximum one of the resonant frequency f_r and switching frequency f_s. For the DCM and critical DCM operations, f_{eq} equals to the resonant frequency f_r.

The output capacitance of the voltage-doubler rectifier can be designed based on the maximum allowed voltage ripple. The trapezoid voltage-doubler structure can be roughly estimated as

$$C \geq \frac{I_o \cdot (2 \cdot f_{\mathrm{eq}} - f_s)}{2 \cdot \Delta V_{o\_\max} \cdot f_s \cdot f_{\mathrm{eq}}} \tag{6}$$

where $\Delta V_{o\_\max}$ is the maximum allowed voltage ripple, which is larger than the conventional center-tapped rectifier since the transformer's secondary-side current is not fed to the output in half the switching period.

Also, the capacitor C_{O2} shown in Fig. 2 has high current stress due to the trapezoid voltage-doubler structure. The current through C_{O2} is the same as the transformer secondary side current i_{sec} given in (3). The RMS current of C_{O2} can be easily derived based on (3)–(5). For example, under critical DCM

condition, the capacitor RMS current can be $2.22^{*}I_o$. Therefore, the capacitor with very small equivalent series resistor (ESR), such as the ceramic capacitor, should be used to minimize the power loss.

The proposed SR-driving circuits are quite simple. The key parameters for the proposed SR-driving method are the turns ratio $N_{\rm CT}$ of the CT and its magnetizing inductance $L_{m\_{\rm CT}}$.

Basically, $N_{\rm CT}$ is designed based on the required turn-ON delay time and related power loss. The gate voltage during Mode 1 is given in (1) and $i_{\rm sec}$ is given in (5) based on the assumption. Since the time for turn-ON delay is quite small compared to the switching period or resonant period, $i_{\rm sec}$ can be simplified to a linear one as given in (7). Therefore, the turn-ON delay time $T_{\rm d\_on}$ can be calculated as follows by neglecting the magnetizing current of the CT:

$$i_{\rm sec}(t) = I_{\rm sec\_pk} \cdot \sin(2 \cdot \pi \cdot f_r \cdot t) \approx I_{\rm sec\_pk} \cdot 2 \cdot \pi \cdot f_r \cdot t \tag{7}$$

$$T_{d\_{\rm on}} = \sqrt{\frac{V_{\rm gs\_th} \cdot C_{\rm gs} \cdot N_{\rm CT}}{I_{\rm sec\_pk} \cdot \pi \cdot f_r \cdot \beta}} \tag{8}$$

where $V_{\rm gs\_th}$ and $C_{\rm gs}$ are the turn-ON threshold and gate capacitance of SR, respectively. It is clear that the turn-ON delay time can be reduced by small $N_{\rm CT}$. Because the sensed current can be fed to the output, a small turns ratio is possible in the proposed SR-driving method.

Although the sensed energy can be fed to the output, there is still conduction loss related to the diodes in the current path, such as D_1/D_2/D_5/D_6. Assuming all the diodes have the same voltage drop V_D, the conduction loss can be estimated by (9). Based on (7) and (8), $N_{\rm CT}$ can be determined with required delay time and desired power loss

$$P_{\rm con} = \frac{4 \cdot I_o \cdot V_D}{N_{\rm CT}}. \tag{9}$$

Another important parameter for the CT is its magnetizing inductance. The magnetizing current is given in (2) and the clamp voltage $V_{\rm clamp}$ is V_o/2 in the proposed SR-driving method. The amplitude of the magnetizing current of CT determines the turn-OFF point of the SR, which can be used to compensate the turn-OFF delay of the SR-driving circuit to prevent the reverse current flowing through the SRs. As soon as the sensed transformer secondary-side current $i_{\rm sec}$ equals $i_{{\rm CT}m}$ as shown in Fig. 3, the SR turns OFF. The larger the amplitude, the earlier the SR turns OFF.

Since Modes 1 and 3 are quite short compared to the whole switching cycle, the maximum magnetizing current of CT $I_{\rm CT\_max}$ can be calculated as follows based on (2):

$$I_{\rm CT\_max} = \frac{V_{\rm clamp} + 2 \cdot V_D}{L_{m\_{\rm CT}}} \cdot \frac{1}{4 \cdot f_{\rm eq}}. \tag{10}$$

Once the secondary-side current $i_{\rm sec}$ reaches $N_{\rm CT}{*}I_{\rm CT\_max}$, the SR starts to turn OFF. Therefore, this current can also be treated as the SR turn-OFF current considering the CT's turns ratio. With the secondary-side current $i_{\rm sec}$ given in (3), the leading time T_d for the SR turn OFF under the DCM or critical DCM operation can be calculated as

$$T_d = \arcsin\left(\frac{N_{\rm CT} \cdot I_{\rm CT\_max}}{I_{\rm sec\_pk}}\right) \cdot \frac{1}{2 \cdot \pi \cdot f_r}. \tag{11}$$

From the aforementioned equation, the turn-OFF leading time also varies with the secondary-side current peak value $I_{\rm sec\_pk}$. For certain output power, $I_{\rm sec\_pk}$ is larger in DCM operation, which means a smaller leading time with a fixed $I_{\rm CT\_max}$.

Therefore, based on (10) and (11), with a desired leading time, such as 100 or 200 ns, the magnetizing inductance of the CT can be determined. However, this value is designed based on DCM and critical DCM operation. For the CCM operation, the current slew rate will be much higher, and the leading time at the same turn-OFF point will be reduced. The current slew rate depends on the circuit parasitic inductance, including stray inductance and transformer leakage inductance, which is not easy to predict. The designed turn-OFF leading time based on (11) should also be checked under the CCM operation. A good rule of thumb is to design the turn-OFF point before the primary-side switches change the status in the CCM operation.

Based on the calculated turns ratio $N_{\rm CT}$ and magnetizing inductance $L_{m\_{\rm CT}}$, a proper core can be determined. However, since the core size and permeability are only available in a certain value, the magnetizing inductance may not meet the target with the desired turns ratio. We can design the CT with desired turns ratio and a higher magnetizing inductance. Also, a gate pull-down resistor from gate to source of SR can be used to compensate the difference, which is usually required to prevent gate floating in the practical applications. Considering this gate resistance, the leading time T_d can be estimated as

$$T_d = \arcsin\left[\frac{N_{\rm CT} \cdot (I_{\rm CT\_max} + V_{\rm clamp}/R_{\rm gs})}{I_{\rm sec\_pk}}\right] \cdot \frac{1}{2 \cdot \pi \cdot f_r} \tag{12}$$

where $R_{\rm gs}$ is the gate pull-down resistance.

The other parameters in the circuit are quite simple to design. The maximum voltage across PMOS Q_7 is the output voltage V_o. A small signal PMOS can be used. Also, the bipolar transistors in the driving circuit should have the voltage rating slightly above V_o. The capacitor C_1 is used to block any potential dc bias of the CT. Therefore, the capacitance selection is a little arbitrary, the resonant frequency formed by the C_1 and $L_{m\_{\rm CT}}$ should be well below the switching frequency to prevent any potential parasitic resonance, and the voltage ripple across C_1 should be small. Since the SR duty cycle is always 50% and the feedback loop response is usually slow in the *LLC* resonant converter, the voltage change in the C_1 during transient (such as load transient and startup) is also slow and smooth, which means the potential parasitic ring caused by C_1 can almost be eliminated. For the diodes in the proposed SR-driving circuit, the signal Schottky diode is preferred to reduce the forward-voltage drop and achieve good performance.

The voltage rating of the SRs is V_o, which is reduced by half in the center-tapped rectifier without considering the voltage spikes. And the current stress of transformer secondary winding and SRs is doubled compared to the center-tapped rectifier. Generally, the ON resistance of MOSFET increases rapidly with

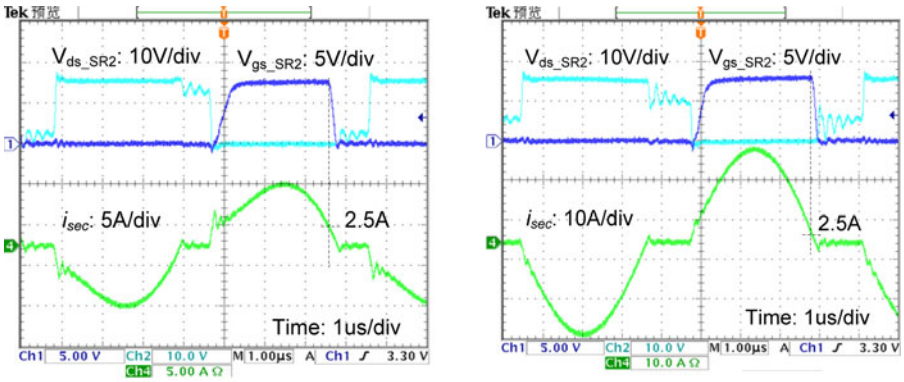

Fig. 5. SR waveforms under the DCM operation, $V_{\rm in} = 360$ V. (a) Light load ($I_o = 2$ A). (b) Full load ($I_o = 5.6$ A).

its breakdown voltage rating using the same manufacturing process and die size. Therefore, the increased current rating can be compensated by the reduced ON resistance of the SR due to the reduced voltage rating.

Theoretically, the voltage rating for SR in the center-tapped rectifier is at least twice that in the voltage-doubler rectifier. Considering the voltage spikes caused by the parasitic ring in the center-tapped rectifier, the voltage rating difference is even higher [5]. For low output voltage applications (below 10 V), the minimum voltage rating for the available trench MOSFET is around 20 V, which means that the voltage rating for SRs in the voltage-doubler and center-tapped rectifiers is almost the same. And the efficiency is poor for the voltage-doubler rectifier with the same device due to high current stress. Furthermore, since the proposed SR-driving method clamps the driving voltage to half the output voltage, the gate voltage may not be sufficient without any extra circuit. Therefore, it may not be preferred in these low output voltage applications. For a relative high output voltage, such as 16–48 V (as in telecom applications), the SR may have a big voltage rating difference with different rectifier structure, and lower voltage rating MOSFET with lower ON resistance can be used for voltage-doubler structure to compensate the increased current rating. For example, if the device derating factor is 0.8, for 24-V output, the SR voltage rating is 30 and 80 V for the voltage-doubler and center-tapped rectifiers, respectively. If the output voltage is 48 V, the SR voltage rating is 60 and 150 V for the voltage-doubler and center-tapped rectifiers, respectively [24]. In these applications, the voltage-doubler structure presented in this paper can be considered. Nevertheless, due to the inherent high current stress, the output current cannot be very high. The potential application is LED drivers and adapters.

IV. Experimental Results

To verify the proposed SR-driving methods with voltage-doubler structure, a prototype for adapter application is built and tested. The input is 300–400 V and the output is 16 V/5.6 A. The turns ratio of CT is 100 and the magnetizing inductance of CT is 0.4 mH. The primary-side resonant inductance is 70 μH (including the transformer leakage inductance) and the resonant capacitance is 13.6 nF (two 6.8 nF capacitors in parallel). The resonant frequency is around 160 kHz. Based on (10) and (11), the turn-OFF current is around 3.3 A assuming the signal Schottky diode forward voltage is 0.3 V. Ten ceramic capacitors (22 μF/25 V with 3 mΩ ESR) in parallel are used for C_{O2} to minimize the power loss. Since the waveforms for the two SR are almost the same, only the waveforms of SR_2 (low side SR) are shown for simplicity.

Fig. 5 shows the SR waveforms at 360-V input, and the converter operates in the DCM mode. From Fig. 5, it is clear that the SR turn-OFF point is around 2.5 A under light-load and full-load conditions, which is quite close to the designed point 3.3 A. The difference is mainly caused by the inevitable delay which exists in the SR driver circuit. Also, the SR gate drive signal is clamped to zero when both SRs are OFF in the DCM operation. Fig. 6 shows the SR waveforms at critical DCM operation with 400 V dc input. The waveforms under the CCM operation with higher input voltage (420 V here) are shown in Fig. 7. In Figs. 5 and 6, the SR turn-OFF point is almost kept the same at 2.5 A under different load conditions and operation modes, which is determined by the magnetizing current of the CT as mentioned earlier. The turn-OFF point for the CCM operation shown in Fig. 7 is slightly lower due to higher switching frequency. The leading time varies with the peak amplitude of secondary-side current as given in (9). The minimum leading time is around 200 ns as shown in Fig. 7 under the CCM and full-load condition, which compensate the circuit delay. Also, the drain–source voltage of SR is clean and there is no parasitic ring. The operation of the proposed SR-driven method matches the theoretical analysis quite well.

The SR waveforms under load transient are shown in Fig. 8. From Fig. 8, the SR works quite well under load dynamic condition. The waveform of the voltage across capacitor C_1 (2.2 μF/16 V) is shown in Fig. 9 under the DCM operation. It is clear that the voltage across C_1, i.e., V_{C1}, is very small, 500 mV, and it is almost kept the same under the load transient condition.

An *LLC* converter with the center-tapper rectifier shown in Fig. 1 is also built for comparison. The SR in the center-tapper rectifier is driven by the CDSR proposed in [18], which is also shown in Fig. 10. The resonant inductor, resonant capacitor, and the magnetizing inductance are kept the same for these

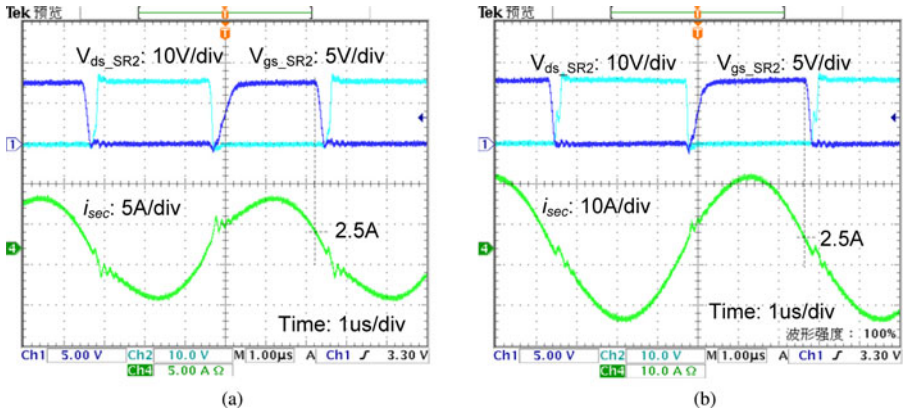

Fig. 6. SR waveforms under the critical DCM operation, $V_{\rm in} = 400$ V. (a) Light load ($I_o = 2$ A). (b) Full load ($I_o = 5.6$ A).

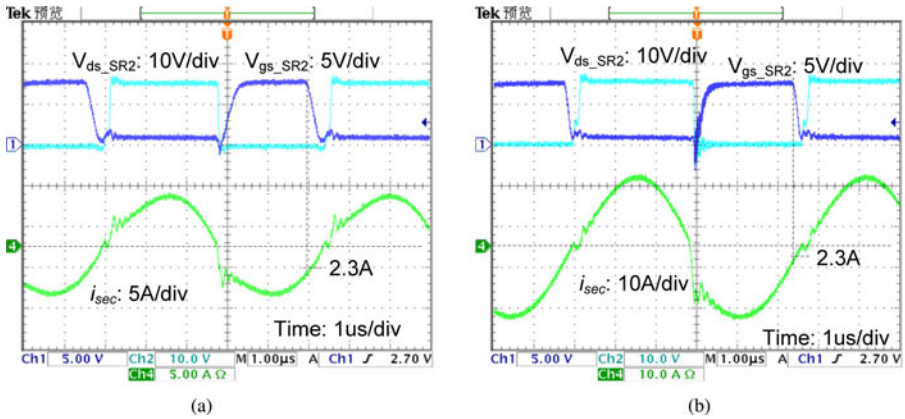

Fig. 7. SR waveforms under the CCM operation, $V_{\rm in} = 420$ V. (a) Light load ($I_o = 2$ A). (b) Full load ($I_o = 5.6$ A).

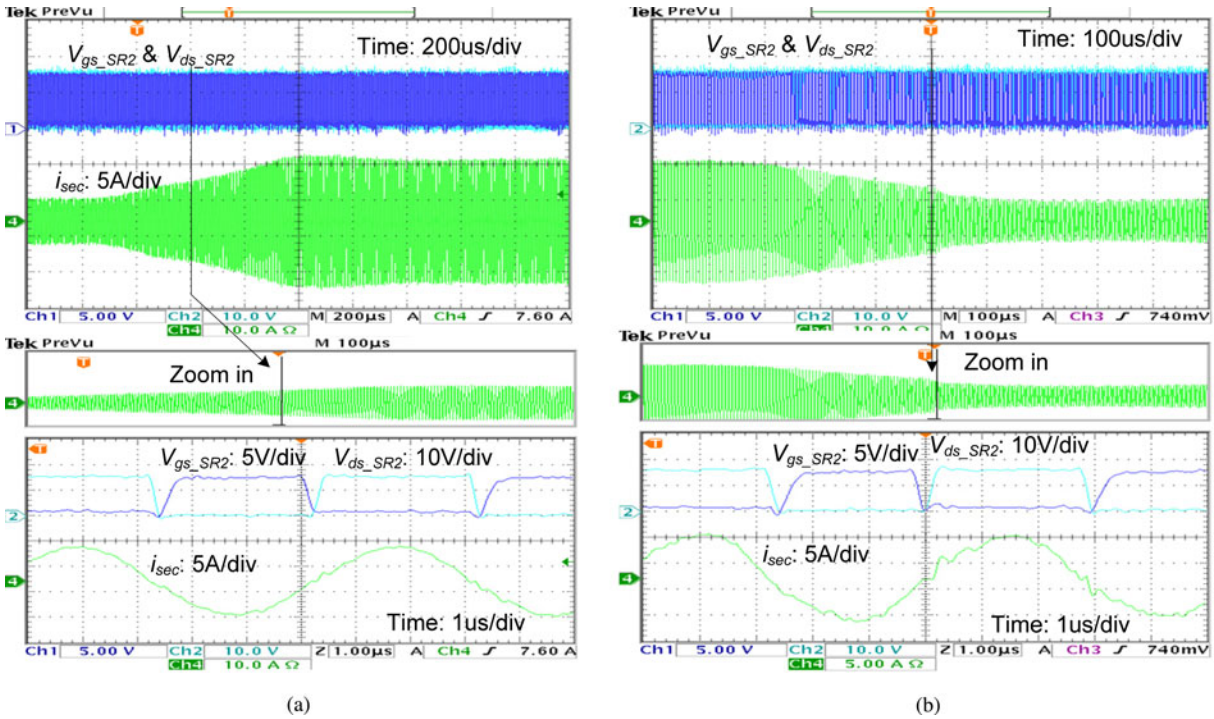

Fig. 8. SR waveforms under load transient at $V_{\rm in} = 400$ V. (a) Load step up (30–100%). (b) Load step down (100–30%).

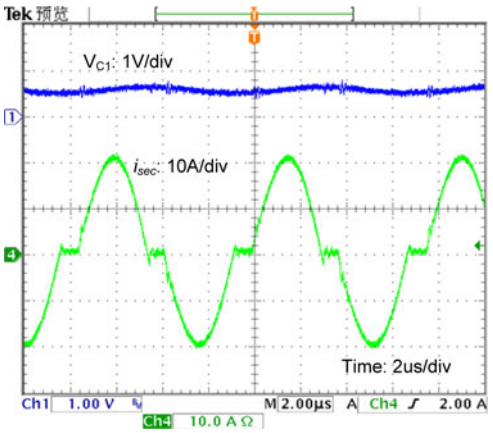

Fig. 9. Voltage waveform across C_1 under the DCM operation.

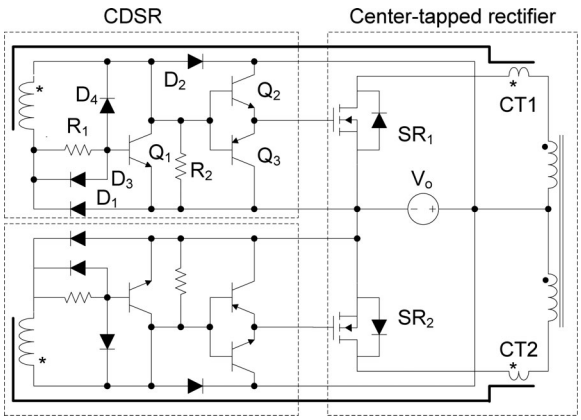

Fig. 10. CDSR for the center-tapped rectifier [18].

two prototypes. The transformer turns ratio is different to keep the same output voltage. Since there is no parasitic ring across the drain–source of the SR, considering the derating factor for practical applications, such as 0.8, a 20-V MOSFET can be used. For the center-tapped rectifier, the voltage rating for SR should be at least 60 V considering the parasitic ring caused by the transformer leakage inductance. With the same silicon die size, the ON resistance $R_{\rm dson}$ of the SR with higher voltage rating should be much larger. Since it is not practical to measure the die size of the SRs that we used, we simply choose the ON-state resistance of SR for a voltage-doubler rectifier four times smaller than that for the center-tapped rectifier to achieve similar SR conduction loss. Also, the cost of the SR should be comparable. The detailed parameters for these two prototypes are given in Table I.

The measured drain–source voltage $V_{\rm ds}$, transformer secondary side current $i_{\rm sec}$, and primary-side resonant inductor current i_{Lr} in the center-tapped rectifier are shown in Fig. 11. It is clear that $V_{\rm ds}$ of SR has some parasitic rings and the peak voltage of $V_{\rm ds}$ is around 45 V. Therefore, the voltage rating of SR should be at least 60 V for the center-tapped rectifier. Also, from Fig. 11, the current through the two SRs is not symmetrical because the parameters difference existed in the positive and negative half-cycles in the practical applications, especially

TABLE I
DIFFERENCES BETWEEN THE PROTOTYPES WITH VOLTAGE-DOUBLER AND CENTER-TAPPED RECTIFIERS

		Voltage-doubler	Center-tapped
Transformer	turns ratio	25:1	25:2:2
	Primary windings	0.27mm*3	0.27mm*3
	Secondary windings	0.1mm*50*8	0.1mm*50*4
	Magnetizing inductance	700µH	700µH
SR		HAT2169 (40V/2.8m)	IRF7854 (80V/11m)
Resonant inductance		70uH	70uH
Resonant capacitance		13.6nF	13.6nF

under the light-load condition, such as primary side duty cycle asymmetrical, which may causes one SR to have higher conduction loss. However, the currents through two SRs are always symmetrical in the voltage-doubler structure as shown in Figs. 5–7, which is an advantage of the voltage-doubler rectifier.

Another advantage of the voltage-doubler rectifier is the improved circuit reliability in the case the SR turn-OFF leading time is not sufficient. For evaluation, we increased the CT's magnetizing inductance to 4 mH with big ferrite core; therefore, the SR turn-OFF current will be negative due to the delay. Fig. 12 shows the SR waveforms in the center-tapped rectifier when the SR turn-OFF leading time is not sufficient. In this case, the SR will have severe reverse current (from SR drain to source). Since the two secondary windings have some leakage inductance, the reverse current will cause high voltage spike across SR like an unclamped inductive load. As shown in Fig. 12(b), if SR_2 turns OFF with a reverse current (from drain to source), the energy in $L_{\rm k2}$ will introduce a severe voltage spike across SR_2 since SR_1 is ON and the transformer is not perfectly coupled. If the energy is large enough, the SR will be in avalanche or even damaged. However, in the voltage-doubler rectifier, since the SRs are well clamped by the output capacitor, there is no voltage spike even if there is reverse current. Fig. 13 shows the SR waveforms in the voltage-doubler rectifier with reverse current; it is clear that there is almost no voltage spike compared to Fig. 12(a). Therefore, the actual SR-driving circuit in the center-tapped rectifier is more sensitive for parameters variation and should be checked under corner conditions to prevent any voltage overstress, such as startup or load transient. For the voltage-doubler rectifier, the SR voltage overstress is eliminated, and thus, the circuit is more reliable.

The measured efficiency from the two prototypes with SR is shown in Fig. 14. The efficiency is almost the same since the ON resistance of SR in the voltage-doubler rectifier is around one-fourth of that in the center-tapped rectifier. Under the full-load condition, the prototype efficiency is around 94%. For comparison, the efficiency of the prototype with the state-of-the-art Schottky diode rectifier is also shown in Fig. 14. The Schottky diode for the center-tapped rectifier is MBRB2060CT (60 V/20 A), and the Schottky diode for the voltage-doubler rectifier is MBRB30H30CT (30 V/30 A). With the Schottky diode rectifier, the efficiency of the prototype with the center-tapped rectifier is about 1.5% higher than that with the voltage-doubler

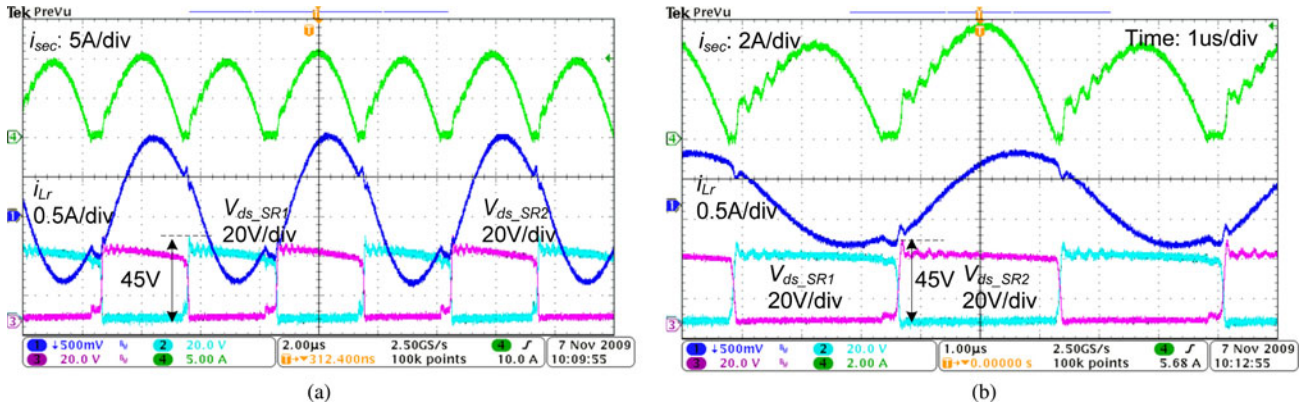

Fig. 11. SR waveforms in the conventional center-tapped rectifier, $V_{\rm in} = 400$ V, critical DCM. (a) Full load ($I_o = 5.6$ A). (b) Light load ($I_o = 2$ A).

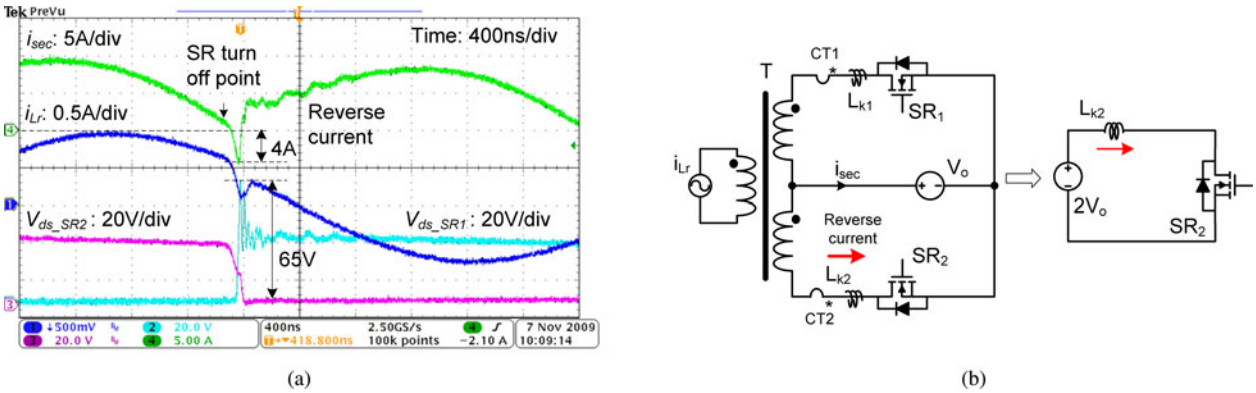

Fig. 12. SR voltage spikes in the center-tapped rectifier with small SR turn-OFF leading time. (a) SR waveforms. (b) Equivalent circuit.

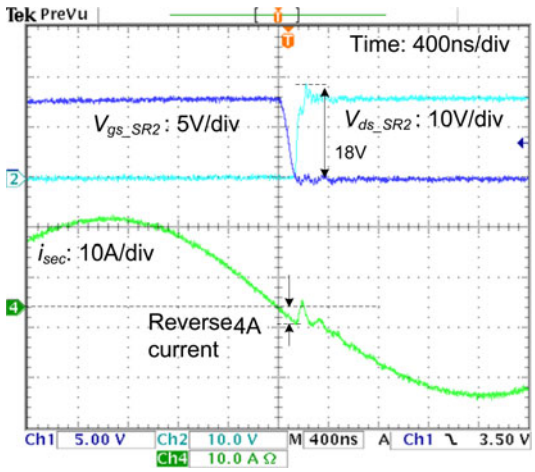

Fig. 13. SR voltage spikes in a voltage-doubler rectifier with small SR turn-OFF leading time.

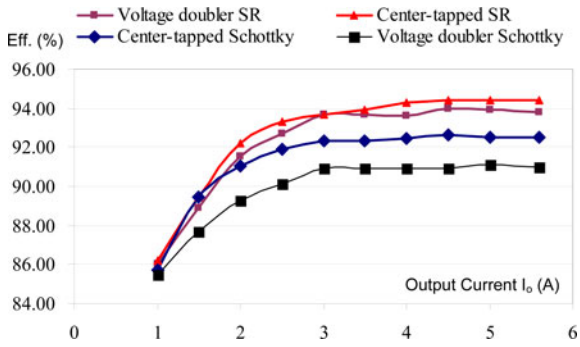

Fig. 14. Measured efficiency of the prototypes.

structure, which is mainly caused by the high conduction loss of the Schottky diode in the voltage-doubler structure. Compared to the efficiency from the center-tapped rectifier with the Schottky diode, using the proposed SR, the efficiency is 1.5% higher.

The measured efficiency of the prototypes is not very high as those reported. This is because the efficiency of the *LLC* converter is heavily affected by the resonant parameters design, especially the inductance ratio (L_m/L_r) and characteristic factor Q. In the prototype, the input voltage for the prototype ranges from 300 to 420 V, which covers the DCM, critical DCM, and CCM operation to verify the operation of the proposed SR-driven method under all operation modes. The input or output voltage range will affect the prototype efficiency since the *LLC* resonant converter is not suitable for the wide I/O range operation. Therefore, the resonant parameters design of the prototype is not optimized to maximize the prototype efficiency. Furthermore, the passive components (such as magnetic components and capacitors) and PCB layout also affect the prototype efficiency, which should also be considered carefully in order to

improve the efficiency. Nevertheless, in this paper, we mainly focus on verifying the operation of the proposed SR-driving method, and the comparison is done based on the same prototype; therefore, the efficiency comparison is also reasonable.

The voltage-doubler rectifier has simple structure of transformer, which is more attractive for planar PCB transformers widely used in the brick dc/dc converter, since the secondary winding turns can be four times less. For higher output voltage applications, such as 24 V or similar, the SR voltage rating difference will be bigger compared to the center-tapped rectifier as discussed earlier; thus, the advantage of the proposed voltage-doubler rectifier will be more significant.

V. Conclusion

In this paper, we present a current-driving scheme for SR with trapezoid voltage-doubler rectifier structure for the *LLC* resonant converter. The voltage-doubler structure can reduce the SR's voltage rating without the existence of parasitic ring in the conventional center-tapped rectifier though the current rating is increased. The SR voltage stress is well clamped to the output voltage under any condition, which improves the reliability of the circuit. The low voltage rating MOSFET with low ON resistance can be adopted as SRs to offset the increased current rating. The proposed driving method only uses a simple CT with one secondary winding to drive the two SRs in the voltage-doubler rectifier, which dramatically reduce the cost and complexity of the whole circuit. Due to the inherent energy-feedback mechanism, the proposed driving circuit also features low power loss and good performance. The experimental results from 16 V/5.6 A output prototypes confirm the theoretical analysis and the advantages mentioned earlier.

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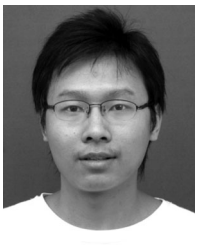
Junming Zhang (M'10) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1996, 2000, and 2004, respectively.

He is currently an Associate Professor at the College of Electrical Engineering, Zhejiang University. His research interests include power electronics system integrations, power management, and high-performance dc/dc converters and inverters.

Jiawen Liao was born in Chongqing, China, in 1985. He received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2008 and 2011, respectively.

He is currently at the Electric Power Research Institute of Chongqing Electric Power Corporation, Chongqing, China. His research interests include high-efficiency dc/dc converters, high power density dc/dc converters, and synchronous rectifiers.



Jianfeng Wang was born in Zhejiang, China, in 1987. He received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2009. He is currently working toward the M.S. degree in electrical engineering at Zhejiang University, Hangzhou, China.

His current research interests include high-efficiency dc/dc converters, synchronous rectifiers, and high-efficiency LED drivers.

Zhaoming Qian (SM'92) studied radio engineering and graduated from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1961, and he received the Ph.D. degree in applied science from the Catholic University of Leuven and the Interuniversity Microelectronics Center (IMEC), Leuven, Belgium, in 1989.

Since 1961, he has been involved in teaching and research work on electronics and power electronics at Zhejiang University. He has been a Professor in the Department of Electrical Engineering, Zhejiang University, since 1992. His main professional interests include power electronics and its industrial applications, power electronic system integration, and EMC in power electronic systems. He authored one book on EMC design and more than 200 papers.

Dr. Qian received Excellent Education Award from the China Education Commission and from Zhejiang University in 1993, 1997, and 1999, respectively, and the Science and Technology Development Award from the China Education Commission in 1999 and 2003, respectively.