A Design Procedure for Optimizing the *LLC* Resonant Converter as a Wide Output Range Voltage Source

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***Abstract*—LLC resonant converter is one of the most suitable circuit topologies that have been introduced for designing constant output voltage switched-mode power supplies. In this paper, a design procedure is introduced for using this converter as a wide output range voltage source. Unlike constant output voltage applications which need small converter inductance ratio and narrow switching frequency variations, for wide output range applications, large values of these parameters are needed simultaneously and should be optimized. Instead of minimizing the components stresses, leading to a great value of the inductance ratio, proper choice of the converter parameters resulting in a smaller inductance ratio has been done. Maximum value of the capacitor in parallel with the power MOSFETs drain-sources has been derived to realize the zero voltage switching operation in the converter inductive region. Soft switching is achieved for all power devices under all operating conditions. A prototype of the converter has been tested for different regulated output voltages (35–165 V_{dc}) under different loads (0–3 A_{dc}) and input voltages (320–370 V_{dc}) for using an ion implanter arc power supply, with maximum efficiency value of 94.7%. Experimental results confirm the high performance of the wide output range LLC resonant converter even under the worst case conditions.**

***Index Terms*—*LLC* resonant converter, switched-mode power supply (SMPS), wide output range, zero current switching (ZCS), zero voltage switching (ZVS).**

NOMENCLATURE

a, n	Converter inductance ratio and transformer turns ratio.
$I_{\text{in}\,N}$ and $I_{\text{in}\,\max N}$	Normalized ac input current and its maximum value.
I_{out} and $I_{\text{out}\,\max}$	Output dc current and its maximum value.
I_{DSM1} and I_D	MOSFET drain-source and diode currents.
k_z	Converter's input impedance ratio.
V_{in}, $V_{\text{in}\,\min}$, and $V_{\text{in}\,\max}$	DC input voltage and its maximum and minimum values.
$V_{\text{in}\,N}$, $V_{\text{in}\,\min N}$, and $V_{\text{in}\,\max N}$	Normalized dc input voltage and its maximum and minimum values.
V_{out}, $V_{\text{out}\,\min}$, and $V_{\text{out}\,\max}$	DC output voltage and its maximum and minimum values.
$V_{\text{out}\,N}$, $V_{\text{out}\,\min N}$, and $V_{\text{out}\,\max N}$	Normalized dc output voltage and its maximum and minimum values.
V_{outFL} and V_{outNL}	DC output voltage under the maximum output current and no-load conditions.
V_{C_r}, $V_{r\text{out}}$	Resonant capacitor voltage and output ripple.
$V_{C_r\,\max}$, $V_{C_r\,\max N}$	Resonant capacitor maximum voltage and its normalized value.
V_{DSM} and V_{CAD}	Power MOSFET drain-source and power diode cathode–anode voltages.
V_{ARR}	Output voltage adjustable range ratio.
P_{out} and $P_{\text{out}\,\max}$	Output power and its maximum value.
Q and $Q_{\max L}$	Quality factor and its value for maximum output current and voltage.
f_r, f_s, $f_{s\,\min}$, and $f_{s\,\max}$	Resonant frequency, switching frequency, and its minimum and maximum values (in hertz).
f_n, $f_{n\,\min}$, and $f_{n\,\max}$	Normalized switching frequency and its minimum and maximum values (dimensionless), respectively.
Z_{in}, $Z_{\text{in}\,0}$, $Z_{\text{in}\,\infty}$, and $Z_{\text{in}\,N}$	Input impedance, its values at short-circuit and no-load conditions, and its normalized value.
$I_{D\text{peak}}$ and I_1	Output rectifier stage peak current and the converter resonant input current first harmonic.
$P_{\text{con.}}$ and $P_{\text{con.}\,\max}$	Conduction loss and its maximum value.
$P_{\text{con.}N}$ and $P_{\text{con.}\,\max N}$	Normalized conduction loss and its maximum value.
ΔT and λ	Converter dead time and the rectifier stage conduction angle.
ψ_1	Phase shift of the converter resonant input current first harmonic as compared to the power MOSFETs drain-sources square-wave voltage.
R_L, L_r, L_m, C_r, and C_{out}	Output load resistance, resonant inductance, magnetizing inductance, resonant capacitance, and output capacitance, respectively.
$\text{ESR}_{C_{\text{out}}}$	Output capacitor's equivalent series resistance.
C_p	Effective capacitance appeared in parallel with the power MOSFETs drain-sources.

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I. Introduction

THE LLC resonant converter has been widely used as a dc–dc converter, being one of the most suitable circuit topologies for designing constant output voltage switched-mode power supplies (SMPSs). This converter has been analyzed in [1]–[8]. Also, it has been used for designing a dc–dc converter with integrated magnetic approach [9]. The LLC resonant converter as a constant output voltage source with synchronous or diode rectifications as its output stage has been analyzed by many authors [10]–[13]. Soft-switched phase-shift full-bridge dc/dc converter has been used widely to design constant output voltage SMPSs [1], [14], [15]. But, phase-shift converters are not suitable for wide output voltage applications [14].

As mentioned earlier, many authors have analyzed the LLC resonant converter for constant output voltage applications. But there is a significant difference between constant $V_{\rm out}$, variable $I_{\rm out}$, and adjustable $V_{\rm out}$, variable $I_{\rm out}$ resonant converters. The latter is more general than the first. In earlier works, this converter has been used for designing wide output range SMPSs and it has been shown that by using frequency control, this converter can handle a wide-range of regulated output voltage even when input voltage and load have large variations [16]–[18]. To attain this purpose, zero voltage switching (ZVS) operation even under the worst case conditions is one of the most important subjects that must be realized for reducing electromagnetic interference (EMI) and improving the efficiency and performance of the converter. Output stage diodes of this converter are always turned ON and OFF with zero current switching (ZCS) which reduces the switching losses. In MOSFET-based primary-side LLC resonant converter, the ZVS operation causes lower dissipation than ZCS, because the switching losses of the reverse recovery process are eliminated [19].

Wide output voltage range is achievable from this topology since it has a variable voltage gain during a wide frequency variation. Stray inductances and parasitic capacitances of its components can be merged in the main elements. Moreover, without employing external components, soft switching can be achieved in the whole output voltage and load variation ranges, which makes it suitable for high switching frequencies. Considering these particular specifications illustrates that the LLC resonant topology is suitable for wide dynamic load and wide output voltage applications with a good light-load specification in its inductive region [17]. Until now, there has been no straightforward design procedure for optimizing the LLC resonant converter for these applications. A design procedure that can be derived based on the aforementioned conventional analyses has not included the output voltage variations. Thus, it can only be used for the constant output voltage applications, as can be concluded from [19]. Also, the given approaches in [16]–[18] need more investigation in order to be implemented, practically. According to the [19], the first-harmonic approximation (FHA) approach can only be used for analyzing the resonant converters near the resonant frequency. But here it is proved that this simple approach can be used for analyzing the wide output range voltage source LLC resonant converter even under the worst case conditions.

In this paper, designing a *wide output range* LLC resonant converter based on the FHA approach is investigated and a design procedure is introduced for optimizing this resonant converter for wide output voltage range and wide dynamic load applications. Unlike the pulsewidth modulation converters' soft-switching techniques [20], [21], we used auxiliary circuits to reduce the switching losses and EMI; in the proposed resonant converter, not only such circuits are not used, but also all of the parasitic elements are merged in the converter's main components. Therefore, its price, size, and weight are reduced as well.

LLC resonant-converter-normalized dc output voltage and its input impedance are derived based on the FHA approach in Sections II and III. Maximum and minimum values of the output voltage are calculated based on the FHA approach in Section IV. By accounting the higher order harmonics, minimum output voltage is calculated in Section V. Then, the converter output voltage adjustable range is derived in Section VI. Power MOSFET peak current, conduction losses, and maximum voltage of the resonant capacitor are calculated in Sections VII and VIII, respectively. Improving the converter performance under the light-load conditions is discussed in Section IX. The design procedure is introduced in Section X. Experimental results and conclusions are presented in Sections XI and XII, respectively. The effect of the power factor correction (PFC) converter's output voltage ripple on the LLC resonant converter's frequency variation range is discussed in Appendix I. The normalized output voltage and the resonant capacitor maximum voltage are calculated in Appendices II and III. The converter's input impedance ratio is defined in Appendix IV. Finally, the effects of the higher order harmonics are calculated in Appendix V.

II. LLC Resonant-Converter-Normalized DC Output Voltage

LLC resonant converter can be used for wide output range SMPSs for supplying output loads which change between full load and no load [16]. This converter and its ac equivalent circuit, based on the FHA approach, have been depicted in Fig. 1.

As we know from [22], the LLC resonant converter in constant output voltage applications has a flat voltage gain curve above the resonant frequency and the FHA approach is not accurate enough without the correction of higher harmonics. This is due to the presence of the higher order harmonics with high magnitudes. In the wide output range LLC resonant converter, the voltage gain has a selective characteristic as compared to the other applications. This subject reduces the higher order harmonics magnitudes effectively, and increases the accuracy of FHA approach. In Appendix IV, it has been proved that the FHA approach can be applied to the wide output range LLC resonant converter.

The FHA approach is based on the assumption that the power conversion from the source to the load through the resonant tank is associated with the fundamental harmonics of the currents and voltages involved. The other harmonics of the switching frequency are ignored [19]. In this equivalent circuit, R_o is

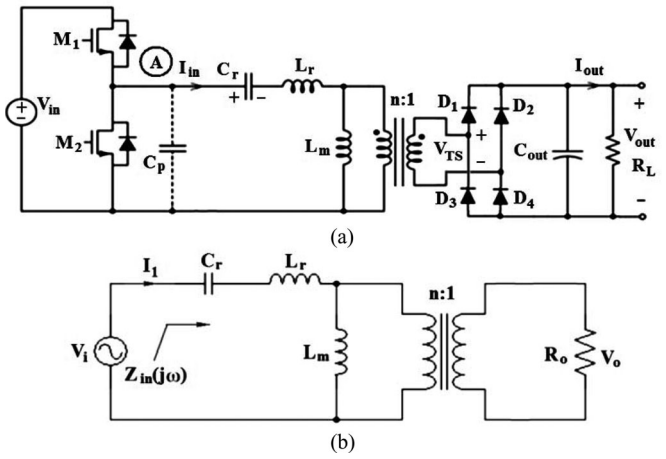

Fig. 1. LLC resonant converter. (a) Circuit topology. (b) AC equivalent circuit based on the FHA approach.

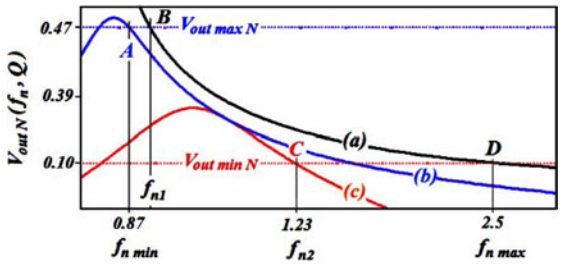

Fig. 2. Typical LLC resonant converter normalized dc output voltage versus f_n under different conditions. (a) $V_{\text{in}\,N} = 1.057$, $Q = 9 \times 10^{-3}$. (b) $V_{\text{in}\,N} = 0.914$, $Q = 0.539$. (c) $V_{\text{in}\,N} = 0.914$, $Q = 2.54$ [17].

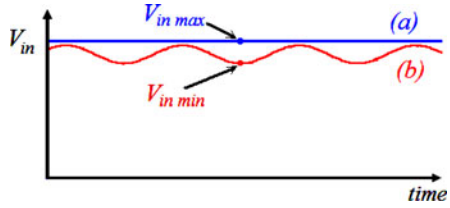

Fig. 3. PFC converter output voltage under two different conditions: (a) no load and (b) full load.

derived as follows [5], [16]–[19], [23]:

$$R_o = \frac{8}{\pi^2}\frac{V_{\text{out}}^2}{P_{\text{out}}} = \frac{8}{\pi^2}\frac{V_{\text{out}}}{I_{\text{out}}} = \frac{8}{\pi^2}R_L. \tag{1}$$

We would like to normalize the parameters to make them easier in description and in practice. The normalized dc input and output voltages are defined as follows:

$$V_{\text{in}\,N} = V_{\text{in}}/V_{\text{in norm}},\ V_{\text{out}\,N} = V_{\text{out}}/V_{\text{in norm}} \tag{2}$$

where

$$V_{\text{in norm}} = (V_{\text{in min}} + V_{\text{in max}})/2. \tag{3}$$

Using the FHA approach and considering (1), (2), and Fig. 1, the normalized dc-output voltage is obtained [17]

$$V_{\text{out}\,N}(a, Q, f_n) = \frac{V_{\text{in}\,N}}{2n\sqrt{\left(Qf_n\left(1 - f_n^{-2}\right)\right)^2 + \left(1 + a - af_n^{-2}\right)^2}} \tag{4}$$

where

$$a = \frac{L_r}{L_m},\quad f_n = \frac{f_s}{f_r},\quad Q = \frac{\pi^2 I_{\text{out}}}{8n^2 V_{\text{out}}}\sqrt{\frac{L_r}{C_r}},\quad f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \tag{5}$$

Equation (4) depends on Q, but this parameter is also a function of V_{out} (5). By inserting (5) into (4), the elliptical output characteristic of the LLC resonant converter is obtained, as derived in Appendix I (1A). The general form of the elliptical output characteristic of the resonant converters can be found in [14]. Using (4), the LLC converter-normalized dc-output voltage versus normalized switching frequency, for different values of Q and input and output voltages, has been plotted in Fig. 2 [17]. In this figure, the A-B interval illustrates the frequency variation range to regulate the maximum output voltage value.

In Fig. 2, the converter operates under the no-load conditions on curve (a) and the input voltage is maximum. On curve (b), minimum value of the input voltage has been applied to the converter. On this curve, the output current at point A is equal to the maximum desired value. The C-D interval illustrates the frequency variation range to regulate the minimum output voltage when input voltage or load changes in wide ranges. Thus, Fig. 2 intends to express that normalized frequency variations of $\Delta f_{n1} = f_{n1} - f_{n\,\min}$ and $\Delta f_{n2} = f_{n\,\max} - f_{n2}$ are required for compensating the input voltage and output load changes to regulate the output voltage at its maximum and minimum values, respectively. The converter input voltage is generated by a PFC stage, in practice. Therefore, the resonant converter input voltage is modulated by twice the line frequency, and its minimum value depends on the output voltage and current. To deliver the maximum output current to the output load, this minimum value only depends on the output voltage. The converted power under the minimum output voltage and maximum output current condition [point C on curve (c)] is lower than the maximum output power that occurs at maximum output voltage and maximum output current [point A on curve (b)]. In other words, $V_{\text{out min}} I_{\text{out max}} < V_{\text{out max}} I_{\text{out max}}$. Thus, when the resonant converter operates at point C, the resonant converter input voltage (PFC output voltage) does not approach to its minimum value which occurs at point A. This subject leads to a frequency variation smaller than Δf_{n2}, in practice.

As mentioned earlier, the presence of the second harmonic in the PFC converter output voltage and wide output load and input voltage changes leads to different input voltages for curves (b) and (c) in Fig. 2. In this figure, for simplifying the discussion, these input voltages have been considered to be equal in both previously mentioned cases. To identify the worst case of frequency variations for regulating each output voltage value, PFC converter output voltage under the no-load and full-load conditions has been plotted in Fig. 3. Boundary conditions of the LLC resonant converter input voltage have been shown in Fig. 3. To identify the frequency variation range for regulating each output voltage value, we note that the ripple in the output voltage of the PFC converter is proportional to the output power, but its frequency is twice the line frequency. So, the PFC stage output voltage is not fixed at a certain output power.

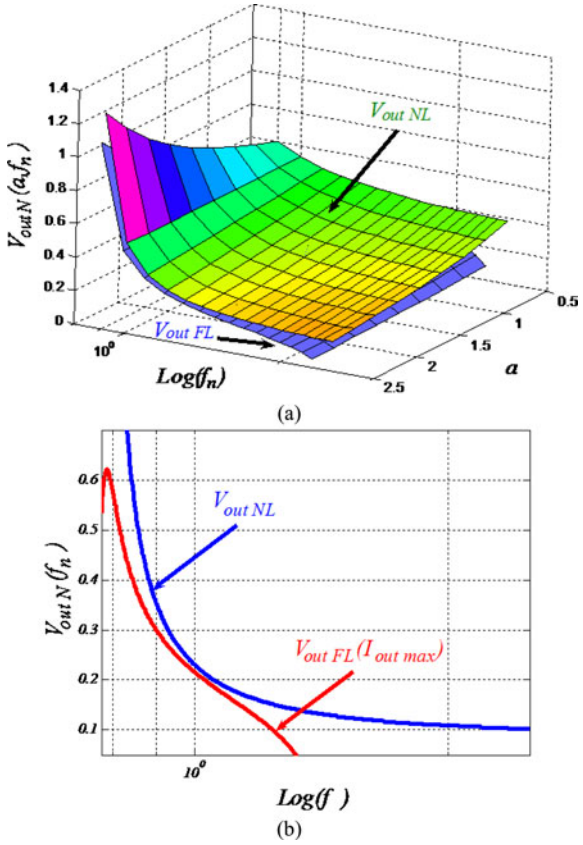

Fig. 4. $V_{\text{out}\,N}$ variations when output load changes between full-load and no-load conditions. (a) Versus f_n and a. (b) Versusf_n, $a = 1.5$.

From Appendix I, (5A) and (6A) include frequency variations to regulate the output voltage in a wide range while input voltage (320–370 V_{dc}) and output load (0–3 A_{dc}) change, as plotted in Fig. 4.

III. Calculating the LLC Resonant Converter Input Impedance

From (5) and Fig. 1(b), normalized input impedance of the equivalent circuit can be defined and expressed as follows:

$$Z_{\text{in}\,N} = \frac{Z_{\text{in}}\,(a, Q, jf_n)}{\sqrt{L_r/C_r}} = \frac{\chi}{Q\,(1+\chi)} + j\frac{\sqrt{\chi}}{Q}\left[a\left(1-\frac{1}{f_n^2}\right)+\frac{1}{1+\chi}\right] \tag{6}$$

where

$$\chi = \left(Qf_n/a\right)^2. \tag{7}$$

Equation (6) can be plotted versus output voltage, by considering (5A) and inserting (5) into (6) and (7), as shown in Fig. 5. Using larger values of a, to achieve wider output adjustable ranges, reduces the normalized input impedance. From (6), for the normalized input impedance value under the full-load condition, we can properly choose $\sqrt{L_r/C_r}$ to reduce the converter maximum input current. From Fig. 5, it is concluded that the circulating currents are reduced for low output voltage values which also reduce the conduction losses.

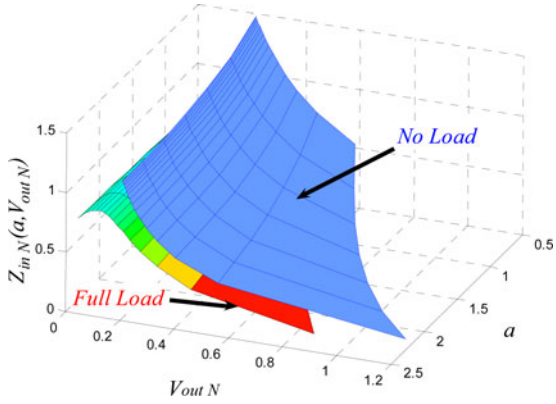

Fig. 5. Normalized magnitude of the input impedance versus normalized output voltage and a under the maximum output current and no-load conditions.

IV. Calculating Maximum and Minimum Values of the Output Voltage Based on the FHA Approach

For the given values of a and Q, the normalized output voltage is maximized when the imaginary part of the input impedance, i.e., $\text{Im}\,[Z_{\text{in}}]$, is zero. This can be concluded, easily, by considering Fig. 2. From this figure, the converter operates in the inductive region at frequencies above the frequency where the output voltage has peak value. On the other hand, at frequencies below the output voltage peak value, the converter operates in the capacitive region. Thus, somewhere between these areas, $\text{Im}\,[Z_{\text{in}}]$ must be zero.

As in Appendix II, from (12A), the normalized maximum output voltage under the full-load condition is obtained as follows:

$$V_{\text{out}\,\max N} = \sqrt{1 + a^2 Q_{\max L}^{-2} f_{n\,\min}^{-2}}\,\frac{V_{\text{in}\,\min N}}{2n}. \tag{8}$$

According to (8), maximum output voltage must be achievable even when minimum input voltage is applied to the converter. The LLC resonant converter available input voltage range, for achieving maximum output voltage, is determined by its peak voltage gain. Thus, the resonant network should be designed so that the gain curve has enough peak value to cover the input voltage range. As we know from [19], the ZVS operation is lost below the peak gain point in the LLC resonant converter capacitive region. Therefore, some margin is required for determining the maximum gain to guarantee stable ZVS operation during the transient conditions. Typically, 10–20% of the maximum gain is required as a margin for practical design. On the other hand, under the light- or no-load conditions $Q \approx 0$, minimum output voltage must be achievable even when maximum input voltage is applied to the converter. Considering (4), this value can be expressed in the normalized form

$$V_{\text{out}\,\min N} = \frac{V_{\text{in}\,\max N}}{2n\,(1 + a - af_{n\,\max}^{-2})}. \tag{9}$$

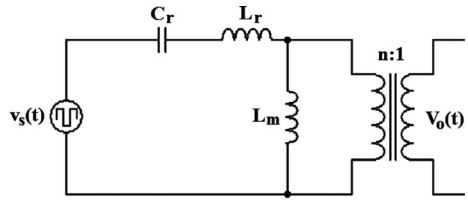

Fig. 6. LLC resonant converter simplified circuit under the no-load condition.

V. Calculating Minimum Value of the Output Voltage by Accounting the Higher Order Harmonics

As we know from [19], the FHA approach is valid and accurate enough at the region close to the resonant frequency. But for wide output range applications, FHA should not be applied directly without verification. Otherwise, it may be lead to significant errors. For wide range applications, A, B, and C operation points in Fig. 2 are close to the resonant frequency, practically. Thus, using the FHA approach in these points is acceptable. But according to Fig. 2, point D is far from the resonant frequency as compared to the other operating points. To calculate the induced error due to the FHA approach at this quiescent point, the converter can be simplified under the maximum input voltage, minimum output voltage, and no-load conditions. Under these conditions, the rectifying stage can be ignored. So, the switch network (M_1 and M_2) drives a linear time invariant (LTI) resonant tank network, as illustrated in Fig. 6. Therefore, dc output voltage of the converter is equal to the peak value of $v_o(t)$. By accounting the output-voltage higher order harmonics, more accurate calculations can be derived. Ignoring the dead-time intervals for simplicity, this switch network generates a symmetrical square-wave output voltage which can be expressed in the normalized form in the Fourier series as follows:

$$v_{sN}(t) = \frac{V_{\text{in}\max N}}{2} + \sum_{m=1,3,5,\ldots} \frac{2V_{\text{in}\max N}}{m\pi} \sin(m\omega_s t). \tag{10}$$

The dead-time value is usually chosen much smaller than the minimum switching period. In other words, $\Delta T \langle\langle T_{s\min}$ is always satisfied, practically. So, it can be concluded intuitively that ignoring this time interval does not introduce significant error in the derived expressions. From Fig. 6, under the no-load condition, the voltage gain of the converter is derived as follows:

$$h(j\omega_s) = \frac{V_o}{V_i} = \frac{j\omega_s L_m/n}{j\omega_s(L_r+L_m) - j/(\omega_s C_r)} = \frac{n^{-1}(1+a)^{-1}}{1-f_n'^{-2}}. \tag{11}$$

Here

$$f_n' = \sqrt{\frac{a}{1+a}} f_n. \tag{12}$$

Considering the superposition law in the aforementioned LTI circuit, the minimum value of the output voltage is obtained

$$v_{oN}(t) = \sum_{m=1,3,\ldots} \frac{2V_{\text{in}\max N}}{m\pi} |h(jm\omega_{s\max})| \times \sin(m\omega_{s\max} t - \psi_m). \tag{13}$$

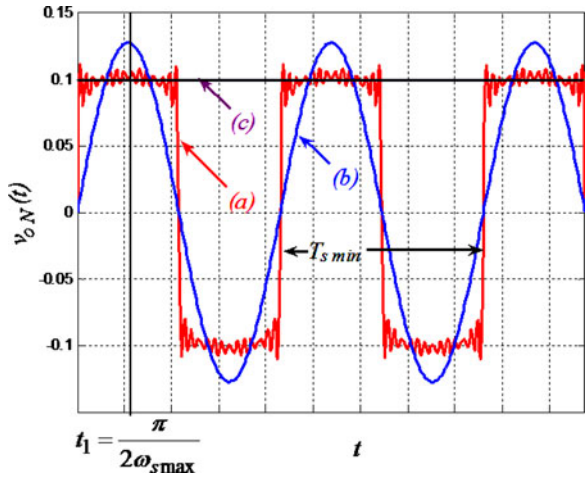

Fig. 7. Typical waveforms of (a) $v_{oN}(t)$, (b) first component of the normalized output voltage, and (c) $V_{\text{out}\min N}$ ($n = 2.33$, $V_{\text{in}\max N} = 1.057$, $a = 1.51$, $f_r = 126$ kHz, $f_{n\max} = 2.5$, and $m = 1, 2, 3, \ldots, 17$).

Here, $|h(jm\omega_{s\max})|$ and ψ_m are the magnitude and phase of $h(jm\omega_s)$, respectively

$$|h(jm\omega_{s\max})| = |h(j2\pi m f_r f_{n\max})| = \frac{1}{n(1+a)} \frac{m^2}{m^2 - f_{n\max}'^{-2}} \tag{14}$$

$$\psi_m = \angle h(jm\omega_{s\max}) = \begin{cases} 0 & f_{n\max}' \geq 1/m \\ \pi & f_{n\max}' < 1/m. \end{cases} \tag{15}$$

If $f_{n\max}' \geq 1$, then from (13), (14), and (15), the normalized output voltage of the converter is obtained

$$v_{oN}(t) = \sum_{m=1,3,5,\ldots} \frac{2V_{\text{in}\max N}}{n(1+a)\pi} \frac{m}{m^2 - f_{n\max}'^{-2}} \sin(m\omega_{s\max} t). \tag{16}$$

This normalized voltage has been plotted in Fig. 7. In Appendix V, equations for $f_{n\max}' < 1$ have also been derived. The minimum value of the normalized dc output voltage $V_{\text{out}\min N}$ is equal to the amplitude of $v_{oN}(t)$. Considering (16) and Fig. 7, we can calculate $V_{\text{out}\min N}$ as follows:

$$V_{\text{out}\min N} = \frac{2V_{\text{in}\max N}}{n\pi(1+a)} \sum_{m=1}^{\infty} \frac{(2m-1)(-1)^{m-1}}{(2m-1)^2 - f_{n\max}'^{-2}}. \tag{17}$$

This value has been shown in Fig. 7.

Two derived expressions [i.e., (9) and (17)] have been plotted in Fig. 8. In this figure, higher order harmonics up to 33 have been accounted to clarify that the FHA approach does not introduce significant error even under the worst case condition, at point D, which is far from the resonant frequency as compared to the other operating conditions.

A typical voltage transfer function of the LLC resonant converter under the different load conditions has been plotted in Fig. 9. As illustrated in this figure, the converter's voltage transfer function has become more selective by increasing the load current as compared to its no-load transfer function. Thus, under each output load condition, higher order harmonics ($3f_s$, $5f_s$,

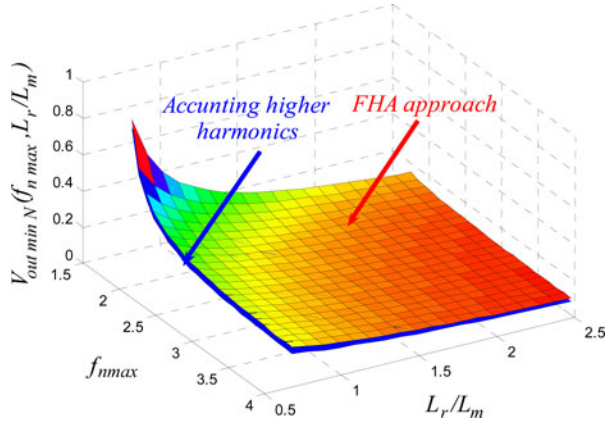

Fig. 8. Minimum value of the normalized dc output voltage under the no-load condition versus $f_{n\,\max}$ and L_r/L_m ($n = 2.33$, $V_{\text{in}\,\max\,N} = 1.057$).

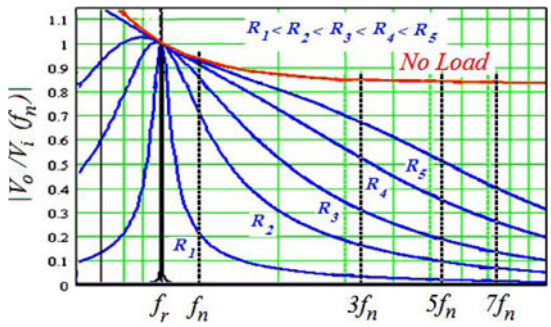

Fig. 9. Typical voltage gain of the LLC resonant converter versus normalized switching frequency at different loads ($a = 0.2$, proper for constant output).

$7f_s \ldots$) are reduced more than their values under the no-load condition, as shown in Fig. 9. So, it can be concluded that for each output voltage value, the introduced dominant error due to the FHA approach occurs under the no-load condition.

On the other hand, Figs. 7 and 8 show that this error can be ignored in wide output range applications of the LLC resonant converter even under the no-load condition due to its selective transfer function. Thus, using the FHA approach for analyzing this converter does not introduce significant error. Comparing the no load curves in Figs. 2 and 9 shows the differences of the no-load transfer functions of the LLC resonant converter in its constant ($a = 0.2$) and wide output range ($a = 1.44$) applications.

VI. Output Voltage Adjustable Range

According to Figs. 7 and 8, using the FHA approach for simplifying the analysis is well advised. This will be confirmed by the experimental results. Thus, FHA as a simple approach can be used to calculate the minimum dc output voltage, as well. From (8) and (9), adjustable range ratio of the output voltage can be defined and expressed as follows:

$$V_{\text{ARR}} = \frac{V_{\text{out}\,\max\,N}}{V_{\text{out}\,\min\,N}} = k\left(1 + a - af_{n\,\max}^{-2}\right) \times \sqrt{1 + a^2 Q_{\max\,L}^{-2} f_{n\,\min}^{-2}}. \quad (18)$$

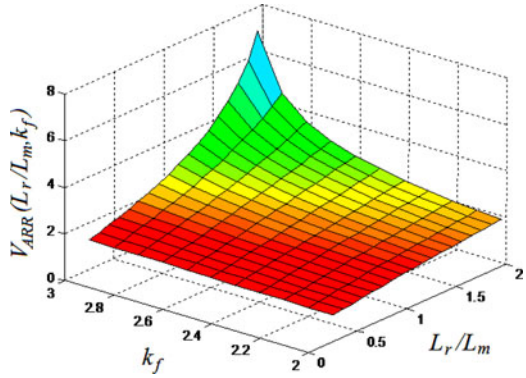

Fig. 10. V_{ARR} versus k_f and L_r/L_m ($k = 0.86$, $f_{n\,\max} = 2.5$).

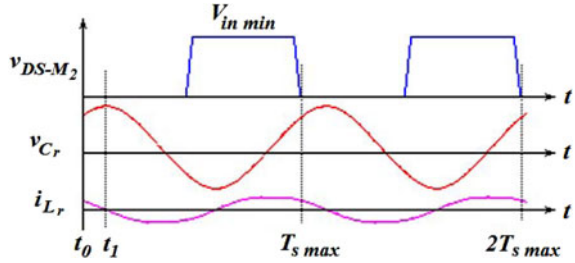

Fig. 11. Typical LLC resonant converter waveforms, power MOSFET drain–source voltage, resonant capacitor voltage, and resonant inductor current.

Here, $k = V_{\text{in}\,\min}/V_{\text{in}\,\max}$. Considering (10A) and (18), V_{ARR} can be simplified as

$$V_{\text{ARR}} = k\frac{1 + a - af_{n\,\max}^{-2}}{\sqrt{1 + a - af_{n\,\min}^{-2}}}. \quad (19)$$

We define the frequency variation range ratio as follows:

$$k_f = \frac{f_{n\,\max}}{f_{n\,\min}}. \quad (20)$$

Thus, (19) can be rewritten as

$$V_{\text{ARR}} = k\frac{1 + a - af_{n\,\max}^{-2}}{\sqrt{1 + a - ak_f^2 f_{n\,\max}^{-2}}}. \quad (21)$$

V_{ARR} has been plotted versus L_r/L_m and k_f in Fig. 10. As illustrated in this figure, unlike the constant output voltage applications of this converter (which need small values of L_r/L_m and narrow switching frequency variations), here, large values of these parameters are needed simultaneously, and they should be optimized by the designer.

VII. Power MOSFET Peak Current and Conduction Losses Under the Full-Load Condition

According to the FHA approach a sine-wave current can be used instead of the power MOSFET current $i_{\text{DS}M_2}$ during its conduction state [19]. Key waveforms of the LLC converter have been plotted in Fig. 11 for calculating the conduction losses of the power MOSFETs and peak value of the voltage of the

resonant capacitor. From Figs. 1 and 11, we can write

$$i_{\mathrm{DS}M_2}(t) = I_1 \sin(\omega t - \psi_1), \quad M_1 : \text{off}, \; M_2 : \text{on}. \tag{22}$$

Amplitude of the first harmonic of the square-wave output voltage of a half-bridge resonant converter is equal to $2V_{\mathrm{in}}/\pi$ [19]. From Fig. 1, (5), and (6), I_1 and ψ_1 are given as follows:

$$I_1 = \frac{2}{\pi}\sqrt{\frac{C_r}{L_r}}\frac{V_{\mathrm{in}}}{Z_{\mathrm{in}\,N}(a,Q,f_n)} \tag{23}$$

$$\psi_1 = \arctan\left[\left(a(1+\chi)\left(1-f_n^{-2}\right)+1\right)/\sqrt{\chi}\right]. \tag{24}$$

To simplify calculations of the power MOSFET conduction losses $P_{\mathrm{con}.M_2}$, we consider resistor r_{DS} instead of this device and its antiparallel diode in their on-state So, we can write

$$P_{\mathrm{con}.M_2} = \frac{1}{T_s}\int_0^{T_s/2} r_{\mathrm{DS}} i_{\mathrm{DS}M_2}^2(t)dt \approx \frac{1}{4} r_{\mathrm{DS}} I_1^2. \tag{25}$$

From (23) and (25), the normalized power MOSFET peak current and conduction losses are defined and calculated

$$I_{\mathrm{in}\,N} = \frac{I_1}{V_{\mathrm{in\,norm}}}\sqrt{\frac{L_r}{C_r}} = \frac{2}{\pi}\frac{V_{\mathrm{in}\,N}}{Z_{\mathrm{in}\,N}(a,Q,f_n)} \tag{26}$$

$$P_{\mathrm{con}.N} = \frac{P_{\mathrm{con}M_2}}{r_{\mathrm{DS}}V_{\mathrm{in\,norm}}^2 L_r/C_r} = \frac{1}{\pi^2}\frac{V_{\mathrm{in}\,N}^2}{Z_{\mathrm{in}\,N}^2(a,Q,f_n)}. \tag{27}$$

These parameters are increased monotonously, by increasing the output voltage at full-load conditions. Thus, maximum values of these parameters occurred at $V_{\mathrm{out\,max}\,N}$, $f_{n\,\min}$, $V_{\mathrm{in\,min}\,N}$, and $Q_{\max L}$. Substituting (7A) into (6), the normalized input impedance can be expressed as follows:

$$Z_{\mathrm{in}\,N} = \frac{1}{Q_{\max L}}\frac{\chi}{1+\chi} = \frac{Q_{\max L} f_{n\,\min}^2}{a^2 + Q_{\max L}^2 f_{n\,\min}^2}. \tag{28}$$

Inserting (28) into (26) and (27), the power MOSFET normalized peak current and conduction losses are derived

$$I_{\mathrm{in\,max}\,N} = \frac{2}{\pi}\frac{a^2 + Q_{\max L}^2 f_{n\,\min}^2}{Q_{\max L} f_{n\,\min}^2} V_{\mathrm{in\,min}\,N} \tag{29}$$

$$P_{\mathrm{con.\,max}\,N} = \frac{1}{\pi^2}\frac{\left(a^2 + Q_{\max L}^2 f_{n\,\min}^2\right)^2}{Q_{\max L}^2 f_{n\,\min}^4} V_{\mathrm{in\,min}\,N}^2. \tag{30}$$

VIII. Maximum Voltage of the Resonant Capacitor

As mentioned earlier, maximum values of the power MOSFET peak current and conduction losses occur at $V_{\mathrm{out\,max}\,N}$, $f_{n\,\min}$, $V_{\mathrm{in\,min}\,N}$, and $Q_{\max L}$. Also, maximum voltage of the resonant capacitor occurs under these operating conditions. As shown in Appendix III, the resonant capacitor maximum voltage in the normalized form is derived. From (15A), lower values of $f_{n\,\min}$ cause higher stresses on the resonant capacitor. Fig. 12 shows $V_{C_r\,\max N}$ versus a and $Q_{\max L}$. From this figure, for each value of a there is a value of $Q_{\max L}$ which minimizes the resonant capacitor voltage. $\partial V_{C_r\,\max N}/\partial Q_{\max L} = 0$ leads to

$$Q_{\max L} = a/f_{n\,\min}. \tag{31}$$

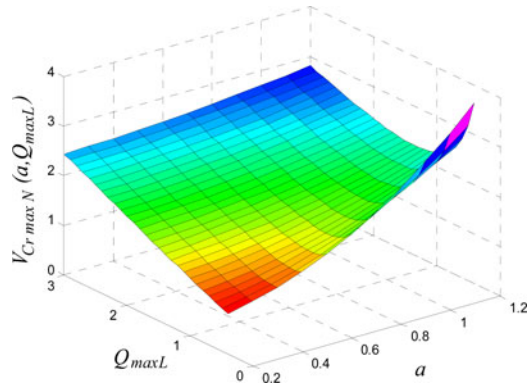

Fig. 12. $V_{C_r\,\max N}$ versus a and $Q_{\max L}$ ($V_{\mathrm{in\,min}\,N} = 0.93$ and $f_{n\,\min} = 0.9$).

The same results are given for the power MOSFET current (29) and conduction losses (30). Reducing the minimum switching frequency increases the stresses of the components of the resonant converter.

Considering (29), (30), (11A), and (15A), to reduce the frequency variation range and also the components' stresses, we have to choose $f_{n\,\min}$ as close as possible to unity ($f_{n\,\min} < 1$). To design the converter for realizing the aforementioned optimized stresses, from (31) and (18), the necessary value of a for achieving a desired value of V_{ARR} is obtained by

$$a = \frac{V_{\mathrm{ARR}}/(\sqrt{2}k) - 1}{1 - f_{n\,\max}^{-2}}. \tag{32}$$

Equation (32) illustrates that large values of a are necessary for achieving wide output voltage adjustable ranges. These values can be achieved easily by increasing L_r and decreasing L_m. This approach is useful for low values of the output voltage range. Its drawback is the necessity of high value of a which requires large external inductor to achieve wide output range.

To achieve wide output voltage range, a tradeoff between the converter inductance ratio and its components' maximum stresses leads to a smaller inductance ratio, instead of minimizing the components' stresses which leads to a great value of the converter inductance ratio. Considering (18) and (15A), V_{ARR} and $V_{C_r\,\max N}$ can be plotted versus a and $Q_{\max L}$, as illustrated in Fig. 13. A wide output voltage range converter can be designed for low values of $Q_{\max L}$, even when smaller values of a (for reducing the converter's cost) are used, as shown in Fig. 13(b). Nonetheless, the necessary values of a are high enough which cannot be achieved using merely transformer magnetizing and its primary-referred leakage inductances. Thus, using an external inductor is unavoidable.

IX. Improving the Converter Performance Under the Light-Load Conditions

The gate drive circuit must be able to sink charges of the MOSFET's gate-source capacitors and turn them OFF before their drain-source voltages rise significantly above zero. To assist the transistor turn-off process, small capacitor may be added

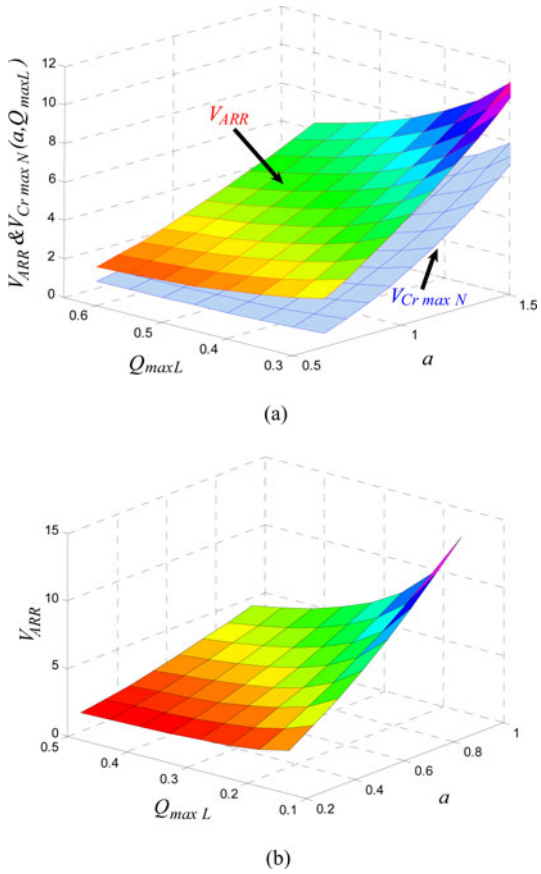

Fig. 13. (a) V_{ARR} and $V_{C_r\,\max N}$ versus $Q_{\max L}$ and a. (b) V_{ARR} versus small values of $Q_{\max L}$ and a ($f_{n\,\min} = 0.85$, $f_{n\,\max} = 2.5$).

in parallel with the drain-sources of the power MOSFETs. In Fig. 1(a), C_p is the summation of the added capacitor and the parasitic capacitors of the drain-sources of the power MOSFETs. Soft switching is one of the most important topics that must be satisfied for using the LLC resonant converter as a wide output range voltage source [24], [25]. To achieve ZVS operation at primary side of the converter at MOSFET turn-on times, the converter should operate in the inductive region and the resonant inductor's current must be high enough to charge or discharge C_p [16]. Amplitude of the circulating current should be reduced as much as possible to minimize the conduction losses of the converter; but the reduced circulating current may not be enough to satisfy the ZVS operation. In the inductive region of the LLC resonant converter, soft switching is achieved for all power devices even under the worst case conditions, by choosing dead-time value, C_p, and maximum switching frequency, properly. The worst case happens at light- or no-load conditions when output voltage is adjusted at its minimum value and maximum input voltage is applied to the converter. Under these conditions, the resonant inductor current is minimized. Thus, to charge and discharge C_p effectively during the given value of the dead time, maximum value of C_p should be limited, properly. By accounting the higher order harmonics of the resonant inductor current and ignoring the voltage dependence of the drain-sources parasitic capacitances, the necessary dead time for achieving the ZVS operation even under the worst case condition can be found, as reported in [17], [24], and [25]. Based on these analyses, maximum value of C_p is obtained

$$C_p = \frac{2\Delta T}{\pi}\sqrt{\frac{C_r}{L_r}}\frac{1+\left(\pi^2/8-1\right)\left(1-af_{n\,\max}^{-2}/(1+a)\right)}{f_{n\,\max}\left(1+a^{-1}-f_{n\,\max}^{-2}\right)}. \tag{33}$$

The selected dead time affects the efficiency of the converter, because the energy is not transferred from the primary side to the output load during this time interval, effectively, as can be concluded from [26]. Thus, the effective duty cycle for energy transferring is smaller for the longer dead times and higher input resonant currents are required to deliver the same output power as compared to the smaller dead-time values. So, the primary- and secondary-side conduction losses, turn-off switching losses, inductor and transformer losses are increased which reduce the converter efficiency under the full-load conditions. On the other hand, the ZVS operation is lost for smaller dead-time values under the light-load condition, leading to lower efficiency. Thus, the optimum value of the dead time can be chosen based on the efficiency considerations and specifications of the devices. Then, the maximum value of C_p is obtained from (33). The ZVS operation is lost above this value.

Reducing the amplitude of the input resonant current as low as possible to minimize the converter conduction losses is another important topic that must be satisfied for increasing the LLC resonant converter light-load performance. For a given value of the full-load impedance to obtain good efficiency at light loads, we should have $|Z_{\mathrm{in}\infty}(j\omega_{s\,\max})|\rangle\rangle|Z_{\mathrm{in}\,0}(j\omega_{s\,\min})|$. In other words, from (17A) and (18A), we must have

$$k_z = \left|\frac{Z_{\mathrm{in}\infty}(j\omega_{s\,\max})}{Z_{\mathrm{in}\,0}(j\omega_{s\,\min})}\right| = \frac{\left(1+a^{-1}\right)f_{n\,\max}^2-1}{1-f_{n\,\min}^2}\frac{f_{n\,\min}}{f_{n\,\max}}\rangle\rangle 1. \tag{34}$$

Larger values of k_z lead to higher values of the input impedance under the no-load conditions; this object reduces the converter input current under the no-load condition and improves the light-load efficiency. Higher value of k_z is desired, and it is limited by the frequency variation range and the components' stresses, and also by the output voltage range through the converter inductance ratio, as illustrated in (34). From this equation, the converter inductance ratio is derived

$$a = \left[f_{n\,\max}^{-2} + k_z\left(f_{n\,\min}^{-1} - f_{n\,\min}\right)/f_{n\,\max} - 1\right]^{-1}. \tag{35}$$

Considering (19) and (35), V_{ARR} can be expressed as follows:

$$V_{\mathrm{ARR}} = \frac{V_{\mathrm{in}\,\min}/V_{\mathrm{in}\,\max}}{\sqrt{\left(1-\frac{f_{n\,\max}}{k_z f_{n\,\min}}\frac{1-f_{n\,\max}^{-2}}{f_{n\,\min}^{-2}-1}\right)\left(1-\frac{f_{n\,\max}}{k_z f_{n\,\min}}\frac{f_{n\,\min}^{-2}-f_{n\,\max}^{-2}}{f_{n\,\min}^{-2}-1}\right)}}. \tag{36}$$

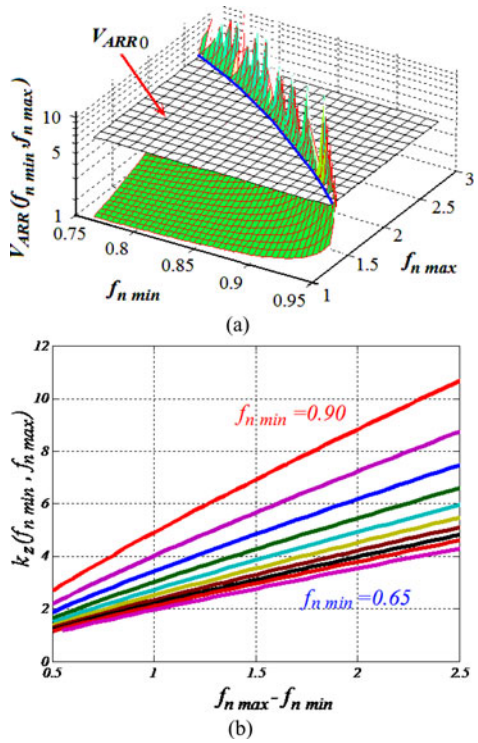

Fig. 14. V_{ARR} versus $f_{n\,\mathrm{min}}$ and $f_{n\,\mathrm{max}}$ ($k_z = 4.287$, $V_{\mathrm{in\ min}\,N} = 0.914$, and $V_{\mathrm{in\,max}\,N} = 1.057$, $V_{\mathrm{ARR0}} = 5.2$) (b) k_z versus $f_{n\,\mathrm{min}}$ and $f_{n\,\mathrm{max}}$ ($V_{\mathrm{ARR0}} = 5.2$ and difference between $f_{n\,\mathrm{min}}$ in two adjacent curves is $\Delta f_{n\,\mathrm{min}} = 0.025$).

Considering (36), the desired value of k_z is obtained as follows:

$$\left\{\begin{array}{l} \dfrac{1}{k_z} = \dfrac{1}{A} + \dfrac{1}{B} - \sqrt{\left(\dfrac{1}{A} - \dfrac{1}{B}\right)^2 + \dfrac{4}{AB}\dfrac{V_{\mathrm{in\,min}}^2}{V_{\mathrm{ARR}}^2 V_{\mathrm{in\,max}}^2}} \\ A = \dfrac{f_{n\,\mathrm{max}}}{f_{n\,\mathrm{min}}}\dfrac{1 - f_{n\,\mathrm{max}}^{-2}}{f_{n\,\mathrm{min}}^{-2} - 1}, B = \dfrac{f_{n\,\mathrm{max}}}{f_{n\,\mathrm{min}}}\dfrac{f_{n\,\mathrm{min}}^{-2} - f_{n\,\mathrm{max}}^{-2}}{f_{n\,\mathrm{min}}^{-2} - 1} \end{array}\right\}. \tag{37}$$

From (36), V_{ARR} has been plotted in Fig. 14(a). The intersection of (36) and V_{ARR0} shows the variations of $f_{n\,\mathrm{min}}$ and $f_{n\,\mathrm{max}}$ for achieving a desired value of V_{ARR0}, as plotted in Fig. 14(a).

By considering (37), k_z has been plotted in Fig. 14(b) versus $f_{n\,\mathrm{max}} - f_{n\,\mathrm{min}}$ for different values of $f_{n\,\mathrm{min}}$. From this figure, a tradeoff between higher values of k_z to improve the light-load efficiency and lower values of $f_{n\,\mathrm{max}} - f_{n\,\mathrm{min}}$ to achieve narrow switching frequency variation can easily be done.

X. Wide Output Range LLC Voltage Source Design Procedure

For the given values of $V_{\mathrm{in\,min}}$, $V_{\mathrm{in\,max}}$, $f_{s\,\mathrm{max}}$, and the desired values of $I_{\mathrm{out\,max}}$, $V_{\mathrm{out\,min}}$, and $V_{\mathrm{out\,max}}$, the converter can be designed as follows. The following parameters are considered, as the prototype converter required: $V_{\mathrm{in\,min}} = 320$ V, $V_{\mathrm{in\,max}} = 370$ V, $f_{s\,\mathrm{max}} = 315$ kHz, $I_{\mathrm{out\,max}} = 3.0$ A, $V_{\mathrm{out\,min}} = 35$ V, $V_{\mathrm{out\,max}} = 165$ V, and $V_{r\,\mathrm{out}} = 30$ mV).

Step 1: V_{ARR} should be plotted versus $f_{n\,\mathrm{min}}$ and $f_{n\,\mathrm{max}}$ for an assumed value of $k_z \rangle\rangle 1$, as shown in Fig. 14. Then, $f_{n\,\mathrm{min}}$ and $f_{n\,\mathrm{max}}$ for the desired value of V_{ARR} can be chosen.

Typically, 10–20% of the maximum output voltage adjustable range ratio is required as a margin to avoid the capacitive region even when the converter delivers maximum power to the output load and minimum input voltage is applied to the converter. (Assuming 10% margin for V_{ARR}, and plotting it for $k_z = 4.287 \rangle\rangle 1$, we can choose $f_{n\,\mathrm{min}} = 0.8$ and $f_{n\,\mathrm{max}} = 2.5$).

Step 2: a can be identified from (35) for the obtained values of $f_{n\,\mathrm{min}}$, $f_{n\,\mathrm{max}}$, and assumed value of $k_z (a = 1.51)$.

Step 3: Calculate the transformer turns ratio from (9) for the given values of $V_{\mathrm{in\,max}\,N}$, $V_{\mathrm{out\,min}\,N}$, and achieved values of a and $f_{n\,\mathrm{max}}$. [From (2) and (3), we have $V_{\mathrm{in\,max}\,N} = 1.057$ and $V_{\mathrm{out\,min}\,N} = 0.1$ which leads to $n = 2.33$].

Step 4: Calculate $Q_{\mathrm{max}\,L}$ from (10A) for the obtained values of a and $f_{n\,\mathrm{min}}$, ($Q_{\mathrm{max}\,L} = 0.795$). Now, $\sqrt{L_r/C_r}$ is identified from (9A) for the given values of $I_{\mathrm{out\,max}}$, $V_{\mathrm{out\,max}}$, and achieved value of n. (For $I_{\mathrm{out\,max}} = 3.0$ A and $V_{\mathrm{out\,max}} = 165$ V, we have $\sqrt{L_r/C_r} = 192.4\ \Omega$).

Step 5: f_r is obtained from (5) for the given value of $f_{s\,\mathrm{max}}$ and the obtained value of $f_{n\,\mathrm{max}}$ and then $\sqrt{L_r C_r}$ is identified (for $f_{s\,\mathrm{max}} = 315$ kHz and $f_{n\,\mathrm{max}} = 2.5$, we have $f_r = 126$ kHz and $\sqrt{L_r C_r} = 1.2631\ \mu$s/rad). Thus, L_r and C_r are given by accounting the identified value of $\sqrt{L_r/C_r}$ at the former step, L_m is obtained from (5), and $V_{C_r\,\mathrm{max}}$ is obtained from (15A). L_r is the summation of the transformer primary-referred leakage inductance and the added inductance to the converter to achieve large inductance ratio. (The calculations lead to $L_r = 243\ \mu$H, $L_m = 161\ \mu$H, $C_r = 6.6$ nF, and $V_{C_r\,\mathrm{max}} = 1.5$ kV.)

In general, transformers and inductors are two key parts of the converters. For properly choosing the core shape, material, and winding structure of these magnetic devices the designer should refer to, for example, [14] and [27].

Step 6: The power MOSFET peak voltage is equal to the maximum input voltage and its peak current can be obtained from (26) and (29) as follows:

$$I_{\mathrm{DSM1}} = I_1 = \sqrt{C_r/L_r}\, I_{\mathrm{in\,max}\,N} V_{\mathrm{in\,norm}} \tag{38}$$

(MOSFET peak voltage is 370 V and $I_{\mathrm{DSM1}} = I_1 = 5.59$ A).

Step 7: The optimum value of the dead time is achieved from the specifications of the identified power MOSFETs. From (33), calculate the maximum value of C_p for realizing the ZVS operation (Choosing $\Delta T = 350$ ns leads to $C_p \leq 373.5$ pF).

Step 8: The output rectifier peak voltage is equal to the maximum output voltage, and based on the FHA approach, the rectifier peak current can be obtained as follows:

$$I_{D\mathrm{peak}} \approx \frac{\pi^2}{2\lambda} I_{\mathrm{out\,max}}. \tag{39}$$

Here, $\lambda \leq \pi$ is the output rectifier stage conduction angle [23]. It can be plotted versus normalized operating frequency for different values of load coefficient and inductance ratio to identify the rectifier peak current, as depicted in [23]. Equations (38) and (39) can be used for calculating the currents rms values to select proper Litz wire for designing the external inductor and transformer windings. (The output rectifier peak voltage is equal to

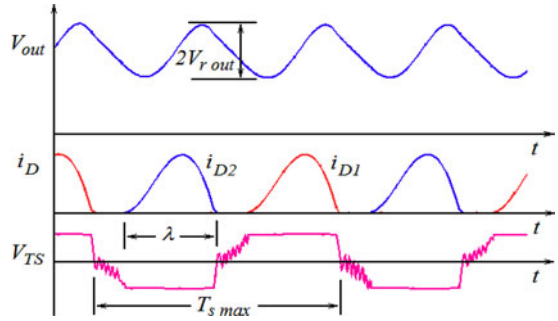

Fig. 15. Simulated waveforms of the LLC resonant converter under the full-load condition (i.e., $V_{\text{out max}}, I_{\text{out max}}$) to evaluate the specifications of C_{out}.

165 V. From [23], for $I_{\text{out max}} = 3$ A and the other obtained parameters, $\lambda = 2.2$. Thus, the output rectifier peak current is 6.7 A.) In practice, the margins of the device specifications must be chosen, properly. Based on the FHA approach, the power MOSFET's conduction losses under the maximum output current condition for different output voltage can be calculated by using (27). The resonant inductor and the transformer primary winding losses can be calculated by considering (26) for different output voltages. From (39), the transformer secondary winding losses and the output rectifying stage diodes' conduction losses can be calculated. For $I_{\text{out}} = I_{\text{out max}}$, these losses depend on the output voltage variations through λ, as shown in (39).

Step 9: Considering (39) and Figs. 1 and 15, capacitance of the output capacitor can be identified as follows:

$$C_{\text{out}} \geq \frac{1-\lambda/\pi}{f_{s\,\min}\left[\frac{4V_{r\,\text{out}}}{I_{\text{out max}}} - \text{ESR}_{C\text{out}}\left(\frac{\pi^2}{\lambda}-2\right)\right]}. \quad (40)$$

(If $I_{\text{out max}} = 3$ A, $\lambda = 2.2$, $V_{r\,\text{out}} = 25$ mV, $f_{s\,\min} = 101$ kHz, and $\text{ESR}_{C_{\text{out}}} \leq 10.5$ mΩ, then from (40), we should have $C_{\text{out}} \geq 410$ μF. Practically, $C_{\text{out}} = 470$ μF has been chosen.)

In practice, we prefer to design the converter with small frequency variation range and small component sizes. Using a design flowchart for evaluating the components' values and stresses is a good approach to arrive at a suitable tradeoff, as illustrated in Fig. 16. Initial values of a, I_{DSM}, and $V_{C_r\,\text{max}}$ can be calculated based on the given approach, as discussed in the different steps. According to the given design flowchart in Fig. 16, minimum switching frequency, minimum current and voltage stresses, minimum converter inductance ratio, and maximum efficiency under the full-load (lower $I_{\text{DS}\,M1}$) and no-load (higher k_z) conditions can be realized to achieve the desired output voltage adjustable range. If some parameters need to be smaller than the derived values, a tradeoff between these parameters and the others can be done. For example, if wider switching frequency variation range is available, then we can reduce the converter inductance ratio further, as can be concluded from Fig. 16.

To reduce the frequency variation range, small values of $f_{n\,\text{max}}$ are preferred and the aforementioned approach gives quite accurate results. For large values of $f_{n\,\text{max}}$, this procedure

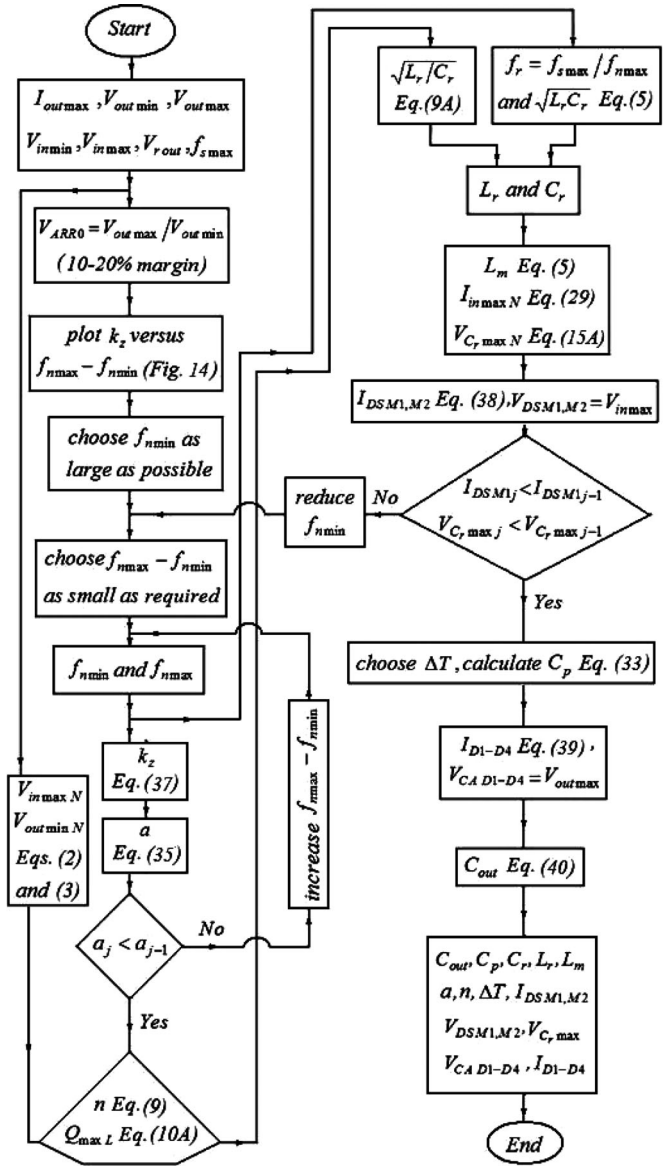

Fig. 16. Wide output range LLC resonant converter design flowchart.

is less accurate, but still valid, due to the presence of the higher order harmonics which have been ignored in the FHA approach for deriving the output voltage adjustment range. Thus, for applications in which large values of $f_{n\,\text{max}}$ are unavoidable, using a circuit simulator in addition to this procedure is useful.

Finally, it must be mentioned that the transient analysis and control design of the LLC resonant converter for constant output voltage applications have been discussed by many authors [7] and [28]–[32]. But these analyses do not cover wide output voltage with wide dynamic loading applications, and more investigations are necessary. When the output voltage is tried to be adjusted in a new desired value, the incorrect initial conditions for resonant components and the voltage gain mismatch cause high surge current in the circuit. Thus, the controller must be designed to have a proper and safe inrush current. Control design is very important and it should be studied in detail to achieve acceptable overshot and transient response at start-up for each

TABLE I
KEY PARAMETERS OF THE DESIGNED PROTOTYPE CONVERTER

	Parameter	Symbol	Value
1	Resonant Controller	-	L6599 (STMicroelectronics)
2	Power MOSFETs	M_1, M_2	2×STP12NM50
3	Power Diodes	$D_1 - D_4$	4×STTH802
4	Inductance-ratio	a	1.51
5	Resonant capacitance	C_r	$3\times 2.2\,nF$ 2kV
6	Magnetizing inductance	L_m	161 μH
7	Resonant inductance	L_r	243 μH
8	Effective cap. across the MOSFETs drain-sources	C_p	$\cong 330\,pF$
9	Dead-time	ΔT	350 ns
10	Transformer turns ratio	n	2.33
11	Output capacitor	C_{out}	470 μF

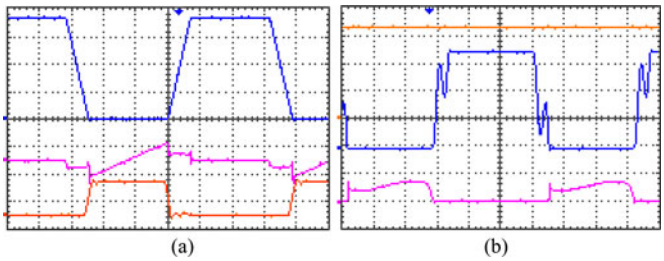

Fig. 17. LLC waveforms under the no-load condition $I_{\rm out} = 45$ mA, $V_{\rm out} = 33.15$ V, $V_{\rm in} = 370$ V, $f_s = 315$ kHz, time/division $= 500$ ns. (a) Primary-side waveforms. (Top) $v_{{\rm DS}M_2}$, 100 V/div. (Middle) $i_{{\rm DS}M_2}$, 250 mA/div. (Bottom) $v_{{\rm GS}M_2}$, 10 V/div. (b) Secondary-side waveforms. (Top) $V_{\rm out}$, 10 V/div. (Middle) $v_{{\rm KA}D_3}$, 10 V/div. (Bottom) i_{D_3}, 100 mA/div.

output voltage value, turn-off moments, and versus input/output voltages and load variations for the resonant converters in wide output voltage range applications. Here, a design procedure has been introduced for optimizing the converter power stage. Thus, it has been tested in steady state under different conditions, as briefly reported in the next section.

XI. EXPERIMENTAL RESULTS

The adapted resonant controller and key parameters of the designed converter have been tabulated in Table I. In this table, C_r is made from parallel-connected capacitors. To study the behavior of the designed converter under load and input voltage variations in steady state, it has been tested under different conditions. Figs. 17–19 show the corresponding experimental graphs. Fig. 17 shows the converter waveforms when maximum input voltage is applied to the converter and under the no-load condition its output voltage is adjusted at minimum value to illustrate the realization of the ZVS operation with maximum switching frequency.

As mentioned earlier, the gate drive circuit must be able to sink charges of the power MOSFET's gate-source capacitors and turn them OFF before their drain-source voltages rise signifi-

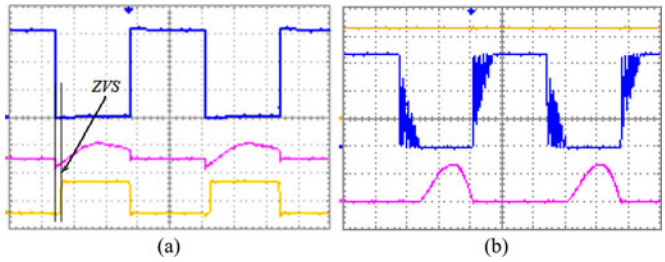

Fig. 18. LLC waveforms under the full-load condition $I_{\rm out} = 3$ A, $V_{\rm out} = 166.5$ V$_{\rm dc}$, $V_{\rm in} = 320$ V, $f_s = 107$ kHz, time/division $= 2\,\mu$s. (a) Primary-side waveforms. (Top) $v_{{\rm DS}M_2}$, 100 V/div. (Middle) $i_{{\rm DS}M_2}$, 5 A/div. (Bottom) $v_{{\rm GS}M_2}$, 10 V/div. (b) Secondary-side waveforms. (Top) $V_{\rm out}$, 50 V/div. (Middle) $v_{{\rm KA}D_3}$, 50 V/div. (Bottom) i_{D_3}, 5 A/div.

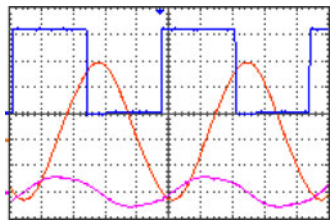

Fig. 19. LLC different waveforms under the full-load condition $I_{\rm out} = 3$ A, $V_{\rm out} = 166.5$ V$_{\rm dc}$, $V_{\rm in} = 320$ V , time/division $= 2\,\mu$s, $f_s = 107$ kHz. (Top) $v_{{\rm DS}M_2}$, 100 V/div. (Middle) v_{C_r}, 500 V/div. (Bottom) i_{C_r}, 5 A/div.

cantly above zero. To assist the transistor turn-off process, small capacitor C_p may be added in parallel with the drain-sources of the power MOSFETs, as shown in Fig. 1(a). So, the power MOSFET turn-off switching losses can be reduced. Choosing C_p, maximum switching frequency, and dead-time values properly, the power MOSFETs are switched ON and OFF without any ringing, as shown in Fig. 17(a). Thus, the ZVS operation is achieved even under the worst case conditions, i.e., light- or no-load condition, minimum output, and maximum input voltages.

Choosing C_p, maximum switching frequency, and dead-time values improperly generates ringing at MOSFET turn-on times (no more ZVS operation) under the worst case condition. These ringings are associated with the stored energy in C_p and the stray inductances of the circuit at MOSFETs turn-on times. Fig. 18 illustrates the converter primary- and secondary-side experimental waveforms to deliver maximum power to the output load when minimum input voltage (320 V$_{\rm dc}$) is applied to the converter. As shown in this figure, ZCS is achieved at the output rectifier stage. This subject is realized for whole output load and input and output voltages' variation ranges.

In Fig. 18(a), drain-source voltage rise and fall times are approximately equal to 63 and 52 ns, respectively. These time intervals are much smaller than the necessary dead time [see Fig. 17(a)]. This is due to the higher values of the drain-source current under the full-load condition at turn ON and OFF times, as compared to the conditions under which the given waveforms in Fig. 17(a) have been measured. Discontinuous conduction mode (DCM) operation of the converter output rectifying stage occurs below the resonant frequency. Thus, the output rectifying stage diodes' conduction angles are less than π, as

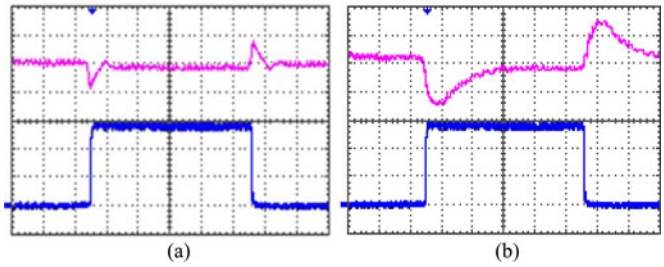

Fig. 20. Load-step responses of the designed converter at two different conditions, time/division =50 μs. (a) $V_{\rm out}$ = 165 $V_{\rm dc}$, $V_{\rm in}$ = 320 V. (Top) $V_{\rm out}$, 2V/div. (Bottom) $I_{\rm out}$, 1 A/div. (b) $V_{\rm out}$ = 35 $V_{\rm dc}$, $V_{\rm in}$ = 360 V. (Top) $V_{\rm out}$, 0.5 V/div. (Bottom) $I_{\rm out}$, 1 A/div.

TABLE II
COMPARING THE PROTOTYPE CONVERTER CALCULATED AND EXPERIMENTAL RESULTS

	Parameter	*Symbol*	*Experimental*	*Calculation*
1	*Input voltage*	V_{in}	320 – 370 *V dc*	320 – 370 *V dc*
2	*Output current*	I_{out}	44 *mA* – 3 *A dc*	0 – 3 *A dc*
3	*Output voltage*	V_{out}	33.1 – 166.5 *V dc*	35 – 165 *V dc*
4	*Switching frequency*	f_s	107 – 315 *kHz*	101 – 315 *kHz*
5	*Resonant capacitor voltage*	$V_{C_r \max}$	1.5 *kV*	1.5 *kV*
6	*MOSFET current*	I_1	5.7 *A*	5.59 *A*
7	*Rectifier current*	$I_{D\,peak}$	6.8 *A*	6.7 *A*
8	*Efficiency*	-	*94.7%*	-

illustrated in Fig. 18(b). When the rectifying stage operates in DCM, transformer secondary-side leakage inductance and rectifying-stage parasitic capacitance cause some ringing, as shown in Figs. 17(b) and 18(b).

Fig. 19 illustrates the LLC resonant converter primary-side waveforms to deliver maximum power to the output load when minimum input voltage (320 $V_{\rm dc}$) is applied to the converter. Smaller output voltages are converted at higher switching frequencies to deliver the same output current to the output loads. Generally, higher switching frequencies generate higher inductor's and transformer's core losses, but higher frequencies increase the input impedance which leads to lower circulating currents, lower semiconductors conduction losses, and lower transformer's and inductor's core and copper losses.

Finally, load-step responses of the designed converter at two different conditions have been illustrated in Fig. 20. The converter has a good closed-loop load transient response in both cases. The designed prototype converter calculated and experimental results have been tabulated in Table II. As shown in this table and also illustrated in Figs. 17–20, the experimental results are in good agreement with the calculated values.

Efficiency of the prototype voltage source versus output current has been plotted in Fig. 21 under two different conditions. Under light loads, the efficiency is reduced, due to increasing

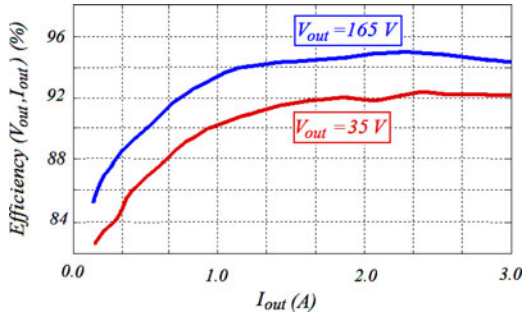

Fig. 21. Efficiency of the wide output range LLC resonant converter versus output current for maximum and minimum values of the output voltage (the LLC resonant converter input voltage modulated by twice of the line frequency, its variations depend on its output load, due to the poor load regulation of the PFC stage. These variations are limited between 320 and 370 V).

the switching frequency and increasing the reactive power which occurred in the constant output voltage applications of the LLC resonant converter. Also, in general, the circulating currents in the resonant converters do not reduce proportional to the output load reduction.

When output load varies between light- and full-load conditions, power losses of the output diodes vary proportional to the output load. But this is not true with power MOSFETs and transformer losses, due to the aforementioned reasons and no ZVS operation of the power MOSFETs at turn-off times. Because of the soft-switching operation of the LLC resonant converter, increasing the input voltage reduces the conduction losses and improves its efficiency for the chosen power MOSFETs.

XII. CONCLUSION

A design procedure has been introduced for designing wide output range voltage source based on the LLC resonant converter. For this purpose, converter large inductance ratio and wide switching frequency variations are needed simultaneously, which should be optimized. Power MOSFET peak current and conduction losses, maximum voltage of the resonant capacitor, and output voltage adjustable range have been calculated based on the FHA approach. Considering the optimum deadtime value and maximum switching frequency, the maximum value of the capacitance appeared in parallel with the power MOSFETs drain-sources has been identified to realize the ZVS operation in the inductive region. A tradeoff between the converter inductance ratio and its components' maximum stresses for achieving wide output voltage range causes a smaller inductance ratio. Nonetheless, the necessary inductance ratio cannot be achieved using merely transformer magnetizing and its primary-referred leakage inductances, and using an external inductor is unavoidable. A developed prototype of the converter has been tested for different regulated output voltages (35–165 $V_{\rm dc}$) under different loads (0–3 $A_{\rm dc}$) and input voltages (320–370 $V_{\rm dc}$) conditions with maximum efficiency of 94.7% for using as an ion implanter arc power supply.

APPENDIX I

EFFECT OF THE PFC CONVERTER'S OUTPUT VOLTAGE RIPPLE ON THE LLC RESONANT CONVERTER'S FREQUENCY VARIATION RANGE

Inserting (5) into (4) we can write

$$4n^2\alpha^2 I_{\text{out}}^2 + 4n^2\beta^2 V_{\text{out}}^2 = V_{\text{in}}^2. \tag{1A}$$

Here

$$\alpha = r f_n \left(1 - f_n^{-2}\right), \quad \beta = \left(1 + a - a f_n^{-2}\right), \quad r = \frac{\pi^2}{8n^2}\sqrt{\frac{L_r}{C_r}}. \tag{2A}$$

We can consider this simplifying assumption that the resonant converter input voltage varies between its minimum and maximum values proportional to the output power, due to the existence of the second harmonic in the PFC converter output voltage and its poor regulation. Therefore, by considering Fig. 3, lower value of the LLC converter input voltage can be written as follows for each output power value:

$$V_{\text{in}} = V_{\text{in}\max} - \left(V_{\text{in}\max} - V_{\text{in}\min}\right)\frac{P_{\text{out}}}{P_{\text{out}\max}}. \tag{3A}$$

In fact, there is a nonlinear relationship between the resonant converter input voltage and output power which complicates the calculations. But we can consider a linear behavior for simplicity. So, for maximum output current we have

$$V_{\text{in}} = V_{\text{in}\max} - M V_{\text{outFL}}, \; M = (V_{\text{in}\max} - V_{\text{in}\min})/V_{\text{out}\max}. \tag{4A}$$

Considering (1A) and (4A), this output voltage value can be derived as follows:

$$V_{\text{out FL}} = \frac{2n\sqrt{\beta^2 V_{\text{in}\max}^2 + \alpha^2(M^2 - 4n^2\beta^2)I_{\text{out}\max}^2} - M V_{\text{in}\max}}{4n^2\beta^2 - M^2}. \tag{5A}$$

Also, from (4), (2A), and (3A), the output voltage under the no-load condition can be expressed as follows:

$$V_{\text{out NL}} = \frac{V_{\text{in}\max}}{2n\beta}. \tag{6A}$$

Equations (5A) and (6A) include frequency variations to regulate the output voltage in a wide range while input voltage and output load change.

APPENDIX II

CALCULATING THE NORMALIZED MAXIMUM OUTPUT VOLTAGE

Considering (7) and equating imaginary part of (6) to zero and rearranging it, we can write

$$\frac{1}{f_{n\min}^2} = 1 + \frac{1}{a\left(1 + \chi_m\right)} \tag{7A}$$

where

$$\chi_m = \left(Q_{\max L} f_{n\min}/a\right)^2. \tag{8A}$$

Considering (5), we have

$$Q_{\max L} = \frac{\pi^2 I_{\text{out}\max}}{8n^2 V_{\text{out}\max}}\sqrt{\frac{L_r}{C_r}}. \tag{9A}$$

Substituting (8A) into (7A), $Q_{\max L}$ is given as follows:

$$Q_{\max L} = \sqrt{a\left(1 - f_{n\min}^2\right)^{-1} - a^2 f_{n\min}^{-2}}. \tag{10A}$$

To obtain a real value for $Q_{\max L}$, we should have

$$a \le f_{n\min}^2/\left(1 - f_{n\min}^2\right), \quad f_{n\min} < 1. \tag{11A}$$

Considering (7A), (8A), and (4), $V_{\text{out}\max N}$ is obtained

$$V_{\text{out}\max N} = \sqrt{1 + a^2 Q_{\max L}^{-2} f_{n\min}^{-2}}\,\frac{V_{\text{in}\min N}}{2n}. \tag{12A}$$

APPENDIX III

DERIVING THE RESONANT CAPACITOR MAXIMUM VOLTAGE

According to Fig. 1 and considering (5), (6), and $V_i = 2V_{\text{in}\min}/\pi$, peak value of the ac voltage of the resonant capacitor is given as follows:

$$V_{C_r} = \frac{I_1}{2\pi f_{s\min} C_r} = \frac{1}{2\pi f_{s\min} C_r}\frac{V_i}{|Z_{\text{in}}|} = \frac{2}{\pi}\frac{V_{\text{in}\min}}{f_{n\min} Z_{\text{in}N}}. \tag{13A}$$

Considering the resonant capacitor dc voltage $V_{\text{in}\min}/2$, its maximum voltage in the normalized form is derived

$$V_{C_r\max N} = \frac{V_{C_r\max}}{V_{\text{in norm}}} = \left(\frac{1}{2} + \frac{2}{\pi}\frac{1}{f_{n\min} Z_{\text{in}N}}\right) V_{\text{in}\min N}. \tag{14A}$$

Considering (28), this maximum value is rearranged as follows:

$$V_{C_r\max N} = \left[\frac{1}{2} + \frac{2}{\pi}\frac{a^2 + Q_{\max L}^2 f_{n\min}^2}{f_{n\min}^3 Q_{\max L}}\right] V_{\text{in}\min N}. \tag{15A}$$

APPENDIX IV

DEFINING THE CONVERTER INPUT IMPEDANCE RATIO

Considering Fig. 1(b), the converter input impedances under the output short- and open-circuit conditions are derived

$$Z_{\text{in}0}(s) = \frac{1}{C_r s} + L_r s, \; Z_{\text{in}\infty}(s) = \frac{1}{C_r s} + (L_r + L_m)s. \tag{16A}$$

We define the converter's input impedance ratio as follows:

$$k_z = \left|\frac{Z_{\text{in}\infty}(j\omega_{s\max})}{Z_{\text{in}0}(j\omega_{s\min})}\right|. \tag{17A}$$

Here, $\omega_{s\min}$ and $\omega_{s\max}$ are corresponding to $f_{n\min}$ and $f_{n\max}$, respectively. Considering (5), (16A), and (17A), k_z can be expressed as follows:

$$k_z = \frac{\left(1 + a^{-1}\right) f_{n\max}^2 - 1}{1 - f_{n\min}^2}\frac{f_{n\min}}{f_{n\max}}. \tag{18A}$$

$$V_{\text{out}\min N}=\begin{cases}\dfrac{2V_{\text{in}\max N}}{n\pi\left(1+a\right)}\left[\displaystyle\sum_{m=1}^{l-1}\frac{\left(2m-1\right)\left(-1\right)^{m}}{\left(2m-1\right)^{2}-f_{n\max}^{\prime-2}}+\sum_{m=l}^{\infty}\frac{\left(2m-1\right)\left(-1\right)^{m-1}}{\left(2m-1\right)^{2}-f_{n\max}^{\prime-2}}\right], & \dfrac{1}{l}\le f_{n\max}^{\prime}<1\\ \dfrac{2V_{\text{in}\max N}}{n\pi\left(1+a\right)}\displaystyle\sum_{m=1}^{\infty}\frac{\left(2m-1\right)\left(-1\right)^{m-1}}{\left(2m-1\right)^{2}-f_{n\max}^{\prime-2}}, & f_{n\max}^{\prime}\ge 1.\end{cases}\tag{23A}$$

APPENDIX V
ACCOUNTING THE EFFECTS OF THE HIGHER ORDER HARMONICS

To account the effects of the higher order harmonics, (18), (19), (21), and (32) should be rewritten as follows, respectively

$$V_{\text{ARR}}=\frac{V_{\text{out}\max N}}{V_{\text{out}\min N}}=\frac{k\pi\left(1+a\right)}{4}\frac{\sqrt{1+a^{2}Q_{\max L}^{-2}f_{n\min}^{-2}}}{\sum_{m=1}^{\infty}\frac{(2m-1)(-1)^{m-1}}{(2m-1)^{2}-f_{n\max}^{-2}}}\tag{19A}$$

$$V_{\text{ARR}}=\frac{k\pi\left(1+a\right)/4}{\sqrt{1+a-af_{n\min}^{-2}}\sum_{m=1}^{\infty}\frac{(2m-1)(-1)^{m-1}}{(2m-1)^{2}-f_{n\max}^{-2}}}\tag{20A}$$

$$V_{\text{ARR}}=\frac{k\pi\left(1+a\right)/4}{\sqrt{1+a-ak_{f}^{2}f_{n\max}^{-2}}\sum_{m=1}^{\infty}\frac{(2m-1)(-1)^{m-1}}{(2m-1)^{2}-f_{n\max}^{-2}}}\tag{21A}$$

$$a=V_{\text{ARR}}\frac{2\sqrt{2}}{k\pi}\sum_{m=1}^{\infty}\frac{\left(2m-1\right)\left(-1\right)^{m-1}}{\left(2m-1\right)^{2}-f_{n\max}^{-2}}-1.\tag{22A}$$

These equations can be applied for $f_{n\max}^{\prime}\ge 1$. By considering the minimum normalized dc output voltage for different values of $f_{n\max}^{\prime}$ which can be derived as follows, similar equations can be obtained for $f_{n\max}^{\prime}<1$. Equation (23A) is as shown at the top of this page.

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