A DSP-Based Dual-Loop Peak DC-link Voltage Control Strategy of the Z-Source Inverter

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***Abstract*—This paper proposes a direct dual-loop peak dc-link voltage control strategy, with outer voltage loop and inner current loop, of the Z-source inverter (ZSI). The peak dc-link voltage is estimated by measuring both the input and capacitor voltages. With this proposed technique, a high-performance output voltage control can be achieved with an excellent transient performance including input voltage and load current variations with minimized nonminimum phase characteristics caused by the right half-plane zero in the control to peak dc-link voltage transfer function. Both controllers are designed based on a third-order small-signal model of the ZSI using the direct digital control method. The performance of the proposed control strategy is verified by simulation and experimental results of a 30-kW ZSI prototype.**

***Index Terms*—DC-link voltage control, direct digital control, dual-loop control, Z-source inverter.**

I. Introduction

THE Z-source inverter (ZSI), as shown in Fig. 1, is an emerging topology for power electronics dc–ac converters [1]. It can utilize the shoot-through (ST) state to boost the input voltage, which improves the inverter reliability and enlarges its application field. In comparison with other power electronic converters, it provides an attractive single-stage dc–ac conversion with buck–boost capability, reduced cost, reduced volume, and higher efficiency due to a lower component number. Therefore, the ZSI is a very promising and competitive topology for renewable energy sources, such as fuel cells, photovoltaic arrays and wind turbines, and new power electronics applications, such as electric and hybrid vehicles. As a research hotspot in power electronics converters, the ZSI topology has been greatly explored from various aspects, such as ST control methods [1]–[6], designing of the Z-network elements [7], [8], modeling of the ZSI [9]–[11], and feedback control strategies [12]–[23] in addition to the topology improvement [24]–[28].

Four ZSI shoot-through control methods have been proposed in the literature, which are simple boost control (SBC) [1], maximum boost control [2], maximum constant boost control (MCBC) [3], and modified space vector modulation boost control (MSVMBC) [4]. In [5], [6], the authors present a comparative study based on simulation and experimental results between these four ST control methods for different ZSI topologies with a conclusion that the MCBC method is the most suitable ST control methods for different ZSI topologies. The MCBC requires less inductor value and results in less switch voltage stress, less output current total harmonic distortion, better Z-network behavior, high obtainable ac output voltage and higher efficiency.

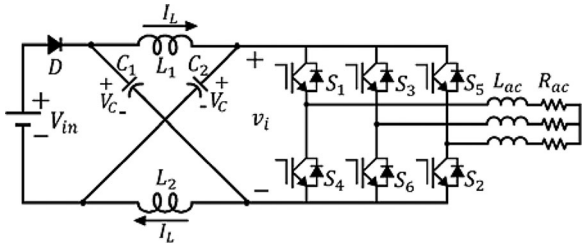

Fig. 1. ZSI basic structure.

The Z-network is a combination of two inductors and two capacitors, choosing the parameters of Z-network elements will affect the inverter performance and its operation modes. In order to avoid operating the ZSI in the unwanted operation modes, theses modes will not contribute to the power conversion process, which appear only when operating the ZSI with small inductance or at low power factor [7]. Therefore, a proper design guideline for selecting the ZSI passive and semiconductors elements is needed, as presented in [8].

An accurate small-signal model of the ZSI gives not only a global, but also a detailed view of the system dynamics, and provides the required transfer functions for controller design. Several small-signal models have been proposed for the ZSI [9]–[11]. In [9], a second-order model was presented, where the capacitor voltage and the inductor current of the Z-network are the state variables, in which the ac load was represented by a constant current source without any dynamics. However, in [10] and [11], a third-order model was presented by referring the ac side of the ZSI to its dc side, representing it with *RL* load and taking its current as a third state. Therefore, this model describes the dynamics of both the Z-network and the ac load.

Control strategies of the ZSI are important issue and several feedback control strategies have been investigated in recent publications [12]–[23]. There are four methods for controlling the dc-link voltage of the ZSI: capacitor voltage control [12]–[18], indirect dc-link voltage control [19], [20], direct dc-link control [21], [22], and unified control [23]. In [12] and [13], the

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capacitor voltage is controlled by regulating the ST duty ratio D_0 using different control methods, where, a PID controller is used to control the ST duty ratio and the modulation index is set to be $M = 1–D_0$ using the SBC method in [12]. While, in [13], a PI controller tuned by neural networks for wide range control is used with the MSVMBC method. In [14] and [15], the capacitor voltage is controlled by the regulating the ST duty ratio, and the output voltage is controlled by regulating the modulation index using the MSVMBC method through two separate control loops with PI controllers as in [14] and a neural network controllers as in [15]. In [16]–[18], nonlinear control methods are used to control the capacitor voltage using the SBC method, where the gain scheduling combined with a state feedback control method is used in [16], sliding mode control method was used in [17] and the model predictive control was used in [18]. In [19], a PID-like fuzzy controller is used to control the dc-link voltage indirectly by controlling its average value using the SBC method, where the average dc-link voltage is estimated by measuring the capacitor voltage V_C using $V_i = V_C /(1–D_0)$. Moreover, in [20], the peak dc-link voltage is controlled indirectly by controlling the peak ac output voltage using a PI controller to regulate the modulation index, and the ST duty ratio is calculated by measuring the input voltage $V_{\rm in}$ and comparing it by the required peak dc-link voltage V_{ip} using $V_{ip} = V_{\rm in} /(1–2D_0)$, where the MSVMBC method was used. In [21], the peak dc-link voltage is directly controlled by regulating the ST duty ratio; due to the pulsating nature of the peak dc-link voltage, an additional sensing circuit is used to measure it. This additional sensing circuit must to be carefully designed and it increases the complexity of the controller design. In [22], the peak dc-link voltage is directly controlled by regulating the ST duty ratio using the SBC method, where the peak dc-link voltage was estimated by measuring both the input and the capacitor voltages as $V_{ip} = 2V_C–V_{\rm in}$; however, this paper simplifies the inverter bridge by a single switch in its simulation and experimental validation. In [23], the unified control method is used to regulate the modulation index and the ST simultaneously by controlling the ac output voltage through a single PI controller using the MSVMBC method; however, this method is suitable for isolated operations.

The aforementioned methods have the following drawbacks. By controlling the capacitor voltage, the peak dc-link voltage will increase when there is a step change in the input voltage. Therefore, the ac output voltage will be distorted and the voltage stress of the switches will increase. Furthermore, the indirect control of the dc-link voltage cannot bring high performance due to the nonlinear property of the V_i /V_C relation. In addition, the existing direct peak dc-link voltage control methods, either using an external sensing circuit with special design or simplify the inverter bridge by a single switch. Finally, in all the aforementioned methods, a single-loop voltage control was used. In high-power converters, a single-loop voltage control has two problems. The first problem is that the inductor current is not regulated and can be overloaded during transient events and the limited stability margin is the second problem [29]. Therefore, a dual-loop voltage control is preferred over a single-voltage control in high-power converters to overcome the aforementioned problems [30], [31].

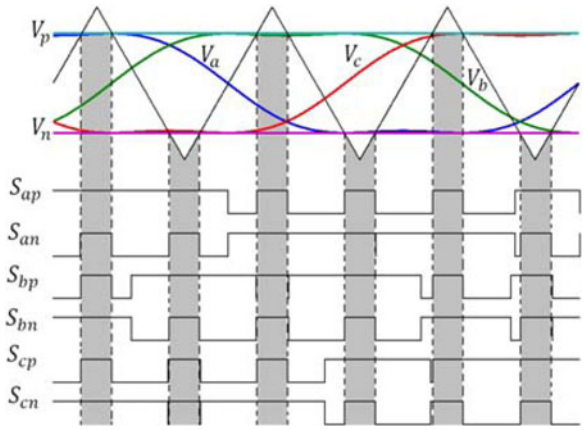

Fig. 2. MCBC method with 1/6 third-harmonic injection sketch map.

II. Shoot-Through Control Method

In order to reduce the volume and the cost of the passive elements of the Z-network, it is important to keep the ST duty ratio constant. At the same time, a greater voltage boost for any given modulation index is desired to reduce the voltage stress across the insulated gate bipolar transistors (IGBTs). The MCBC method achieves the maximum voltage gain while always keeping the ST duty ratio constant. Fig. 2 shows the sketch map of the MCBC with third-harmonic injection. By using a 1/6 of the third-harmonic injection, only two straight lines V_p and V_n are needed to control the ST time. In the MCBC, the ST duty is expressed by [3]

$$D_0 = \frac{2 - \sqrt{3}M}{2}. \tag{1}$$

III. Designing of the Impedance Network Elements

The Z-network is a combination of two inductors and two capacitors. The Z-network is the energy storage and filtering element for the ZSI. The purpose of the inductors is to limit the current ripples through the devices during boost mode with the ST state. Moreover, the purpose of the capacitor is to absorb the current ripples and maintain a constant voltage to keep the ac output voltage sinusoidal. In order to decrease the size and weight of the inductor and the capacitor, the ripples in inductor current and capacitor voltage should be limited. The changes of capacitor voltage and inductor current can be assumed as linear instead of sinusoidal for simpler analysis and designing of the Z-network [8].

For MCBC method the Z-network capacitor C and inductor L values can be expressed by [8]

$$C = \frac{\sqrt{3}(T_s/n)\,\hat{i}_{\rm ac}\,\cos\varphi\,(\sqrt{3}\hat{v}_{\rm ac} - V_{\rm in})}{4k_v\,V_{\rm in}(2\sqrt{3}\hat{v}_{\rm ac} - V_{\rm in})} \tag{2}$$

$$L = \frac{V_{\rm in}(T_s/n)(\sqrt{3}\hat{v}_{\rm ac} - V_{\rm in})}{\sqrt{3}k_i\hat{i}_{\rm ac}\cos\varphi(2\sqrt{3}\hat{v}_{\rm ac} - V_{\rm in})} \tag{3}$$

where, $\hat{v}_{\rm ac}$, $\hat{i}_{\rm ac}$, and cosφ are the peak ac output voltage, peak ac load current, and load power factor, respectively. k_v and k_i

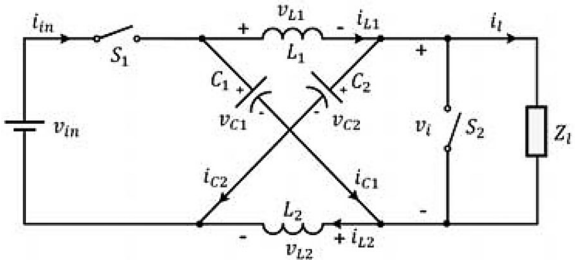

Fig. 3. Simplified equivalent circuit for the ZSI.

are voltage and current ripple factors, respectively. T_s is the switching period and n is the number of ST state insertion per switching cycle, where $n = 2$ for the MCBC method.

IV. Small-Signal Modeling of the ZSI

Many methods for modeling power electronic converters have been reported in the literature. Among these methods, is the state space averaged small-signal modeling, which is the most widely used method to model power electronic converters. Therefore, an accurate small-signal model of the ZSI is needed, which gives not only a global, but also a detailed view of the system dynamics, and provides guidelines for system controller design since the required transfer functions could be derived accordingly [32].

A third-order small-signal model of the ZSI can be illustrated by simplifying the ac side circuit to an equivalent dc load, $Z_l = R_l + j\omega L_l$ in parallel with a switch S_2 and the input diode D is represented by a switch S_1, as shown in Fig. 3 [10], where, R_l is calculated based on output power balance of the two circuits using the MCBC method (see Figs. 1 and 3) as follows:

$$R_l = \frac{2\,|Z_{\rm ac}|}{\cos\varphi}. \tag{4}$$

Here $|Z_{\rm ac}|$ is the magnitude of the ac load impedance per phase and cosφ is the load power factor. In addition, L_l is determined so that the time constant of the dc load is the same as the ac load as

$$\frac{L_l}{R_l} = \frac{L_{\rm as}}{R_{\rm ac}} \tag{5}$$

where $R_{\rm ac}$ and $L_{\rm ac}$ are the resistance and the inductance of the ac load per phase, respectively. Two operation modes involving two different circuit topologies can be identified in the ZSI operation as shown in Fig. 4. In Mode 1, ST mode [see Fig. 4(a)], the energy transferred from source to load is zero because the load side and source side are decoupled by the ST state and the open status of S_1. In Mode 2, nonshoot-through (NST) mode [see Fig. 4(b)], real energy transfer between source and load occurs.

The state variables are defined as capacitor voltage, inductor current, and ac load current. Assuming that $L1 = L2 = L$ and $C1 = C2 = C$, using state space averaging method, and performing small signal perturbation for a given operating point, one gets (6); after its Laplace transformation, it becomes (7). The steady-state values can be calculated by $\mathbf{Ax} + \mathbf{Bu} = \mathbf{0}$, represented

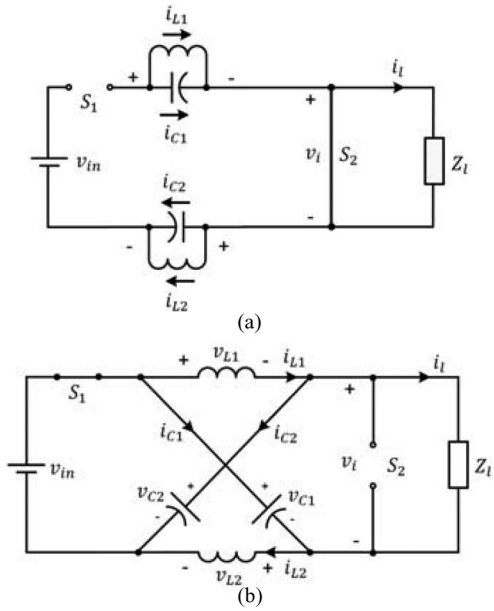

Fig. 4. Basic two equivalent operation modes of the ZSI: (a) ST state; (b) NST state.

by (8)

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_L(t)\\ \tilde{v}_c(t)\\ \tilde{i}_l(t)\end{bmatrix} = \begin{bmatrix}0 & \dfrac{2D_0-1}{L} & 0\\ \dfrac{1-2D_0}{C} & 0 & \dfrac{-(1-D_0)}{C}\\ 0 & \dfrac{2(1-D_0)}{L_l} & \dfrac{-R_l}{L_l}\end{bmatrix} \cdot \begin{bmatrix}\tilde{i}_L(t)\\ \tilde{v}_c(t)\\ \tilde{i}_l(t)\end{bmatrix} + \begin{bmatrix}\dfrac{1-D_0}{L}\\ 0\\ \dfrac{-(1-D_o)}{L_l}\end{bmatrix} \cdot \tilde{v}_{\rm in}(t) + \begin{bmatrix}\dfrac{2V_C - V_{\rm in}}{L}\\ \dfrac{-2I_L + I_l}{C}\\ \dfrac{-2V_C + V_{\rm in}}{L_l}\end{bmatrix} \cdot \tilde{d}_0(t) \tag{6}$$

$$\begin{aligned} sL\tilde{i}_L(s) &= (2D_0-1)\tilde{v}_c(s) + (1-D_0)\tilde{v}_{\rm in}(s) + (2V_C - V_{\rm in})\tilde{d}_0(s)\\ sL\tilde{v}_c(s) &= (1-2D_0)\tilde{i}_L(s) - (1-D_0)\tilde{i}_l(s) + (-2I_L + I_l)\tilde{d}_0(s)\\ sL\tilde{i}_l(s) &= 2(1-D_0)\tilde{v}_c(s) - R_l\tilde{i}_l(s) - (1-D_0)\tilde{v}_{\rm in}(s) + (-2V_C + V_{\rm in})\tilde{d}_0(s) \end{aligned} \tag{7}$$

$$\begin{aligned} V_C &= \frac{1-D_o}{1-2D_0}V_{\rm in}\\ I_L &= \frac{1-D_o}{1-2D_0}I_l\\ I_l &= \frac{V_C}{R_l}. \end{aligned} \tag{8}$$

The dc-link voltage v_i is a square waveform due to the ST state. During the NST states, the dc-link voltage is at its peak value, $v_{ip} = 2v_c - v_{\text{in}}$, and it is zero during the ST states. Therefore, the perturbation in the dc-link peak voltage $\tilde{v}_{ip}$ can be written as [22]

$$\tilde{v}_{ip} = 2\tilde{v}_c - \tilde{v}_{\text{in}}. \tag{9}$$

In small-signal modeling and transient analysis, the response of one state variable to multiple small-signal perturbations can be expressed as a linear combination of the variable response to each individual perturbation. The capacitor voltage and the inductor current can be expressed as a linear combination of the variable response to each individual perturbation as

$$\begin{aligned}
\tilde{v}_c(s) &= G_{vd}(s)\tilde{d}_0(s) + G_{vi}(s)\tilde{v}_{\text{in}}(s) \\
\tilde{i}_L(s) &= G_{id}(s)\tilde{d}_0(s) + G_{ii}(s)\tilde{v}_{\text{in}}(s) \\
\tilde{v}_{ip}(s) &= G_{vpd}(s)\tilde{d}_0(s) + G_{vpi}(s)\tilde{v}_{\text{in}(s)}
\end{aligned} \tag{10}$$

where $G_{vd}(s), G_{vi}(s), G_{id}(s), G_{ii}(s), G_{vpd}(s)$ and $G_{vpi}(s)$ are given (11–16) as shown at the bottom of this page.

The derived transfer functions prove the presence of a right half-plane zero in the ZSI control to capacitor voltage transfer function, resulting in the dc-link voltage having a nonminimum phase response. This nonminimum phase response tends to destabilize the wide bandwidth feedback loops, implying high gain instability and imposing control limitations [10].

V. Dual-Loop Direct Peak DC-Link Voltage Control Technique

The capacitor voltage V_C is somewhat equivalent to the peak dc-link voltage V_{ip} of the inverter, but the peak dc-link voltage is nonlinear function of the capacitor voltage as shown in Fig. 5. Thus, only controlling the capacitor voltage cannot bring the high performance due to the nonlinear property of the V_{ip}/V_C relation [19]. Fig. 6 shows that the peak dc-link voltage V_{ip} changes at $t = 0.2$ s, while V_C is controlled to be constant.

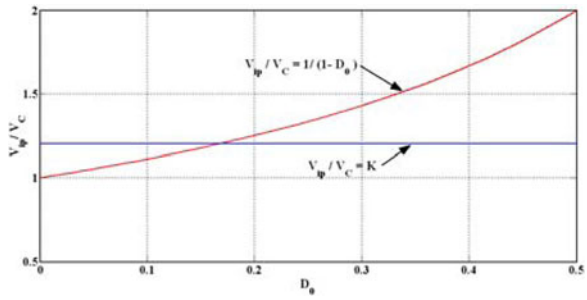

Fig. 5. Nonlinear relation between V_{ip} /V_C

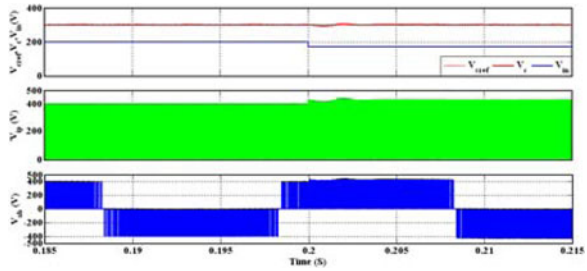

Fig. 6. The dc-link and output voltage waveforms when there is a step change in the input voltage using dual-loop capacitor voltage control

These effects could be transferred into the ac output side, which distort the ac output voltage, introduce difficulty in its controller design, and increase the voltage stress across the switches.

In this paper, the direct digital design method is used to design the dual-loop peak dc-link voltage controllers, using the following steps: first, the continuous time control to output transfer functions $G_{vpd}(s)$ and $G_{id}(s)$ of the ZSI are discretized using the zero-order hold (ZOH) method. After that, once the discrete transfer functions of the system are available, the digital controllers are designed directly in the z-domain using methods similar to the continuous time frequency response methods.

This has the advantage that the poles and zeros of the digital controllers are located directly in the z-domain, resulting in a

$$G_{vd}(s) = \frac{(-2I_L + I_l)L_l L s^2 + [(-2I_L + I_l)R_l L + (1-D_0)(2V_C - V_{\text{in}})L + (1-2D_0)(2V_c - V_{\text{in}})L_l]s + (1-2D_0)(2V_c - V_{\text{in}})R_l}{L_l LCs^3 + R_l LCs^2 + [2L(1-D_0)^2 + L_l(2D_0-1)^2]s + R_l(2D_0-1)^2} \tag{11}$$

$$G_{vi}(s) = \frac{[(1-D_0)^2 L + (1-D_0)(1-2D_0)L_l]s + (1-D_0)(1-2D_0)R_l}{L_l LCs^3 + R_l LCs^2 + [2L(1-D_0)^2 + L_l(2D_0-1)^2]s + R_l(2D_0-1)^2} \tag{12}$$

$$G_{id}(s) = \frac{(2V_C - V_{\text{in}})L_l Cs^2 + [R_l C(2V_C - V_{\text{in}}) + (1-2D_0)(-2I_L + I_l)L_l]s + (1-D_0)(2V_C - V_{\text{in}}) + (1-2D_0)(-2I_L + I_l)R_l}{L_l LCs^3 + R_l LCs^2 + [2L(1-D_0)^2 + L_l(2D_0-1)^2]s + R_l(2D_0-1)^2} \tag{13}$$

$$G_{ii}(s) = \frac{(1-D_0)L_l LCs^2 + (1-D_0)(1-2D_0)R_l Ls + (1-D_0)^2 L}{L_l LCs^3 + R_l LCs^2 + [2L(1-D_0)^2 + L_l(2D_0-1)^2]s + R_l(2D_0-1)^2} \tag{14}$$

$$G_{vpd}(s) = 2G_{vd}(s) \tag{15}$$

$$G_{vpi}(s) = 2G_{vi}(s) - 1. \tag{16}$$

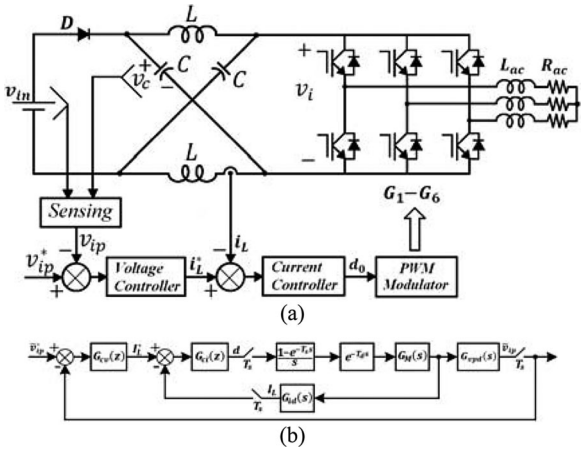

Fig. 7. ZSI closed loop dual-loop peak dc-link voltage control of the (a) ZST and (b) its block diagram.

better load transient response, as well as better phase margin and bandwidth for the closed loop controlled power electronics converter [33].

Fig. 7 shows the entire dual-loop peak dc-link voltage control technique block diagram of the ZSI containing the voltage loop and current loop controllers $G_{cv}(z)$, $G_{ci}(z)$, the ZOH $(1-e^{-T_s s})/s$, the computational delay $(e^{-T_d s})$, the control to output transfer functions $G_{vpd}(s)$, $G_{id}(s)$ and the modified modulation to ST transfer function $G_M(s)$, respectively, where $G_M(s)$ is expressed by [12] as follows:

$$G_M(s) = \frac{D_0(s)}{v'_m(s)} = \frac{2}{V_{\text{tri}}} \tag{17}$$

where V_{tri} is the amplitude of the triangle carrier signal. In this implementation, the chosen sampling scheme results in a computation delay of half the sampling period ($T_d = T_s/2$) [30].

The loop gains for inner current loop and outer voltage loop can be expressed as follows:

$$T_i(z) = G_{ci}(z) \cdot G_{id}(z) \tag{18}$$

$$T_v(z) = \frac{G_{cv}(z) \cdot G_{ci}(z) \cdot G_{vd}(z)}{1 + T_i(z)} \tag{19}$$

where the discretized peak dc-link voltage and inductor current to control transfer functions are given as

$$G_{vpd}(z) = Z\left\{\frac{1-e^{-T_s s}}{s} \cdot e^{-T_d s} \cdot G_M(s) \cdot G_{vpd}(s)\right\} \tag{20}$$

$$G_{id}(z) = Z\left\{\frac{1-e^{-T_s s}}{s} \cdot e^{-T_d s} \cdot G_M(s) \cdot G_{id}(s)\right\}. \tag{21}$$

In this paper, a digital PI controller with antiwindup will be designed based on the required phase margin φ_m and critical frequency f_{cz} using the Bode diagram of the discrete time domain, as explained in [30] and [31], the transfer function of the digital PI controller is given by

$$G_c(z) = K_p + \frac{K_i T_s z}{z-1} \tag{22}$$

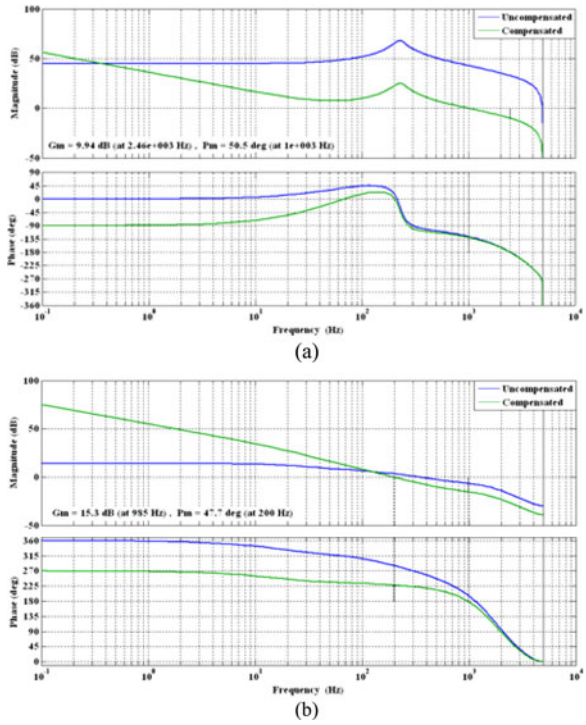

Fig. 8. Bode diagrams for (a) inner current loop and (b) outer voltage loop.

TABLE I
EXPERIMENTAL PARAMETERS OF THE ZSI

Parameter	Value
Input voltage	200 V
Peak dc-link voltage reference	300 V
Inductance	650 µH
Inductance internal resistance	0.22 Ω
Capacitance	320 µF
Capacitance internal resistance	0.9 mΩ
Switching frequency	10 kHz
AC load inductance	340 µH
AC load resistance	12.5 Ω

where

$$K_p = \frac{\cos\theta}{|G_p(z)|} \tag{23}$$

$$K_i = \frac{\sin\theta \cdot f_{cz}}{|G_p(z)|} \tag{24}$$

and

$$\theta = 180^\circ + \varphi_m - \angle G_p(z). \tag{25}$$

Fig. 8 shows the Bode plots for the inner current loop gain and the outer voltage loop gain, respectively, with the system parameters listed in Table I. The plots indicate that the current loop gain has a crossover frequency as high as 1 kHz, with a phase margin of 50° and a gain margin of 10 dB. To avoid interaction between the subsystems, low control bandwidth is used for the voltage loop. The resulting outer voltage loop has a crossover frequency of 200 Hz and a phase margin of 48° and a gain margin of 15 dB.

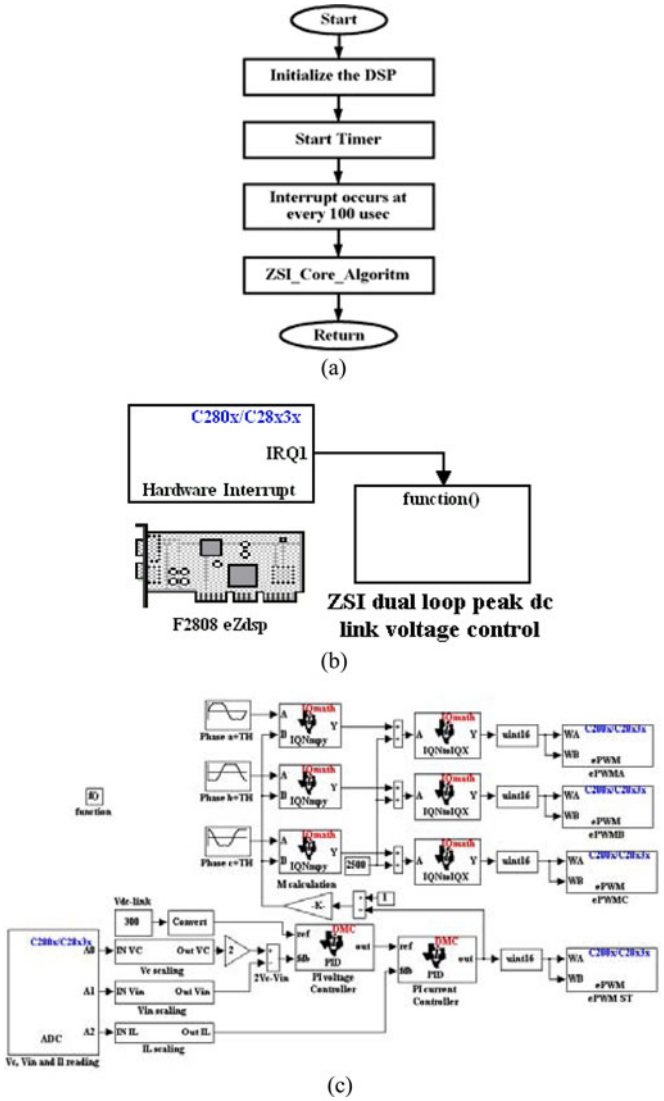

Fig. 9. (a) Main control algorithm flow chart. (b) Its Simulink model. (c) Simulink model for the dual-loop peak dc-link voltage control.

VI. Control Algorithm Implementation

Real-time workshop (RTW) is one of the DSP development tools, which produce code directly from the block set models for use with MATLAB and Simulink. It reduces algorithm coding to an automated process, which includes coding, compiling, linking, and downloading to the targeted hardware. Thereby, it shortens the development cycles and in turn reduces the cost [35].

The inner current and outer voltage loop algorithms are implemented on the DSP TMS320F2808. It consists of series of submodule programs performing the individual task. The main control algorithm, as shown in Fig. 9(a), is composed of an initialization routine followed by periodic interrupts triggered by an internal timer for calling the ZSI core control algorithm submodule. This is implemented by the interrupt request in the DSP as indicated in Fig. 9(b). The interrupt timer has the same frequency as the IGBT switching frequency, which is 10 kHz. Fig. 9(c) shows the Simulink model used for code generation.

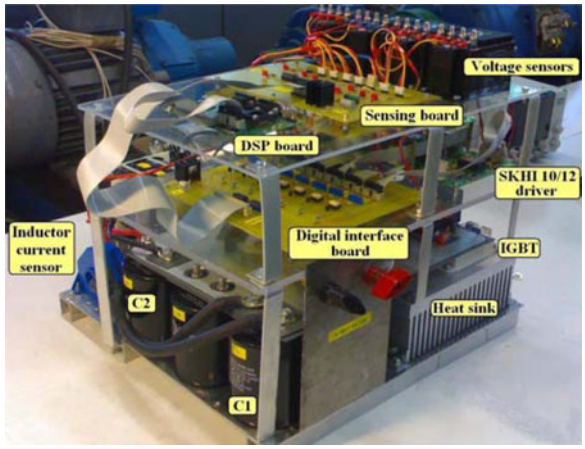

Fig. 10. Experimental setup of a 30-kW ZSI.

After scanning the ADC, formatting the input variables and calculating the actual peak dc-link voltage value, the PI voltage controller generates the inductor current reference by comparing the actual and reference values of the peak dc-link voltage. After that, the PI current controller generates the ST duty ratio by comparing the actual and reference values of the inductor current. Finally, the modulation index is calculated according to the MCBC method. It should be noted that, in case of motor drive or grid-tied application, the modulation index is determined by the ac side controller, as presented in [31].

VII. Simulation and Experimental Results

The dynamic performance of the ZSI with the proposed dual-loop peak dc-link voltage control has been tested using MATLAB simulation and experimental verification. A 30 kW prototype of the ZSI, as shown in Fig. 10, has been designed and implemented using the parameters in Table I. This prototype is tested up to 10 kW. The eZdsp F2808 evaluation board based on the TMS320F2808 DSP is used for the realization of the proposed peak dc-link voltage control technique and the real time workshop (RTW) is used for automatic code generation.

Figs. 11–13 show the simulation and experimental results of the proposed dual-loop peak dc-link voltage control technique during input voltage step, load transient, and steady-state operations. As shown in Fig. 11, the input voltage stepped-down by 7.5% with the rated load, the peak dc-link voltage remains constant at 300 V, the load phase current and line voltage are not affected by decreasing input voltage and the inductor current is increased to supply the same output power. Fig. 12 shows the ZSI response during load increasing and decreasing by 50%. As noticeable the inductor current is doubled during the 50% load increase and the output line voltage and the peak dc-link voltage remain unchanged. Fig. 13 shows the steady-state performance of the Z-network variables in switching frequency and output frequency and the steady-state waveforms of the output line voltages and phase currents in line frequency, as noticeable from this figure, the inductor current is controlled and there are no oscillations in the inductor current or in the dc-link voltage.

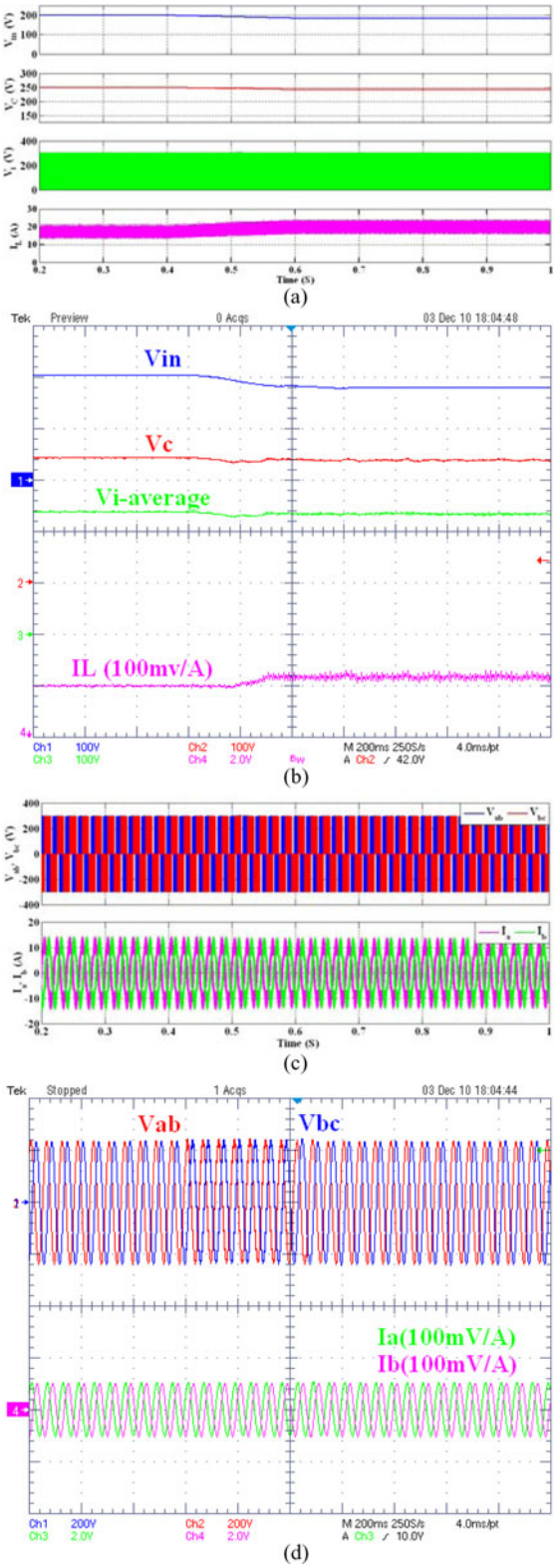

Fig. 11. ZSI response during input voltage step down by 7.5%: (a, b) Z-network variables and (c, d) output variables. (a) Simulation results. (b) Experimental results. (c) Simulation results. (d) Experimental results.

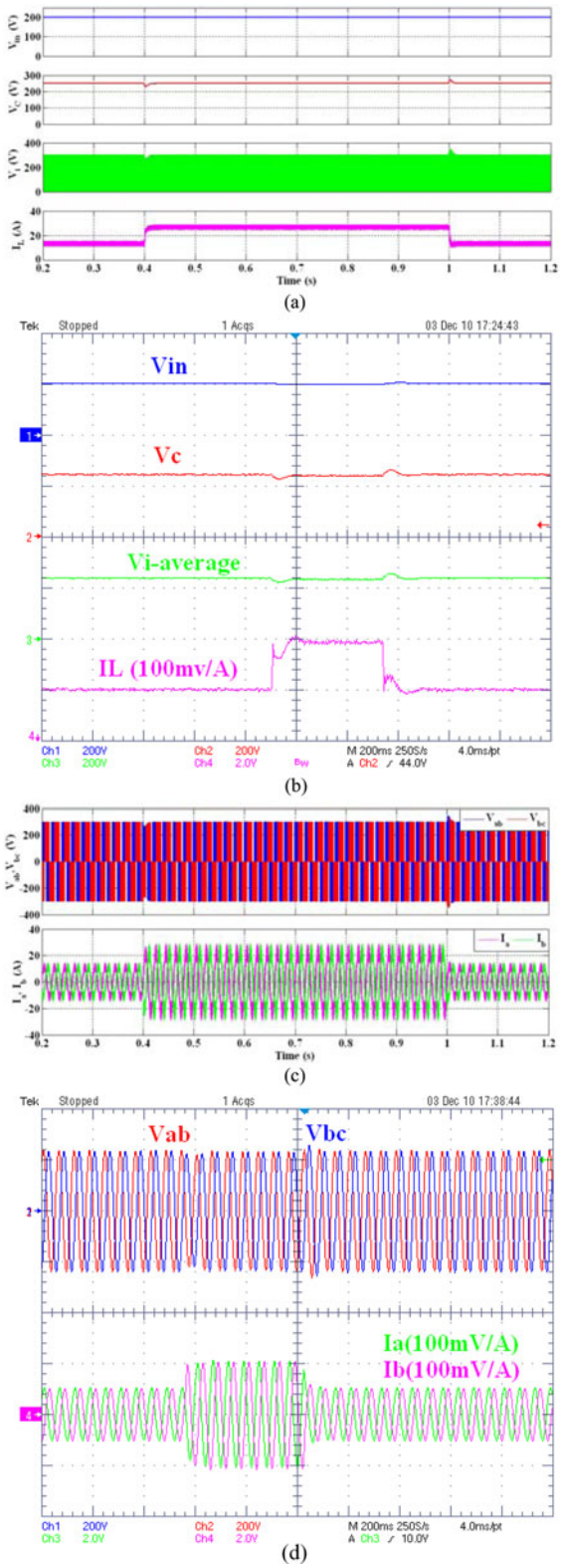

Fig. 12. ZSI response during load increasing and decreasing by 50%. (a) Z-network variables and (b) output variables. (a) Simulation results. (b) Experimental results. (c) Simulation results. (d) Experimental results.

It is noticeable that the experimental results match the simulation results very well, which verify the performance of the proposed dual-loop peak dc-link voltage control for the ZSI. It should be noted that, the experimental waveforms of the output variables (line voltages and phase currents) are filtered waveforms.

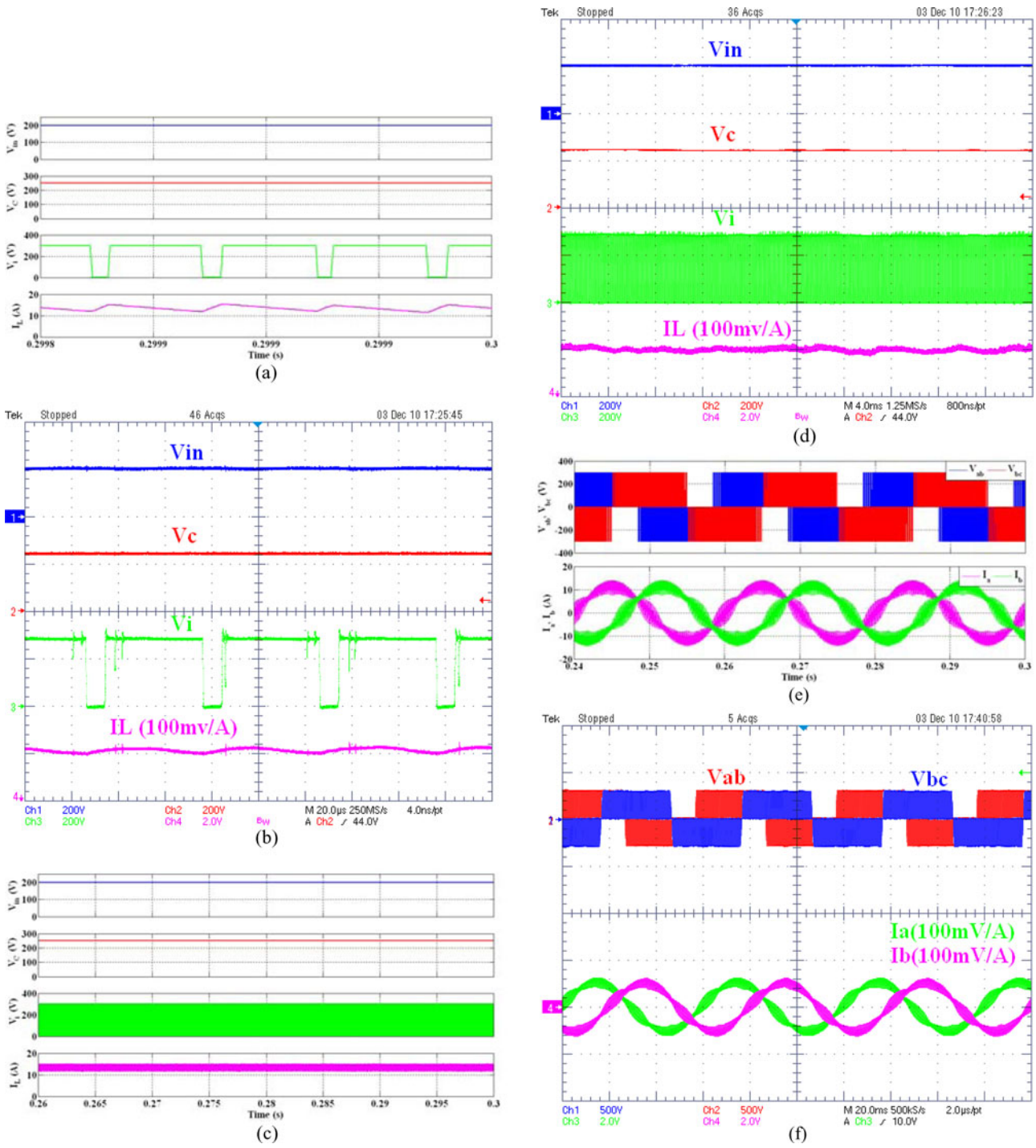

Fig. 13. Steady-state waveforms of the ZSI: (a, b, c, d) Z-network variables and (e, f) output variables. (a) Simulation results in switching frequency. (b) Experimental results switching frequency. (c) Simulation results. (d) Experimental results. (e) Simulation results. (f) Experimental results.

VIII. Conclusion

This paper proposes a dual-loop peak dc-link voltage control technique for controlling the peak dc-link voltage for a ZSI with inductive load, where the outer voltage loop provides the inductor current reference and the inner current loop produces the ST duty ratio and the modulation index is calculated based on the MCBC method, where, the peak dc-link voltage is estimated by measuring both the input and capacitor voltages. The two controllers are designed based on a third-order small signal model of the ZSI using Bode diagram. Both controllers are implemented using the direct digital design method using a DSP-linked with MATLAB for automatic code generation.

The proposed control strategy is verified by simulation and experimental results under different disturbances and steady-state operation modes. The experimental results match the simulation results very well, which verify the performance of the proposed peak dc-link voltage control technique.

REFERENCES

[1] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[2] F. Z. Peng, M. Shen, and Z. Qian, "Maximum boost control of the Z-source inverter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 833–838, Jul. 2005.

[3] Peng, M. Shen, J. Wang, A. Joseph, F. Zheng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 770–778, May/Jun. 2006.

[4] P. C. Loh, D. M. Vilathgamuwa, Y. S. Lai, G. T. Chua, and Y. Li, "Pulse-width modulation of Z-source inverters," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1346–1355, Nov. 2005.

[5] O. Ellabban, J. Van Mierlo, and P. Lataire, "Comparison between different PWM control methods for different Z-source inverter topologies," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 8–10 Sep., 2009, pp. 1–11.

[6] O. Ellabban, J. Van Mierlo, and P. Lataire, "Experimental study of the shoot-through boost control methods for the Z-source inverter," *Eur. Power Electron. J.*, vol. 21, no. 2, pp. 18–29, Jun. 2011.

[7] M. Shen and F. Z. Peng, "Operation modes and characteristics of the Z-source inverter with small inductance or low power factor," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 89–96, Jan. 2008.

[8] S. Rajakaruna and L. Jayawickrama, "Steady-state analysis and designing impedance network of Z-source inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2483–2491, Jul. 2010.

[9] P. C. Loh, D. M. Vilathgamuwa, C. J. Gajanayake, Y. R. Lim, and C. W. Teo, "Transient modeling and analysis of pulse-width modulated Z-source inverter," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 498–507, Mar. 2007.

[10] J. Liu, J. Hu, and L. Xu, "Dynamic modeling and analysis of Z source converter-derivation of AC small signal model and design-oriented analysis," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1786–1796, Sep. 2007.

[11] V. P. Galigekere and M. K. Kazimierczuk, "Small-signal modeling of PWM Z-source converter by circuit-averaging technique," *IEEE Int. Symp. Circuits Syst.*, pp. 1600–1603, 15–18 May, 2011.

[12] X. Ding, Z. Qian, S. Yang, B. Cui, and F. Peng, "A PID control strategy for dc-link boost voltage in Z-source inverter," in *Proc. IEEE 22nd Annu. Appl. Power Electron. Conf.*, 2007, pp. 1145–1148.

[13] M. J. Rastegar Fatemi, S. Mirzakuchaki, and S. Rastegar Fatemi, "Wide-range control of output voltage in Z-source inverter by neural network," in *Proc. Int. Conf. Electr. Mach. Syst.*, 2008, pp. 1653–1658.

[14] Q.-V. Tran, T.-W. Chun, H.-G. Kim, and E.-C. Nho, "Minimization of voltage stress across switching devices in the Z-source inverter by capacitor voltage control," *J. Power Electron.*, vol. 9, no. 3, pp. 335–342, May 2009.

[15] H. Rostami and D. A. Khaburi, "Neural networks controlling for both the DC boost and AC output voltage of Z-source inverter," in *Proc. 1st Power Electron. Drive Syst. Technol. Conf.*, 17–18 Feb., 2010, pp. 135–140.

[16] M. Shen, Q. Tang, and F. Z. Peng, "Modeling and controller design of the Z-source inverter with inductive load," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 1804–1809.

[17] A. H. Rajaei, S. Kaboli, and A. Emadi, "Sliding-mode control of Z-source inverter," in *Proc. IEEE 34th Annu. Conf. Ind. Electron.*, 10–13 Nov., 2008, pp. 947–952.

[18] W. Mo, P. C. Loh, and F. Blaabjerg, "Model predictive control for Z-source power converter," in *Proc. 8th Int. Conf. Power Electron.*, May 30–Jun. 3, 2011, pp. 3022–3028.

[19] X. Ding, Z. Qian, S. Yang, B. Cui, and F. Peng, "A direct DC-link boost voltage PID-like fuzzy control strategy in Z-source inverter," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 405–411.

[20] Y. Tang, S. Xie, and C. Zhang, "Feedforward plus feedback control of the improved Z-source inverter," *IEEE Energy Convers. Congr. Expo.*, pp. 783–788, 20–24 Sep. 2009.

[21] X. Ding, Z. Qian, S. Yang, B. Cui, and F. Peng, "A direct peak DC-link boost voltage control strategy in Z-source inverter," in *Proc. IEEE 22nd Annu. Appl. Power Electron. Conf.*, 2007, pp. 648–653.

[22] G. Sen and M. Elbuluk, "Voltage and current programmed modes in control of the Z-source converter," *IEEE Trans. Ind. Appl.*, vol. 46, no. 2, pp. 680–686, Mar./Apr. 2010.

[23] S. Yang, X. Ding, F. Zhang, F. Z. Peng, and Z. Qian, "Unified control technique for Z-source inverter," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 3236–3242.

[24] Y. Tang, S. Xie, C. Zhang, and Z. Xu, "Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 409–415, Feb. 2009.

[25] M. Zhu, K. Yu, and F. L. Luo, "Switched-inductor Z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, Aug. 2010.

[26] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, and L. K. Siow, "Extended-boost Z-source inverters," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2642–2652, Oct. 2010.

[27] D. Vinnikov and I. Roasto, "Quasi-Z-source-based isolated DC/DC converters for distributed power generation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 192–201, Jan. 2011.

[28] M. Nguyen, Y. Lim, and G. Cho, "Switched-inductor quasi-Z-source inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3183–3191, Apr. 2011.

[29] D. G. Holmes, B. P. McGrath, D. Segaran, and W. Y. Kong, "Dynamic control of a 20 kW interleaved boost converter for traction applications," in *Proc. IEEE Ind. Appl. Soc. Annu. Meet.*, 5–9 Oct., 2008, pp. 1–8.

[30] O. Ellabban, J. Van Mierlo, and P. Lataire, "A DSP based dual loop digital controller design and implementation of a high power boost converter for hybrid electric vehicles applications," *J. Power Electron.*, vol. 11, no. 2, pp. 113–119, Mar. 2011.

[31] O. Ellabban, J. Van Mierlo, and P. Lataire, "Design and implementation of a DSP based dual-loop capacitor voltage control of the Z-source inverter," *Int. Rev. Electr. Eng.*, vol. 6, no. 6, pp. 98–108, Feb. 2011.

[32] T. Suntio, I. Gadoura, and K. Zenger, "Small-signal modelling of switched-mode converters—A unified approach," *Nordic Workshop Power Ind. Electron.*, 12–14 Aug. 2002.

[33] V. Mummadi, "Design of robust digital PID controller for H-bridge soft-switching boost converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2883–2897, Sep. 2010.

[34] W.-S. Gan, Y.-K. Chong, W. Gong, and W.-T. Tan, "Rapid prototyping system for teaching real-time digital signal processing," *IEEE Trans. Educ.*, vol. 43, no. 1, pp. 19–24, Feb. 2000.

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