A Filtered SVPWM for Multiphase Voltage Source Inverters Considering Finite Pulse-Width Resolution

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***Abstract*—A filtered space-vector pulse-width modulation (SVPWM) considering finite pulse-width resolution is proposed to produce a switching sequence with reduced baseband harmonics for multiphase voltage source inverters (VSI). The conventional SVPWM is sensitive to the pulse-width resolution which leads to increased harmonic distortion in digital-based implementations. By incorporating a pseudofeedback loop regarding weighted voltage difference between desired and produced phase voltages, the quantization error induced by finite pulse-width resolution is compensated, yielding a better tracking performance. The gating signals for multiphase VSIs are presented through rigorous mathematical derivation. In simulations and experiments, harmonic distortions of SVPWMs with and without filter compensation under various pulse-width resolutions are shown. The results confirm the effectiveness of the proposed scheme. The main advantage realized is reduction of acoustic noise and increased tracking accuracy.**

***Index Terms*—Maximum modulation index, multiphase, pulse-width modulation (PWM), space vector, voltage-source inverters.**

I. Introduction

VARIOUS pulse-width modulations (PWM) such as third-harmonic injection PWM [1], zero-sequence injection PWM [2], space-vector PWM (SVPWM) [3]–[9], and unified PWM [5] have been proposed to generate the control commands of three-phase voltage source inverter (VSI) for ac variable-speed drives. In recent years, multiphase PWMs have been proposed because of their increased efficiency [10], reduced torque pulsation, improved fault tolerance [11], [12], and lower power handling requirement [13] by adopting multiphase machines. For example, both five-phase [14] and seven-phase [15] PWMs were derived using multiple *d–q* spaces concept. A six-phase PWM [16] was proposed based on vector space decomposition. A nine-phase PWM [17] considering load circuits of different gating patterns was reported. The work in [18] presented a unified solution to general multiphase PWM by solving the signal matching problem.

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In recent years, the embedded digital signal processor that allows real-time multichannel digital modulation has been generally used [19], [20]. In the digital implementation, multiphase reference voltages are sampled and fed into the digital modulator to produce gating signals at a constant clock rate *f*. This means a finite pulse-width resolution because the gating state transition can only occur at some specific time instants depending on *f*. This will result in a deviation of produced phase voltages from the desired phase voltages, i.e., increasing harmonic distortion especially for a small modulation index signal. For example, when system master clock frequency and reference sampling frequency are given as 48 and 3 kHz, respectively, the maximum refreshing rate of gating signals is $f = 48$ kHz and the pulse-width resolution is 4-bit within each input period ($48k = 3k \times 2^4$). Thus, the worst-case rounding error for the duty ratio is $1/32 = 0.03125$. For small modulation index, the effect of error on signal distortion becomes quite significant. Further, if a 16-bit pulse-width resolution is desired, the master clock needed is 196.61 MHz for 3 kHz reference sampling frequency and is about 1.31 GHz for ultrasonic carrier. This will increase the cost and power consumption of the devices.

Methods to reduce acoustic noise and harmonic distortion of three-phase motor drives include random PWM with fixed switching frequency [21], [22] and random switching frequency PWM [19], [23]. However, all of them concern about the tonal components caused by intrinsic PWM characteristic. In recent years, a novel selective harmonic elimination considering complete system optimization [24] and a generic six-step direct PWM for a current-controlled converter [25] have been proposed. The advantages include increased dc-current utilization and reduced switching frequency [25]. To alleviate the adverse effect induced by finite pulse-width resolution, proposals in [26] and [27] were reported to achieve higher precision of duty ratios without increasing clock rate. In [26], a single-phase PWM to regulate a dc voltage command was proposed by using an error accumulator and lookup tables. The method in [27] uses random numbers to compensate the remainder value of the desired voltage command. None of the work mentioned earlier dealt with the problem in multiphase systems. A feedback quantization scheme proposed in [28] for three-phase VSI spreads the spectrum of the produced phase currents/voltages in a wide frequency band.

The general solution using SVPWM for multiphase VSIs was reported in [18]. The multiphase SVPWM was formulated as a matching problem between the reference and the switching waveform without considering the finite pulse-width resolution. In this study, the frequency-weighted error due to finite resolution is considered in the objective function to emphasize

the quality of in-band signal matching. The frequency weighting is realized by filtering the error signals. This results in a multiple-input–multiple-output (MIMO) pseudofeedback architecture. Based on similar analysis in [18], the block diagram for VSI systems of any phase number can be obtained.

The rest of this paper is organized as follows. Section II gives the mathematical formulation of the proposed modulator and solves the optimal matching problem. The analyses of conduction time and quantization error of the proposed modulator are shown in Section III. Section IV presents an implementation of the modulator without using multipliers as well as simulation results for various pulse-width resolutions. Conclusions are drawn in Section VI.

II. Filtered SVPWM With Pseudofeedback

A. Multiphase Voltage Source Inverter

Fig. 1 depicts the simplified structure of an *N*-phase VSI where $S_1, S_2, \ldots, S_N$ are the output phase voltages of the inverter (with reference to the neutral point). Two switching states exist in one phase leg: only the upper or the lower switch is turned ON. The switching state is denoted as $+1$ (0) when the upper (lower) switch of the phase leg is turned ON. Then, the gating states can be represented by a vector $\mathrm{s} = [s_1 \quad s_2 \quad \cdots \quad s_N]^T$ where $s_1, s_2, \ldots, s_N \in \{0,1\}$ are the states of phase legs. Equation (1) gives the relationship between phase voltage vector, $\mathrm{S} = [S_1 \quad S_2 \cdots \quad S_N]^T$, and the gating state. Notably, for an *N*-phase VSI, 2^N gating states exist and each corresponds to a different phase voltage vector (also called a space vector) except for two zero switching states, $\mathrm{s} = [0 \quad \cdots \quad 0]^T$ and $\mathrm{s} = [1 \quad \cdots \quad 1]^T$

$$\begin{aligned}\mathrm{S} &= \begin{bmatrix} S_1 \\ S_2 \\ \vdots \\ S_N \end{bmatrix} \\ &= \begin{bmatrix} (N-1)/N & -1/N & \cdots & -1/N \\ -1/N & (N-1)/N & \ddots & \vdots \\ \vdots & \ddots & \ddots & -1/N \\ -1/N & \cdots & -1/N & (N-1)/N \end{bmatrix} \\ &\quad \times \begin{bmatrix} s_1 \\ s_2 \\ \vdots \\ s_N \end{bmatrix} \triangleq \mathrm{S}_c\mathrm{s}. \end{aligned} \tag{1}$$

Remark 1: Multiplying $[1 \quad \cdots \quad 1]$ on both sides of (1), we obtain that the phase voltage vector produced by the *N*-phase VSI (for the *y*-connected load) must satisfy $\sum_{j=1}^{N} S_j = 0$.

B. Signal Matching Objective

Given a desired phase voltage **r**, the objective of the modulator is to produce gating signals for VSI to recover the desired phase voltages on load windings. However, the phase voltages produced are restricted. For example, only seven different phase voltages

$$\mathrm{P} = \left\{ \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}, \begin{bmatrix} 2/3 \\ -1/3 \\ -1/3 \end{bmatrix}, \begin{bmatrix} -1/3 \\ 2/3 \\ -1/3 \end{bmatrix}, \begin{bmatrix} -1/3 \\ -1/3 \\ 2/3 \end{bmatrix}, \begin{bmatrix} -2/3 \\ 1/3 \\ 1/3 \end{bmatrix}, \begin{bmatrix} 1/3 \\ -2/3 \\ 1/3 \end{bmatrix}, \begin{bmatrix} 1/3 \\ 1/3 \\ -2/3 \end{bmatrix} \right\}$$

can be produced by a three-phase VSI. Therefore, it is necessary to consider the characteristics of the load. The load is usually approximated by a serial-connected resistance and inductance circuit (refer to Fig. 2). The phase current is expressed by passing the produced phase voltage through a low-pass filter

$$i_1 = \frac{1}{sL + R} S_1. \tag{2}$$

For an *N*-phase sinusoidal reference input **r** with phase shift $2\pi/N$, it is intuitive that the desired phase currents are also *N*-phase sinusoidal waves. Therefore, the objective is to find the switching states (gating states) such that the produced phase voltages are sinusoidal waves after low-pass filtering or alternatively, the difference between desired and produced phase voltages within low frequency band shall be minimized.

C. Problem Formulation

The *N*-dimensional desired phase voltage vector satisfying (3) can be written in the form $\mathrm{r} = [S_1^* \quad S_2^* \quad \cdots \quad S_N^*]^T$ where

$$S_1^* + S_2^* + \cdots + S_N^* = 0. \tag{3}$$

Assume that the controller input sampling frequency is f_c and that the pulse-width resolution within each input period is *b*

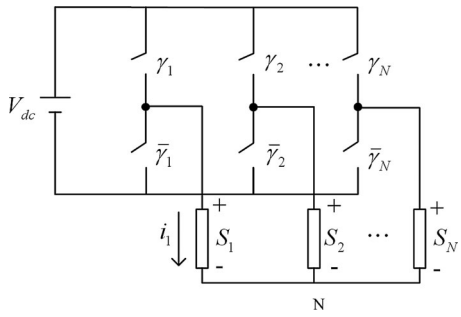

Fig. 1. *N*-phase VSI topology.

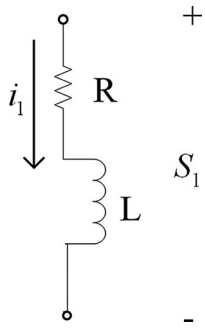

Fig. 2. Model circuit of a winding of a motor.

bits, i.e., the controller outputs are updated at a rate $2^b \times f_c$ Hz. The average phase voltage produced on the windings within one input period is

$$\bar{\mathbf{v}}(k) = \frac{1}{2^b}\sum_{j=0}^{2^b-1}\mathbf{v}(j) = \frac{1}{2^b}\sum_{j=0}^{2^b-1}\mathbf{S}_c\mathbf{s}(j) \tag{4}$$

where $\mathbf{v}(j)$, one of the space vectors, is the corresponding phase voltage vector induced by the *j*th selected gating state $\mathbf{s}(j)$ within one input period. Note that the image of $\bar{\mathbf{v}}$ is all possible linear combinations of 2^b basic vectors.

The objective of the proposed modulator is to determine gating states (or $\mathbf{v}(j)$) that minimize filtered error power within each input period. The filtered error is represented as

$$\mathbf{E}(\mathbf{z}) = \mathbf{W}(z)\left(\mathbf{R}(z) - \bar{\mathbf{V}}(z)\right) \tag{5}$$

where $\mathbf{W}(z)$ is an $N \times N$ filter matrix and $\mathbf{R}(z), \bar{\mathbf{V}}(z)$ are z-transform of the elements in $\mathbf{r}, \bar{\mathbf{v}}$, respectively. A *p*th-order low-pass filter, denoted as $w(z)$, is selected as the weighting filter for each phase to enhance low-frequency-band performance, i.e., $\mathbf{W}(z)$ is a diagonal matrix with $w(z)$, a single-input–single-output (SISO) transfer function, on its diagonal terms. $w(z)$ can be represented in the state-space form as

$$w(z) = d + \mathbf{c}(z\mathbf{I} - \mathbf{a})^{-1}\mathbf{b} \tag{6}$$

where $\mathbf{a} \in R^{p\times p}, \mathbf{b} \in R^p, \mathbf{c} \in R^{1\times p},$ and $d \in R$. Further, the state-space form of $\mathbf{W}(z)$ is

$$\begin{aligned}\mathbf{x}(k+1) &= \mathbf{A}\mathbf{x}(k) + \mathbf{B}(\mathbf{r}(k) - \bar{\mathbf{v}}(k))\\ \mathbf{e}(k) &= \mathbf{C}\mathbf{x}(k) + \mathbf{D}(\mathbf{r}(k) - \bar{\mathbf{v}}(k))\end{aligned} \tag{7}$$

where $\mathrm{e}(k) \in R^N$ is the filtered error vector and $\mathbf{x}(k) \in R^{pN}$ is a system state vector. Then, $(\mathbf{A},\mathbf{B},\mathbf{C},\mathbf{D})$ can be written as

$$\mathbf{A} = \begin{bmatrix}\mathbf{a} & \mathbf{0}_a & \cdots & \mathbf{0}_a\\ \mathbf{0}_a & \mathbf{a} & \ddots & \vdots\\ \vdots & \ddots & \ddots & \mathbf{0}_a\\ \mathbf{0}_a & \cdots & \mathbf{0}_a & \mathbf{a}\end{bmatrix},\quad \mathbf{B} = \begin{bmatrix}\mathbf{b} & \mathbf{0}_b & \cdots & \mathbf{0}_b\\ \mathbf{0}_b & \mathbf{b} & \ddots & \vdots\\ \vdots & \ddots & \ddots & \mathbf{0}_b\\ \mathbf{0}_b & \cdots & \mathbf{0}_b & \mathbf{b}\end{bmatrix},$$

$$\mathbf{C} = \begin{bmatrix}\mathbf{c} & \mathbf{0}_c & \cdots & \mathbf{0}_c\\ \mathbf{0}_c & \mathrm{c} & \ddots & \vdots\\ \vdots & \ddots & \ddots & \mathbf{0}_c\\ \mathbf{0}_c & \cdots & \mathbf{0}_c & \mathbf{c}\end{bmatrix},\ \text{and}\ \mathbf{D} = \begin{bmatrix}d & 0 & \cdots & 0\\ 0 & d & \ddots & \vdots\\ \vdots & \ddots & \ddots & 0\\ 0 & \cdots & 0 & d\end{bmatrix} \tag{8}$$

where $\mathbf{0}_a, \mathbf{0}_b$, and $\mathbf{0}_c$ are the zero matrices with dimensions $\mathbf{0}_a \in R^{p\times p}$, $\mathbf{0}_b \in R^p$, and $\mathbf{0}_c \in R^{1\times p}$. The signal matching problem becomes

$$\begin{aligned}&\min_{\mathbf{v}(j)\in\text{basic vectors}} \|\mathbf{e}(k)\|_2^2 = \min_{\mathbf{v}(j)\in\text{basic vectors}}\\ &\|\mathbf{C}\mathbf{x}(k) + \mathbf{D}\mathbf{r}(k) - \mathbf{D}\bar{\mathbf{v}}(k)\|_2^2\end{aligned} \tag{9}$$

where $\bar{\mathbf{v}}(k) = \frac{1}{2^b}\sum_{j=0}^{2^b-1}\mathbf{S}_c\mathbf{s}(j)$.

D. Solution of the Minimization Problem

The solution to (9) is split into three parts: 1) Finding a feasible and optimal $\bar{\mathbf{v}}(k)$, denoted as $\mathbf{v}^*(k)$, such that power of filtered error is minimized; 2) solving the matching problem $\bar{\mathbf{v}}(k) = \frac{1}{2^b}\sum_{j=0}^{2^b-1}\mathbf{S}_c\mathbf{s}(j) = \mathbf{v}^*(k)$ to obtain $\mathbf{s}(j)$; and 3) gating signal generation.

1) Optimal Solution of $\bar{\mathbf{v}}(k)$ and its Feasibility: Intuitively (refer to (7)), the minimum value of (9) occurs when $\mathrm{e}(k) = 0$ or

$$\bar{\mathbf{v}}(k) = \mathbf{D}^{-1}\mathbf{C}\mathbf{x}(k) + \mathbf{r}(k) \triangleq \mathbf{v}^*(k). \tag{10}$$

Regardless of the pulse-width resolution *b*, $\mathbf{v}^*(k)$ is feasible only if (see *Remark 1*)

$$[1 \quad \cdots \quad 1]\,\mathbf{v}^*(k) = 0. \tag{11}$$

To prove that $\mathbf{v}^*(k)$ is always feasible when $[1 \quad \cdots \quad 1]\,\mathbf{r} = 0$, $\mathbf{v}^*(k)$ in (10) is written as a linear combination of $\mathbf{r}(k)$ and $\bar{\mathbf{v}}(k)$ using (6)–(8)

$$\begin{aligned}\mathbf{v}^*(k) &= \mathbf{D}^{-1}\mathbf{C}\mathbf{x}(k) + \mathbf{r}(k)\\ &= \mathbf{D}^{-1}\mathbf{C}\sum_{j=0}^{k-1}\mathbf{A}^{k-1-j}\mathbf{B}(\mathbf{r}(j) - \bar{\mathbf{v}}(j)) + \mathbf{r}(k)\\ &= \sum_{j=0}^{k-1} d^{-1}\mathbf{c}\mathbf{a}^{k-1-j}\mathbf{b}(\mathbf{r}(j) - \bar{\mathbf{v}}(j)) + \mathbf{r}(k).\end{aligned} \tag{12}$$

Because $[1 \quad \cdots \quad 1]\,\mathbf{r} = 0$ and $[1 \quad \cdots \quad 1]\,\bar{\mathbf{v}} = 0$, (11) is always true.

2) General Solution of Matching Problem: Once the optimal and feasible value $\mathbf{v}^*$ is obtained, the next step is to find the appropriate gating states such that the produced average phase voltage (within one input period) equals $\mathbf{v}^*$. Refer to (1), the instantaneous phase voltage can be obtained by multiplying the switching state with a transition matrix $\mathbf{S}_c$

$$\begin{aligned}\mathbf{S} &= \begin{bmatrix}S_1\\ S_2\\ \vdots\\ S_N\end{bmatrix}\\ &= \begin{bmatrix}(N-1)/N & -1/N & \cdots & -1/N\\ -1/N & (N-1)/N & \ddots & \vdots\\ \vdots & \ddots & \ddots & -1/N\\ -1/N & \cdots & -1/N & (N-1)/N\end{bmatrix}\\ &\quad\times\begin{bmatrix}s_1\\ s_2\\ \vdots\\ s_N\end{bmatrix} \triangleq \mathbf{S}_c\mathbf{s}.\end{aligned}$$

Under *b*-bit pulse-width resolution, 2^b phase voltages (switching states) are selected within one input period and the average

phase voltage must equal $\mathbf{v}^*(k)$, i.e., from (4) and (10)

$$\bar{\mathbf{v}}(k) = \frac{1}{2^b}\sum_{j=0}^{2^b-1}\mathbf{S}_c\mathbf{s}(j) = \mathbf{v}^*(k) = \mathbf{D}^{-1}\mathbf{C}\mathbf{x}(k) + \mathbf{r}(k) \tag{13}$$

where $\mathbf{s}(j)$ is the instantaneous switching state and $\mathbf{S}_c\mathbf{s}(j)$ the instantaneous phase voltages. To solve (13), first observe that elements in $\mathrm{s}(j) \in R^N$ are either 0 or 1 to describe the ON/OFF status of the VSI. As a result, elements of the vector $\frac{1}{2^b}\sum_{j=0}^{2^b-1}\mathrm{s}(j) \triangleq \Theta = [\alpha_1 \quad \alpha_2 \quad \cdots \quad \alpha_N]^T$ belong to the set

$$_b = \left\{0, \frac{1}{2^b}, \frac{2}{2^b}, \frac{3}{2^b}, \cdots \frac{2^b-1}{2^b}, 1\right\}.$$

Note that the *i*th element of $\mathbf{\Theta}$ is the duty cycle for the *i*th inverter phase leg and the finite set $\mathbf{S}_b$ is induced by the *b*-bit pulse-width resolution within one input period. Once the vector $\mathbf{\Theta}$ is obtained, the gating signal can be produced accordingly. From (13) and the definition of $\mathbf{\Theta}$, we can write the matching problem as

$$\mathbf{S}_c\mathbf{\Theta} = \mathbf{D}^{-1}\mathbf{C}\mathbf{x}(k) + \mathbf{r}(k) \tag{14}$$

where elements of $\mathbf{\Theta}$ belong to $\mathbb{S}_b$. The next step would be finding $\mathbf{\Theta}$ with elements belonging to $\mathbb{S}_b$ that satisfy (14). The process is similar to the one in [18] that derives the general solution of multiphase SVPWM. It was proved in [18] that the circulant and symmetric matrix $\mathbf{S}_c$ has eigenvalues $\xi_n, n = 0-N-1$, in the form

$$\xi_n = 1 - \frac{1}{N}\sum_{m=0}^{N-1}\phi_n^m, \text{ where } \phi_n = e^{-(2\pi n/N)j}$$

and the associated eigenvectors are

$$\mathbf{v}_n = \frac{1}{\sqrt{N}}\left[1 \quad \phi_n \quad \phi_n^2 \quad \cdots \quad \phi_n^{N-1}\right]^T.$$

Obviously, the matrix $\mathbf{S}_c$ has an eigenvalue of zero and all other eigenvalues are 1. The eigenvector corresponding to the zero eigenvalues is $\mathbf{v}_0 = \left[\frac{1}{\sqrt{N}} \quad \frac{1}{\sqrt{N}} \quad \cdots \quad \frac{1}{\sqrt{N}}\right]^T$. Hence, the eigenvalue decomposition of the matrix $\mathbf{S}_c$ becomes

$$\mathbf{S}_c = \begin{bmatrix}\mathrm{V}_c\\ \mathrm{v}_0^T\end{bmatrix}^T\begin{bmatrix}\mathbf{I} & \mathbf{0}\\ \mathbf{0} & 0\end{bmatrix}\begin{bmatrix}\mathbf{V}_c\\ \mathbf{v}_0^T\end{bmatrix} \tag{15}$$

where $\mathbf{V}_c \in R^{(N-1)\times N}$, whose row vectors are eigenvectors corresponding to the eigenvalue of 1. From (15), (14) becomes

$$\begin{bmatrix}\mathbf{V}_c\\ 0\end{bmatrix}\mathbf{\Theta} = \begin{bmatrix}\mathbf{V}_c\\ \mathbf{v}_0^T\end{bmatrix}\mathrm{v}^*(k). \tag{16}$$

This leads to

$$\mathbf{V}_c(\mathbf{\Theta} - \mathbf{v}^*(k)) = 0 \tag{17}$$

and

$$\mathbf{v}_0^T\mathbf{v}^*(k) = 0. \tag{18}$$

Equation (18) is always true since (11) is always satisfied. From (17), the solution $(\mathbf{\Theta} - \mathbf{v}^*(k))$ must lie in the right null space of the matrix $\mathbf{V}_c$. One can easily see that the right null space is vector $\mathbf{v}_0$ as all row vectors of $\mathbf{V}_c$ are orthogonal to $\mathbf{v}_0$. Therefore, the general solution of (17) (regardless of finite pulse-width resolution) can be represented by

$$\mathbf{\Theta} = \mathbf{v}^*(k) + \lambda\mathbf{d} \tag{19}$$

where $\mathbf{d} = [1 \quad 1 \quad \cdots \quad 1]^T$ and λ is an arbitrary real value. Because elements in $\mathbf{\Theta}$ should be positive, λ is selected to be greater than the negative value of the smallest value in the vector $\mathbf{v}^*(k)$, i.e.

$$\lambda(k) \geq -\min(\mathbf{v}^*(k)). \tag{20}$$

Notably, elements of the right-hand-side vector in (19) are arbitrary positive values, i.e., a *b*-bit quantization is needed to find applicable duties in $\mathbf{\Theta}$ and is denoted as

$$\mathbf{\Theta}(k) = q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\} \tag{21}$$

where elements of $q_b\{\mathrm{y}\}$ are defined as the nearest value of the element in $\mathbb{S}_b$ to $\mathbf{y}$. The block diagram of the proposed modulator is shown in Fig. 3. In the implementation, $q_b\{.\}$ involves only bit truncation.

3) Gating Sequence Generation Pattern: The vector $\mathbf{\Theta}$ is the corresponding duties for an *N*-phase VSI system. Once the vector $\mathbf{\Theta}$ is obtained, the gating signals can be produced accordingly. As an illustrative example, define $q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\} = [\rho_1 \quad \rho_2 \quad \cdots \quad \rho_N]^T$, i.e., (21) becomes

$$\mathbf{\Theta}(k) = q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\} = [\rho_1 \quad \rho_2 \quad \cdots \quad \rho_N]^T. \tag{22}$$

Fig. 4 shows two examples of the gating signals for upper switches (refer to Fig. 1).

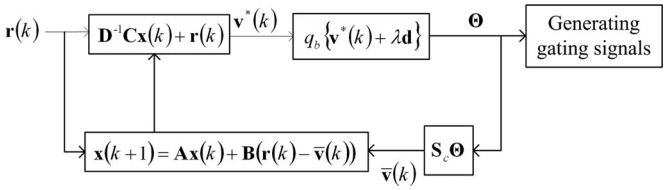

Fig. 3. Block diagram of GSG.

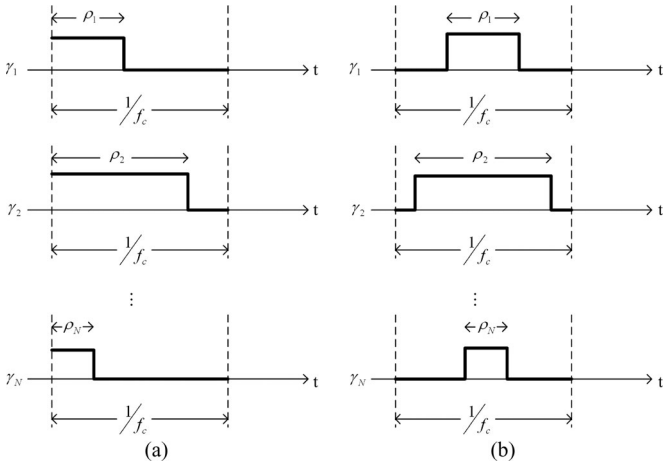

Fig. 4. Examples of gating signals. (a) Single-sided method. (b) Central method.

III. Performance Analysis

A. Range of λ and its Influence

The value of $\mathbf{\Theta}$ is fixed once λ is selected [refer to (22)]. To have feasible duties, elements of $\mathbf{\Theta}$, ρ_i, for $i = 1--N$, should be kept within the range $0 \le \rho_i \le 1$. Therefore, the acceptable range of λ is limited. To see this, first define the permutation matrix $\mathbf{P}_M$ as

$$\mathbf{P}_M \mathbf{v}^*(k) = [\,\hat{v}_1 \quad \hat{v}_2 \quad \cdots \quad \hat{v}_N\,]^T \quad \text{such that } \hat{v}_1 \ge \hat{v}_2 \ge \cdots \ge \hat{v}_N. \tag{23}$$

Therefore,

$$\mathbf{P}_M q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\} = [\,\hat{\rho}_1 \quad \hat{\rho}_2 \quad \cdots \quad \hat{\rho}_N\,]^T \tag{24}$$

where $\hat{\rho}_1 \ge \hat{\rho}_2 \ge \cdots \ge \hat{\rho}_N$. Then, the feasible range of ρ_i, for$i = 1--N$, is

$$\begin{aligned} &\max(\mathbf{\Theta}) = \hat{\rho}_1 = q_b\{\hat{v}_1 + \lambda\mathbf{d}\} \le 1 \\ &\text{and } \min(\mathbf{\Theta}) = \hat{\rho}_N = q_b\{\hat{v}_N + \lambda\mathbf{d}\} \ge 0 \end{aligned} \tag{25}$$

or alternatively, $-\hat{v}_N \le \lambda \le 1 - \hat{v}_1$ regardless of finite pulse-width resolution, and $-\hat{v}_N + \frac{1}{2^{b+1}} \le \lambda \le 1 - \hat{v}_1 - \frac{1}{2^{b+1}}$ considering *b*-bit pulse-width resolution.

Applying the coefficient $\beta \in [0 \quad 1]$, λ can be written as

$$\lambda = (1-\beta)\left(-\hat{v}_N + \frac{1}{2^{b+1}}\right) + \beta\left(1 - \hat{v}_1 - \frac{1}{2^{b+1}}\right). \tag{26}$$

Remark 2: Refer to Fig. 4, $2N$ switching number occurs within one input period. When λ is selected as its boundary value, $-\hat{v}_N + \frac{1}{2^{b+1}}$ or $1 - \hat{v}_1 - \frac{1}{2^{b+1}}$, the switching number is reduced to $2(N-1)$ since either $\hat{\rho}_1 = 1$ or $\hat{\rho}_N = 0$ occurs which implies one phase leg staying at the same level during the whole input period.

B. Minimum Total Conduction Time

The total conduction time is defined as the sum of duties of the active gating states applied within one input period. Minimum total conduction time implies the maximum modulation index. Note that for an *N*-phase VSI system, 2^N gating states exist and two zero switching states, $\mathbf{s}_0$ and $\mathbf{s}_{2^N-1}$, correspond to the same space vector, $\mathbf{S} = \mathbf{0}$. Maximizing the duties of $\mathbf{s}_0$ and $\mathbf{s}_{2^N-1}$ results in minimum total conduction time.

Consider the permutated phase duty vector $\mathbf{P}_M\mathbf{\Theta}$ [see (22) and (24)]. It is intuitive that the maximum duties for $\mathbf{s}_0$ and $\mathbf{s}_{2^N-1}$ are $1 - \hat{\rho}_1$ and $\hat{\rho}_N$, respectively. Therefore, the minimum total conduction time is obtained by subtracting the duty of $\mathbf{s}_{2^N-1}$ from the maximum duty among phase legs $\hat{\rho}_1 - \hat{\rho}_N$.

Remark 3: From *remark 2*, give $\lambda = -\hat{v}_N + \frac{1}{2^{b+1}}$ or $1 - \hat{v}_1 - \frac{1}{2^{b+1}}$, and the modulator has minimum switching number $2(N-1)$. Therefore, the proposed gating signal generator operates at minimum total conduction time and minimum switching number point, yielding a maximum modulation index and minimum switching loss.

C. Quantization Error

The quantization error vector $\mathbf{\Delta}_b$ is defined as the difference between input and output of the quantizer $q_b\{.\}$ which is the same as the conventional methods, i.e. (refer to Fig. 3)

$$\mathbf{\Delta}_b = (\mathbf{v}^* + \lambda\mathbf{d}) - q_b\{(\mathbf{v}^* + \lambda\mathbf{d})\}. \tag{27}$$

The concept of error analysis is extended from [29] to the MIMO system. $\mathbf{e}$ in (7) is written as the following expression using (9) and (10) and Fig. 3:

$$\begin{aligned} \mathbf{e}(k) &= \mathbf{C}\mathbf{x}(k) + \mathbf{D}(\mathbf{r}(k) - \bar{\mathbf{v}}(k)) \\ &= \mathbf{C}\mathbf{x}(k) + \mathbf{D}\mathbf{r}(k) - \mathbf{D}\mathbf{S}_c q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\} \\ &= \mathbf{D}(\mathbf{v}^*(k) - \mathbf{S}_c q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\}). \end{aligned} \tag{28}$$

Then from (27), (28) becomes

$$\begin{aligned} \mathbf{e}(k) &= \mathbf{D}(\mathbf{v}^*(k) - \mathbf{S}_c q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\}) \\ &= \mathbf{D}(\mathbf{v}^*(k) - \mathbf{S}_c(\mathbf{v}^*(k) + \lambda\mathbf{d} - \mathbf{\Delta}_b)) \\ &= \mathbf{D}(\mathbf{v}^*(k) - (\mathbf{v}^*(k) - \mathbf{S}_c\mathbf{\Delta}_b)) \\ &= \mathbf{D}\mathbf{S}_c\mathbf{\Delta}_b. \end{aligned} \tag{29}$$

Therefore, the signal $\mathbf{e}$ is dependent on the quantization error $\mathbf{\Delta}_b$. Notably, the portion $\mathbf{S}_c\mathbf{\Delta}_b$ is the influence of quantization error $\mathbf{\Delta}_b$ on the load. Further, because the filter matrix is in diagonal form, $\mathbf{D}$ is a diagonal matrix, i.e., $\mathbf{e}$ is the scaled quantization error that appears on the load windings and is minimized by the proposed modulator.

IV. Simulation Results

Simulation that compares the influence of filter matrix is done under the five-phase setting. MATLAB is used as a simulation platform. Five-phase sinusoidal references with large/small modulation indices are applied to verify the compensating ability of the proposed switching strategy.

A. Simulated System and Implementation

The modulator with first- and second-order weighting filters is compared with the conventional SVPWM under the digital implementation settings. The weighting filters are the first- and second-order integrator systems, $z/(z-1)$ and $z^2/(z^2-2z+1)$. We denote the one having no feedback loop as SVPWM. The system state-space matrices for the first- and second-order filter matrices are $\mathbf{a} = \mathbf{b} = \mathbf{c} = d = 1$ (denoted as PWM_1st) and $\mathbf{a} = \begin{bmatrix} 2 & -1 \\ 1 & 0 \end{bmatrix}$, $\mathbf{b} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$, $\mathbf{c} = [2 \quad -1]$, $d = 1$ (denoted as PWM_2nd), respectively [refer to (6)–(8)].

Referring to Fig. 3, the implementation block diagram is shown in Fig. 5. Notably, no multipliers are needed in the implementation. Because the coefficients of filters are either 1 or 2, only adders and shifters are needed to implement weighting filter. The quantization block $q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\}$ involves only bit truncation. Further, only counters and comparators are needed to generate gating signals given the phase duties $\mathbf{\Theta}$. Finally,

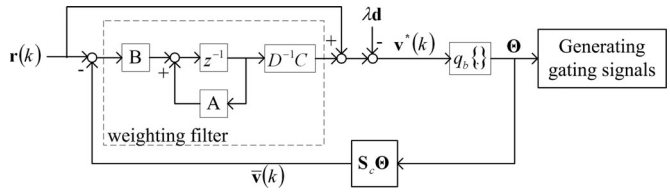

Fig. 5. Implementation block diagram.

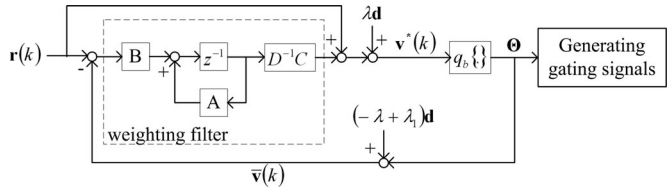

Fig. 6. Implementation block diagram in MATLAB.

consider the feedback loop

$$\bar{\mathbf{v}}(k) = \mathbf{S}_c\boldsymbol{\Theta} \text{ where } \mathbf{S}_c = \begin{bmatrix} (N-1)/N & -1/N & \cdots & -1/N \\ -1/N & (N-1)/N & \ddots & \vdots \\ \vdots & \ddots & \ddots & -1/N \\ -1/N & \cdots & -1/N & (N-1)/N \end{bmatrix}. \quad (30)$$

From (27) and Fig. 5, we can write

$$\begin{aligned} \bar{\mathbf{v}}(k) &= \mathbf{S}_c q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\} \\ &= \mathbf{S}_c(\mathbf{v}^*(k) + \lambda\mathbf{d} - \boldsymbol{\Delta}_b) \\ &= \mathbf{v}^*(k) - \mathbf{S}_c\boldsymbol{\Delta}_b \end{aligned} \quad (31)$$

and

$$\boldsymbol{\Theta} = q_b\{\mathbf{v}^*(k) + \lambda\mathbf{d}\} = \mathbf{v}^*(k) + \lambda\mathbf{d} - \boldsymbol{\Delta}_b. \quad (32)$$

Therefore, the relation between $\bar{\mathbf{v}}(k)$ and $\boldsymbol{\Theta}$ is

$$\begin{aligned} \bar{\mathbf{v}}(k) &= \mathbf{v}^*(k) - \mathbf{S}_c\boldsymbol{\Delta}_b \\ &= \boldsymbol{\Theta} - \lambda\mathbf{d} + (\mathbf{I} - \mathbf{S}_c)\boldsymbol{\Delta}_b \\ &= \boldsymbol{\Theta} - \lambda\mathbf{d} + \lambda_1\mathbf{d} \end{aligned} \quad (33)$$

where $\lambda_1 = \left(\frac{1}{N}\mathbf{d}^{\mathrm{T}}\boldsymbol{\Delta}_b\right)$. Equation (33) states that only adders are needed to implement feedback loop. The block diagram implemented in MATLAB is shown in Fig. 6.

B. Simulation Results

A five-phase sinusoidal reference input with normalized amplitude 0.51 and frequency 60 Hz is applied. The carrier frequency is 3 kHz and the pulse-width resolution is 8, yielding a clock rate of $2^8 \times 3k = 768k$ Hz. Figs. 7(a)–9(a) show one of the leg voltages, line-to-line voltages, and phase voltages for the three aforementioned PWMs. The five-phase voltages produced on the load are also shown in Figs. 7(b)–9(b) to verify the correctness of the gating signals. In Figs. 10–12, the filtered phase voltage of the load and its frequency analysis for different weighting filters are shown.

To have a precise comparison, Tables I and II list the switching number and the harmonic distortion for modulation indices 0.51 and 0.1. It is seen that with the shaping filter that relocates the noise in the higher frequency band, the harmonic distortion of PWM_1st and PWM_2nd is reduced within [0 500] Hz compared to that of SVPWM, especially for small modulation index. Further, the shaping effect is more obvious in PWM_2nd than in PWM_1st, i.e., the lowest harmonic distortion (within [0 500] Hz) is obtained in PWM_2nd. The harmonic distortion within [0 5 k] Hz for these three systems is comparable yielding approximately the same level of error power which is induced by finite pulse-width resolution. Therefore, with the shaping filter, components of error tend to be distributed over high-frequency band.

C. Sensitivity of Pulse-Width Resolution

To address the influence of the quantization and weighting filter, different pulse-width resolutions are applied to SVPWM, PWM_1st and PWM_2nd. Input references are five-phase sinusoidal waves with modulation indices 0.51 and 0.1. Figs. 13 and 14 show the harmonic distortion within [0 500] Hz. Obviously, the harmonic distortion deteriorates under low pulse-width resolution, especially for small modulation index. With the shaping filter, the deterioration alleviates. Comparing the harmonic distortion of PWM_1st (PWM_2nd) and SVPWM, the reduction of 50% (75%) is obtained for low pulse-width resolution. Therefore, the pulse-width resolutions needed to achieve the same harmonics performance are 6, 7, and 8 bits for systems PWM_2nd, PWM_1st, and SVPWM, yielding a reduced system clock rate requirement.

V. Experimental Results

To confirm the effectiveness of the proposed switching strategy, a five-phase two-level VSI system with *R–L* load is built. The implementation block diagram is shown in Fig. 15. Three modulators, SVPWM, PWM_1st, and PWM_2nd (refer to Section IV), are implemented on FPGA EP2C20F484C8 (Cyclone II). A wye-type *R–L* circuit with resistance of 10 Ω and inductance of 0.5 mH is connected to the output of the VSI as the load. IGBT modules PS21564-P DIP-IPM (Mitsubishi) are used as the five-phase voltage source inverter. DC supply voltage and dead time of VSI are 20 V and 2.2 μs, respectively. Fig. 16 shows a photograph of experimental platform.

Five 20 Hz sinusoidal waves with $2\pi/5$ phase shift are applied as the reference signals. The carrier frequency is 1 kHz. This is reasonable for high-power applications because of the limited IGBT switching frequency. From the simulation results, the improvement is obvious under the low modulation index. Therefore, the normalized amplitude of the five-phase reference is selected as 0.1 to show the effectiveness of the proposed strategy. Figs. 17(a)–19(a) show various signals measured from the first phase of the *R–L* circuit with 8-bit pulse-width resolution. The five-phase load voltages in Figs. 17(b)–19(b) state that the switching strategies produce the desired signals properly. The five-phase current waveforms are also shown in Figs. 17(c)–19(c). Because of the small modulation index, all modulators

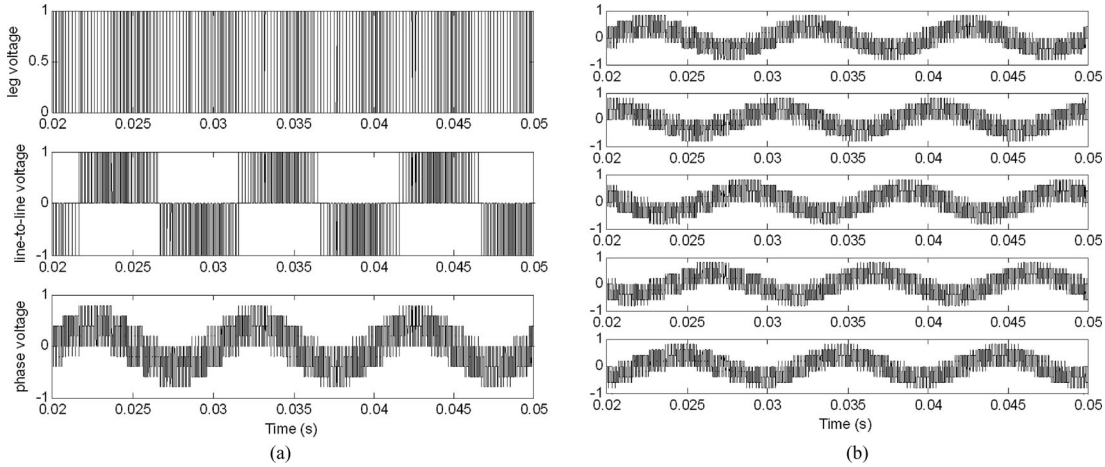

Fig. 7. Simulation results of SVPWM. (a) Leg voltage (top), line-to line voltage (middle), and phase voltage (bottom). (b) Five-phase load voltages.

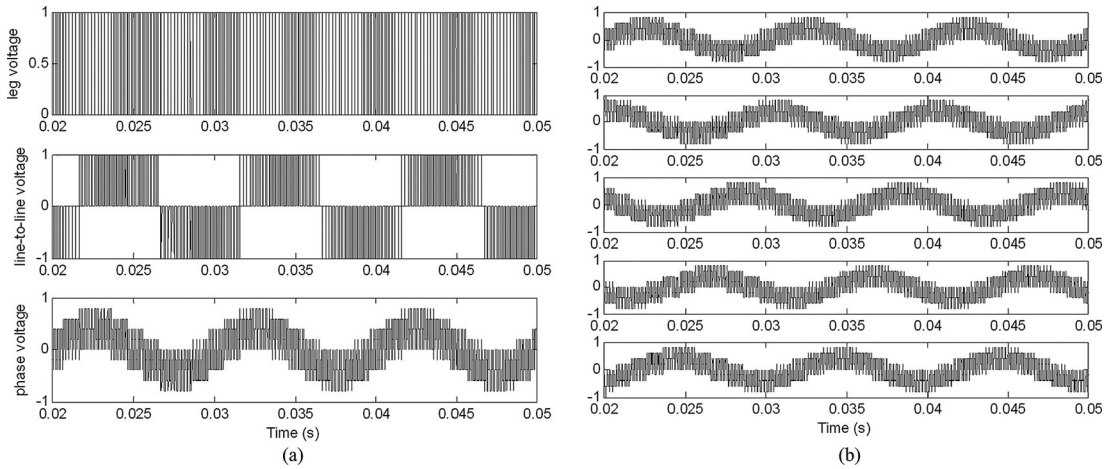

Fig. 8. Simulation results of PWM_1st. (a) Leg voltage (top), line-to-line voltage (middle), and phase voltage (bottom). (b) Five-phase load voltages.

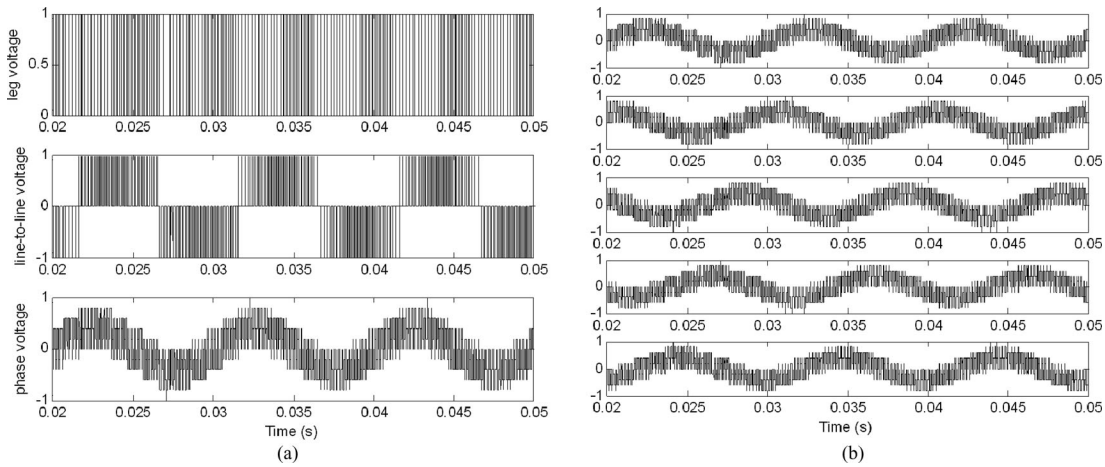

Fig. 9. Simulation results of PWM_2nd. (a) Leg voltage (top), line-to-line voltage (middle), and phase voltage (bottom). (b) Five-phase load voltages.

produce phase currents with large ripple. Nevertheless, as shown in Table III, introduction of the feedback loop can improve the harmonic distortion.

To see the influence of pulse-width resolution and weighting filter, Fig. 20 shows harmonic performance under various pulse-width resolutions. Observations similar to the simulation results are obtained. For low pulse-width resolution, the harmonic distortion of SVPWM worsens. With the shaping filter, the harmonics are reduced. The reduction rate is 40% under 6-bit pulse-width resolution and 10% under 7 bits. It is worth

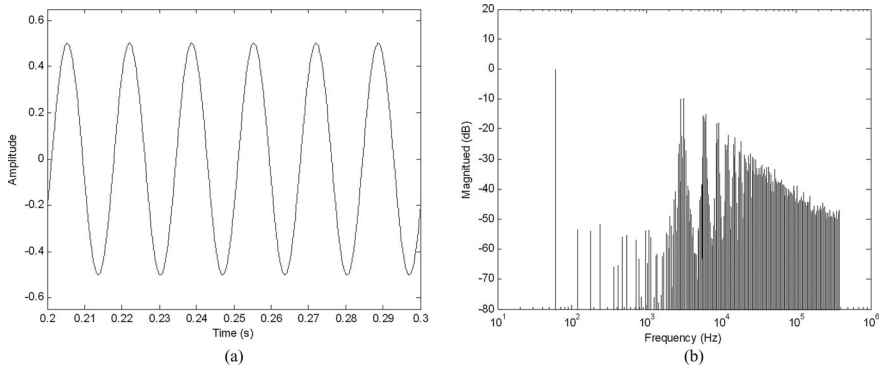

Fig. 10. Phase voltage of SVPWM. (a) Time-domain response. (b) Frequency-domain analysis.

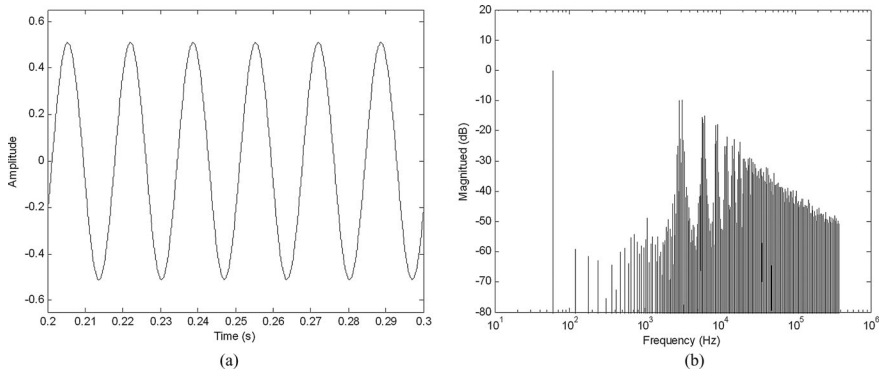

Fig. 11. Phase voltage of PWM_1st. (a) Time-domain response. (b) Frequency-domain analysis.

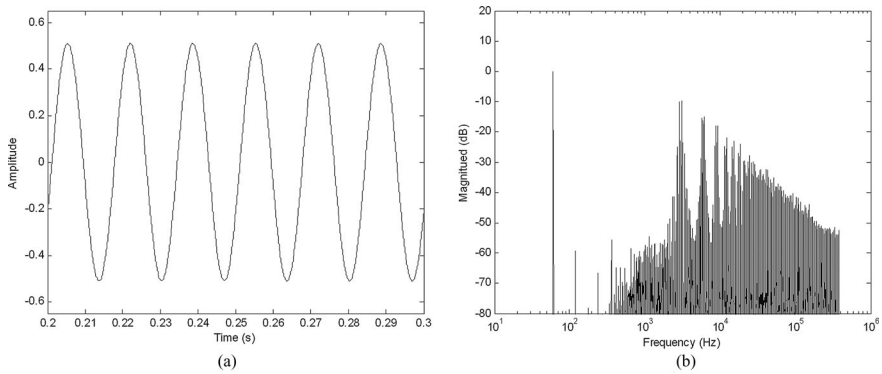

Fig. 12. Phase voltage of PWM_2nd. (a) Time-domain response. (b) Frequency-domain analysis.

TABLE I
HARMONIC DISTORTION AND SWITCHING NUMBER FOR 8-BIT PULSE-WIDTH RESOLUTION (WITH INPUT AMPLITUDE 0.51)

Input amplitude: 0.51	SVPWM	PWM_1st	PWM_2nd
Harmonics distortion within [0 500] Hz (%)	0.439	0.244	0.215
Harmonics distortion within [0 5000] Hz (%)	43.072	43.150	43.154
Switching number (per second)	24k	24k	24k

TABLE II
HARMONIC DISTORTION AND SWITCHING NUMBER FOR 8-BIT PULSE-WIDTH RESOLUTION (WITH INPUT AMPLITUDE 0.1)

Input amplitude: 0.1	SVPWM	PWM_1st	PWM_2nd
Harmonics distortion within [0 500] Hz (%)	2.258	0.903	0.413
Harmonics distortion within [0 5000] Hz (%)	80.173	80.117	80.099
Switching number (per second)	22.8k	23.4k	23.28k

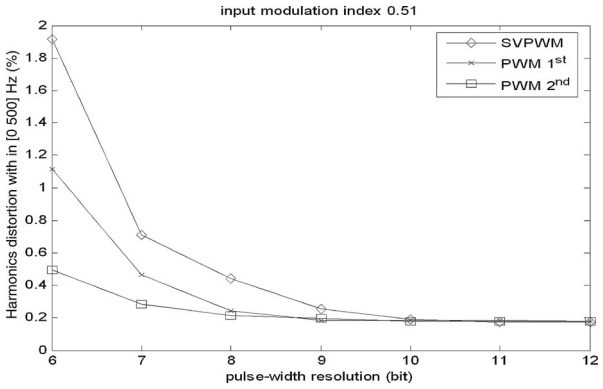

Fig. 13. Harmonic distortion under different pulse-width resolutions (modulation index 0.51).

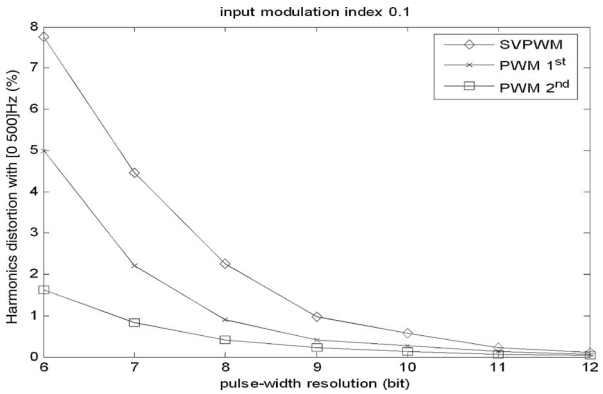

Fig. 14. Harmonic distortion under different pulse-width resolutions (modulation index 0.1).

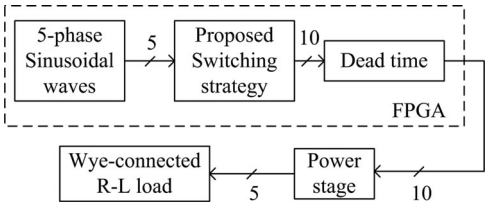

Fig. 15. Implementation block diagram.

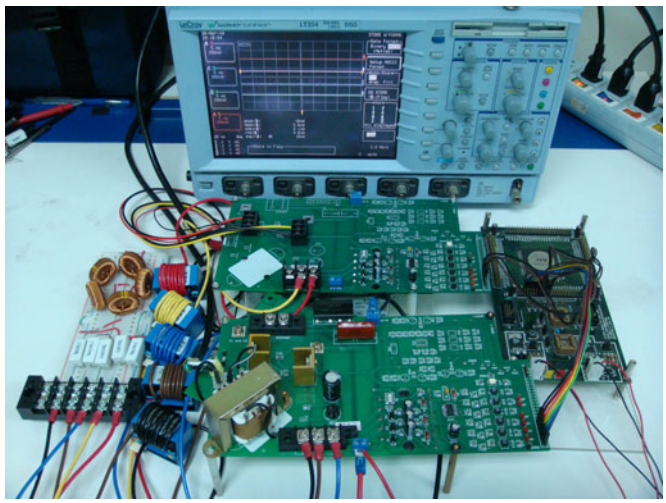

Fig. 16. Experimental platform.

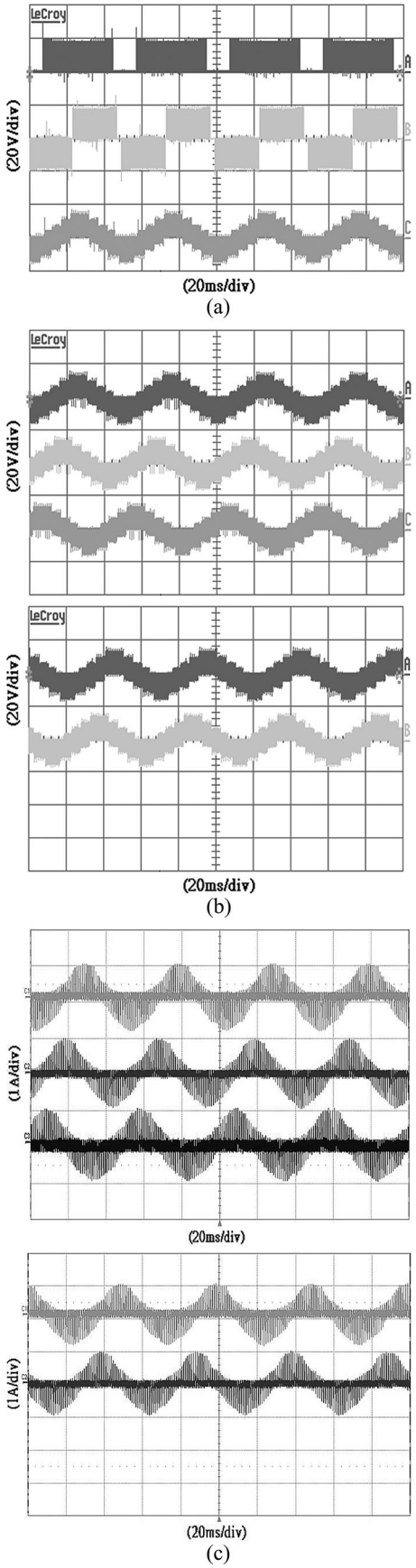

Fig. 17. Experimental results of SVPWM. (a) Leg voltage (top), line-to-line voltage (middle), and phase voltage (bottom). (b) Five-phase load voltages. (c) Five-phase load currents.

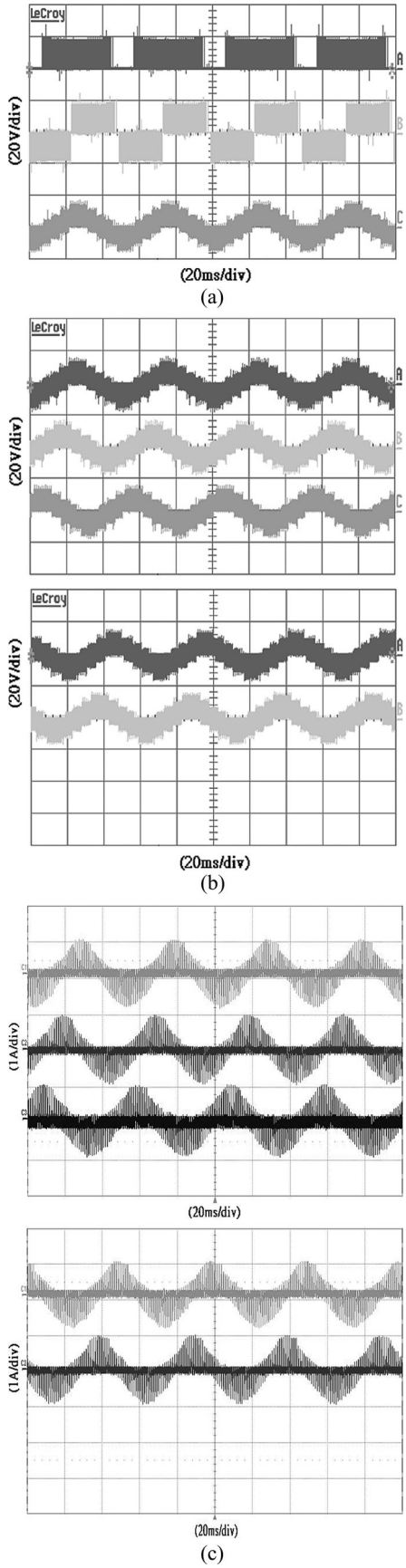

Fig. 18. Experimental results of PWM_1st. (a) Leg voltage (top), line-to-line voltage (middle), and phase voltage (bottom). (b) Five-phase load voltages. (c) Five-phase load currents.

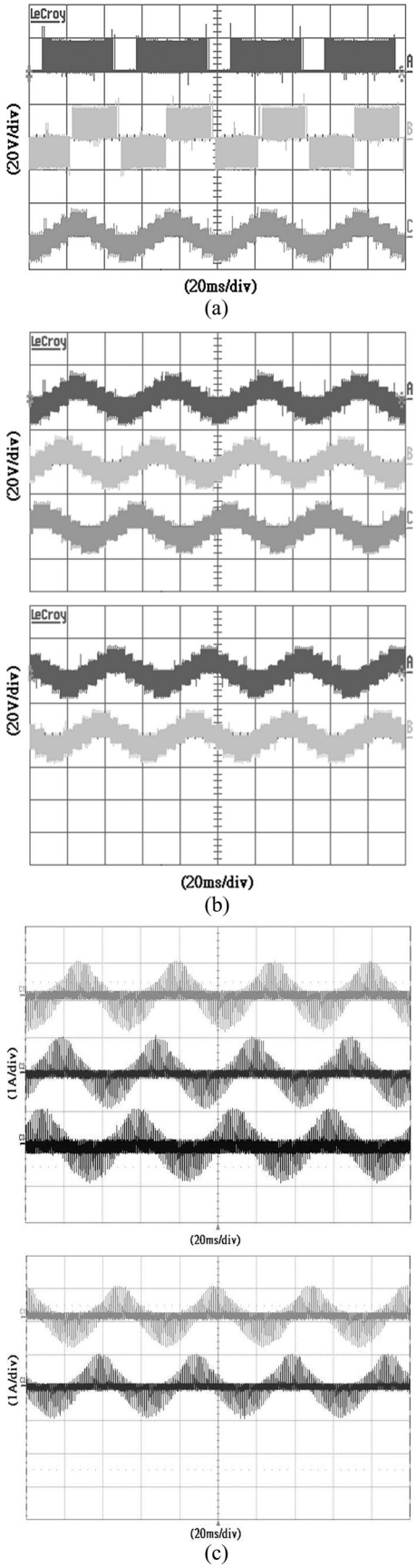

Fig. 19. Experimental results of PWM_2nd. (a) Leg voltage (top), line-to-line voltage (middle), and phase voltage (bottom). (b) Five-phase load voltages. (c) Five-phase load currents.

TABLE III
HARMONIC DISTORTION OF THE PHASE CURRENT

Input amplitude: 0.1	SVPWM	PWM_1st	PWM_2nd
Harmonics distortion within [0 300] Hz (%)	5.1394	5.9727	3.7378

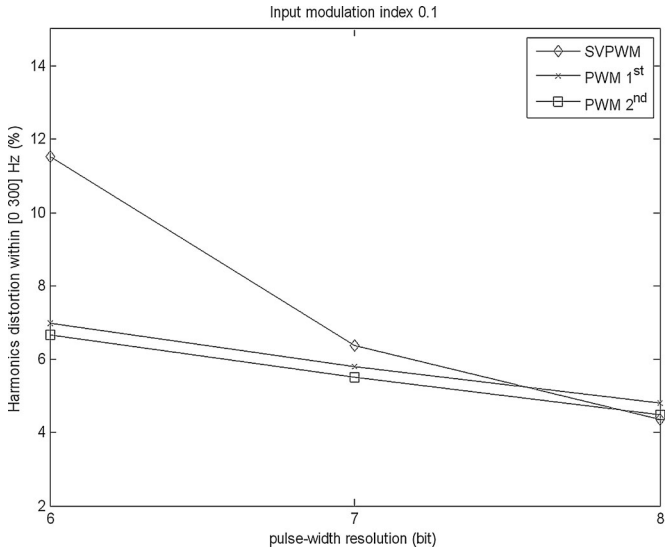

Fig. 20. Harmonic distortion under different pulse-width resolutions (modulation index 0.1).

mentioning that other than finite pulse-width resolution, nonideal factors such as nonzero rising/fall time of IGBTs and dead time of each phase leg can also influence the tracking precision. These factors cause the differences in the simulation results. Nevertheless, the improvements shown by experiments prove that the proposed strategy could compensate for the effect of finite pulse-width resolution.

VI. CONCLUSION

This paper adopts an algebraic analysis viewpoint of optimal matching problem as opposed to a vector analysis viewpoint which is commonly adopted. Based on the load model, the optimized reference for the matching problem is discussed with feasibility analysis. By applying eigenspace decomposition, a general solution to match feasible optimal reference signals under limited space vectors can be derived and the selection of gating states to minimize total conduction time and switching number is described. Furthermore, no other complex calculation is needed when phase number increases. In the simulations, two shaping filters, first-order and second-order integrator systems, are applied to compare with SVPWM. Implementation block diagram of overall system is discussed. Further study of implementing feedback loop without multipliers is shown.

The simulation results state that SVPWM is sensitive to the pulse-width resolution. Similar observations are obtained in the experimental results. By applying the feedback loop with weighting filter, the harmonic distortion is reduced compared with SVPWM, i.e., the proposed filtered SVPWM is capable of compensating the quantization error induced by finite pulse-width resolution especially for small modulation index signals.

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