A High-Power Input-Parallel Output-Series Buck and Half-Bridge Converter and Control Methods

Qing Du, Bojin Qi, Tao Wang, Tao Zhang, and Xiao Li

***Abstract*—The two-switch cascade converter is the most appropriate solution for efficient high-power applications among the existing converter topologies. However, the cascade structure and the nonlinear dc gain of boost circuit are more likely to cause severe oscillations if the criterion for the selection of the operation mode is chosen improperly during step-up/step-down transition. A novel high-power input-parallel output-series buck-half-bridge (IPOSBHB) converter is proposed in this paper. The circuit structure, operating principles, and basic relations are analyzed. Comparisons between IPOSBHB and two-switch cascade converter are also elaborated on with respect to voltage and current stress, total volume of magnetic components, and efficiency. In addition, the inconformity of the transfer functions, the discontinuity caused by the switching time delay, and the disturbance of input voltage are analyzed. Methods for compensation are also proposed. The proposed converter can achieve satisfactory comprehensive performance when the step-up ratio is low. The combinational control strategy and the compensation methods proposed in this paper are easy to carry out in order to achieve effective control at steady state, smooth transition at mode change, and reduction of the adverse effect caused by the disturbance of input voltage. A 15-kW prototype is used to validate the proposed theory.**

***Index Terms*—Control, efficiency, high power, step-up/step-down converter, transition.**

NOMENCLATURE

$V_{\rm in}$, V_o	Input voltage and output voltage.
I_o	Output current.
V_g, I_g	Desired voltage and current.
N	Step-up ratio of the converter ($V_o/V_{\rm in}$).
V_m, I_m	Peak voltage and current of all switch device.
T_s	Switching cycle of S_1, S_2, and S_3.
L, L_1, L_2	Inductance of inductors.
R	Load.
C_1–C_4	Capacitance of the capacitors.
v_{S1}, v_{S3}, v_{D1}, v_{D5},	Voltage of S_1, S_3, D_1, and D_5.
i_{S1}, i_{S3}, i_{D1}, i_{D5}, i_T	Current of S_1, S_3, D_1, D_5, and T.
$V_{\rm CE3}$, V_{D1}	Conduction voltage drop of T_3 and D_1.
$D_{\rm Buck}$	Duty cycle of Buck module (S_3).
$D_{\rm HB}$	Duty cycle of half-bridge module (S_1 or S_2).
$d_{\rm ctrl}$, $d_{\rm Buck}$, $d_{\rm HB}$	Theoretical values of duty cycle.
$d_{\rm Buck\_act}$, $d_{\rm HB\_act}$	Actual values of duty cycle.
D_{Z1}, D_{Z2}	Duty cycles of turning ON and OFF delay.
$d_{\rm shift}$	Shift distance of carrier wave.
Δi_L	Ripple current.
I_L	Average current of the inductor L.
N_P, N_S	Primary winds and secondary winds of transformer T.
n	Transformer turns ratio (N_S/N_P).
A_p	Area product.
P_t, $P_{O(T)}$	Apparent power and output power of the transformer.
W	Transferring energy of the transformer.
η, η_T, $\eta_{\rm HB}$	Efficiencies of the converter, the transformer, and half-bridge module.
e_u, e_i	Error signals of voltage loop and current loop.
e	Input error signal for compensation algorithm.
$v_{\rm ctrl}$, $v'_{\rm ctrl}$	Modulation error signal and auxiliary error signal.
$v_{\rm tri1}$, $v_{\rm tri2}$	Carrier waves for buck and half-bridge modules.
H	Sampling coefficient.
$G_{\rm cmp1}$, $G_{\rm cmp2}$	Inconformity compensation factors of buck and half-bridge modules.
G_c	Transfer function of compensation network.
G_p	Transfer function of control object.
G'_p	Transfer function of control object after inconformity compensation.
k_F	Gain factor of feed-forward compensation.

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Q. Du, B. Qi, T. Wang, and T. Zhang are with the School of Mechanical Engineering and Automation, Beihang University, Beijing 100191, China (e-mail: danielduqing@163.com; qbj@buaa.edu.cn; wangtao2118@126.com; zhangtao_tiger@163.com).

X. Li was with the School of Mechanical Engineering and Automation, Beihang University, Beijing 100191, China. He is now with Carnegie Mellon University, Pittsburgh, PA 15213-3890 USA (e-mail: shawnlee007@hotmail.com).

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I. INTRODUCTION

IN recent years, dc–dc converters with step-up/step-down characteristics have been widely used in applications such as portable devices [1]–[4], communication power supply [5], [6], power factor correction [7]–[10], hybrid electrical vehicles or fuel-cell vehicles [11]–[13], and photovoltaic (PV) power generation [14], [15]. The last two applications need higher

power supply of kilowatt level or over. The output power of fuel-cell engines could go up to 100 kW for buses [16]; the power of small rooftop PV power generation equipments is about 2–5 kW [28], and the power of large PV power systems is up to 10 kW, or even up to hundreds of kilowatts or over [17]. Demand for high power and wide range of input voltage greatly increases the difficulty of converter design. Moreover, in addition to realizing the basic functions, having high-reliability, high-efficiency, high-power density, and large margin of stability of the converter are also common requirements for all applications. Therefore, the design of dc–dc converters that have step-up/step-down characteristics and meet the aforementioned requirements has important practical significance.

The basic topologies that can achieve step-up and step-down functions are classified as isolated and nonisolated [11]. Due to the introduction of the transformer, the former can easily be grouped together by serial or parallel at input or output to achieve special functions [18]. Compared to the latter, isolated converter cannot achieve high efficiency since all of the input energy must go through the transformer to the output. The latter contains single-switch topologies, such as buck–boost converter, Cuk converter, single-ended primary-inductance converter, Zeta converter, two-switch cascade converter, namely noninverting buck–boost and boost–buck converters, and some other novel converters with coupled inductors [9], [19], [20], which are often used in situations of high voltage gain [21]–[26]. Through the analysis of energy transferring mechanism [7], [27], it is known that the voltage and current stress of the single-switch converter mentioned earlier are high due to the absence of direct energy transfer path from input to output. High stresses not only increase the cost of components, but also decrease the efficiency and reliability of the converter. The converters with coupled inductors can be used for applications that have wide range of input and output voltage, but the leakage of coupled inductors will cause oscillation and high voltage spike across the switches. Clamp circuits are needed to clamp voltage spikes upon switches so as to recycle the leakage energy [20]. Noninverting buck–boost and boost–buck converters have been attacting much attention since their output voltage and input voltage have the same polarity and the components bear lower stress [1]–[3], [7], [8], [10]–[15], [27]–[29]. The circuit structures of noninverting buck–boost and boost–buck converters are presented in Fig. 1.

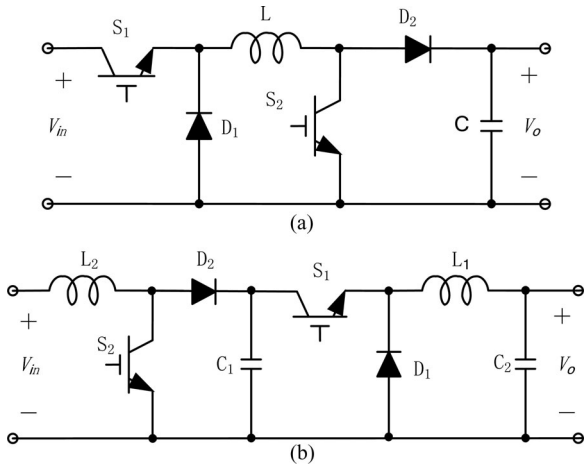

Fig. 1. Two-switch cascade converter. (a) Noninverting buck–boost converter. (b) Noninverting boost–buck converter.

Compared with single-switch nonisolated converter, coordinating the operation mode of the two-switch cascade converter poses a new challenge. The cascade structure has coupling relations between prestage and poststage circuits, because the input of the poststage circuit is the output of the prestage circuit. It is more likely to cause severe oscillations if the criterion for the selection of the operation mode is chosen improperly during step-up/step-down transition [2], and the oscillations would worsen as the output power increases. Taking noninverting boost–buck converter as an example, the easiest way to coordinate the operation mode is to compare the magnitudes of the input and output voltages. In this way, when the output voltage is close to the input voltage, any input power or load variations will immediately affect the level of input voltage and output voltage; then the operation mode will frequently switch between buck and boost, and v_{C1} and v_{C2} will fluctuate. The fluctuation of v_{C1} would further deteriorate the stability of v_{C2}. Furthermore, the voltage drops in the components, which vary with load current, must be taken into consideration. In addition, the discontinuity of the actual duty cycle caused by the switching time delay and the nonlinear dc gain of output voltage to duty cycle in boost mode will also worsen the transients [28].

The control methods of two-switch cascade converters include synchronous control [15], interleaving control [14], and combinational control. The advantages offered by synchronous control include simple control circuit design and no change of operation mode, however it needs a large inductor and the switches suffer high current stress. Each switch turns ON and OFF once during every switching cycle, so the switching loss is high. Interleaving control has the same characteristics of synchronous control, but it needs smaller inductor volume. Combinational control has the advantages of lower current stress and switching loss because only one switch turns ON and OFF once during every switching cycle, but it is difficult to realize smooth transition between two operation modes. In an effort to solve this problem, a compensation method that involves inserting a buck–boost mode between step-down and step-up modes was investigated, but the current stress and switching loss are still high during transition [29]. Another method was proposed that introduced a "filter mode" to make the converter have maximum efficiency when the input voltage is close to the output voltage, but this method is an open-loop control and the transition is not smooth [6]. Another method investigated by researchers inserted a combination of buck and boost modes instead of a buck–boost operating mode. This is a closed-loop control and can improve the efficiency of the converter [2], [3]. A technique to reduce the discontinuity due to devices' switching time delay at mode change was achieved by compensating the discontinuity and nonlinearity between the output voltage and the effective duty cycle [28]. This technique can realize the smooth transition during mode change, but the compensation algorithm is complex.

In this paper, a novel input-parallel output-series buck and half-bridge converter (IPOSBHB) is proposed. This topology is a combination of buck and half-bridge in which the input nodes connect in parallel and the output nodes connect in series. The complete decoupling is realized from inputs in IPOSBHB, which eliminates the mutual effects between modules and avoids oscillations; there is no nonlinear dc gain in the circuit, so it is easy to achieve smooth transition. This novel converter can achieve satisfactory comprehensive performance when the step-up ratio is not very high (no more than 1.6). A combinational control strategy and compensation methods are proposed in this paper to achieve effective control at steady state and to improve dynamic performance at mode change.

This paper has been organized as follows. In Section II, the circuit structure, operating principles, and the basic relations of IPOSBHB are analyzed. The voltage and current stress of switching device, the volume of magnetic components, and efficiency of the converter are also presented in this section in comparison with the two-switch cascade converter. Section III shows the small-signal model of IPOSBHB and the ideal pulsewidth modulation (PWM)-pulse-generation method for step-up and step-down modes. And, on this basis, a compensation technique is presented to deal with the problem of different transfer functions in step-up and step-down modes. Another compensation technique of carrier wave parallel shifting is also presented to solve the problem of discontinuity caused by switching time delay and an input-voltage feed-forward compensation technique is proposed to suppress disturbances and improve the dynamic performance. Verifications of the proposed theories and techniques via a 15-kW prototype are provided in Section IV. Finally, in Section V, conclusions are drawn based on the previous analysis.

II. IPOSBHB

A. Circuit Structure

The circuit structure of IPOSBHB is shown in Fig. 2. The buck module is composed of C_3, S_3, D_5, and L, and the half-bridge module is composed of C_1, C_2, S_1, S_2, D_1–D_4, L, and T. The primary winding of the transformer T is N_P and the secondary winding is N_S. The input nodes of buck and half-bridge connect in parallel sharing the same power supply and the output nodes connect in series sharing the same inductor L, so the overall output voltage is equal to the summation of buck output voltage and half-bridge output voltage.

Step-up/step-down functions can be achieved by controlling the duty cycle $D_{\rm HB}$ of half-bridge module (S_1 or S_2) and the duty cycle $D_{\rm Buck}$ of buck module (S_3). When $D_{\rm Buck} = D_{\rm HB} = 0$, then $V_o = 0$. As $D_{\rm Buck}$ and $D_{\rm HB}$ increase, V_o will also increase, and when $D_{\rm Buck}$ and $D_{\rm HB}$ are relatively small, then $V_o < V_{\rm in}$, which is step-down mode. When $D_{\rm Buck} = 1$, S_3 is ON, and the output voltage of the buck module is approximate to the input voltage, so if $D_{\rm HB} > 0$, then $V_o > V_{\rm in}$, which is step-up mode.

The efficiency of the buck module can be as high as 96% at rated power, while the efficiency of the half-bridge module is only about 90%. It is thus conducive to improving the overall efficiency when buck module could provide more power. Therefore, an efficient mode of IPOSBHB is designed and shown in Fig. 3. When the input voltage is higher than the desired output voltage, S_3 works while S_1 and S_2 are OFF, and all the input power is transferred through buck module. When the input voltage is lower than the desired output voltage, S_3 is ON, and S_1 and S_2 work, and the half-bridge circuit provides the additional voltage between output and input.

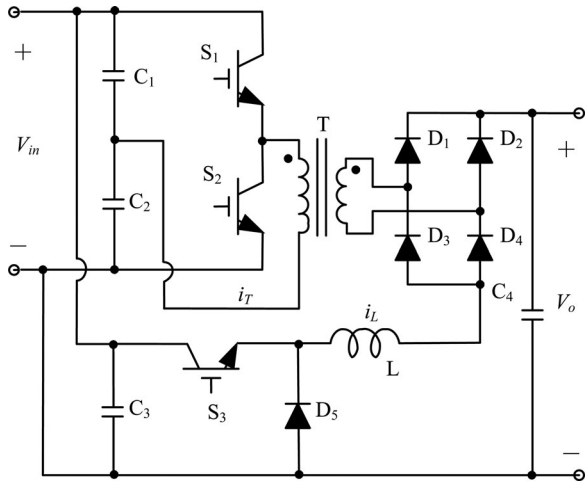

Fig. 2. IPOSBHB circuit structure.

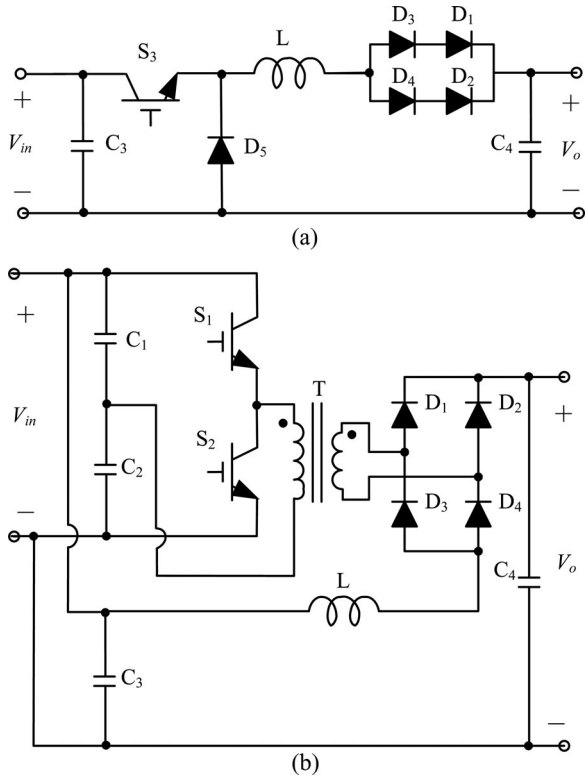

Fig. 3. Equivalent circuit of IPOSBHB. (a) Step-down mode. (b) Step-up mode.

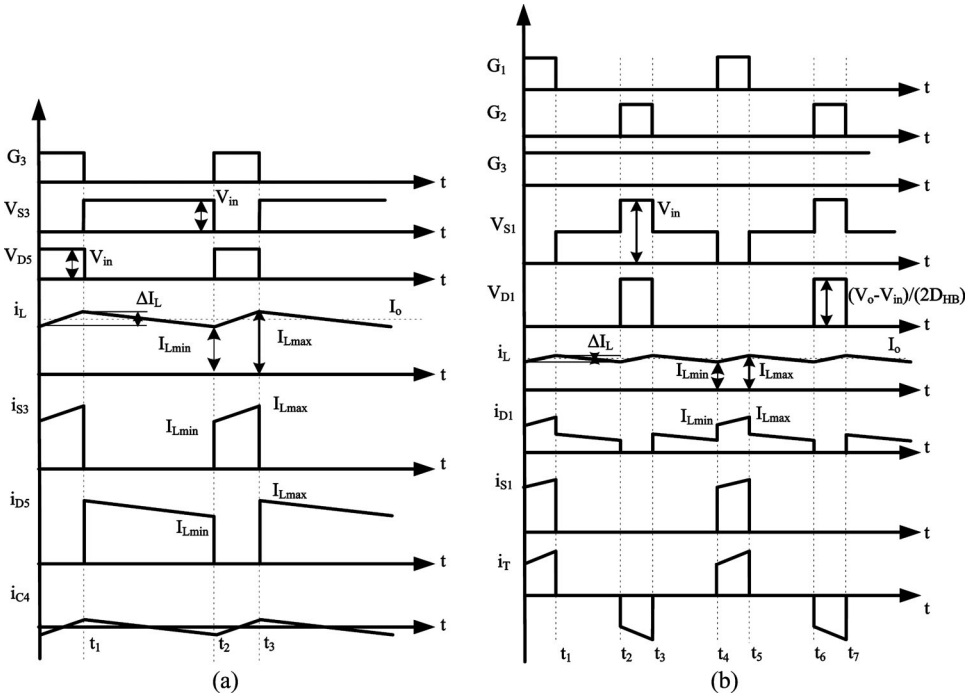

Fig. 4. Waveforms in CCM of IPOSBHB. (a) Step-down mode. (b) Step-up mode.

B. Operating Principles

To simplify the analysis of the IPOSBHB converter's operating principles in continuous conduction mode (CCM), the following essential assumptions are made. The switches turn ON/OFF with near or zero time delays and with no conductive losses. The inductor and the transformer are also ideal elements and work in the unsaturated regions, and the parasitic resistance and leakage inductance are assumed to be zero. The capacitor equivalent series resistance is zero and the ratio of ripple to output voltage is extremely small so that the steady-state capacitor voltage can represent the dynamic voltage. And the path transmission loss can also be ignored.

1) Step-Down Mode: Compared to pure buck circuit, IPOSBHB has additional diodes D_1–D_4 in step-down mode. Because of the continuous inductor current, the diodes are always ON, and the current going through every diode is equal to half of the inductor current. Waveforms of chief elements of IPOSBHB in step-down mode are shown in Fig. 4(a). G_3 is the driving signal of S_3, and v_{S3}, v_{D5}, i_{S3}, and i_{D5} are the voltages and currents of S_3 and diode D_5, respectively.

a) Mode 1 (0–t_1): S_3 is ON and D_5 is OFF. The inductor current is increasing linearly, and when $t = t_1$, the inductor current reaches its maximum value I_{Lmax}. The ripple current Δi_L is

$$\Delta i_L = \frac{V_{\mathrm{in}} - V_o}{L} D_{\mathrm{Buck}} T_s \tag{1}$$

where T_s is the switching cycle of S_1, S_2 and S_3.

b) Mode 2 (t_1–t_2): S_3 is OFF and D_5 is ON. The inductor current is decreasing linearly, and when $t = t_2$, the inductor current reaches its minimum value I_{Lmin}. The ripple current Δi_L is

$$\Delta i_L = \frac{V_o}{L} (1 - D_{\mathrm{Buck}}) T_s. \tag{2}$$

2) Step-up Mode: S_3 is always ON in step-up mode, so the output voltage of IPOSBHB can be equivalent to the input voltage in series with the output voltage of half-bridge circuit. Waveforms of the chief elements of IPOSBHB in step-up mode are shown in Fig. 4(b). G_1 and G_2 are the driving signals of S_1 and S_2, and v_{S1}, v_{D1}, i_{S1}, and i_{D1} are the voltages and currents of S_1 and D_1, respectively, and i_T is the transformer current.

a) Mode 1 (0–t_1): S_1 is ON and S_2 is OFF. The voltage of C_1 is applied on the primary winding of the transformer *T*. Since $C_1 = C_2$, the voltage on primary winding of the transformer equals to $0.5V_{\mathrm{in}}$, and at this moment, D_2 and D_3 are OFF, while D_1 and D_4 are ON. The inductor current i_L is increasing linearly, and when $t = t_1$, the inductor current reaches its maximum value I_{Lmax}. The ripple current Δi_L is

$$\Delta i_L = \frac{(1 + 0.5n)V_{\mathrm{in}} - V_o}{L} D_{\mathrm{HB}} T_s. \tag{3}$$

b) Mode 2 (t_1–t_2): S_1 and S_2 turn OFF simultaneously, so the voltage of the primary winding is equal to zero and the output current goes through the diodes D_1–D_4. The inductor current i_L is decreasing linearly, and when $t = t_2$, the inductor current reaches its minimum value I_{Lmin}. The ripple current Δi_L is

$$\Delta i_L = \frac{(1 - 2D_{\mathrm{HB}})(V_o - V_{\mathrm{in}})}{2L} T_s. \tag{4}$$

TABLE I
SWITCHING DEVICES AND STRESS OF IPOSBHB

IPOSBHB	Step-down mode		Step-up mode	
Switching devices	Peak voltage	Peak current	Peak voltage	Peak current
S_1	$0.5V_{in}$	0	V_{in}	nI_o
S_2	$0.5\ V_{in}$	0	V_{in}	nI_o
S_3	V_{in}	I_o	0	I_o
D_1-D_4	0	$0.5I_o$	$(V_o - V_{in})/(2D_{HB})$	I_o
D_5	V_i	I_o	V_{in}	0

C. Basic Relations

1) Step-Down Mode: Equating (1) and (2) leads to (5). The IPOSBHB large-signal dc gain of step-down mode is

$$V_o = V_{\rm in} D_{\rm Buck}. \tag{5}$$

2) Step-Up Mode: Equating (3) and (4) leads to (6). The IPOSBHB large-signal dc gain of step-up mode is

$$V_o = V_{\rm in}(1 + nD_{\rm HB}). \tag{6}$$

D. Performance Analysis of the Topology

It can be seen from Fig. 3 that buck module and half-bridge module are less likely to cause oscillations since their inputs connect in parallel which means that they are independent from each other. It could be seen from (5) and (6) that the output voltage of IPOSBHB in large-signal dc gain is always in a linear relation with duty cycle. To further assess the overall performance of IPOSBHB, comparisons are made between IPOSBHB and two-switch cascade converter with respect to switch stress, magnetic elements, and efficiency. Several assumptions are made before analysis: 1) the power and output voltage are constant; 2) the ranges of the input voltage are the same; and 3) the inductor current ripples are negligible compared to the average current.

1) Comparisons of Switch Devices: Table I presents the switching devices and their stresses in IPOSBHB. In the entire operating range of the converter, the maximum voltage and current of every switch device are shown in Table I marked with shadow. The peak voltage of all switch devices is

$$V_m = \max\left[V_{\rm in}, \frac{(V_o - V_{\rm in})}{(2D_{\rm HB})}\right] \tag{7}$$

and the peak current is

$$I_m = \max[I_o, nI_o]. \tag{8}$$

In the two-switch cascade converter, the maximum voltage and current of all switch devices under combinational control method are $V_m = V_{\rm in}$ and $I_m = I_{\rm in}$, respectively. In terms of the number of elements, IPOSBHB circuit includes more elements and is more complex than the two-switch cascade converter. In terms of voltage and current stress, as for IPOSBHB topology, when $V_m = V_{\rm in}$, considering the dead-zone and taking the upper limit of $D_{\rm HB}$ as 45%, $V_o \le 1.9V_{\rm in}$ is to be obtained. In this condition, the peak voltage of all elements of IPOSBHB is no higher than $V_{\rm in}$, which is on the same level with the two-switch cascade topology. When $I_m = nI_o$, in order to make the peak currents of all elements no higher than that of two-switch cascade topology, $nI_o \le I_{\rm in}$ is needed. Consider (6) and ignore the loss and also take the upper limit of $D_{\rm HB}$ as 45%, then $V_o \le 1.82\,{\rm V_{in}}$ is to be obtained. Set the step-up ratio of the converter as $N = V_o/V_{\rm in}$; the requirement that the peak currents of all elements are no higher than that of two-switch cascade topology is

$$N \le 1.82. \tag{9}$$

In conclusion, when the output and input voltage always meet the requirement of (9), the maximum voltage stress of switch devices in IPOSBHB is the same as two-switch cascade topology, while the maximum current stress will be equal or lower than two-switch cascade topology. For switching devices, low-stress means high reliability.

2) Comparisons of the Magnetic Elements: Magnetic elements make up a great proportion in size and weight of switch power supply (20–30%) [30]. The size and weight of magnetic elements increase with the area product A_p of magnetic core [31], and this parameter represents the power-handling capability of the magnetic core. As for the transformer, A_p is proportional to the apparent power P_t of the transformer, and $P_t = (1 + 1/\eta_T)P_{o(B)}$, where η_T is the efficiency of the transformer and $P_{o(T)}$ is the output power of the transformer. As for the inductor, A_p is proportional to the transferring energy W [31], and $W = 0.5LI_L^2$, where L is the inductance and I_L is the average current of the inductor.

For the IPOSBHB converter, the transferring power of the transformer is given by $P_{o(T)} = P_o(V_o - V_{\rm in})/V_o$. When the difference between input and output voltage is small, the size of the transformer is also small. The area product of the inductor is proportional to inductance L and the square of the inductor average current I_L. Due to the fact that the average current of L in IPOSBHB and of L_1 in noninverting boost–buck is always the same as the output current, when the inductance of L is the same as L_1, the inductor L and L_1 could be the same. However, the design of the area product of the inductor L_2 in noninverting boost–buck converter must be based on the input current in step-up mode since the input current is higher than the output current. For the same inductance L, the inductor L_2 will definitely have larger size and more weight than the inductor L_1. In the noninverting buck–boost converter, the inductor L is the same size as L_2 in the noninverting boost–buck converter.

It can be concluded that the overall volume of the magnetic elements in the noninverting buck–boost converter is smaller than that of the noninverting boost–buck converter. If the step-up ratio is not very high, the overall volume of magnetic elements in the IPOSBHB is smaller than the noninverting boost–buck converter, while the overall volume of magnetic elements in the IPOSBHB and in the noninverting buck–boost needs to be calculated according to specifications.

3) Comparisons of Efficiency: Power loss analysis of converters is of great importance in enhancing system efficiency and power density, as well as in choosing elements and designing the radiator. In high-power applications, the two-switch

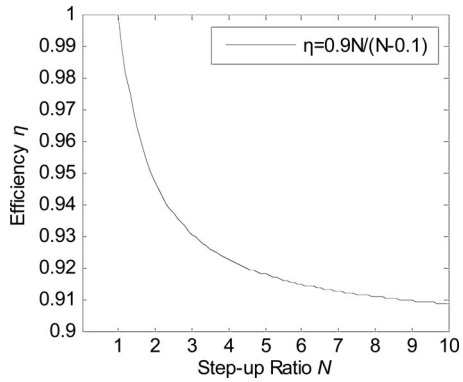

Fig. 5. Relationship of efficiency η and step-up ratio N.

cascade topology has approximately the same efficiency as buck and boost topologies at rated power, and the efficiency can be as high as 96% or more. Although introducing a transformer, IPOSBHB is essentially a nonisolated topology since the buck and the half-bridge connect in parallel. Thus, its efficiency should be between isolated converter and cascade converter.

It is known from Fig. 3 that IPOSBHB is basically the same as buck in step-down mode, though it has more output diodes than buck circuit. It can reasonably achieve the same efficiency as buck, which is 96%. When $v_{in} = v_o$, the converter works in the critical state, which would be called as equal mode. In this mode, S_3 is ON and S_1 and S_2 are OFF. There are no any switching actions of the converter in the time; thus, the main power loss only exists in conduction loss of S_3, and D_1–D_4. The overall efficiency η of IPOSBHB could be calculated by

$$\eta = 1 - \frac{V_{\mathrm{CE3}} I_o + 4V_{D1} I_o/2}{V_o I_o} = 1 - \frac{V_{\mathrm{CE3}} + 2V_{D1}}{V_o}. \quad (10)$$

If the output voltage level is high (up to several hundreds volts), and the conduction voltage drops of the switches and diodes are close to zero (about 1–2 V), η will be close to 100%. When working in step-up mode, S_3 is ON, and the efficiency of buck is still assumed to be 100%. If the efficiency of the half-bridge module is assumed to be η_{HB}, then η is given as

$$\eta = \frac{N}{1 + (N - 1/\eta_{\mathrm{HB}})} = \frac{N\eta_{\mathrm{HB}}}{\eta_{\mathrm{HB}} + N - 1}. \quad (11)$$

Set $\eta_{\mathrm{HB}} = 90\%$; the relationship of η and N could be shown as in Fig. 5. η decreases as N increases. When $N = 10$, η is already below 91%. Nevertheless, even if the step-up ratio continues to increase, the efficiency will not be less than 90%. If η is no lower than 96%, then the step-up ratio N should meet

$$N \leq 1.6. \quad (12)$$

In addition, it can be expected, by comparing the loss of three modes, that the efficiency of the converter will reach the highest point in equal mode.

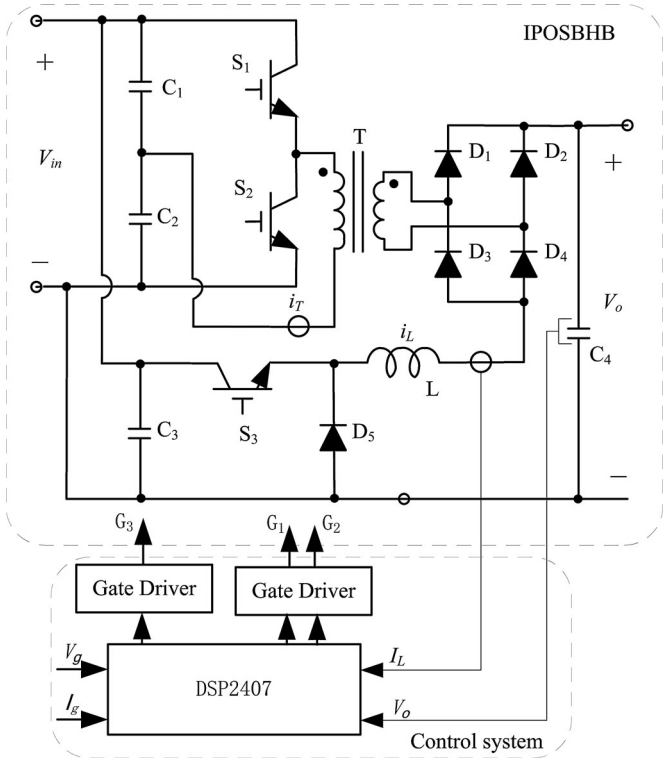

Fig. 6. Overall control scheme of IPOSBHB.

III. Control System Design

A. Small-Signal Model

Based on state-space average method, small-signal models of IPOSBHB in step-down and step-up modes are derived as (13) and (14), respectively:

$$\hat{v}_o(s) = \frac{V_{\mathrm{in}}}{LC_4 s^2 + (L/R)s + 1}\hat{d}_{\mathrm{Buck}}(s) + \frac{D_{\mathrm{Buck}}}{LC_4 s^2 + (L/R)s + 1}\hat{v}_{\mathrm{in}}(s) \quad (13)$$

$$\hat{v}_o(s) = \frac{V_{\mathrm{in}} N_S}{N_P(LC_4 s^2 + (L/R)s + 1)}\hat{d}_{\mathrm{HB}}(s) + \frac{N_P + N_S D_{\mathrm{HB}}}{N_P(LC_4 s^2 + (L/R)s + 1)}\hat{v}_{\mathrm{in}}(s). \quad (14)$$

It can be seen that the output voltage is linear to the duty cycle in both step-down and step-up modes, except that there is an additional coefficient n in step-up mode.

B. Overall Scheme

The overall digital control scheme of IPOSBHB is shown in Fig. 6, taking DSP2407 as the core. The voltage of C_4 and the current of L measured by Hall sensor are chosen as feedback signal, and they are sent to DSP2407. After analog-to-digital conversion, the signal will be in comparison with the desired voltage or current to get the error signal e_u or e_i. The smaller one of the two will be chosen as the input error signal e ($e = \min[e_u, e_i]$). Through compensation algorithm, the modulation

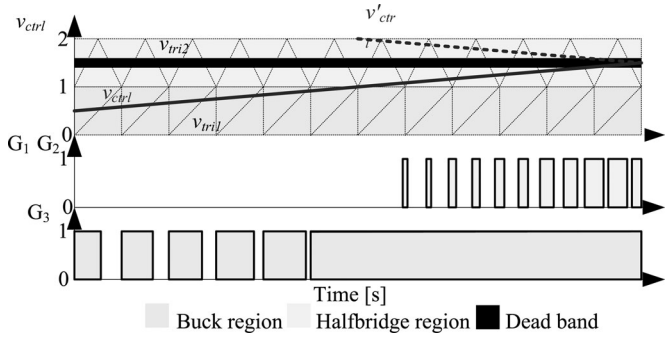

Fig. 7. PWM modulation approach.

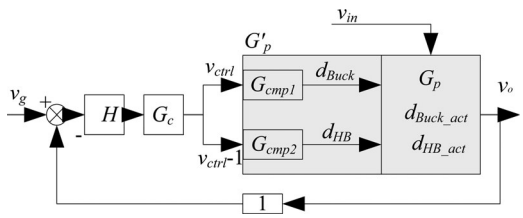

Fig. 8. Block diagram for inconformity compensation of transfer functions.

error signal $v_{\rm ctrl}$ will be obtained. Then, the duty cycle $d_{\rm ctrl}$ is obtained by comparing $v_{\rm ctrl}$ and the carrier wave signal generated by timer. After amplified by the drive circuit, the drive signals of the switches are finally obtained.

PWM modulation waveforms of the three switches are shown in Fig. 7. The two carrier waves for buck and half-bridge are $v_{\rm tri1}$ and $v_{\rm tri2}$, respectively, which have the same frequency and the same amplitude of "1." Drive signal G_1–G_3 equals to "1" means that the switch is ON, while "0" represents that the switch is OFF. $v_{\rm tri1}$ is an asymmetrical triangle carrier wave. When $v_{\rm ctrl}$ is higher than $v_{\rm tri1}$, the output of G_3 is equal to "1;" $v_{\rm tri2}$ is a symmetrical triangle carrier wave, the drive signal G_1 is directly obtained by comparing $v_{\rm ctrl}$ and $v_{\rm tri2}$. When $v_{\rm ctrl}$ is higher than $v_{\rm tri2}$, the output of G_1 is equal to "1." The auxiliary signal $v'_{\rm ctrl}$ is obtained by $(1 - v_{\rm tri2})$, and then comparing $v'_{\rm ctrl}$ and $v_{\rm tri2}$; when $v'_{\rm ctrl}$ is lower than $v_{\rm tri2}$, the output of G_2 is equal to "1." This modulation approach can realize 180° phase difference signal for bridge drive without additional phase splitter circuit and can also be easily carried out by programming. Furthermore, it is necessary to limit the amplitude of $v_{\rm ctrl}$ in half-bridge region so that the duty cycle of G_1 and G_2 can be limited under 50% and S_1 and S_2 would not conduct at the same time.

In order to ensure the converter works at efficient mode, use of a carrier wave parallel-shifting method is suggested, which is to parallel shift $v_{\rm tri2}$ from [0, 1] to [1, 2]. When $V_o \le V_{\rm in}$, $v_{\rm ctrl} \in [1, 2]$ only intersects with $v_{\rm tri1}$ and is always lower than $v_{\rm tri2}$. In this case, only G_3 has PWM output signal. When $V_o > V_{\rm in}$, $v_{\rm ctrl} \in [1, 2]$ only intersects with $v_{\rm tri2}$ and is always higher than $v_{\rm tri1}$. In this case, the output of G_3 is "1," and both G_1 and G_2 have PWM output signal.

It should be noted that this paper focuses on the transition between step-up and step-down modes under the constant voltage mode, and the current loop is just used as to limit the maximum output current. Only when the output current is close to the set current, the current loop will work.

C. Compensation for Inconformity of Transfer Functions

Noninverting buck–boost converter's large signal dc gain is nonlinear in boost mode, which makes the transition worse at mode change [28]. A compensation method for nonlinearity is introduced in [28], but it is complex to some degree. For IPOSBHB, it is known from (5), (6), (13), and (14) that in both step-down and step-up modes, output voltage in large and small signal dc gains have linear relation with duty cycle, so compensation is not needed and consequently the control difficulty can be reduced. Nevertheless, there is an additional coefficient n in step-up mode compared to step-down mode, so if $n \neq 1$, it must lead to an inflection point in dc gain curve. On the one hand, the inflection point would make the transition worse. On the other hand, the inconformity of transfer functions makes it difficult to achieve ideal control effect by using only one control algorithm G_c. Therefore, it has to strike a balance between step-down and step-up modes in designing G_c. From the aforementioned analysis, it can be concluded that if the transfer functions of the two modes can be identical by compensation, the difference between step-down and step-up modes is negligible. Then, according to the compensated transfer functions, it is easy to design and optimize the controller to achieve ideal control effect.

Based on the idea of making the transfer functions identical, a compensation scheme is designed as shown in Fig. 8. H is the sampling coefficient and $G_{\rm cmp1}$ and $G_{\rm cmp2}$ are the inconformity compensation factor. Regarding the transfer function of step-down mode as a standard, set $G_{\rm cmp1} = 1$ and $G_{\rm cmp2} = 1/n$, then a new control object G'_p is obtained. Due to the amplitude of the carrier wave is "1," the transfer function of the modulation-wave error signal to the duty cycle is negligible. Moreover, instead of parallel shifting the carrier wave $v_{\rm tri2}$ upward, as shown in Fig. 7, the modulation-wave error signal $v_{\rm ctrl}$ in step-up mode is parallel shifted downward in the scheme, which is easier realized by programming. The two approaches are essentially identical on control effect. $d_{\rm Buck\_act}$ and $d_{\rm HB\_act}$ in the scheme represent the actual duty cycle considering the switching time delay. A discussion of the compensation approach dealing with it follows.

D. Compensation for Discontinuity at Mode Change

Due to the switching time delay caused by switches and gating circuits, the actual duty cycle will become 0 when the theoretical duty cycle is approaching 0, and the actual duty cycle will become 1 in advance of the theoretical duty cycle, as shown in (15)

$$d_{\rm act} = \begin{cases} 0, & 0 \le d_{\rm ctrl} < D_{Z1} \\ \dfrac{1}{1-D_{Z1}-D_{Z2}}(d_{\rm ctrl}-D_{Z1}), & D_{Z1} \le d_{\rm ctrl} \le 1-D_{Z2} \\ 1, & 1-D_{Z2} < d_{\rm ctrl} \end{cases} \tag{15}$$

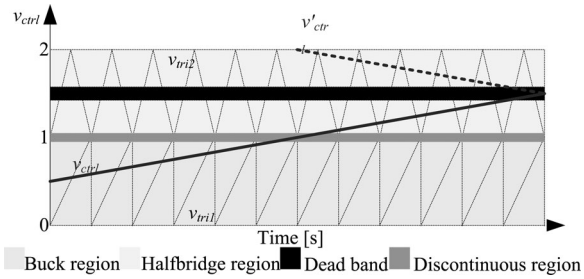

Fig. 9. Discontinuous region caused by switching time delay.

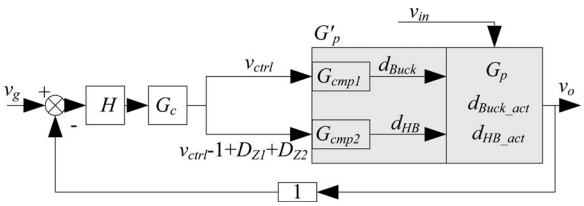

Fig. 10. Block diagram for the discontinuity compensation at mode change.

where D_{Z1} and D_{Z2} stand for the duty cycles of turning ON and OFF delay, respectively, and $d_{\rm ctrl}$ and $d_{\rm act}$ are the theoretical and actual values of duty cycle, respectively [28].

For IPOSBHB converter, when the input voltage is near to the output voltage, $D_{\rm Buck}$ approaches 1 and $D_{\rm HB}$ approaches 0, so there must be a discontinuous region during mode change as shown in Fig. 9. Since the amplitudes of $v_{\rm tri1}$ and $v_{\rm tri2}$ are "1," IPOSBHB will enter the discontinuous region when $v_{\rm ctrl}$ is in the range from $(1 - D_{Z2})$ to $(1 + D_{Z1})$. The transients of output voltage can be worsened at mode change because of the presence of the discontinuous region. This is mainly reflected in: 1) It is difficult to suppress the disturbance of input voltage to output voltage in the discontinuous region because the duty cycle of buck is 100% while half-bridge is 0, which leads the output voltage following the change of the input voltage; and 2) the increasing of $v_{\rm ctrl}$ in the discontinuous region cannot bring the increasing of $d_{\rm act}$, which must lead to a platform at mode change; therefore, the response speed is reduced. So if D_{Z1} and D_{Z2} are not small enough, it is necessary to compensate for the discontinuous region.

As shown in Fig. 9, if the carrier wave for half-bridge is to be parallel shifted downward, the area of the discontinuous region will be decreased. When the shift distance $d_{\rm shift}$ reaches $(D_{Z1} + D_{Z2})$, the discontinuous region will be just eliminated. If $d_{\rm shift}$ is to be further increased, switches S_1, S_2, and S_3 will engage switching action simultaneously, which would lead to more switching loss. This should be avoided. The block diagram for the discontinuity compensation at mode change is shown in Fig. 10.

E. Feed-Forward Compensation for the Disturbance of Input Voltage

As mentioned earlier, the input voltage disturbance $\hat{v}_{\rm in}$ exists in transfer functions of IPOSBHB in both step-down and step-up modes, and it will have negative effect on output voltage.

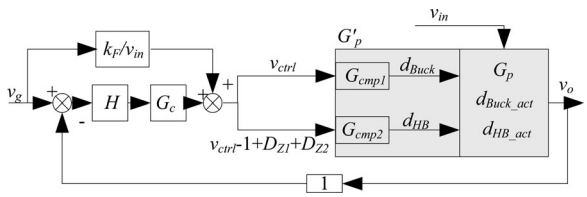

Fig. 11. Block diagram of the feed-forward compensation for the input voltage disturbance.

When renewable energy sources such as fuel cells and PV cells are taken as the power supply, the input voltage will vary widely with changing factors such as load and temperature, so it is necessary to restrain the disturbance to enhance the voltage regulation factor of the converter. Feed-forward control provides an effective means of restraining the disturbance. It is an open-loop control strategy, which is different from feedback control based on errors, and it can be compensated precisely at the very time that the disturbance occurs, without waiting for the error signal to be produced. Thus, feed-forward control could reduce or even eliminate the effects of the disturbance and enhance the anti-interference ability and dynamic performance of the system.

The feed-forward control scheme can be achieved by introducing a feed-forward factor $k_F/\hat{v}_{\rm in}$, where k_F is the gain factor. The proportion of feed-forward in the overall duty cycle is inversely related to the input voltage. When input voltage increases suddenly, this proportion would decrease rapidly, as a result the overall duty cycle would decrease to prevent the output voltage increasing and vice versa. This control scheme enhances the anti-inference ability of the system to the variance of $\hat{v}_{\rm in}$. Because of the existence of the transformer, the difference between the dc gains in step-down and step-up modes makes it difficult to introduce feed-forward compensation for the whole system. After adopting the compensation method for the inconformity of the transfer functions as introduced Section III-C, this difference has been eliminated, which makes it possible to design the feed-forward compensation algorithm for the whole system just according to the buck model. Fig. 11 shows the block diagram of the feed-forward compensation for the input voltage disturbance.

After introducing the three compensation methods, the final criterion of step-up and step-down modes change could be expressed as

$$\begin{cases} 0 < v_{\rm ctrl} \le 1 - D_{Z2}, & v_{\rm in} \le v_o \\ v_{\rm ctrl} > 1 - D_{Z2}, & v_{\rm in} > v_o. \end{cases} \tag{16}$$

IV. Verification Through Experiments

A 15-kW prototype of IPOSBHB is developed, which is used for the power system of a solar airship. The input of the converter is solar cells. The rated power of solar cells is about 15 kW, and its output voltage range is 0–450 V. The output of the converter is lithium batteries and motors. The former are used to store excess energy for nighttime use, and the latter are used for flight attitude control of the airship. The total power of the motors is

TABLE II
PROTOTYPE SPECIFICATIONS

Input voltage	220V～450V
Output voltage	270V～350V
Power	15kW
S_1- S_3, D_5	FF200R12KS4
D_1-D_4	DSEP2-101-04A
Inductor	L=600uH
Transformer	Np:Ns=0.67
C_1-C_3(Capacitance/Withstand voltage)	2*40u/1250V
C_4(Capacitance/Withstand voltage)	4*40u/1250V

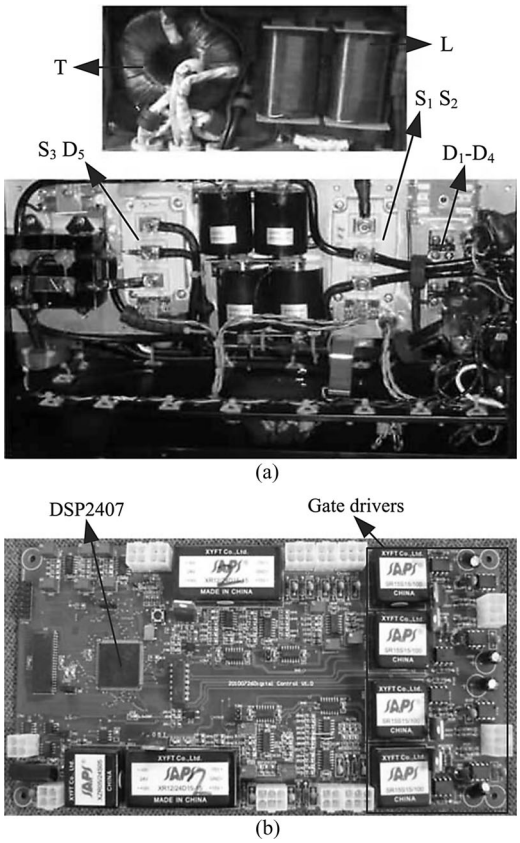

Fig. 12. 15-kW prototype. (a) Converter. (b) Control system.

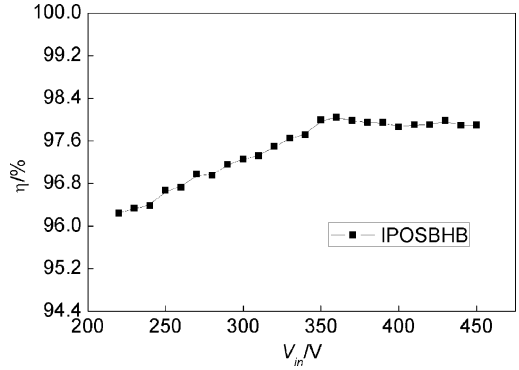

Fig. 13. Efficiency curves.

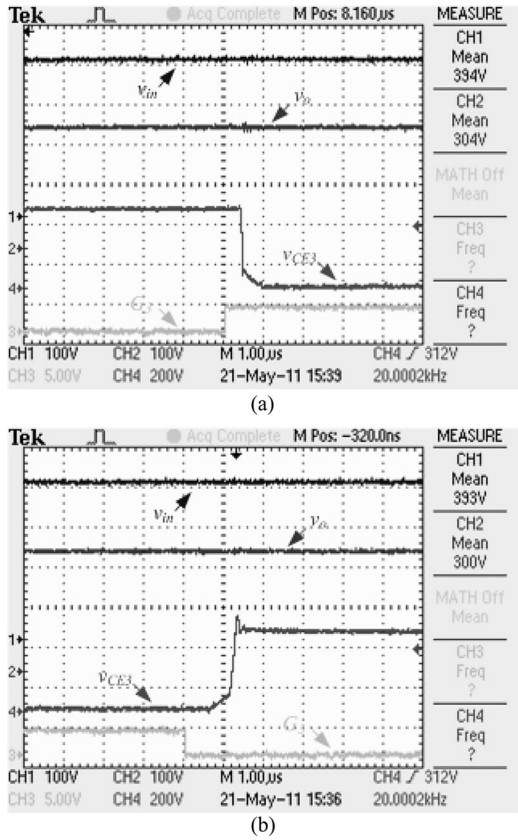

Fig. 14. Waveforms of switching delay. (a)Turn-ON delay. (b) Turn-OFF delay.

16 kW, and their input voltage range is 270–350 V. The details of the specifications are presented in Table II. Fig. 12 shows a photograph of the prototype. DSP2407 is chosen as the control chip and the control system can provide four drive outputs. PI controller is adopted as the compensation network G_c.

It can be determined from the range of input voltage and output voltage that the maximum step-up ratio is $N = 350/220 \approx 1.59 < 1.6$, which meets the requirements of (9) and (12); consequently, the converter would have low current stress and high efficiency. It is known from theoretical calculation that the maximum current stress at rated power of IPOSBHB is the current that goes through S_1 and S_2, which has been average value of about 64 A, which is lower than the input current 68.2 A of two-switch cascade converter of the same power level. The efficiency curve of the converter under rated power is presented in Fig. 13 when $V_o = 350$ V. It can be seen that the efficiency of IPOSBHB working in the range of its input voltage is no lower than 96%, and the efficiency is higher when it works at step-down mode rather than at step-up mode. The highest efficiency appears when input voltage is close to output voltage, and also the lowest efficiency appears at the lowest point of input

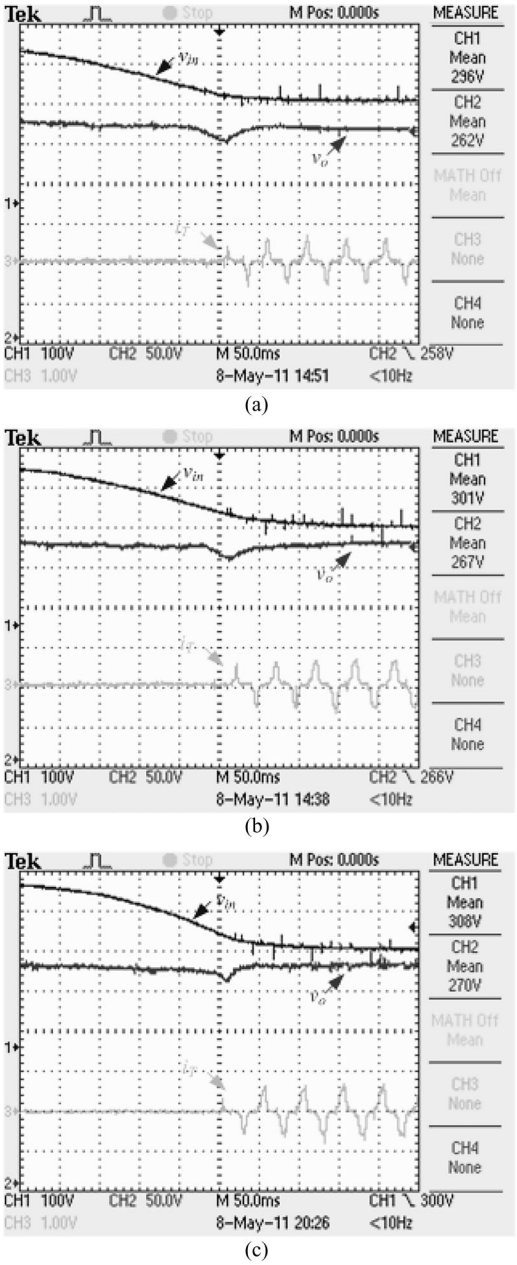

Fig. 15. Transient response of output voltage after introducing inconformity compensation. (a) $G_{\mathrm{cmp2}} = 0.4$. (b) $G_{\mathrm{cmp2}} = 0.7$. (c) $G_{\mathrm{cmp2}} = 1.5$.

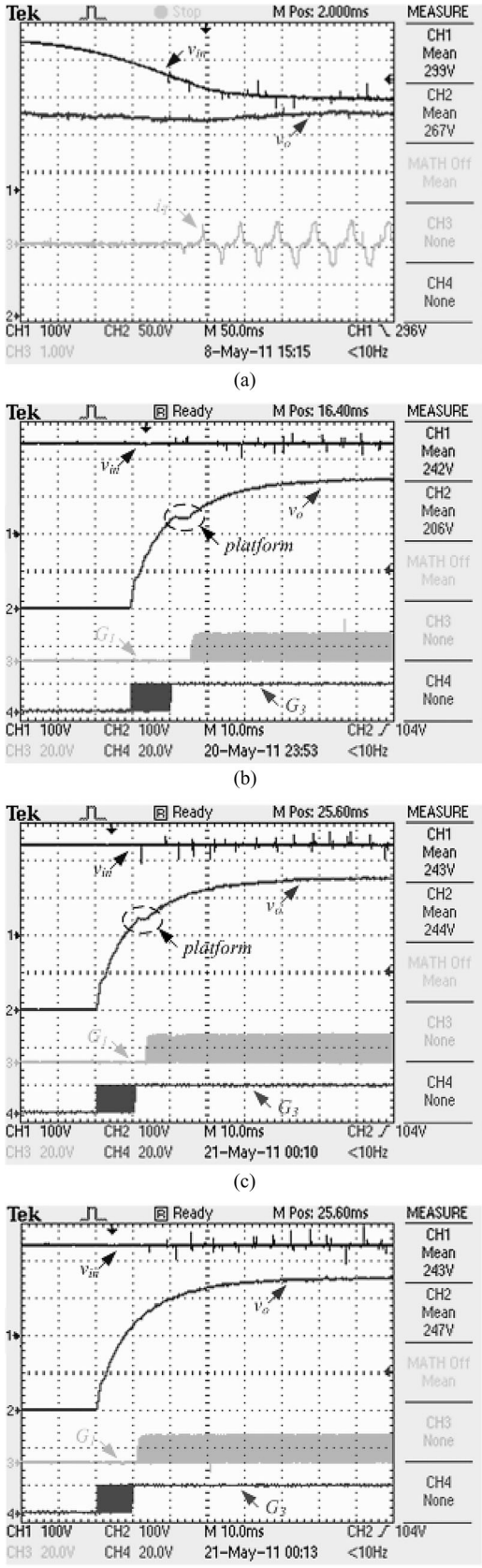

Fig. 16. Transient response of output voltage after introducing discontinuity compensation. (a) Input voltage decreased and $d_{\mathrm{shift}} = 0.036$. (b) Step response and $d_{\mathrm{shift}} = 0$. (c) Step response and $d_{\mathrm{shift}} = 0.018$. (d) Step response and $d_{\mathrm{shift}} = 0.036$.

voltage. The results are consistent with the preceding analysis in Section II-D.

Fig. 14 shows the turning ON and OFF time delay of S_3. The switching frequency is 20 kHz, the turning ON time delay is about 0.4 μs, the turning OFF time delay is about 1.3 μs, and the corresponding $D_{Z1} = 0.008$, $D_{Z2} = 0.026$.

Fig. 15 shows the transient response of output voltage when the input voltage decreases from 400 to 240 V suddenly; the desired output voltage is set to 270 V and the resistive load is set to 40 Ω. As the input voltage drops, the converter will automatically shift from step-down mode to step-up mode at the point of $v_{\mathrm{in}} = v_o$. The sampling current of the transformer's primary side i_T is chosen to represent the working state of half-bridge

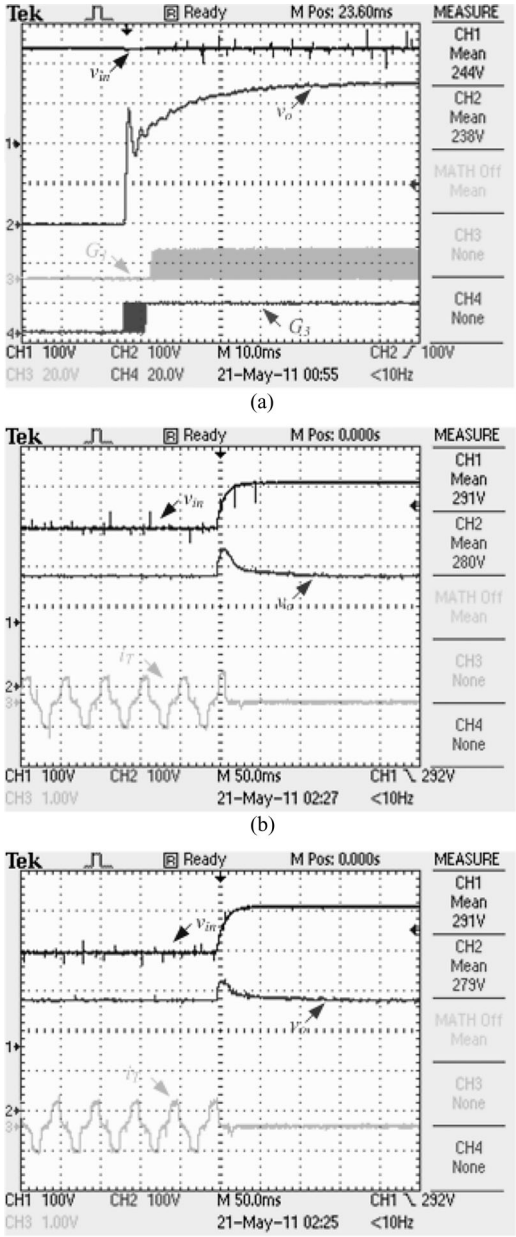

Fig. 17. Comparison of feed-forward effect. (a) Step response and $k_F = 0.4$. (b) Response when input voltage increases suddenly and $k_F = 0$. (c) Response when input voltage increases suddenly and $k_F = 0.4$.

circuit in the figures (the waveform in channel 3 is an envelope of the sampling current). The inconformity compensation factor $G_{\rm cmp2}$ in Fig. 15(a)–(c) are set to 0.4, 0.7, and 1.5, respectively, among which $G_{\rm cmp2} = 0.7$ is the closest one to the theoretical value $G_{\rm cmp2} = 1/n = 0.67$. It can be seen from Fig. 15(b) that the transient of v_o is a little lower than v_g in both step-down and step-up modes due to the decrease of $v_{\rm in}$, but there is little difference in the voltage regulation between the two modes, which verifies that the transfer functions in step-down and step-up modes are almost same. It can be also seen from Fig. 15(a) and (c) that when $G_{\rm cmp2} = 0.4$, the voltage regulation in step-up mode is a little lower than that in step-down mode; and when $G_{\rm cmp2} = 1.5$, the situation is just the opposite. The results are in accordance with the analysis in Section III-C.

In addition, there is an apparent drop zone of v_o at mode change, and the width and the amplitude of the region will decrease as the compensation factor increases. Actually, the drop zone is caused by $v_{\rm ctrl}$ coming into the discontinuity region. When $1 - D_{Z1} \le v_{\rm ctrl} \le 1 + D_{Z2}$, S_3 is ON while S_1 and S_2 are OFF, and v_o will decrease as $v_{\rm in}$ decreases. Larger $G_{\rm cmp2}$ will accelerate the increasing speed of $v_{\rm ctrl}$ in step-up mode and thus shortens the time needed from 1 to $1 + D_{Z2}$, which is beneficial to decreasing the width and the amplitude of the drop zone during transition, but it is adverse to keeping the transfer functions identical and it cannot achieve the same voltage regulation, so it is not an optimal solution.

Fig. 16(a) shows the waveform of compensation for the discontinuity when using the method discussed in Section III-D. When $d_{\rm shift} = 0.036$, the decrease region is almost eliminated. Comparisons of the step response of v_o with different values of $d_{\rm shift}$ are shown in Fig. 16(b)–(d), and the drive signals G_1 and G_3 are used to represent the working state of half-bridge and buck modules. Still choosing $G_{\rm cmp2} = 0.7$, and $v_{\rm in} = 245\,{\rm V}$, $R = 40\ \Omega$, from the step response of v_o changing from 0 to 280 V, it can be concluded that the platform at mode change will decrease as $d_{\rm shift}$ increases, and when $d_{\rm shift} = 0.036$, the platform is almost eliminated and the response time is apparently reduced.

Fig. 17(a) shows the step response of output voltage after introducing feed-forward control, from which it can be seen that the rising speed at the start-up phase has been significantly improved compared with that in Fig. 16(d). Fig. 17(b) and (c) shows the comparison of the transition when $v_{\rm in}$ changes from 240 to 350 V suddenly without and with the feed-forward control, respectively. When $v_{\rm in}$ increases suddenly, the peak response of v_o decreases about 20 V after introducing the feed-forward control scheme, which verifies that the feed-forward control scheme can restrain the disturbance of $v_{\rm in}$.

V. Conclusion

A novel IPOSBHB converter has been proposed to fit the demand of high power applications. The circuit achieves complete decoupling from the input so that the mutual effects between modules are eliminated and thus oscillations are avoided. The converter can achieve satisfactory comprehensive performance when the step-up ratio is low and smooth transition is achieved since the circuit has no nonlinear dc gain. The inconformity of the transfer functions, the discontinuity caused by the switching time delay, and the disturbance of the input voltage have been analyzed, and the methods for compensation have been proposed. The experimental results via a 15-kW prototype show that when the step-up ratio is low, the maximum stresses of switching devices is lower, and the efficiency at the rated working point can achieve 96% or higher. The combinational control strategy and the compensation methods proposed in this paper are easy to carry out in order to achieve effective control at steady state and smooth transition at the mode change, and also reduce the adverse effect caused by the disturbance of the input voltage.

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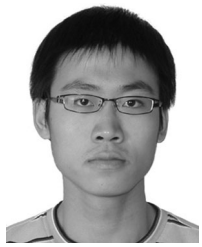


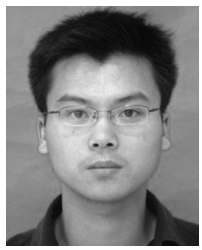
Qing Du received the B.S. degree in mechanical engineering from Beihang University, Beijing, China, in 2005, where he is currently working toward the Ph.D. degree.

Since September 2005, he has been involved in the study of high-power converters, especially dc–dc converters. His current research interests include high-power dc–dc converters and control methods for fuel-cell vehicles and photovoltaic power generation and battery charger.

Bojin Qi received the B.S. and Ph.D. degrees from the Department of Materials Processing, Tsinghua University, Beijing, China, in 1990.

He is currently a Professor and Director of the Department of Materials Processing, Beihang University, Beijing. He has long been involved in welding automation technology, advanced power conversion theory and application, and industrial process control theory and applications. His current research interests include advanced welding technology and equipments, high-power dc–dc converters, battery charger, battery management system, and some special power supply.

Dr. Qi is a member of the Chinese Mechanical Engineering Society.

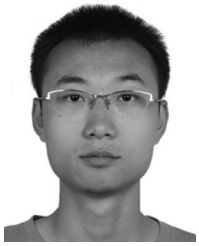


Tao Wang received the B.S. degree in mechanical engineering from Beihang University, Beijing, China, in 2009, where he is currently working toward the Master's degree.

Since September 2009, he has been with the DC–DC Research Group of the Mechanical Engineering and Automation Department, Beihang University. His current research interests include soft switching and digital control of high-power dc–dc converter.

Tao Zhang is currently working toward the Master's degree in mechanical engineering at Beihang University, Beijing, China.

Since 2009, he has been involved in the study of high-power converters, especially dc/dc converters. His current research interests include the inverter magnetic bias mechanism and the methods to inhibit the magnetic bias.



Xiao Li received the B.S. degree in mechanical engineering from Beihang University, Beijing, China, in 2011. He is currently working toward the Master's degree at Carnegie Mellon University, Pittsburgh, PA.

From February 2011 to July 2011, he was with the DC–DC Research Group of the Mechanical Engineering and Automation Department, Beihang University, where he finished his academic dissertation. His current research interests include robust control and adaptive control theories applied in robotics.