A Low-Power AC–DC Single-Stage Converter With Reduced DC Bus Voltage Variation

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Abstract—A new low-power single-stage ac–dc converter is proposed in the paper. The outstanding feature of the converter is that it can operate with a sinusoidal input current and a low primary-side dc bus voltage that is much less variable than that found in other single-stage converters. The operation of the converter is discussed in the paper and its various modes of operation are explained in detail. An analysis of the converter's steady-state characteristics is performed and the results are used in the design of the converter. Experimental results obtained from a prototype converter are also presented.

Index Terms—AC–DC converter, dc bus voltage, low-power converter, single-stage converter.

I. INTRODUCTION

SINGLE-stage ac–dc converters simultaneously perform both input power factor correction and dc–dc power conversion with just a single converter [1]–[9]. They can be synthesized by combining an ac–dc front-end converter (typically a boost converter) with a dc–dc converter (typically a flyback or a forward converter), then removing all redundant elements. A single-stage converter usually has only one controller, which is used to regulate the output voltage. This means that the intermediate dc bus voltage—the dc voltage at the transformer primary side that needs to be stepped down—is therefore dependent on the input line and output load conditions and can thus vary considerably.

When a single-stage converter is synthesized from an ac–dc boost converter, as is the case with most single-stage converters, the intermediate dc bus voltage has the potential to become very high as it does not have a separate and independent front-end converter to regulate it. This is especially true when the converter is operating under light-load conditions as the intermediate dc bus capacitor used to smooth out the voltage has less opportunity to discharge. Power electronics researchers have proposed many techniques to try to keep the bus voltage to a maximum level of less than 450 V to avoid large switch voltage stresses and capacitor size. These techniques can be classified as follows.

1) Variable switching frequency techniques [10]–[12] that limit the amount of input power that is transferred to the dc bus capacitor by increasing the switching frequency at decreasing load and vice versa.

2) Bulk capacitor voltage feedback techniques [13], [14] that use one or more auxiliary windings from the main power transformer to produce a counter voltage that limits the amount of voltage that is placed across the input inductor. Doing so reduces the charging current in the input inductor when the load is decreasing.

3) Load current feedback techniques [15] that adjust the input current by using information that is sensed at the load.

4) Direct power transfer techniques [16]–[21] that allow some of the power from the converter's input section to be transferred directly to the output instead of the dc bus capacitor to reduce the amount of charge placed in this capacitor.

None of these techniques, however, significantly limits the variation in the dc bus voltage that can occur when the converter needs to operate under universal input line conditions. This can affect the design of the main power transformer as it must be designed to operate for all potential operating conditions. It can also affect the design of the converter with respect to hold-up time if this needs to be considered. A widely varying dc bus voltage means that the converter must have appropriate hold-up time when the dc bus voltage is low or high, which, in turn, means that the dc bus capacitors must be selected for several bus voltages instead of just one.

A new ac–dc single-stage converter is proposed in the paper. The outstanding feature of this converter is that its dc bus voltage is far less dependent on its operating conditions than is the case for most previously proposed single-stage converters. The significant reduction in dc bus voltage variation allows for a reduction in dc bus capacitor size as the need to satisfy hold-up time requirements for both low and high dc bus voltage is done away with. In the paper, the operation of the converter is discussed and its modes of operation are explained and analyzed. The analysis is used to develop a design procedure for the converter that is demonstrated with an example. The feasibility of the converter is confirmed with results obtained from an experimental prototype.

II. CONVERTER OPERATION

The proposed single-stage converter is shown in Fig. 1. It consists of a diode bridge rectifier, transformers T_1 and T_2, switch S, dc bus capacitor C, output capacitor C_o, and diodes D_1 to D_4. T_1 and T_2 have turns ratio of n_1 and n_2, respectively, and each contain a magnetizing inductance L_{m1} and L_{m2}. Each magnetizing inductance can be considered to be parallel to ideal transformer; the leakage inductances of T_1 and T_2 are negligible.
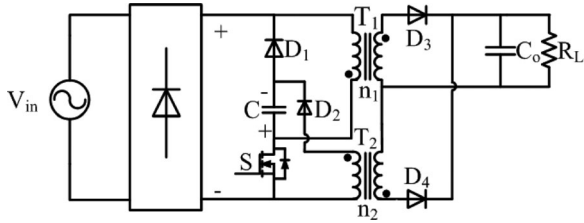
Fig. 1. Proposed converter.

The input current is discontinuous and is bounded by a sinusoidal envelope so that it is essentially a sinusoidal waveform with HF harmonic components. The magnetizing current of each transformer can be either discontinuous or continuous. For the purpose of simplicity, it will be assumed that these currents are discontinuous so that both transformers are fully demagnetized after the switch is turned OFF. Moreover, making the magnetizing current of T_2 discontinuous will make V_C less susceptible to load variation. The proposed converter has two distinct modes of operation, depending on the dc bus voltage V_C. In one mode, transformer T_1 acts like an inductor while T_2 acts like a flyback transformer; in the other mode, both transformers act like flyback transformers. Both modes are described in this section.

A. Mode 1: Single Flyback Transformer Mode of Operation

The converter is in this mode of operation when the dc bus capacitor voltage is less than $n_1 V_o$. This means that diode D_3 never conducts and T_1 becomes like an input inductor as no energy is transferred to the output. T_2 is the only transformer in the converter that actually operates as a flyback transformer.

The converter goes through the following intervals when operating in the single flyback transformer mode of operation, with typical converter waveforms and equivalent circuit diagrams shown in Figs. 2 and 3, respectively:

Interval 1 [t_0–t_1][see (Fig. 3(a)]: Switch S is turned ON at t_0. The rectified input line voltage $|V_{in}|$ is applied to the magnetizing inductance of T_1, L_{m1}. Current in L_{m1}, i_{Lm1}, begins to flow and increases linearly. Also during this interval, dc bus voltage V_C is applied across the magnetizing inductance of T_2, L_{m2}, causing its current i_{Lm2} to increase linearly through D_2. During this interval, there is no power transfer to the load, which is being supplied by C_o.

Interval 2 [t_1–t_2][see Fig. 3(b)]: Switch S is turned OFF at t_1. All the energy that was placed in T_1 during interval 1 is transferred to bus capacitor C during this interval. Also during this time, all the energy that was placed in T_2 during interval 1 is transferred to the output through D_4. At some instant $t = t_2$, both T_1 and T_2 have been fully demagnetized and remain so until the start of the next switching cycle.

B. Mode 2: Dual Flyback Transformer Mode of Operation

The converter is in this mode of operation when the dc bus capacitor voltage is $V_C = n_1 V_o$. Ideally, V_C can never exceed $n_1 V_o$ because diode D_3 conducts if it tries to do so, allowing energy that would otherwise charge C to be transferred to the output.
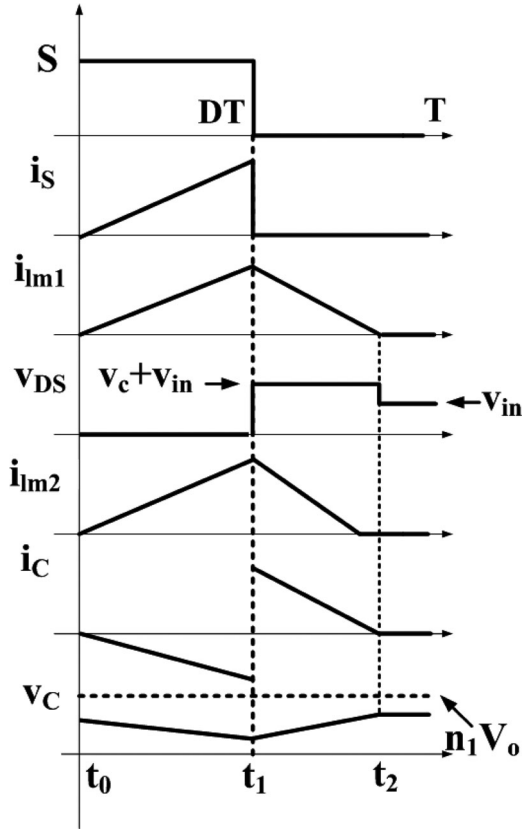

Fig. 2. Typical waveforms describing single flyback transformer mode when $V_C > n_1 V_o$.
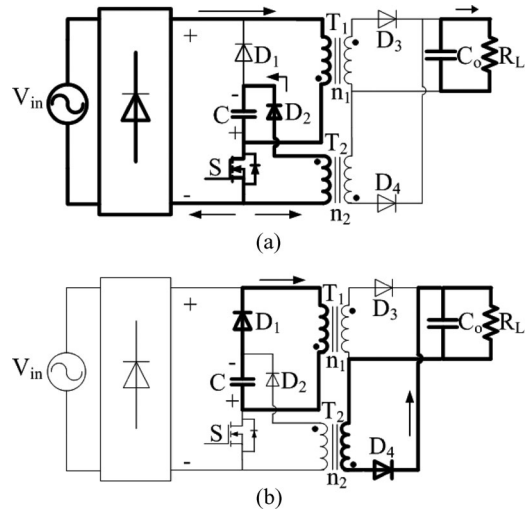

Fig. 3. Equivalent circuits.

During this mode, both T_1 and T_2 act like flyback transformers that demagnetize through their secondaries when switch S is OFF. It should be mentioned that a part of stored energy in the magnetizing inductance of T_1 goes to the dc bus capacitor after S has been turned OFF to make up for the drop in V_C that would otherwise occur due to the transfer of energy from C to T_2.
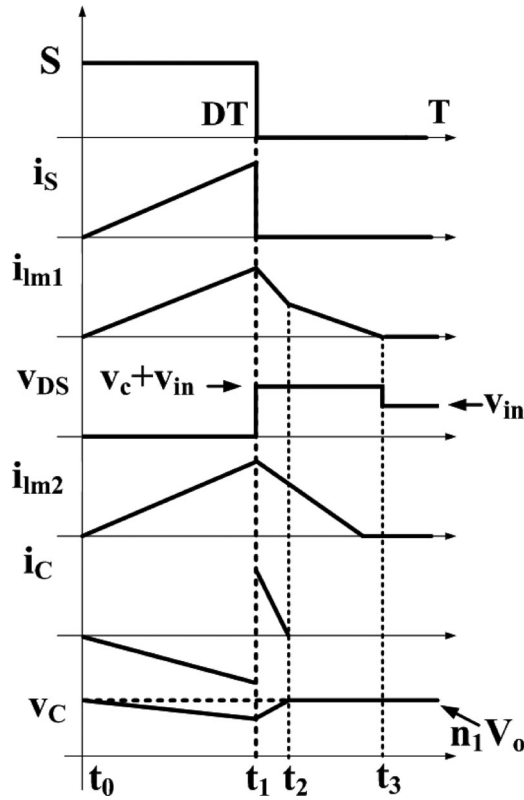
Fig. 4.   Typical waveforms when $n_1 V_o = V_C$.

Fig. 5.   Equivalent circuits.

The converter goes through the following intervals when operating in the dual flyback transformer mode of operation, with typical converter waveforms and equivalent circuit diagrams shown in Figs. 4 and 5, respectively.

Interval 1 [$t_0 - t_1$][see Fig. 5(a)]: The converter operates in the same way as it does for Mode 1, Interval 1.

Interval 2 [$t_1 - t_2$][see Fig. 5(b)]: Switch S turns OFF at t_1. The converter operates in the same way as it does for mode 1 interval 2 as energy stored in T_1 is transferred to C to make up for the drop in V_C after the previous interval. The dc bus voltage reaches $n_1 V_o$ at $t = t_2$. T_2 has not been fully demagnetized at this time.

Interval 3 [$t_2 - t_3$][see Fig. 5(c)]: At $t = t_2$, V_C is equal to $n_1 V_o$ and D_3 begins to conduct as it becomes forward biased. This releases the remaining energy stored in T_1 to the output. Also during this time interval, all the energy that was placed in T_2 during interval 1 is transferred to the output through D_4. At some instant $t = t_3$, both T_1 and T_2 have been fully demagnetized and remain so until the start of the next switching cycle.

In addition to the modes of operation, the following should also be mentioned about the operation of the proposed converter.

1) Regardless of the mode of operation, the maximum voltage that is placed across S is placed while T_2 is demagnetizing and is

$$V_{s,\max} = V_C + V_{\text{in}}. \qquad (1)$$

The voltage across S becomes V_{in} after T_1 has been demagnetized.
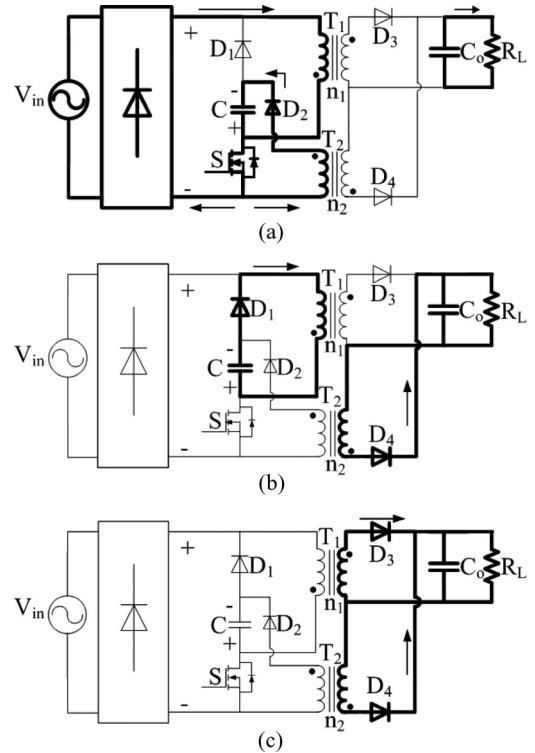
2) In practice, when V_C reaches $n_1 V_o$, the converter is most likely to be in Mode 2 when the rectified input voltage $|V_{\text{in}}|$ is close its peak value as the energy stored in T_1 is more than that transferred to T_2. During the zero crossing of the line cycle, the converter is most likely in Mode 1 since the absorbed energy by L_{m1} in this area is less than.

3) There are two mechanisms that help make the dc bus voltage in the proposed converter less variable than that of previously proposed single-stage ac–dc converters. One is the substitution of the input inductor with a flyback transformer, which acts to clamp the dc bus voltage. The second is that the input section is not based on the boost converter, but is instead based on a buck–boost converter operating with $D \leq 0.5$ like a buck converter. The combination of the two mechanisms reduces potential voltage variation better than just one mechanism by itself.

4) In a "real" converter prototype, voltage V_C may exceed $n_1 V_o$ slightly due to nonidealities in the transformer and the clamping diode D_3 such as leakage and winding inductance and diode forward voltage drop.

III. STEADY-STATE ANALYSIS AND DESIGN

The key parameters that affect the operation of the proposed converter are the magnetizing inductances of T_1 and T_2, L_{m1} and L_{m2}, and the turns ratio of T_1 and T_2, n_1 and n_2. A design procedure is needed to determine appropriate values for these parameters. This can be done by analyzing the converter's steady-state characteristics and reviewing a number of

parameter combinations. The following assumptions can be been made to simplify the analysis: All components are lossless.

1) The duty ratio of the converter remains constant during line cycle.
2) The switching frequency is much higher than the input line frequency.
3) C is large enough to assume that V_C is constant. There is no ripple over V_C or output voltage.
4) T_1 has been substituted with an inductor. Based on technical needs, n_1 will be fixed.

It should also be noted that the leakage inductances of T_1 and T_2 are neglected in the analysis. When the switch is turned OFF, leakage inductance energy from T_1 goes into C and leakage inductance energy from T_2 is dissipated by some snubber (typically a simple dissipative RCD snubber) that should be placed across T_2 to keep overvoltage spikes from appearing across the switch. Since the leakage inductance energy from T_2 comes from C, there is a situation where more energy is transferred to C than what would be under ideal circumstances with T_1 not having leakage inductance, but also more energy is transferred out of C than what would be under ideal circumstances with T_2 not having leakage inductance. In other words, there is additional energy coming into C, but there is also additional energy coming out of C as well so that the net effect on V_C is not as large as one might think. Since this is the case and since including leakage inductance in the analysis would make it very complicated with little benefit, leakage inductance has been neglected in the analysis.

A procedure for the selection of the converter's key component values (L_{m1}, L_{m2}, n_1 and n_2) is presented in this section and is demonstrated with an example. For example, the converter will be designed for

Input voltage: $V_{in} = 85\text{–}265\ \text{V}_{rms}$
Output voltage: $V_o = 48\ \text{V}_{dc}$
Maximum output power: $P_o = 100\ \text{W}$
Switching frequency: $f_{sw} = 100\ \text{kHz}$.

The converter will be designed so that 1) it operates with a fully discontinuous input current so that it is bounded by a sinusoidal envelope and contributes to an excellent input power factor, 2) the converter's maximum duty cycle does not exceed $D = 0.5$, and 3) there is no direct energy transfer from the primary of T_1 to the output when the input voltage is at its minimum value of $V_{in} = 85\ \text{V}_{rms}$. Condition 3 helps to set the voltage across C at which $n_1 V_o$ should be set to clamp so that the variation of this voltage due to varying line and load conditions is minimized. Once this voltage has been established, then the ratio of energy that is transferred to the output through one transformer relative to that through the other can be considered. The design procedure can be summarized as follows.

1) The procedure begins by considering the operation of the converter with transformer T_1 acting as an inductor L_{m1}, with no direct energy transfer taking place. This will help select a value for L_{m1}.
2) Next, values of L_{m2} and n_2 will be selected based on the value of L_{m1} that was previously selected.

3) Then, the operation of the converter implemented with T_1 having a magnetizing inductance of $L_1 = L_{m1}$ will be considered. A value of n_1 will be selected based on peak switch voltage stress.
4) Finally, a check of the converter's operation with the selected values of L_{m1}, L_{m2}, n_1, n_2 will be made based on the distribution of energy transferred to the load among transformers T_1 and T_2.

A. Selection of Magnetizing Inductance L_{m1}

The value of L_{m1} needs to be sufficiently low so that the magnetizing current of T_1 does not become continuous and the converter operates in input discontinuous conduction mode (DCM). If the maximum allowable duty cycle is $D = 0.5$ and if it is possible for the converter to operate past the boundary between input DCM and input continuous conduction mode (CCM), it is most likely to do so when D is at its maximum value of 0.5 and V_{in} is the minimum input line voltage [18]. Assuming that the input section is in DCM, then the following expression for L_{m1}, which is based on (2), must be satisfied [22]:

$$L_{m1} \leq \frac{D^2 V_{in}^2}{2 P_o f_{sw}}. \tag{2}$$

The reader is referred to the Appendix for a detailed derivation of this relation. Substituting the appropriate parameter values into (2) gives

$$L_{m1} \leq \frac{0.5^2 (85\ \text{Vrms})^2}{2 \times 100\ \text{W} \times 100\ \text{kHz}} = 90\ \mu\text{H}. \tag{3}$$

Since the maximum output power of the converter is 100 W, the value of L_{m1} cannot exceed 90 μH. The value of L_{m1}, however, should not be much lower than this in order to minimize the peak current in the input section of the converter and the peak current flowing through the switch. Moreover, if L_{m1} is lower than this value, then the duty cycle will also become lower and may, in fact, become too narrow when the input voltage is at its maximum rms value, which is not desirable. Therefore, the value of L_{m1} has been set at $L_{m1} = 90\ \mu$H for this example.

B. Selection of L_{m2} and n_2

With the value of L_{m1} selected in the previous section, the next step is to select appropriate values of L_{m2} and n_2. For this step, the assumption that T_1 acts like an inductor and there is no direct transfer of energy from the input section of the converter to the output will continue to hold. The main criterion that will be used to select L_{m2} and n_2 is whether the level of the bus capacitor voltage V_C is high enough to completely demagnetize L_{m1} during the $(1 - D)T$ time in each switching cycle when the switch is OFF. This criterion must be satisfied so that the input current will be fully discontinuous. There is, however, no closed-form equation or solution that can be used to determine whether this criterion is satisfied.

Since the magnetizing current of T_1 (input section transformer) and of T_2 (output section transformer) can be either fully discontinuous or "semicontinuous," as shown in Fig. 6, there are four possible current operating modes that need to be
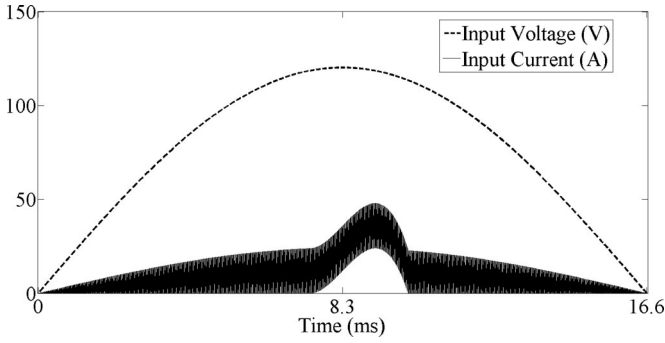
Fig. 6. Example of input voltage and current of a single-stage converter in semicontinuous current mode. Upper signal: line voltage ($V_{\mathrm{peak}} = 120$ V); lower signal: semicontinuous input current (peak 40 A).

considered when trying to analyze the steady-state characteristics of the converter with a particular set of parameter values for a particular set of line and load conditions. These can be referred to as input DCM, input semi-CCM, output DCM, and output CCM, based on the magnetizing currents of the "input" transformer T_1 and the "output" transformer T_2. It is the fact that it is possible for the converter to operate in one of these four combinations of "input/output" modes makes it difficult to establish closed-form equations that can be used in an analysis, as it is not possible to determine in which of the four current modes the converter is operating in just by looking at the converter's line and load conditions and component values. As a result, some sort of computer program is needed to analyze the converter's steady-state characteristics.

Such a program can be developed based on the energy equilibrium that must exist at the dc bus capacitor when there is no energy that is directly transferred from the input to the output. The energy stored in the dc bus capacitor during a half input line cycle (rectified line cycle) must be the same as that removed from the capacitor during the same time so that there is no net charge placed in the capacitor. This equilibrium can also be stated in terms of current—the average current that flows into the dc bus capacitor during a half line cycle must be the same as that which flows out during the same time so that there is no net average or dc current flowing in the capacitor. Once such equilibrium has been established for a set of operating conditions, only then does it become possible to analyze the converter's operation for this set of conditions. If the input section is in CCM, then the energy transferred to the dc bus capacitor from the input is

$$W_{\mathrm{in\text{-}CCM}} = \sum_{m=1}^{n} \int_0^{T_s} I_{\mathrm{avg}} V_C \, dt \tag{4}$$

where V_C is the voltage of dc bus capacitor C, T_s is the switching period, n is the number of switching cycles per line period, and I_{avg}, the average current absorbed by the capacitor during a switching cycle, is

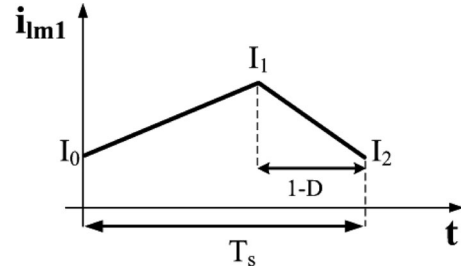$$I_{\mathrm{avg}} = \frac{(I_1 + I_2)(1 - D)}{2} \tag{5}$$

Fig. 7. Typical continuous current waveform.

I_1 and I_2 are the minimum and maximum of the current during one switching cycle. Fig. 7 shows a typical waveform of i_{Lm1} in CCM.

If the magnetizing current of T_1, i_{Lm1}, is fully discontinuous and the converter is operating with input DCM, then the energy transferred to the dc capacitor C from the input during a line cycle can be expressed in terms of an equation. This equation is

$$W_{\mathrm{in\text{-}DCM}} = \int_0^{T_L} \frac{D^2 V_m^2}{4 L_{m1} f_s} \, dt \tag{6}$$

where V_m is the peak value of the input voltage, D is the duty ratio of the switch, L_{m1} is the magnetizing inductance of T_1, f_s is switching frequency, and T_L is the line period. Equation (6) is derived in the Appendix.

When the output section is in CCM, the energy transferred out of C is

$$W_{\mathrm{out\text{-}CCM}} = \int_0^{T_l} \frac{(V_C D)^2}{((1-D)n_2)^2 R} \, dt \tag{7}$$

where R is the load resistance and n_2 is the turn ratio of transformer T_2. Equation (7) has been derived from $\int_0^{T_l} (V_o^2/R) dt$ and the voltage ratio of the flyback transformer in CCM has been substituted into this integration. When the output section is in DCM, the energy transferred out of capacitor C is

$$W_{\mathrm{out\text{-}DCM}} = \int_0^{T_L} \frac{D^2 T_s}{2 L_{m2}} V_C^2 \, dt. \tag{8}$$

It can be seen that V_C is either directly or indirectly related to the energy equations; therefore, what a computer program can try to do for a particular set of operating conditions and converter component values is to determine a value of V_C that can make W_{in} and W_{out} equal, regardless of which of the four possible combinations of current conduction modes the converter is in. Such a procedure can be developed as follows for an operating point with input voltage V_{in}, output voltage V_o, switching frequency f_s, duty cycle D, output power P, and component values L_{m1}, L_{m2}, and n_2.

Step 1: Assume that i_{Lm2} is continuous, then find a value of V_C by relating V_o to V_C using the standard CCM flyback equation

$$V_o = \frac{D}{(1-D)} \frac{V_C}{n_2} \tag{9}$$

and rearranging to get

$$V_C = \frac{V_o(1-D)n_2}{D}. \tag{10}$$

Step 2: Confirm that i_{Lm2} is actually continuous using

$$I_{Lm2-\min} = \frac{V_C D}{((1-D)n_2)^2 R} - \frac{V_C D T_s}{2 L_{m2}} > 0 \quad (11)$$

which subtracts the peak magnetizing current ripple from the average magnetizing current. If this equation is satisfied, then i_{Lm2} is actually continuous; otherwise, it is discontinuous and the bus voltage should be determined using

$$V_C = \frac{V_o}{D} \sqrt{\frac{2 L_{m2}}{T_s R}}. \quad (12)$$

Equations (11) and (12) are standard flyback converter equations that can be found in power electronic textbooks such as [23]. The derivation of these equations is, therefore, not shown here.

Step 3: The energy that flows into the dc bus capacitor from the converter's input section should be calculated by using (4) or (6). Before doing so, it should be confirmed whether the input current is semicontinuous or fully discontinuous. If V_C is high enough to demagnetize T_1 by discharging L_{m1} over a time interval equal to $(1-D)$ times the switching period when the input current is at its peak value, then the input current is fully discontinuous and (6) should be used; otherwise, the input current is semicontinuous and (4) should be used. Similarly, the energy that is transferred out of the dc bus capacitor should be calculated by (7) or (8), depending on whether i_{Lm2} is continuous or discontinuous, as determined from the previous steps.

Step 4: If (4) or (6) is equal to (7) or (8), then the calculated dc bus voltage is valid. If not, then D should be changed and the procedure should be repeated until a value of D is found that generates a value of V_C that makes (4) or (6) match (7) or (8).

This procedure can be implemented in a computer program to calculate numerous valid operating points that can then be used to generate graphs of steady-state characteristic curves that can be used in the design of the converter. Fig. 8 shows a graph of curves of V_C versus load power for different values of L_{m2} with input voltage $V_{in} = 85\ V_{rms}, L_{m1} = 90\ \mu H, f_s = 100\ kHz$, and $V_o = 48\ V$. Fig. 9 shows a graph of V_C versus load power curves for different values of n_2 with $V_{in} = 85\ V_{rms}, L_{m1} = 90\ \mu H, f_s = 100\ kHz$, and $V_o = 48\ V$. The regions where L_{m1} is working in DCM or CCM have been differentiated in both graphs. It should be noted that 1) this step of the design procedure is iterative and the graphs shown in Figs. 8 and 9 are the results of the final iteration, 2) the graphs have been drawn for $V_{in} = 85\ V_{rms}$ because if the input current is fully discontinuous for low line and full load, then it will be so for all other operating conditions, and 3) the graphs have been drawn considering T_1 as an inductor.

It can been seen in Fig. 8 that the $L_{m2} = 150\ \mu H$ curve crosses into the CCM region of the graph at about $P_o = 65\ W$ while the $L_{m2} = 200\ \mu H$ curve does not cross into the CCM region until the output power exceeds $P_{o,\max} = 100\ W$. It can been seen in Fig. 9 that the $n_2 = 2$ curve crosses into the CCM region of the graph at about $P = 90\ W$, while the $n_2 = 2.5$ curve does not cross into the CCM region until the output power exceeds $P_{o,\max} = 100\ W$. Based on Figs. 8 and 9, L_{m2} and n_2 have been selected to be $180\ \mu H$ and 2.5, respectively, to keep L_{m1} in the
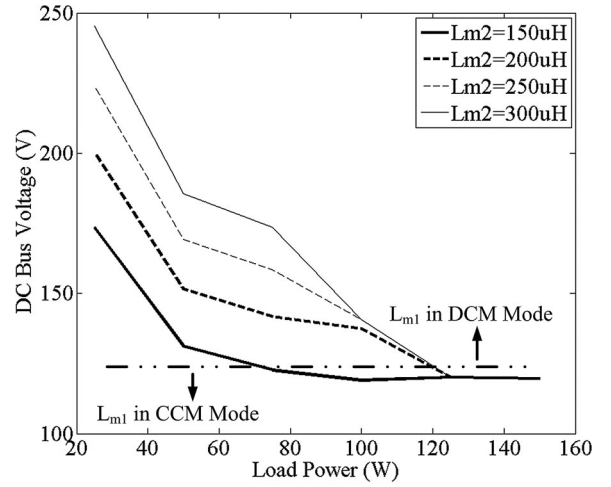

Fig. 8. DC bus voltage versus load power for different values of L_{m2} with $V_{in} = 85\ V_{rms}, L_{m1} = 90\ \mu H, f_s = 100\ kHz, V_o = 48\ V$, and $n_2 = 2.5$.
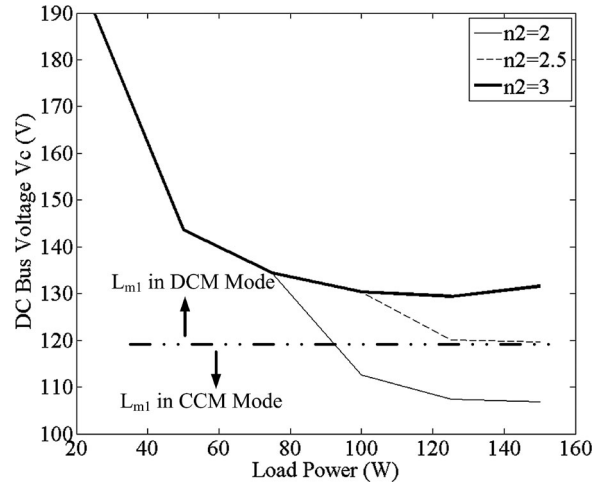

Fig. 9. DC bus voltage versus load power for different values of n_2 with $V_{in} = 85\ V_{rms}, L_{m1} = 90\ \mu H, f_s = 100\ kHz, V_o = 48\ V$, and $L_{m2} = 180\ \mu H$.

DCM for the whole load power range; moreover, T_2 remains in DCM with these selected values.

C. Selection of n_1

The next step of the procedure is to consider the operation of the converter with transformer T_1 able to transfer energy directly from the converter input section to the output. The previous steps have established a combination of L_{m1}, L_{m2}, and n_2 that ensure that the current flowing through T_1 is fully discontinuous throughout the line cycle even if the converter operates with low line and with a duty cycle D that does not exceed 0.5. The duty cycle limitation was confirmed in the generation of the characteristic curves shown in Figs. 8 and 9 so that all operation points on these curves satisfy this criterion. Since the flow of energy directly from T_1 to the output results in a lower V_C voltage then what would result if there is no such flow, n_1 should be selected so that there is little, if any, direct energy transfer when the converter is operating with low line to keep the input current fully discontinuous and thus ensure an

excellent input power factor. In other words, the operation of the converter with T_1 should be the same as if the transformer is implemented with some inductor L_1 under low line conditions. This is why the operation of the converter is just considered with an inductor L_{m1} instead of a transformer T_1 in the initial stages of the procedure.

The turn ratio of T_1, n_1, defines the voltage level of V_C when the converter enters Mode 2, the dual flyback mode of operation, as defined in Section II. It also defines the peak voltage stress across the converter switch as follows:

$$V_{\text{stress}} = \begin{cases} V_{\text{in}} + V_C & V_C \leq n_1 V_o \\ V_{\text{in}} + n_1 V_o & V_C > n_1 V_o \end{cases}. \quad (13)$$

Since the maximum voltage stress is $V_{\text{in}} + n_1 V_o$, rearranging (13) gives

$$n_1 \leq \frac{V_{\text{stress}} - V_{\text{in-max}}}{V_o}. \quad (14)$$

If the peak voltage stress can be limited to 500 V, based on previous iterations, then the maximum value of n_1 can be found from (14) to be

$$n_{1-\text{max}} \leq \frac{500 - 265\sqrt{2}}{48} = 2.65. \quad (15)$$

The value of n_1, however, cannot be too small as it would clamp V_C to a voltage that is too low to demagnetize T_1 based on what has been shown in Figs. 8 and 9. The graphs in these figures show that the minimum acceptable V_C (the value of V_C at the boundary of L_{m1} being in DCM or in CCM) should be 120 V. Since this is the case and the output voltage is 48 V, then a value of $n_1 = 2.5$ should be chosen as follows:

$$V_{C-\text{max}} = 2.5 \times 48 = 120 \text{ V}. \quad (16)$$

D. Energy Transfer Ratio

The final step of the procedure is to examine the ratio of energy transferred through T_2 to that transferred through T_1. It is expected that most of the energy from the input is transferred through T_2 when the input voltage is low and through T_1 when the input voltage is high—when the level of V_C tries to rise, but is clamped by T_1 and its secondary diode. Fig. 10 shows a graph of energy transfer ratio $E = E_{T2}/E_{T1}$ versus input voltage with V_{in} for different values of L_{m2}. The curves were generated with $L_{m1} = 90\ \mu\text{H}$, $f_s = 100\ \text{kHz}$, $V_o = 48\ \text{V}$, $P_o = 100\ \text{W}$, $n_1 = 2.5$, and $n_2 = 2.5$. The amount of energy transferred through T_1, E_{T1}, and T_2, E_{T2} was determined by the computer program. This was done for the maximum power of 100 W by considering the following.

1) Since it has been confirmed in previous procedure steps that the input section of the converter is operating in DCM, (2) can be used to determine the converter's duty cycle D for different values of input voltage as $W_{\text{in-DCM}} = $ power times T_L and the other parameters are known.
2) Since it has been confirmed in previous converter steps that T_2 is fully demagnetized by the end of each switching cycle, and $V_C = 120\ \text{V}$, D, and the other parameters are
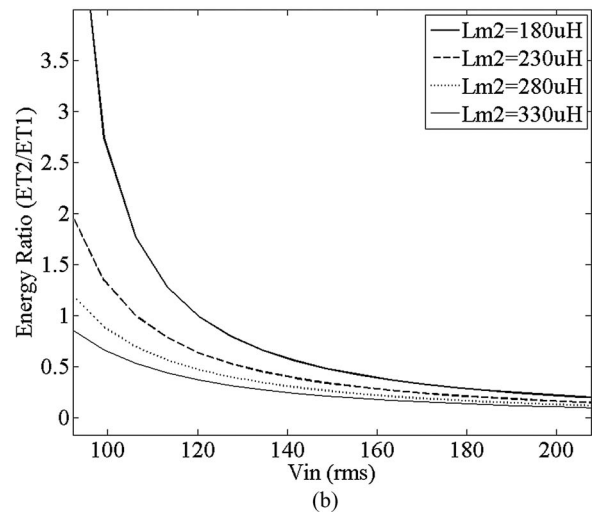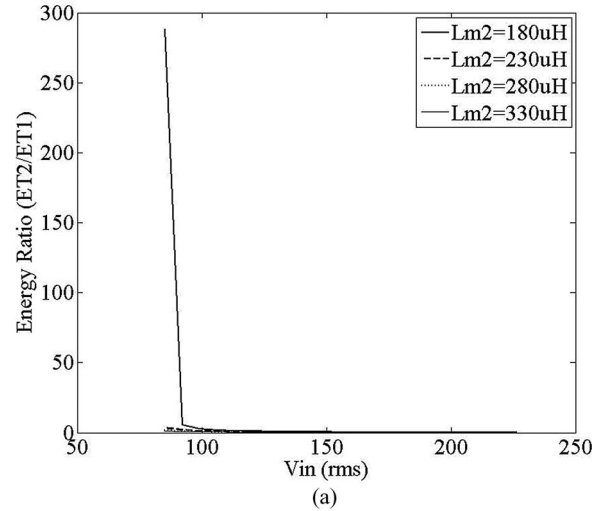

Fig. 10. Energy ratio (E_{T2}/E_{T1}) versus input voltage V_{rms} with $L_{m1} = 90\ \mu\text{H}$, $f_s = 100\ \text{kHz}$, $V_o = 48\ \text{V}$, $P_o = 100\ \text{W}$, $n_1 = 2.5$, and $n_2 = 2.5$.

known, (8) can be used to find the amount of energy that is transferred through T_2, E_{T2}.
3) Since the amount of energy injected from the input to the converter and E_{T2} have been established, E_{T1} must be the difference between the two.

It can be seen from Fig. 10 that more energy goes directly to the output from T_1 if L_{m2} is greater than 180 μH. If L_{m2} is less than 180 μH, then V_C will be less than 120 V and the input may no longer be fully discontinuous throughout the line cycle. What this does is that it makes T_1 the main power transformer through which power is transferred to the output and it increases the output ripple significantly as more of the 120 Hz frequency component due to the rectified voltage of the input diode bridge is reflected to the output. This is especially true when V_{in} is at low line and the input current is at its maximum value. In order to change this ratio and ensure that a greater amount of energy is transferred through T_2, the value of n_1 must be increased so that less energy is transferred directly through T_1. Doing this, however, increases the voltage level at which V_C is clamped and

increases drain–source voltage of the switch so that it exceeds 500 V.

It should be mentioned that the magnetizing current of T_2, i_{Lm2} may become continuous with very large values of L_{m2}. As Fig. 10 shows, increasing L_{m2} reduces the transferred energy from this transformer sharply which is not a desired case; therefore, smaller values for L_{m2} are preferred. It should be noted that Fig. 10(b) is just a magnified portion of Fig. 10(a) and that E_{T2}/E_{T1} approaches infinity in Fig. 10(a) as V_{in} approaches 85 V_{rms} because the converter has been designed so that $E_{T1} = 0$ when the input voltage is 85 V_{rms}. The lowest value of V_{in} shown on the graph of Fig. 10(a) is $V_{in} = 86$ V_{rms}.

E. Diode Voltage Ratings

The maximum steady-state reverse voltages of the diodes that are used in the converter are as follows:

$$V_{rev.-D1} = n_1 V_o + V_{in(peak)}$$

$$= 2.5 \times 48 + \sqrt{2} \times 265 = 445\,V \quad (17)$$

$$V_{rev.-D2} = 2n_2 V_o = 240\,V \quad (18)$$

$$V_{rev.-D3} = \frac{V_{in(peak)}}{n_1 + V_o} = \frac{265\sqrt{2}}{2.5 + 48} = 197\,V \quad (19)$$

$$V_{rev.-D4} = \frac{V_c}{n_2 + V_o} = \frac{120}{2.5 + 48} = 96. \quad (20)$$

IV. EXPERIMENTAL RESULTS

A 100-W experimental prototype was built to verify the working of the proposed configuration. The prototype was designed according to following specifications:

$V_{in} = 85–265$ V_{rms}
$V_o = 48$ V_{dc}
$P_o = 100$ W
$f_{sw} = 100$ kHz.

The following devices were used for the semiconductors in that circuit:

Main switch: IRF840
D_1 and D_2: RHRP1560
D_3 and D_4: U1540
DC bus capacitor (C): 470 μF, 200 V
Output capacitor (C_o): 470 μF, 63 V.

Figs. 11–15 show typical switch voltage waveforms and typical primary and secondary current waveforms of T_1 and T_2 for different input voltages. Fig. 11 shows that T_1 and T_2 are working in DCM when the input voltage is at its minimum and that both transformers are fully demagnetized after the switch is turned OFF. Fig. 12 shows the same currents and voltage for the maximum input voltage. As can be seen, V_{DS} reduces to the input voltage when T_1 has been completely discharged. Fig. 13 shows the output current of T_2 and the drain–source voltage of the switch when input voltage is at the minimum and the load is at its maximum value. It shows that T_2 is completely discharged within the switching cycle. It should be noted that
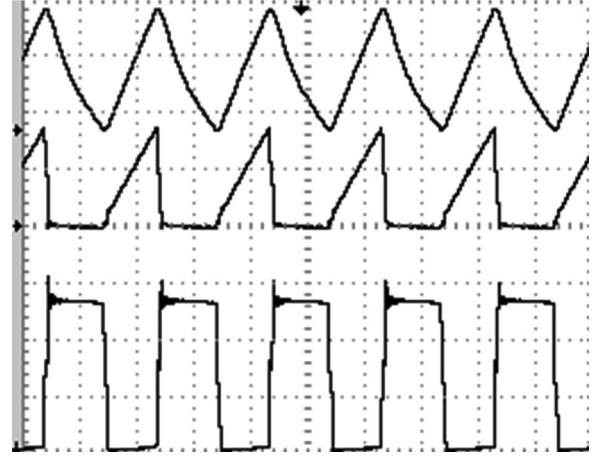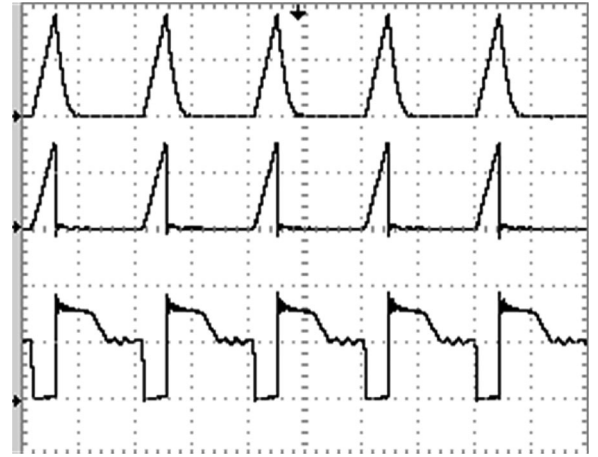

Fig. 11. Primary current of T_1 (upper signal), primary current of T_2 (middle signal), and drain–source voltage of the switch (lower signal), $P = 100$ W, $V_{in} = 85$ V_{rms}, $V_o = 48$ V, $I = 2$ A/div, $V_{DS} = 100$ V/div, $t = 5$ μs/div.

Fig. 12. Primary current of T_1 (upper signal), primary current of T_2 (middle signal), and drain–source voltage of the switch (lower signal), $P = 100$ W, $V_{in} = 230$ V_{rms}, $V_o = 48$ V, $I_{T1} = 2$ A/div, $I_{T2} = 1$ A/div, $V_{DS} = 250$ V/div, $t = 5$ μs/div.

overvoltage spikes that could appear across the switch due to the leakage inductance of T_2 have been snubbed by a typical *RCD* snubber that has been placed across the switch. Fig. 14 shows drain–source voltage of the switch and secondary current of T_1 when input voltage is at its maximum voltage. It shows that T_1 is fully demagnetized before the start of the next switching cycle. Fig. 15 shows an input voltage waveform and the envelope of the secondary current of T_1. It can be seen that the current through T_1 is higher when the input voltage is high, which means that more energy is transferred to the output during this time. Fig. 16 shows the input voltage and filtered current waveforms when the input voltage is 100 and 230 V_{rms}. In both cases, the filtered input current confirms that sinusoidal current waveforms can be achieved by the converter as long as the input section is working in DCM.

Fig. 17 shows the harmonic content of the converter when it is operating at $V_{in} = 100$ V_{rms} and $V_{in} = 230$ V_{rms}. It can be seen that the converter satisfies IEC 61000-3-2 standards.
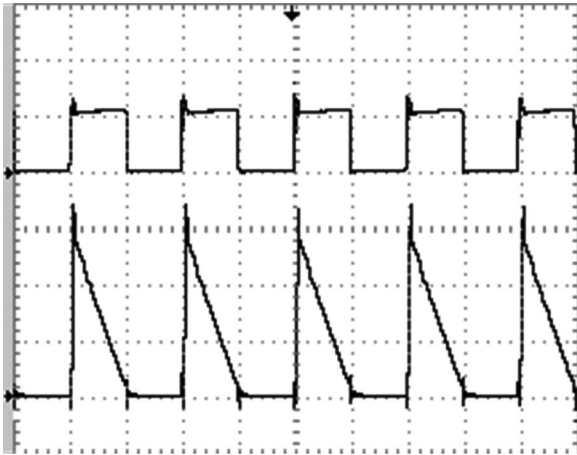
Fig. 13.   Drain–source voltage of the switch (upper signal) and output current of T_2 (lower signal), $P = 100$ W, $V_{\rm in} = 85$ V$_{\rm rms}$, $V_o = 48$ V, $V_{\rm DS} = 250$ V/div, $I = 2$ A/div, $t = 5$ μs/div.

Fig. 14.   Drain–source voltage of the switch (upper signal) and output current of T_1 (lower signal), $P = 100$ W, $V_{\rm in} = 230$ V$_{\rm rms}$, $V_o = 48$ V, $V_{\rm DS} = 250$ V/div, $I = 2$ A/div, $t = 5$ μs/div.
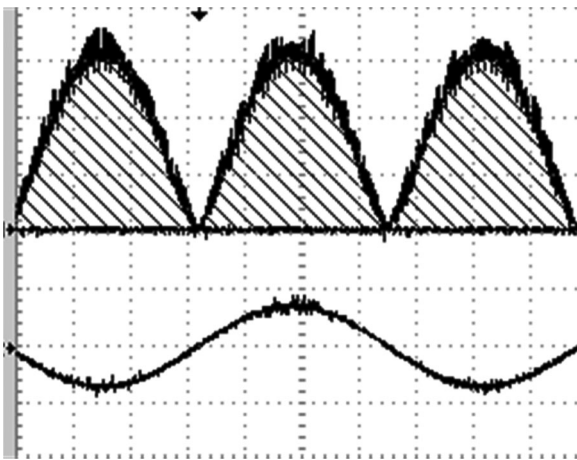

Fig. 15.   Peaks of the output current from secondary winding of T_1 (upper signal) and input voltage (lower signal). $P = 100$ W, $V_{\rm in} = 230$ V$_{\rm rms}$, $V_o = 48$ V, $I = 5$ A/div, $V = 500$ V/div, $t = 2.5$ ms/div. (a) $V_{\rm in} = 100$ V$_{\rm rms}$, $V = 50$ V/div, $I = 1$ A/div, $t = 2.5$ ms/div. (b) $V_{\rm in} = 230$ V$_{\rm rms}$, $V = 100$ V/div, $I = 500$ mA/div, $t = 5$ ms/div.
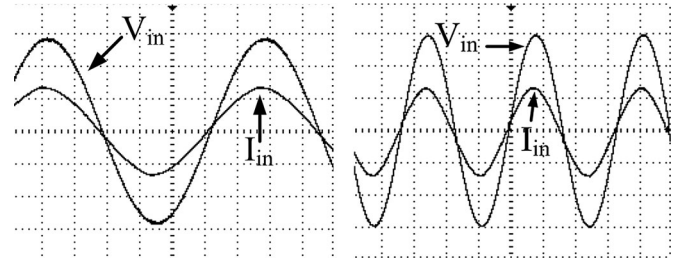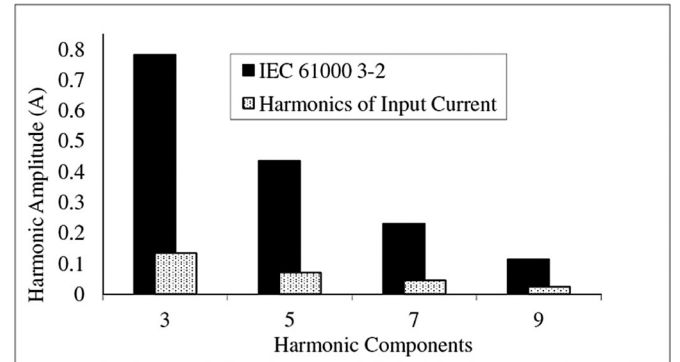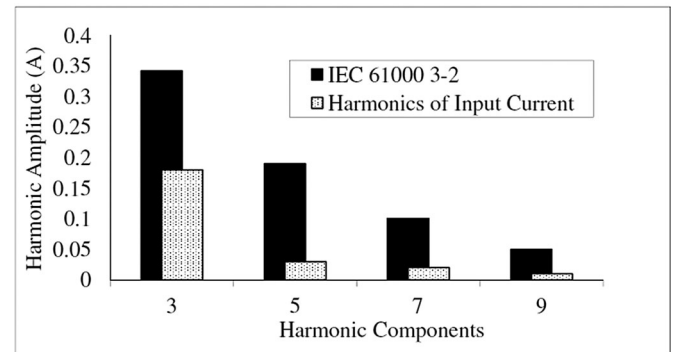

Fig. 16.   input voltage and current waveforms. (a) $V_{\rm in} = 100$ V. (b) $V_{\rm in} = 230$ V.

(a)

(b)

Fig. 17.   Harmonic components of input current when $P_o = 100$ W and $V_o = 48$ V for two different input voltage.

Fig. 18 shows the dc bus voltage versus input voltage for different load power conditions. These results confirm that the dc bus voltage is almost fixed for different load and input voltage conditions. This makes it easier to satisfy hold-up time requirements for all different load and input voltage conditions if such a feature is needed. It should be noted that the bus voltage is not clamped to exactly $n_1 V_o = 120$ V because of nonidealities in the converter components and transformers such as leakage inductance. The increase in V_C that occurs when the input voltage is increased is due to the fact that primary and secondary leakage inductances have voltage drops that become larger as more current flows in T_1, which is what happens as input voltage is increased.

Fig. 19 shows a comparison of dc bus voltage for similar converters [5], [16], [24]. This figure clearly shows that variation of dc bus voltage compared to new similar proposed converter is less. It should be mentioned that the output voltage of the
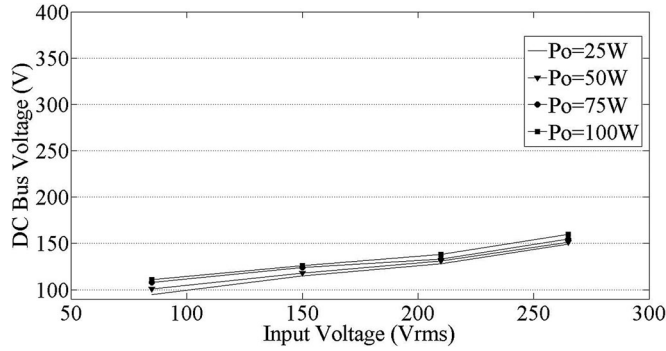
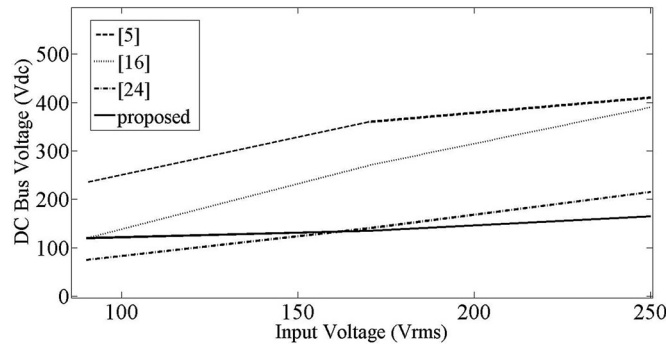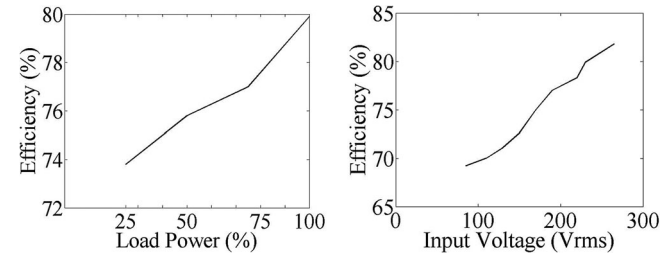Fig. 18.   DC bus voltage versus input voltage for different load power.

Fig. 19.   DC bus voltage comparison. (a) Efficiency versus load power ($V_{\rm in} = 230$ $V_{\rm rms}$). (b) Efficiency versus $V_{\rm in}$ (load power = 100%).

Fig. 20.   Efficiency of the converter.

converters in [5] and [16] are 50 and 54 $V_{\rm dc}$, respectively, which are close to the proposed converter. Also for both of them, maximum accessible load power is defined equal to 80 W.

Fig. 20(a) shows the efficiency versus load power when input voltage is equal to 230 $V_{\rm rms}$. Fig. 20(b) shows the efficiency of the converter versus different input voltage when load power is 100 W. The measured efficiency was found to be very similar to other previously proposed single-stage converters, but the proposed converter has a better input current harmonic content and a nearly fixed dc bus voltage. This allows the converter to operate with smaller dc bus capacitors and smaller sized transformers as they do not have to handle the voltages that these components must handle in other converters. This is especially true if hold-up time is a consideration.
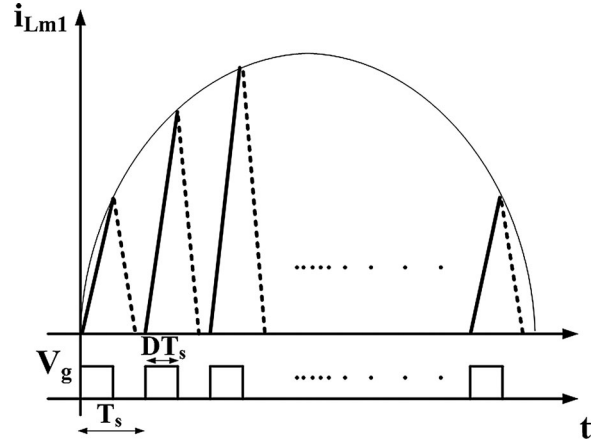

Fig. 21.   Input current waveform.

V. CONCLUSION

In this paper, a new single-stage high-power factor converter is proposed. The outstanding feature of this converter is that its dc bus voltage variation is significantly less than that of other single-stage converters, which allows smaller sized components to be used. This is the result of the buck–boost type input section and clamping of V_C by the secondary winding of T_1 to $n_1 V_o$. In the paper, the operation of the converter was explained, and key characteristic equations were derived and used to design the converter. The feasibility of the converter—its ability to operate with a nearly fixed dc bus voltage regardless of line and load conditions and its ability to operate with an excellent input power factor—was confirmed with results obtained from an experimental prototype.

APPENDIX

If the input current of the proposed converter is fully discontinuous, then the input current over a half-line cycle will look like the current waveform shown in Fig. 21. The current rises when the switch is ON and falls when the switch is OFF. The average power that is injected into the converter during a half-line cycle can be calculated as follows: The instantaneous power injected to the converter is

$$p(t) = v_{\rm in}(t)i_{\rm in}(t). \tag{A1}$$

The average power during a switching cycle is

$$P_{\rm avg} = \frac{1}{T_S} \int_0^{DT_s} P(t)dt. \tag{A2}$$

Since the line frequency is much lower than the switching frequency, the input voltage can be assumed to have a constant value of $V_m \sin(\omega k)$ during any switching cycle k; therefore, (A2) can be rewritten as follows:

$$P_{\rm avg} = \frac{V_m \sin(\omega k)}{T_S} \int_0^{DT_s} i_{\rm in}(t)dt = V_m \sin(\omega k)i_{\rm avg}. \tag{A3}$$

The value of i_{avg} in the switching cycle k is

$$i_{\text{avg}}(k) = \frac{\int_0^{DT_S} i_{\text{in}}(t)dt}{T_S} = \frac{V_m D^2 T_S \sin(\omega k)}{2L_{m1}}. \qquad (A4)$$

The average of the input power during a half-line cycle can be found by substituting these values into (A2), but the integration area is in half a line cycle

$$
\begin{aligned}
P_{\text{in-avg}} &= \frac{2}{T_L} \int_0^{T_L/2} P_{\text{avg}}dt \\
&= \frac{2}{T_L} S_0^{T_L} \left[V_m \sin(\omega t) \right] \left[\frac{V_m D^2 T_S \sin(\omega t)}{2L_{m1}} \right] dt \\
&= \frac{D^2 V_m^2}{4L_{m1}f_s}. \qquad (A5)
\end{aligned}
$$

The integration of (A5) over half a line cycle gives (6).

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