# A Low Cost Flyback CCM Inverter for AC Module Application

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***Abstract*—The unfolding-type flyback inverter operating in discontinuous conduction mode (DCM) is popular as a low-cost solution for a photovoltaic (PV) ac module application. This paper aims to improve the efficiency by using a scheme based on continuous conduction mode (CCM) for this application. Design issues, both for the power scheme and the control scheme, are identified and trade-offs investigated. An open-loop control of the secondary current, based on feedback control of the primary current, is proposed in order to bypass the difficulties posed by the moving right half plane zero in the duty cycle to secondary current transfer function. The results presented show an improvement of 8% in California efficiency compared to the benchmark DCM scheme for a 200-W PV module application. The output power quality at rated power level is capable of meeting IEC61727 requirements. The stability of the flyback inverter in CCM has been verified at selected working conditions.**

***Index Terms*—Current control, distributed power generation, inverters, power quality, power system stability, solar energy.**

## I. Introduction

NOWADAYS, distributed power generation in residential areas, using solar panels, is well accepted and also supported by recent developments in building integrated photovoltaic (BIPV) systems as well as microgrid systems. However, when PV panels are connected in series to feed a string inverter with a global maximum power point tracker (MPPT), a considerable power loss due to modular mismatches caused by both varying panel orientations and shading would occur [1].

A major approach to solve this issue has been to package the PV panel with a module-integrated inverter, called an "ac module" [2], which directly serves the grid. Though requiring a large number of dc–ac conversion stages, the approach allows for easy "plug and play" system expansion. Also, only ac cable wiring is needed, which simplifies the installation.

The acceptability of an ac module depends on its efficiency, cost effectiveness, and reliability. Three major trends are noted in the study of inverter topologies for this application. The first is the use of a transformerless inverter [3]–[8] that is motivated by the benefits of reduction in size and cost and also by possible efficiency improvement [3]. However, the limited voltage boosting capability of such an inverter unit prevents the use of this technology in universal grid voltage range (85–265 V ac) applications.

Another trend is focused on an isolated cascaded scheme that includes one or more dc voltage boosting stage and a conventional full bridge PWM inverter [9], [10]. This type of inverter has by far the highest reported efficiencies compared to other isolated inverters. Also, the electrolytic capacitor for power decoupling can be replaced by a higher voltage film capacitor with longer lifetime. However, the penalty paid for this approach is more component count and hence higher cost.

Considerations of reducing the cost have led to a third approach based on an unfolding type inverter. Here, the voltage boosting, isolation, and output current shaping are all performed by a dc–dc converter that is then followed by a low-frequency unfolding stage. A flyback inverter with center-tapped secondary windings is often adopted leading to a simple overall system [11]. However, in this scheme, the flyback is operated in the discontinuous conduction mode (DCM) resulting in high current stress and lower efficiencies. This is particularly true in low voltage and high-current applications such as the ac module under consideration. Aware of this limitation of the flyback DCM scheme at larger power levels, Ji *et al*. [12] and Kyritsis *et al*. [13] have studied the flyback inverter operating in a dual switching mode between DCM and boundary conduction mode (BCM).

When operated in continuous conduction mode (CCM), a flyback converter has lower peak currents and hence higher efficiencies. This has been exploited before in both dc/dc power conversion and ac/dc power factor (PF) correction applications. However, the control to output current transfer function in a flyback CCM converter has a right half plane (RHP) zero, which causes difficulty in controlling the output current of the converter effectively. This may have prevented the use of the flyback CCM converter in dc/ac inverter applications. Therefore, in our approach, we investigate the feasibility of a flyback inverter operating (mainly) in CCM mode as a grid-connected ac module inverter, with a view to demonstrating that a significant efficiency improvement can be realized without adding to the complexity of both the power and control circuits.

In the industry, efficiency figures weighted over a range of operating conditions (California efficiency [14] or European efficiency [1]) are used to characterize the inverter performance. Additional techniques are usually used to improve this figure

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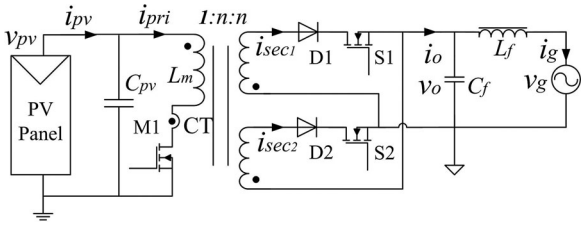


Fig. 1. Circuit topology of flyback inverter.

over what can be obtained with a straightforward power converter topology. Our approach is not targeted at these weighted efficiency (California or European) improvement technologies, but at the efficiency improvement due to change in the basic operating mode of the flyback inverter itself. In order to provide a fair comparison, the designs of the power topology for both the proposed CCM approach and the DCM-only approach (used as a benchmark) are presented and compared in Section II. The control challenges faced in this application and ways of resolving them are discussed in Section III. An open-loop control of the secondary side current, based on the feedback control of the primary side current, is proposed in order to bypass the difficulties posed by the moving RHP zero in the transfer function. The control modeling and design are covered in Section IV. The experimental results are presented in Section V. The pros and cons of the proposed scheme, including the well-known lifetime issue related to large electrolytic capacitor, are discussed in Section VI.

## II. Flyback CCM Inverter—Steady-State Analysis

The topology is the same as that used in a flyback ac module operating in DCM [11] and consists of an input capacitor$C_{\rm pv}$, a flyback dc/dc converter with two secondary windings together with a waveform unfolding arrangement, and an *LC* output filter (see Fig. 1). The secondary side switches S1 and S2 are turned ON and OFF, respectively, during the positive and negative half cycles to generate the ac output. In each half cycle, the inverter works as a dc to dc flyback converter with the average output current ($i_{\rm sec1}$ or $i_{\rm sec2}$) shaped as a half sinusoid at the line frequency. Though the inverter is designed to operate in CCM under full load conditions, it is inevitable that it would enter the DCM region around the zero crossing instants of the line cycle or at low solar irradiation levels.

### A. Quasi-Steady-State Analysis

As the operating condition of the inverter changes slowly during an ac period compared to a switching period, the inverter can be assumed to operate in quasi-steady state around each instant of an ac cycle. It is also assumed that capacitor $C_{\rm pv}$ is large so that the input voltage $V_{\rm pv}$ is nearly constant in an ac cycle.

Unlike in DCM operation, the transformer core will not be fully demagnetized in CCM operation in each switching cycle. This causes the transformer core to serve as an energy buffer, adding to the order of the system. However, our earlier investigations [15] have shown that the effect of this incomplete core demagnetization on the input–output energy balance in each switching cycle is very small and can be neglected. Assuming lossless operation, the power balance equations under both DCM and CCM conditions can be written as

$$V_{\rm pv} I_{\rm pv} = V_{\rm rms} I_{\rm rms} \tag{1}$$

$$I_{\rm pri} V_{\rm pv} = I_g V_g = 2 V_{\rm rms} I_{\rm rms} \sin^2(\omega t) \tag{2}$$

where $V_{\rm pv}$,$I_{\rm pv}$ = the dc values of the PV module voltage and current, $V_{\rm rms}$, $I_{\rm rms}$ = the RMS values of the grid voltage and current, $I_{\rm pri}$ = the quasi-steady-state value of the primary side current averaged over a switching cycle, $I_g$,$V_g$ = the quasi-steady values of the grid current and voltage assumed to be constant in one switching cycle, and $\omega$ = the angular frequency of the ac supply.

Equation (1) is based on the power balance over an ac cycle, while (2) is based on the power balance in each switching cycle. The mismatch between the dc output power of the PV module as in (1) and the pulsating input power of flyback inverter indicated by (2) is handled by the input capacitor $C_{\rm pv}$, as shown in Fig. 1.

Based on converter operating waveforms, the primary side average current $I_{\rm pri}$ can be shown to be

$$I_{\rm pri} = \frac{D_{\rm DCM}^2 V_{\rm pv}}{2 L_m f_s}. \tag{3}$$

Here, $D_{\rm DCM}$ is the duty cycle in DCM operation and $f_s$ is the switching frequency. Also, $L_m$ is the primary side magnetizing inductance of the transformer. By substituting (1) and (3) into (2), the duty ratio of the inverter in DCM is obtained [16]

$$D_{\rm DCM} = 2\sqrt{\frac{I_{\rm pv} L_m f}{V_{\rm pv}}} \left|\sin(\omega t)\right| = D_{\rm amp} \left|\sin(\omega t)\right|. \tag{4}$$

Equation (4) shows that in DCM, the duty cycle varies according to the (rectified) grid voltage, while its amplitude ($D_{\rm amp}$) is determined by the ratio of $V_{\rm pv}$ by$I_{\rm pv}$. In this case, a simple open-loop scheme without current feedback can be adopted. By varying $D_{\rm amp}$, the ratio of $V_{\rm pv}$ over $I_{\rm pv}$ can be varied in order to seek and operate the system at maximum power point (MPP) [11].

When operated in CCM, by assuming quasi-steady-state operation and using inductor volt–seconds balance over a switching period, the duty ratio$D_{\rm CCM}$ can be obtained

$$D_{\rm CCM} = \frac{|V_g|}{(n V_{\rm pv} + |V_g|)}. \tag{5}$$

Here, the duty cycle does not directly determine the current and hence power level. Therefore, a closed-loop current control is necessary in this case.

The peak duty cycle values (denoted by the "^" symbol) in an ac period occur at the ac peak instants in both cases and can be written as

$$\hat{D}_{\rm DCM} = D_{\rm amp} = 2\sqrt{\frac{I_{\rm pv} L_m f_s}{V_{\rm pv}}} \tag{6}$$

$$\hat{D}_{\rm CCM} = \frac{\sqrt{2} V_{\rm rms}}{(n V_{\rm pv} + \sqrt{2} V_{\rm rms})}. \tag{7}$$

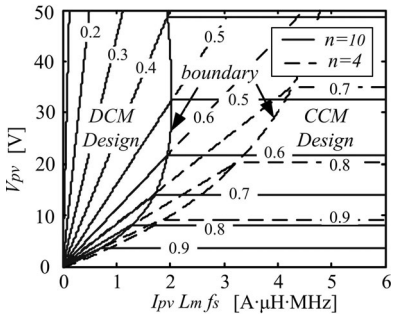


Fig. 2. Design aid diagram of flyback inverter for $V_{\rm rms} = 230$ V. (The numbers on the lines indicate the peak duty ratios.)

TABLE I
WORST-CASE CURRENT AND VOLTAGE STRESSES

| Stresses | Equations | |
|---|---|---|
| Primary side peak current in DCM | $\hat{I}_{P\_DCM} = 2\sqrt{I_{pv}V_{pv}/(L_m f_s)}$ | (9) |
| Primary side peak current in CCM | $\hat{I}_{P\_CCM} = 2I_{pv}V_{pv}\left(n/\sqrt{2}V_{rms}+1/V_{pv}\right)+\frac{1}{2L_m f_s\left(n/\sqrt{2}V_{rms}+1/V_{pv}\right)}$ | (10) |
| Secondary side peak current | $\hat{I}_S = \hat{I}_{P\_DCM}/n$ or $\hat{I}_{P\_CCM}/n$ | (11) |
| Voltage stress of M1 | $\hat{V}_{M1} = V_{pv} + \sqrt{2}V_{rms}/n$ | (12) |
| Voltage stress of D1/D2 | $\hat{V}_{d1,2} = nV_{pv} + \sqrt{2}V_{rms}$ | (13) |
| Voltage stress of S1/S2 | $\hat{V}_{S1,2} = 2\sqrt{2}V_{rms}$ | (14) |

The design condition for the peak duty cycle to occur at the DCM/CCM boundary operation can be derived by equating (6) and (7)

$$I_{\rm pv} L_{mc} f_s = \frac{V_{\rm pv}}{4 \times \left[nV_{\rm pv}/\left(\sqrt{2}V_{\rm rms}\right)+1\right]^2}. \tag{8}$$

Here, $L_{mc}$ is the critical inductance above which the operation is in the CCM mode.

Equations (6)–(8) relate the peak control variable $\hat{D}$, the PV module specifications $V_{\rm pv}$, $I_{\rm pv}$, and the design parameters of the inverter, viz., $n$, $L_m$, and $f_s$, under both DCM and CCM conditions. A design aid diagram is shown in Fig. 2 for an assumed grid voltage of 230 $V_{\rm rms}$ and for two assumed values of the turns ratio $n$ ( = 10 and 4). For the assumed $V_{\rm rms}$ and $n$ values, every point on the graph in Fig. 2 represents a possible inverter design. For example, $n = 10$, $I_{\rm pv} L_m f_s = 3$, and $V_{\rm pv} = 22$ V represents a CCM design with $\hat{D} = 0.6$. The curves marked as "boundary" represent the boundary between CCM design and DCM-only design for the two $n$ values assumed. The choice of $\hat{D}$ influences the component current stresses, as will be discussed in the following sections.

### B. Component Stresses

The worst-case current and voltage stresses in the inverter circuit can be obtained (see Table I) from a basic circuit analysis.

For a DCM-only design, as shown in (9), the peak primary current depends on the input power$I_{\rm pv}V_{\rm pv}$, $f_s$, and $L_m$ values and not on $n$. A larger $L_m$, but less than $L_{\rm mc}$, would reduce the primary side current. For a CCM design, the peak current stress is related to both $n$ and $L_m$ values (10). The primary side peak current has the same value as the peak value of the net transformer magnetizing current (primary side and secondary side combined) reflected on to the primary. In (10), the first term is the average value of the net magnetizing current, while the second term is half of the peak-to-peak ripple in the net magnetizing current. A larger $n$ value would lead to a higher average net magnetizing current (first term) while at the same time reducing the current ripple (second term). As the average magnetizing current is larger than the current ripple in CCM operation, in general, a smaller $n$ value is preferable to reduce the primary side current stress.

Smaller turns ratio would also require a larger peak duty ratio (7). As a result, the diode voltage stress is reduced as well (13) so that a diode with a smaller forward voltage drop can be chosen. However, the secondary side current stress increases (11). The MOSFET voltage stress also increases (12) requiring a MOSFET with larger on resistance (for the same die size). Thus, the trade-off between the current and voltage stresses of devices on both sides of the transformer determines $n$. Since in grid-connected ac module application, the input current and output voltage are large, the primary side current stress and output side voltage stress are more crucial. Therefore, a small $n$ is generally preferred.

### C. Suggested Design Steps

*Step 1:* Identify PV panel specifications. The voltage $V_{\rm pv}$ and current $I_{\rm pv}$ values given by the manufacturer correspond to MPP and vary with solar irradiance and temperature. For design purposes, a constant $V_{\rm pv}$ is used, while the variation of power is considered to be due to current change.

*Step 2:* Choose a switching frequency $f_s$ considering the trade-off between the switching losses and the transformer size.

*Step 3:* Choose an initial transformer turns ratio $n$. This can be tuned later.

*Step 4:* Obtain the peak duty ratio $\hat{D}$ and $L_{mc}$ using (7) and (8).

*Step 5:* Calculate voltage stresses of the primary and secondary side devices using (12)–(14).

*Step 6:* Choose $L_m$ ($>L_{mc}$) based on acceptable primary current stress using (10). A larger $L_m$ reduces the primary current stress, while increasing transformer size.

*Step 7:* Calculate the secondary current stress using (10) and (11).

*Step 8:* Return to steps 3–7 until the voltage and current stresses are acceptable.

If the primary current stress or the secondary diode voltage stress is too large, "$n$" can be reduced. If the secondary side current stress or the primary side voltage stress is too large, then "$n$" can be increased.

In our paper, a flyback inverter was designed for CCM operation for a power level of 200 W for the Kyocera solar module KC200GT. Another flyback inverter was designed for DCM-only operation as a benchmark for the same

TABLE II
DESIGN OF FLYBACK INVERTERS FOR OPERATION IN CCM AND DCM. (SPECIFICATIONS $V_{\rm pv} = 27$ V, $P_{\rm pv} = 0$–200 W, AND $V_{\rm rms} = 230$ V)

| | CCM Design | DCM-only Design |
|---|---|---|
| **Operation parameters** | | |
| $f_s$ (kHz) | 100 | 100 |
| $\hat{D}$ | 0.75 | 0.63 |
| **Transformer Design** | | |
| $n$ | 4 | 4 |
| $L_m$ (μH) | 20 | 3 |
| EE core | Magnetics 45528 | Magnetics 44020 |
| Primary (Litz: 72/28) | 6 turns | 3 turns |
| Secondary (Litz:12/28) | 24 turns | 12 turns |
| **Circuit Design** | | |
| $C_{pv}$ (μF) | 4700 | 4700 |
| $C_f$ (μF) | 0.9 | 0.9 |
| $L_f$ (μH) | 480 | 480 |
| **Voltage and Current Stresses** | | |
| $\hat{I}_p$ (A) | 24.8 | 51.6 |
| $\hat{I}_s$ (A) | 6.2 | 12.9 |
| $\hat{v}_{m1}$ (V) | 108.3 | 108.3 |
| $\hat{v}_{d1,2}$ (V) | 433.3 | 433.3 |
| $\hat{v}_{s1,2}$ (V) | 650.5 | 650.5 |

specifications. Table II gives the design parameters of both inverters as well as the respective current and voltage stresses at rated power. "Magnetics" ferrite cores (R material with the lowest loss at 100°C) are selected as indicated in Table II. The resonant frequency of the output filter is 7 kHz that ensures adequate filtering of the switching frequency ripple component. In Table II, as expected, the current stresses both on the primary and the secondary sides are lower in the CCM design.

## III. OUTPUT CURRENT SHAPING AND CONTROL CHALLENGES

The two basic control requirements are: MPPT capability required by the PV application and output current shaping required by the grid connection. In a single-stage inverter, a dual-loop configuration is usually adopted, wherein a fast inner control loop tracks the line frequency waveform and a slow outer loop ensures operation at MPP. In order to prevent distorting the output ac current, the MPPT tracking speed is purposely designed to be slower than the line frequency. The performance of the implemented MPPT scheme in the outer loop does not, in general, depend on the inverter and the control scheme adopted. Therefore, it is not discussed in this paper. The challenges of the inverter control for the proposed flyback CCM scheme lie in the output current shaping and these are addressed in detail in this paper.

The first challenge is due to the wide-ranging operating conditions of the inverter. Although designed to operate in CCM at rated power level, the inverter, in reality, would operate in a combined CCM/DCM mode, slipping into DCM operation around the zero-crossing instants of the ac cycle. Moreover, the large variation in the PV panel power would make the combined DCM/CCM operation even more complex. For instance, complete operation in DCM region alone can take place at low irradiation/power levels.

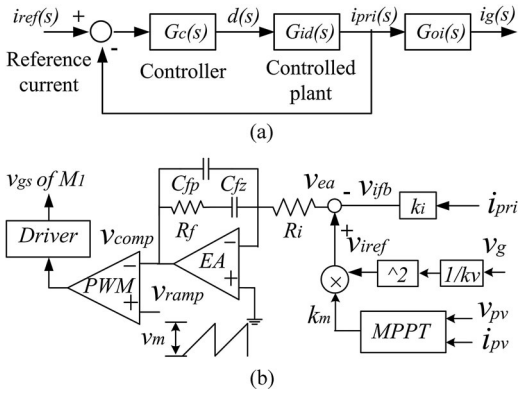


Fig. 3. Proposed indirect control of flyback CCM inverter. (a) Block schematic diagram ($G_c(s)$ includes the current sensing scale factor $k_i$, controller, and PWM gain $1/V_m$). (b) Detailed schematic diagram.

Another difficulty arises in CCM operation due to the nonminimum phase nature of the flyback inverter, which shows up as an RHP zero in the linearized small-signal control to output current transfer function. This would greatly limit the achievable system bandwidth (BW). As indicated earlier, the system operating point varies widely; this would result in large changes in the RHP zero location. A controller designed to accommodate the worst-case (minimum) RHP zero, which occurs at the peak of ac voltage under maximum load, was found to result in unacceptably low BW (even lower than 100 Hz) when the operation changes to DCM at low instantaneous ac voltages. Thus, the widely varying RHP zero in CCM operation results in poor tracking performance in the DCM operating zone, and hence, unacceptable output power quality.

In our approach [see Fig. 3(a) and (b)], this problem is avoided by sensing and controlling the primary switch current directly rather than the output current. In Fig. 3(b), the primary current reference signal's ($v_{\rm iref}$) magnitude is determined by an external MPPT scheme and its shape is determined by the sensed instantaneous grid voltage by assuming input–output power balance based on (2) in each switching cycle. As a result, the output current is controlled in an open-loop manner. The effect of the RHP zero is felt, in this case, only in the uncontrolled dynamics relating the output current to the input current.

We had applied earlier "one-cycle control" (OCC), which is a fast and large-signal nonlinear control method, for the control of the primary current in this application [15]. However, the scheme was found to suffer from bifurcation problems at low-power levels. In this paper, a simple average current mode (ACM) control [see Fig. 3(b)] has been adopted for the primary current control loop.

## IV. CONTROL STABILITY AND DESIGN

Although the PV flyback inverter is a time-varying nonlinear system, it is simplified as a time-invariant linear system by treating it to be in "quasi-steady state" around each instant of the

ac cycle. This is justified due to the relatively slower variation of the ac waveform in comparison to the switching frequency [17]. Due to the variations in output power and instantaneous grid voltage, a set of transfer functions is needed to model all possible operating conditions. The controller design must ensure that the current tracking performance is good and the closed-loop system is stable under all the different conditions.

### A. Small-Signal Modeling of Flyback Inverter

The inverter operation is assumed to be ideal and lossless for now in the modeling. This will be reconsidered in Section V while reviewing the experimental results. For a given power level$P_{\rm pv}$, the boundary grid voltage $V_{\rm gb}$ at which DCM/CCM transition occurs can be obtained by equating (4) and (5)

$$V_{\rm gb} = V_{\rm pv}\left(V_{\rm rms}\sqrt{\frac{1}{2P_{\rm pv}f_sL_m}} - n\right). \tag{15}$$

When $|V_g| < V_{\rm gb}$, the inverter works in DCM and the control-to-primary current transfer function can be shown to be

$$G_{id\_\rm DCM} = \frac{|V_g|}{V_{\rm rms}}\sqrt{\frac{2P_{\rm pv}}{L_m f_s}}. \tag{16}$$

The transfer function is a simple gain that tends toward zero as the instantaneous grid voltage $V_g$ goes toward zero.

When $|V_g| > V_{\rm gb}$, the operation is in CCM and the control-to-primary current transfer function can be shown to be

$$G_{id\_\rm CCM} = \frac{|V_g|}{nsL_m}\left(1 - \frac{s}{s_z}\right) \tag{17}$$

where

$$s_z = -\frac{V_{\rm rms}^2 \times V_{\rm pv}}{P_{\rm pv} \times nL_m \times (|V_g| + nV_{\rm pv})}. \tag{18}$$

This transfer function has a pole at origin followed by a varying left half plane (LHP) zero.

Fig. 4(a) explores the low-frequency gain (gain at $2f_{\rm ac} = 100$ Hz) and LHP zero variations over half ac cycle at four different power levels. It is observed that the gain at 100 Hz in CCM mode is only related to grid voltage, while the LHP zero varies with both power and grid voltage. Compared to the DCM case, flyback converter in CCM operation has much larger gains at 100 Hz at the cost of a smaller phase at lower frequencies. Due to these differences, the design of a single controller to accommodate both operating modes requires a careful trade-off between tracking performance in DCM operation and stability in CCM operation.

In order to simplify the controller design process, a few critical plant operating conditions are chosen as reference conditions. In CCM operation, at the transition between DCM and CCM modes, the smallest 100-Hz gain and the largest LHP zero [see Fig. 4(a)] occur together. When the power level reduces, both the gain at 100 Hz and the LHP zero reduce at the CCM/DCM transition instant, introducing a series of such "worst-case" operating points. Of these cases, the ones under the maximum and minimum power levels are used as the plant references [curves "A" and "B" in Fig. 4(b)]. All the other boundary

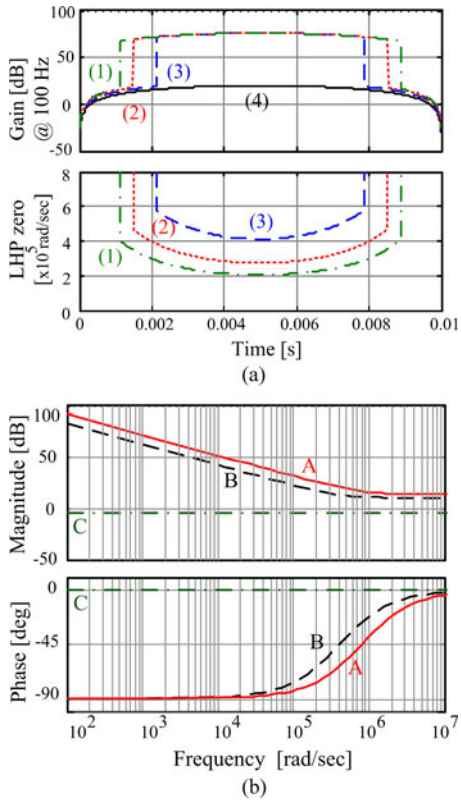


Fig. 4. Variation of plant transfer function with grid voltage and power level. (a) Variation of low-frequency gain (at $2f_{\rm ac} = 100$ Hz) and LHP zero with power level over ac half period (1) 100%, (2) 75%, (3) 50%, and (4) 25% (DCM-only with no LHP zero) of rated power $P_r$ (200 W). (b) Plant references ("A": worst case in CCM at $P_c$; "B": worst case in CCM at $P_r$; "C": DCM at $P_r$ and $V_g = 10$ V).

operating cases at other power levels are within the range defined by these two curves. The minimum power level for CCM operation is given by

$$P_c = \frac{1}{2L_m f_s} \times \frac{1}{\left(n/V_{\rm rms} + \sqrt{2}/V_{\rm pv}\right)^2}. \tag{19}$$

In DCM case, the performance [here, gain as given by (16)] becomes poorer as the grid voltage $V_g$ reduces and also as the power level $P_{\rm pv}$ decreases. There is, in fact, no way to compensate for this fully. In our design, operation at full power with a small grid voltage of 10 V is considered as a reference case, as shown in curve "C" of Fig. 4(b). Though the tracking performance will be poorer at lower voltages and lower power, the main aim is to keep the resulting overall current distortion within acceptable limits at rated power.

### B. Design of Controller

A type II compensator given by (20) is chosen for the design

$$G_C = \frac{k}{s} \times \frac{s+z}{s+p}. \tag{20}$$

This controller (curves "$G_{C1}$" and "$G_{C2}$" in Fig. 5) is essentially a PI controller together with a single-pole filter for the averaging of the current waveform. The integrator increases the

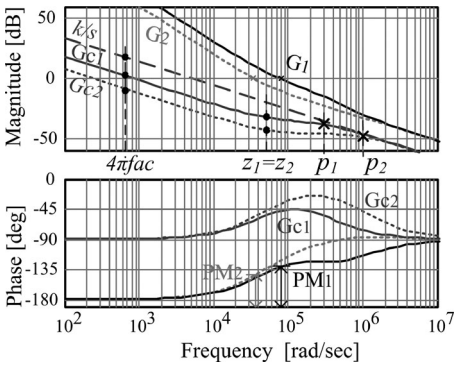


Fig. 5. Illustration of controller design ($k/s$, $G_{C1}$, and $G_{C2}$ with different pole values) and their open-loop Bode plots ($G_1$ and $G_2$ for plant reference "B").

low-frequency gain and the system BW in DCM (curve "C" in Fig. 4). However, as indicated by curves "A" and "B" in Fig. 4, a pole already exists at origin for the flyback in CCM mode. Together with the controller's integrator, this creates a total phase change of $-180^\circ$ in the open-loop response at low frequencies. Therefore, in order to provide an adequate phase margin at crossover frequency in CCM, the zero is needed in the compensator, followed by a pole for filtering the high-frequency switching components.

### C. Design Procedure

The controller is first designed to ensure the stability in CCM; its performance in DCM is then verified. Also, in Fig. 5, the poles $p_1$ and $p_2$ have been located so as to make the design ideas visually clearer; they do not correspond to the actual designed controller.

*1) Choice of k:* A high $k$ value (see Fig. 5) is desired to ensure a high gain at twice the line frequency ($2f_{\rm ac}$) and wide BW, especially in DCM operation. However, to prevent bifurcation, the compensator output $v_{\rm comp}$ in Fig. 3(b) needs to intersect the ramp signal $v_{\rm ramp}$ once every switching cycle. To ensure this for the primary current control of flyback converter, the upslope of $v_{\rm comp}(=k\times V_m\times I_{\rm pri})$ must be smaller than the upslope of $v_{\rm ramp}$ $(=V_m/T_s)$ [18]. Therefore, this limit can be expressed as

$$k<\frac{f_s}{I_{\rm pri}}. \tag{21}$$

Equation (21) provides an upper limit for $k$ depending on the maximum value of $I_{\rm pri}$, which occurs at the peak grid voltage and full power. A margin should be provided in the value of $k$ to account for parameter variations. A second upper limit on $k$ is imposed so as to keep the largest loop BW to be less than $f_s/2$, as required by sampling theory. In practice, the largest BW is made even less (say, less than $f_s/4$)

*2) Choice of k:* With the choice of $k$ value, the curve "$k/s$" is fixed. The zero is then placed at the worst-case crossover frequency of the loop response, assuming a controller of $k/s$ only, so as to achieve a $45^\circ$ phase margin.

TABLE III
PERFORMANCE OF THE DESIGNED SYSTEM AT SEVERAL KEY OPERATION CONDITIONS

| $P_{pv}$ (W) | $V_g$ (V) | Mode | Gain (dB) @ 100Hz | BW (kHz) | PM ($^o$) |
|---|---|---|---|---|---|
| 200 ($P_r$) | 325 | CCM | 88.2 | 23.6 | 51 |
| | 112 ($V_{gb}$) | CCM | 78.9 | 11.3 | 29 |
| | 10 | DCM | 7.78 | 0.24 | 91 |
| 51.4 ($P_c$) | 325 | CCM | 88.2 | 21.0 | 26 |
| | 325 | DCM | 32.1 | 4.44 | 104 |

*3) Choice of p:* Fig. 5 shows two controllers ("$G_{C1}$" and "$G_{C2}$") with the same zero ($z_1=z_2$) but different pole values ($p_1<p_2$); it also shows the corresponding open-loop Bode plots ("G1" and "G2") based on plant "B" (see Fig. 4). First, it may be noted that the maximum gain at $2f_{\rm ac}$ is limited by the curve $k/s$. A larger pole $p_2$ reduces the controller gain at $2f_{\rm ac}$ (see curve "$G_{C2}$") and the loop BW (see curve "$G_2$"). Although a large pole value causes a larger phase bump ("$G_2$" versus "$G_1$"), this does not necessarily lead to a larger phase margin ($\rm PM_1>PM_2$). Also, the pole should be sufficiently small (say, less than $f_s/5$) in order to filter out the switching components. On the other hand, if the pole is too close to the zero, it will deteriorate the phase boost provided by the zero. In our design, the pole $p$ is at 16 kHz, which is sufficiently low to filter the switching components, while at the same time, ensure a phase margin of $29^\circ$ at the boundary conduction condition under the rated power (see Table III).

The designed controller for the flyback CCM inverter is

$$G_C=\frac{5000}{s}\times\frac{s+5\times10^4}{s+10^5}. \tag{22}$$

The controller in (22) can be implemented by the compensation circuit in Fig. 3(b), where $k_i=0.47$, $V_m=3$ V, $R_i=3.9$ kΩ, $R_f=2.2$ kΩ, and $C_{fz}=C_{fp}=8.6$ nF.

The performance of the controller in (22) has been analytically verified at a few quasi-steady-state operating points (see Table III). Here, $P_r$ is the rated power and $P_c$ is the critical power given by (19). Voltage $V_{\rm gb}$ refers to the grid voltage at the CCM/DCM boundary operation. The largest loop BW, which occurs at rated power and maximum grid voltage, is below $f_s/4$ as discussed before. The phase margins show the system to be stable in all the cases considered. The BW and the $2f_{\rm ac}$ gain are both generally high in CCM and DCM at higher voltages. Even at a low grid voltage of 10 V in DCM operation, the system has a reasonable BW and $2f_{\rm ac}$ gain.

## V. IMPLEMENTATION AND EXPERIMENTAL RESULTS

Two experimental inverters, one based on the proposed scheme and the other on the benchmark flyback DCM inverter scheme [11], have been built for a Kyocera's 200-W PV module (KC200GT). Based on (4), the duty cycle of the flyback DCM inverter is directly controlled to follow the rectified grid voltage that results in the output current tracking the sinusoidal grid waveform automatically in an open-loop manner. The circuit parameters (see Fig. 1) and the operating conditions are listed

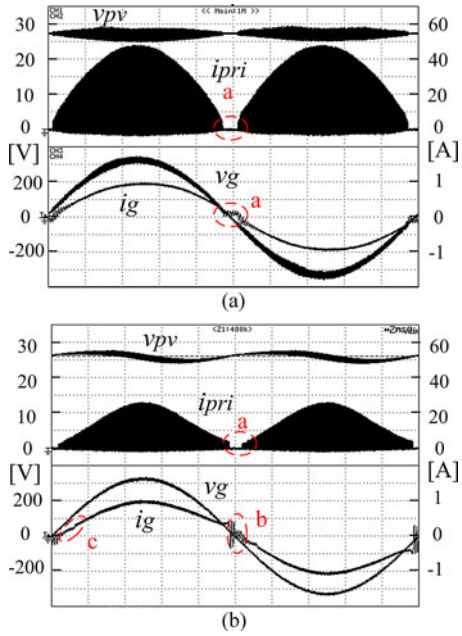


Fig. 6. PV side and grid side waveforms with $V_{\rm pv} = 27$ V and $P_{\rm pv} = 200$ W. (a) DCM scheme. (b) Proposed CCM–ACM scheme.

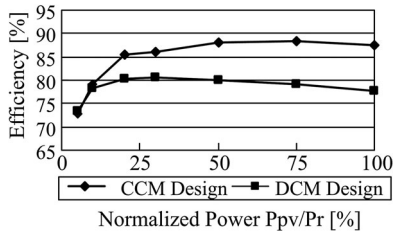


Fig. 7. Efficiency versus normalized power (referred to rated power of 200 W) for the DCM and CCM scheme.

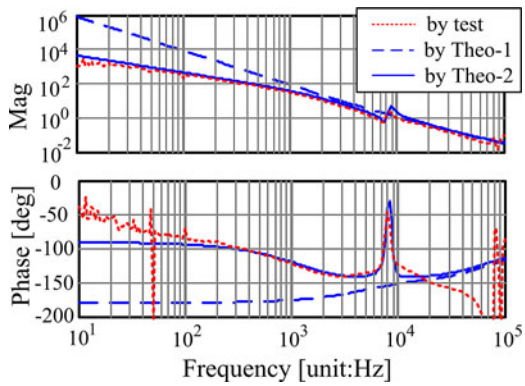


Fig. 8. Open-loop Bode plots verification at $P_r$ (200 W) and $V_{\rm gb}$ (112 V); $R_w = 0.25\ \Omega$ in Theo-2.

in Table II. Both schemes were tested at a fixed input voltage of 27 V and under different input power levels according to [14].

In order to sense the current accurately, a current transformer (CT)-based technique proposed in [19] was adopted and modified for the ac application. Here, the primary side current waveshape is reconstructed on the CT secondary side by restoring the dc component (and any line-frequency-related component) removed by the CT operation.

### A. Steady-State Operation

Fig. 6 shows the input and output waveforms of the proposed flyback CCM scheme and also the benchmark scheme at rated power. As expected, the peak primary current stress in the CCM scheme (25 A) is around half of that in the DCM scheme (48 A), which agrees with the calculated values in Table II.

In Fig. 6, distortion of current waveforms ($i_g$) in both DCM-only and CCM schemes may be noted around the zero-crossing intervals. This is partly caused by a dead time (a) when the ac current goes through zero and the secondary side operation switches from S1 to S2 and vice versa. Another reason is due to the inability of the pulsewidth modulation (PWM) IC (SG3524 here) to reach very low duty cycle values. Besides, in CCM, because of the tracking delay of the controller as well as the incomplete demagnetization of the flyback transformer, the secondary side current in Fig. 6(b) does not fall to zero during switching between S1 and S2, which makes the output current experience a sudden change, thereby causing oscillation (b) at the output filter resonant frequency.

Additionally, when the operation switches between DCM and CCM, the tracking capability of the controller changes, which is reflected as a distortion (c) in the output current waveform $i_g$.

At rated power, the total harmonic distortion (THD) is 4.1% for the DCM scheme and 4.4% for the CCM scheme, while the PF is 0.995 and 0.991, respectively. Both the schemes satisfy the requirements of IEC61727 [20] in this regard.

Fig. 7 shows the marked improvement in the efficiency achieved with the proposed CCM scheme over the benchmark DCM scheme. The weighted efficiencies for the solar powered inverter, i.e., European efficiency and California efficiency [14], were found to be 86.3% and 87.4%, respectively for the CCM scheme and 79.4% and 79.4% for the DCM scheme. Thus, the proposed CCM approach results in significantly higher efficiencies while still maintaining output current distortion within limits.

### B. Stability and Tracking Performance

The low-current THD (<5% as required) verifies that the scheme has satisfactory tracking performance. The current waveform in Fig. 8 also visually shows that the tracking performance is reasonable and the system is stable in all the quasi-steady-state operating points.

It must be noted that the stability of the flyback inverter in DCM is not an issue when the system is already stable in CCM, as the open-loop phase margin in DCM of 90° is larger than that of the CCM case (refer to Figs. 4(b) and 5). The stability test of the inverter under CCM operation was carried out by measuring the open-loop gain under several dc to dc operating conditions (input voltage, output voltage, and current). These conditions were set to correspond to different quasi-steady-state conditions at different power levels. However, the Bode plots of the inverter corresponding to instantaneous power transfer above the rated

power, e.g., $V_g > 2V_{\rm rms}$ at $P_r$, could not be measured due to the higher power burden involved.

One of these test results is shown in Fig. 8, which compares the theoretical and experimental open-loop Bode plots of the system in CCM operation near the boundary conduction condition at rated power.

In Fig. 8, the theoretical modeling given by (17)–(18) (Theo-1) and the experimental results show important differences. The pole at origin has shifted, instead, to a low frequency, which is attributed to the presence of the primary winding resistance $R_w$ of the flyback transformer. Also, the influence of the output filter causes a notch around the resonant frequency of 7 kHz. The modified theoretical model (Theo-2) after inclusion of these effects can be shown to be[1]

$$G_{id2\_\rm CCM} = \frac{s^3 L_f C_f L_m I_{Lm} + s^2 L_f C_f k_a + s I_{Lm}\left(L_f(1-D)/n^2 + L_m\right) + k_a}{s^3 L_f C_f L_m + s^2 L_f C_f R_w + s\left(L_f(1-D)^2/n^2 + L_m\right) + R_w} \tag{23}$$

where $k_a = V_g/n + R_w I_{Lm}$ and $I_{Lm} = I_{\rm pri} + nI_g$ is the flyback transformer magnetizing current at a certain quasi-steady state. The value of $R_w$ was measured to be 0.25 Ω.

The plot of "Theo-2" agrees better with the experimental results. As the filter resonant frequency is very close to the crossover frequency, multiple gain crossovers occur both in Theo-2 and the test curve. The experimental BW of the loop gain (the first crossover) is 6050 Hz, close to the estimated 6650 Hz BW, while the smaller of the two phase margins is 47° (during the first crossover), which is higher than the estimated value of 38.3° using Theo-2.

In addition, the frequency response tests have also been carried out at selected power levels over the set of worst-case conditions defined in Fig. 4(b) (between $P_c$and $P_r$). Here also, the experimental results confirm the theoretical modeling and stability of the system.

## VI. Discussion of the Proposed Scheme

A significant efficiency improvement (8%) has been achieved with the flyback CCM approach. The resulting weighted efficiency of 87.4%, though less than some industry values, still forms a good basis for further efficiency improvement. For example, by adopting nondissipative snubber circuit, interleaving [21], or soft switching techniques [21]–[23], we can expect significant improvements in efficiency at rated power level. Likewise, by adopting burst mode operation [24] or pulse frequency modulation at light load, higher efficiency can be achieved at low-power levels. Through such modifications, it will be possible to obtain higher overall efficiencies (California efficiency or European efficiency).

The higher efficiency of the proposed scheme has been achieved at the cost of higher distortion in the current waveform. However, the current THD value is still below 5% as required by the standards [20]. It has also been demonstrated that the designed system is stable at varying operation conditions.

A major concern in single-stage inverters is the requirement of a large-value input electrolytic capacitor that generally has a short lifetime [1] due to the high operating temperature of the ac module behind the PV module exposed to the sun. The problem exists in both the popular DCM scheme and the proposed CCM scheme.

By proper thermal design, it is possible to extend the lifetime of the capacitor significantly. For example, in [25], four 2200-mF electrolytic capacitors with a rated lifetime of 8000 h at 105 °C are used in parallel. According to [25], by ensuring the core capacitor temperature to be below 65 °C in the inverter design, a capacitor lifetime of 30 years can be realized.

Alternatively, a power decoupling circuit [26]–[28], such as the active filter in [28], can be added to lessen the impact due to the large electrolytic capacitor. The addition of the power decoupling circuit can be expected to reduce the efficiency somewhat.

## VII. Conclusion

This paper has proposed and demonstrated that the flyback CCM scheme can be a viable solution for medium-power ac module application. Design issues, both for the power scheme and the control scheme, have been identified and trade-offs investigated. The results presented show an improvement of 8% in California efficiency compared to the benchmark DCM scheme for a 200-W PV module application. The output power quality at rated power level is satisfactory and is capable of meeting IEC61727 [20] requirements. The stability of the flyback inverter in CCM has been verified at selected working conditions.

[1]The authors will be happy to provide the derivation upon request to an interested reader.

## References


[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[2] R. H. Wills, F. E. Hall, S. J. Strong, and J. H. Wohlgemuth, "The AC photovoltaic module," in *Proc. 25th IEEE Photovolt. Spec. Conf.*, 1996, pp. 1231–1234.

[3] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless photovoltaic inverters connected to the grid," in *Proc. 22nd Annu. IEEE Appl. Power Electron. Conf. (APEC)*, 2007, pp. 1733–1737.

[4] B. Burger and D. Kranzer, "Extreme high efficiency PV-power converters," in *Proc. 13th Eur. Conf. Power Electron. Appl. (EPE)*, 2009, pp. 1–13.

[5] U. Boeke and H. van der Broeck, "Transformer-less converter concept for a grid-connection of thin-film photovoltaic modules," in *Proc. IEEE Ind. Appl. Soc. Annu. Meet. (IAS)*, pp. 1–8.

[6] W. Yu, J. S. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic non-isolated AC module applications," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1253–1260, Apr. 2011.

[7] H. Patel and V. Agarwal, "A single-stage single-phase transformer-less doubly grounded grid-connected PV interface," *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 93–101, Mar. 2009.

[8] S. V. Araujo, P. Zacharias, and B. Sahan, "Novel grid-connected non-isolated converters for photovoltaic systems with grounded generator," in *Proc.IEEE Power Electron. Spec. Conf. (PESC)*, 2008, pp. 58–65.

[9] O. Abdel-Rahim, M. Orabi, and M. E. Ahmed, "Development of high-gain high-efficiency grid-connected inverter for PV Module," in *Proc. 2nd IEEE Int. Symp. Power Electron. Distrib. Generat. Syst. (PEDG)*, 2010, pp. 368–373.

[10] C. Rodriguez and G. A. J. Amaratunga, "Long-lifetime power inverter for photovoltaic AC modules," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2593–2601, Jul. 2008.

[11] N. P. Papanikolaou, E. C. Tatakis, A. Critsis, and D. Klimis, "Simplified high frequency converter in decentralized grid-connected PV systems: A novel low-cost solution," in *Proc. EPE'03*, Toulouse, France, 2003, CD-ROM.
[12] Y.-H. Ji, D.-Y. Jung, J.-H. Kim, C.-Y. Won, and D.-S. Oh, "Dual mode switching strategy of flyback inverter for photovoltaic AC modules," in *Proc. Int. Power Electron. Conf. (IPEC)*, 2010, pp. 2924–2929.
[13] A. C. Kyritsis, E. C. Tatakis, and N. P. Papanikolaou, "Optimum design of the current-source flyback inverter for decentralized grid-connected photovoltaic systems," *IEEE Trans. Energy Convers.*, vol. 23, no. 1, pp. 281–293, Mar. 2008.
[14] C. E. Commission. (Feb. 2009). *Emerging Renewables Program Guidebook* (9th ed.) [Online]. Available: http://www.energy.ca.gov/
[15] L. Yanlin and R. Oruganti, "A flyback-CCM inverter scheme for photovoltaic AC module application," in *Proc. Australasian Univ. Power Eng. Conf. (AUPEC)*, 2008, pp. 1–6.
[16] T. Shimizu, K. Wada, and N. Nakamura, "A flyback-type single phase utility interactive inverter with low-frequency ripple current reduction on the DC input for an AC photovoltaic module system," in *Proc. IEEE 33rd Annu. Power Electron. Spec. Conf. (PESC)*, 2002, vol. 3, pp. 1483–1488.
[17] D. M. Robert and W. Erickson, *Fundamentals of Power Electronics*, 2nd ed. New York: Springer-Verlag, Jan. 2001.
[18] L. Dixon, "Average current mode control of switching power supplies," Unitrode Application Note U-140, 1990.
[19] H. Marecar and R. Oruganti, "Fast and accurate current sensing in a multiphase buck converter," in *Proc. Int. Conf. Power Electron. Drives Syst.*, 2005, pp. 166–171.
[20] *Photovoltaic (PV) Systems—Characteristics of the Utility Interface*, IEC 61727, 2004.
[21] M. Fornage, "Method and apparatus for improved burst mode during power conversion," U.S. Patent US20100091532A1, Apr. 15, 2010.
[22] N. Kasa, T. Iida, and A. K. S. Bhat, "Zero-voltage transition flyback inverter for small scale photovoltaic power system," in *Proc. IEEE 36th Power Electron. Spec. Conf. (PESC 2005)*, pp. 2098–2103.
[23] S. Chandhaket, K. Ogura, M. Nakaoka, and Y. Konishi, "High-frequency flyback transformer linked utility-connected sinewave soft-switching power conditioner using a switched capacitor snubber," in *Proc. 4th Int. Power Electron. Motion Control Conf. (IPEMC)*, 2004, vol. 3, pp. 1242–1247.
[24] M. Fornage, "Method and apparatus for converting direct current to alternating current," U.S. Patent US20070221267, 2007.
[25] J. S. Shaffer. (2009). Evaluation of Electrolytic Capacitor Application in Enphase Microinverters. [Online]. Available: http://enphase.com/support/downloads/
[26] T. Hirao, T. Shimizu, M. Ishikawa, K. Yasui, "A modified modulation control of a single-phase inverter with enhanced power decoupling for a photovoltaic AC module," in *Proc. Eur. Conf. Power Electron. Appl.*, 2005, 10 pp.–P.10.
[27] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the DC input for an AC photovoltaic module system," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, Sep. 2006.
[28] A. C. Kyritsis, N. P. Papanicolaou, and E. C. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected AC-PV modules," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.

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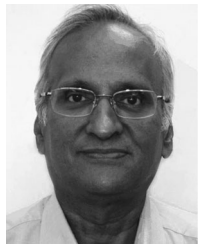

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