A Motor-Friendly Quasi-Resonant DC-Link Inverter With Lossless Variable Zero-Voltage Duration

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***Abstract*—Two quasi-resonant dc-link (QRDCL) inverter topologies are discussed for motor-friendly application. For the control of an inverter, a modified space-vector pulsewidth modulation is implemented, which requires only two resonant cycles per switching period and helps in better utilization of dc-link voltage. The first topology is tested experimentally with a 34-m-long cable connected between inverter and induction machine for reduced voltage overshoot at motor-side cable end and common-mode (CM) voltage. Even though results are satisfying, a freewheeling interval of this topology produces high losses. So a new motor-friendly QRDCL inverter with lossless variable zero-voltage duration is proposed. In this topology, during a zero-voltage interval, energy is stored in a capacitor rather than an inductor. No current is freewheeling through inverter switches, and it clearly helps in reducing the losses under a low-modulation index region. Simulation results are presented to verify the validity of the proposed inverter and its motor-friendly characteristics.**

***Index Terms*—Common-mode voltage, quasi-resonant dc-link inverter, voltage gradient, zero-voltage switching.**

I. Introduction

A HIGH-SWITCHING frequency in pulsewidth modulation (PWM) converters reduces the size and weight of passive components and hence reduces the cost as well as weight of power converters. In hard-switched power converters, switching losses limit the applicable switching frequency. Switching with large dv/dt reduces the switching losses. On the other hand, bigger voltage gradients combined with long feeders lead to high-frequency (HF) parasitic effects, like overvoltages at motor terminals, high common-mode ground current, bearing currents, etc.

The effects of using fast switching semiconductors with long cables are reported in the literature [1], [2]. Voltage reflections are produced due to the impedance mismatch between cable and motor. PWM waves traveling on long cable between inverter and motor behave like traveling waves on transmission line [1]. They produce HF oscillations and overvoltages at motor terminals [1]. The ringing voltage at the motor terminals, due to high dv/dt and motor cable, causes HF noise [3]. HF noise is also caused by the common-mode (CM) voltage between phases and ground, and switching of the semiconductors [5]. The bearing currents due to the fast-switching insulated gate bipolar transistor (IGBTs) are reported in [6]. The bearing currents depend upon the size of the motor, rate of the rise of the CM voltage, and level of the CM voltage.

The common solution for mitigating HF parasitic effects is the use of output filters [2]–[5], [7]. Dv/dt filters increase the rise and fall time of the voltages and there by voltage peaks are reduced. This filter does not reduce the CM voltage and so the bearing stress is not eliminated [4]. With sine-wave electromagnetic compatibility (EMC) filters, the motor is fed by a sinusoidal phase voltage [5]. These filters completely eliminate the bearing damage. Because of high inductor L and capacitor C, these filters have a poor dynamic characteristic and cannot be used universally [4]. The other solutions used in the literature to mitigate HF parasitic effects are use of damping circuits [7], matching the cable and motor input impedance [8], better winding insulations, modified modulation techniques for CM voltage reduction [9], soft gate drive techniques, etc. The resonant converters can also provide solutions for reducing the voltage gradients [10].

In the literature [11]–[22], the increased efficiency can be achieved with resonant converters. The resonant circuits are a combination of passive elements or passive and active elements. But the main operating principle of these converters is to bring a low voltage across and/or low current through semiconductor devices during a switching status change. Thereby, switching losses in resonant converters are reduced. The rising and falling of voltage and currents can also be controlled to reduce the ringing effects.

For resonant dc-link converters, resonant circuit is located near to the dc-link side. The problem with some resonant dc-link converters is that PWM cannot be used. In this case, the switching instants are determined by a resonant circuit [11], [12]. For some resonant dc-link converters, resonant circuit is not continuously oscillating. Whenever a switching is needed, the resonant circuit is initiated by active components. These converters are called quasi-resonant dc-link converters and are capable of PWM [13]–[22]. For motor-friendly inverter application, this type of inverters is suitable due to the voltage spectrum. A method to reduce the CM voltage in quasi-resonant dc-link (QRDCL) inverters is proposed in [23]. This method of CM voltage reduction is possible only when the inverter is completely separated from dc-link voltage. The quasi-resonant circuit must also provide variable zero-voltage duration.

The QRDCL inverters in [13]–[17] use more than two auxiliary switches. The circuit presented in [19] requires a large

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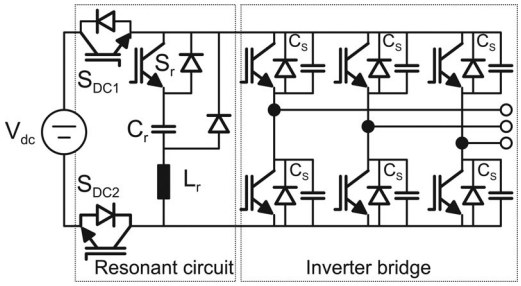

Fig. 1. Circuit diagram of a quasi-resonant dc-link inverter.

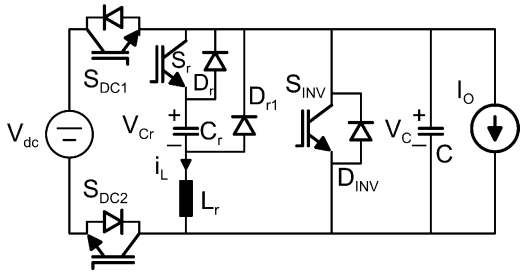

Fig. 2. Simplified circuit of a resonant inverter during the switching period.

capacitor for resonant operation, which keeps a nearly constant voltage during a resonant cycle and energy of the resonant circuit is not zero for the steady state. The resonant circuit presented in [20] needs only two additional switches and makes all the switches in the power inverter operate with zero switching losses. The energy of the resonant circuit is zero in the steady state. For a motor-friendly application, this circuit is investigated in [23]–[26].

A modified PWM is applied to the inverter [25]. This modulation strategy together with the resonant circuit reduces the CM voltage and utilizes the maximum of available modulation index. In a resonant cycle's zero-voltage duration, the resonant inductor current of a circuit [25] freewheels through a diode and inverter switches, respectively. So a considerable part of stored energy in the inductor is wasted as conduction losses [26]. A QRDCL inverter with lossless variable zero-voltage duration is proposed in this paper. This circuit provides soft switching, capable of PWM operation, *dv*/*dt* limitation, reduced CM voltage, and lossless variable zero-voltage duration in a resonant cycle.

II. QRDCL Inverter With Variable Zero-Voltage Duration

A. Resonant Circuit (T1)

The quasi resonant dc-link circuit in [20] is presented in Fig. 1 with an additional switch S_{DC2}. The reduction of CM voltage is proposed by inserting this switch S_{DC2} and completely separating the inverter from dc-link during zero-voltage period in [23]. This inverter will be further called as topology "T1."

For a switching period, the simplified equivalent circuit is shown in Fig. 2. The related operational waveforms are shown in Fig. 3 and different operating modes are in Fig. 4. The six switches of the bridge are represented by a single switch S_{INV} for the purpose of analysis. The equivalent current source I_O represents the inverter's dc-link current, whose value and direction depend on the individual phase currents and the status of inverter switches [13]. The equivalent capacitance C is equal to $3C_S$.

The circuit operation is discussed in [20] and [25] is repeated shortly here in order to understand the extended zero-voltage interval. The resonant cycle starts with the turn-ON of the switch S_r (M1). The resonant current i_L equals zero prior to turn-on of S_r. As soon as the current i_L reaches the turn-OFF current I_{Tp1}, the switches S_{DC1} and S_{DC2} are turned OFF under zero-voltage

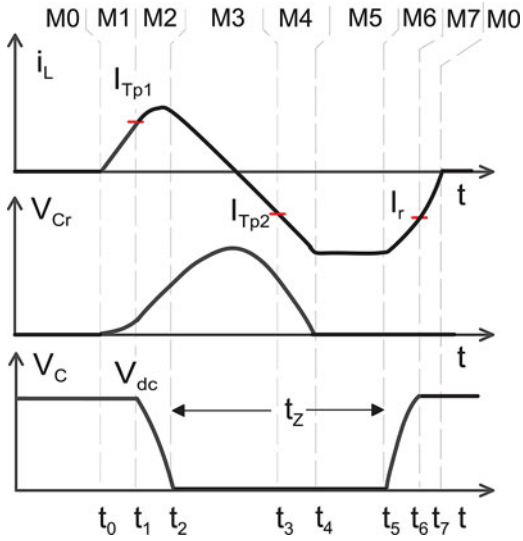

Fig. 3. Typical waveforms.

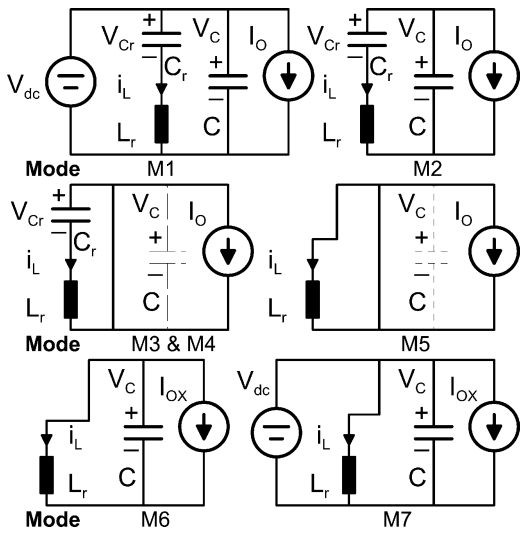

Fig. 4. Operating modes during a resonant cycle.

switching (ZVS) conditions (M2). At this moment starts the resonance between L_r, C_r, and C, which yields a zero-voltage condition on the inverter bridge. At ZVS condition (M3), all six bridge switches are simultaneously turned ON. This is done to provide a path for the resonant current i_L, since eventually its direction will change. The resonance between L_r and C_r makes

the inductor current to decrease and change its direction. The inductor current i_L begins to increase in the negative direction and reaches the second turn-OFF current I_{Tp2}.

During Mode M3, zero voltage is applied to the inverter bridge. The duration of the zero-voltage period t_z can be prolonged. If we keep the switch $S_{\rm INV}$ closed further, the capacitor voltage V_{Cr} discharges to zero (M4) and the total energy is stored in the resonant inductor only. Until we open the switch $S_{\rm INV}$, the inductor current i_L free wheels through D_{r1} and the inverter switches (M5). In this way, the zero-voltage period t_z can be extended. To have low losses, the inductor with high quality factor Q is needed.

A new switch state is set at ZVS condition (M6) and the load current defined by I_O is also changed to the next load current I_{OX}, which is decided by the next states of the inverter devices. The path for the resonant current i_L through the switches is broken and instead, the resonant current begins to charge the capacitor C. The link voltage is restored to the level of the dc-link voltage (M7), where $D_{\rm DC1}$ and $D_{\rm DC2}$ become forward biased, and the excess resonant energy is transferred back to the dc-link capacitor. Now, $S_{\rm DC1}$ and $S_{\rm DC2}$ can be turned ON.

The turn-OFF currents I_{Tp1} and I_{Tp2} should be such that 1) at the end of the resonant cycle, the dc-link voltage is restored and 2) the amplitudes of the resonant current are minimized.

B. Space-Vector PWM Algorithm

The QRDCL inverter changes the switching pattern under zero-voltage condition. It is explicit that the resonant operation requires minimum time for current built-up, the resonant oscillation, zero-voltage interval, and the restoring to $V_{\rm dc}$. It imposes a condition that the PWM pulsewidths should be longer than the required minimum pulse duration.

The inverter is designed to achieve the voltage gradient of 600 V/μS, intended for low overvoltage at the end of a 30-m motor cable [24]. Longer time is needed for resonant cycle to ensure these smaller gradients. But a longer resonant cycle diminishes the active period inside a PWM period which leads to smaller possible modulation indexes. In the conventional space-vector modulation, it requires six resonant cycles per switching period T_S, resulting in poor dc-link voltage utilization. In a switching cycle T_S

$$|V_{\rm ref}|\, e^{j\varepsilon_{\rm ref}} T_s = \vec{V}_0 T_0 + \vec{V}_1 T_1 + \vec{V}_2 T_2. \tag{1}$$

The time T_0 is the on-time of a zero-voltage vector ($\vec{V}_0$ or $\vec{V}_7$). The active vectors ($\vec{V}_1$ and $\vec{V}_2$) on time durations are T_1 and T_2. During a zero-voltage vector either all the upper switches ($\vec{V}_7$) or lower switches ($\vec{V}_0$) are turned ON. The QRDCL inverter produces a shoot-through zero state, where all the upper and lower switches are turned ON (M3, M4, and M5). This zero state ($\vec{V}_{07}$) is equivalent to the normal zero-voltage vector ($\vec{V}_0$ or $\vec{V}_7$), and the inverter output voltage is zero. In order to accommodate the zero vector in a resonant cycle, the zero-voltage period t_z can be extended (see Fig. 3). Fig. 5 shows a modified space-vector modulation which requires only two resonant cycles per switching period T_S [23], [25].

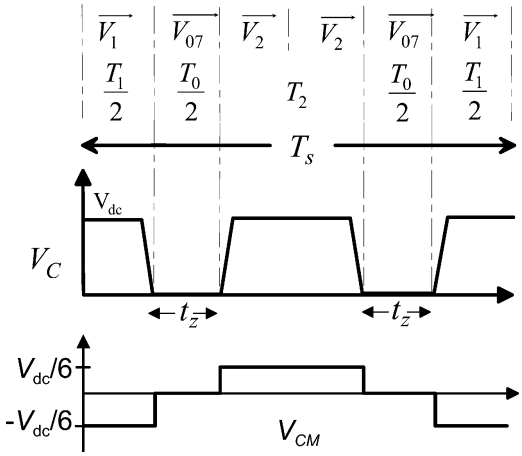

Fig. 5. Modified space-vector PWM.

The theoretical CM voltage is also shown in Fig. 5. When using only $S_{\rm DC1}$, all inverter outputs are short-circuited and connected to minus dc bus during a resonant cycle, which determines CM voltage $V_{\rm CM} = -V_{\rm dc}$ / 2. By inserting an additional switch ($S_{\rm DC2}$) to separate also minus dc-link bus, $V_{\rm CM}$ is canceled (see Fig. 5). Thus, only during PWM periods, when an active voltage vector is selected, the CM voltage will be $\pm V_{\rm dc}$ / 6.

When changing boundaries between the sector 1 and sector 2, the voltage vector pattern in (2) is implemented. When an active vector is too short, the vector dropping algorithm described in [27] is used:

$$\begin{aligned}
&\text{Sector 1:} && \vec{V}_1 \rightarrow \vec{V}_{07} \rightarrow \vec{V}_2 \rightarrow \vec{V}_{07} \rightarrow \vec{V}_1\\
&\text{Sector 1 } (\vec{V}_1 \text{ is too short):} && \vec{V}_{07} \rightarrow \vec{V}_2 \rightarrow \vec{V}_{07}\\
&\text{Sector 2 } (\vec{V}_3 \text{ is too short):} && \vec{V}_{07} \rightarrow \vec{V}_2 \rightarrow \vec{V}_{07}\\
&\text{Sector 2:} && \vec{V}_3 \rightarrow \vec{V}_{07} \rightarrow \vec{V}_2 \rightarrow \vec{V}_{07} \rightarrow \vec{V}_3.
\end{aligned} \tag{2}$$

C. Experimental Results

An experimental test was carried out. It consisted of a resonant inverter driving an induction motor. A 34-m-long LAPP shielded cable is connected between inverter and induction machine. The inverter is fed from a diode bridge rectifier. The diode bridge is connected to the 415-V, 50-Hz, three-phase power grid. The inverter is controlled by using a field-programmable gate array. The inverter is designed to achieve the maximum voltage gradient of 600 V/μs and at the same time to have low peak current and voltage stresses on the devices and thereby to reduce the losses [24]. The selected resonant circuit parameters are as follows: resonant inductor $L_r = 30\ \mu$H, resonant capacitor $C_r = 0.47\ \mu$F, and capacitor $C = 0.141\ \mu$F.

The resonant waveforms are shown in Fig. 6. The resonant waveforms for an extended zero-voltage period of a resonant cycle are shown in Fig. 7. The capacitor voltage V_{Cr} discharges to zero and total energy is stored in a resonant inductor only. The inductor current i_L free wheels through the inverter switches. Fig. 8 shows the line-to-line voltage at the inverter terminals and motor terminals. So the reduced dv/dt almost eliminates the

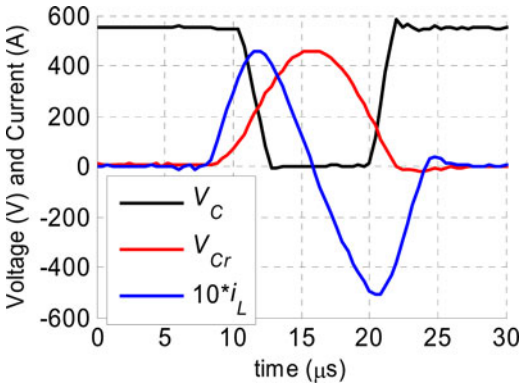

Fig. 6. Experimental result: Resonant circuit waveforms.

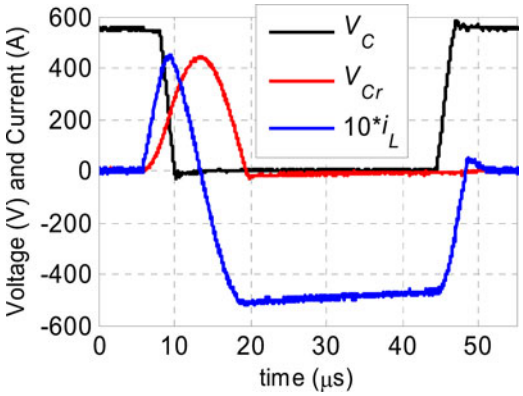

Fig. 7. Experimental result: Resonant circuit waveforms for extended zero-voltage period.

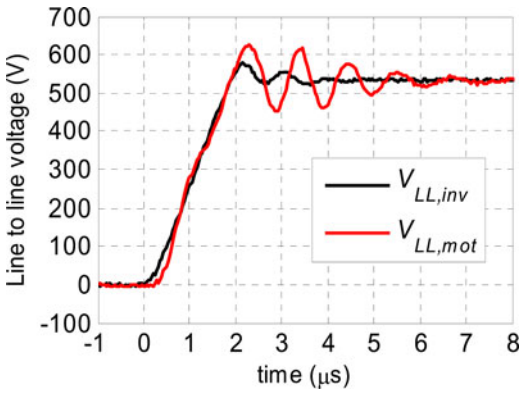

Fig. 8. Experimental result: Line-to-line voltage.

ringing effect in the long cable. The reduced voltage reflections at a motor terminal can be observed. Due to the zero-vector implementation within a resonant cycle, levels of the CM voltage are limited to within ± 100 V (see Fig. 9). The slope of the CM voltage is also reduced causing very low leakage currents.

A motor-friendly QRDCL inverter is an alternative to a hard switching (HS) inverter with a sine-wave EMC output filter [26]. The QRDCL inverter does not need an output filter. So it has good dynamics compare to an HS inverter with a sine-wave EMC output filter, and it reduces the size and cost of the system also. The efficiency of a QRDCL inverter is also an important

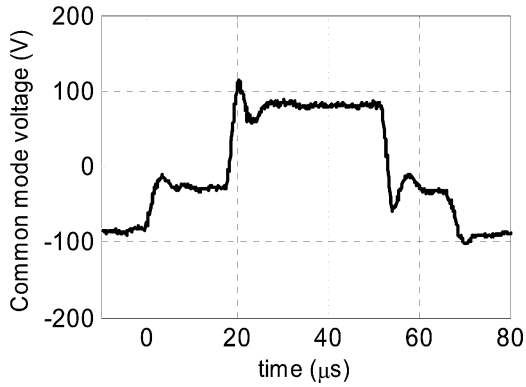

Fig. 9. Experimental result: CM voltage.

issue. The efficiency plots for various speeds and load torques are presented in [26]. It has been observed that the efficiency of a QRDCL inverter is less at low modulation index. The reason is the losses during variable zero-voltage duration of a resonant cycle. Here, the resonant cycles with longer zero-voltage durations are producing high losses in a QRDCL inverter. In order to improve the efficiency, a QRDCL inverter with a lossless variable zero-voltage duration is required.

III. Novel QRDCL Inverter With Lossless Variable Zero-Voltage Duration

A. Introduction

As discussed previously, to reduce the CM voltage level during zero-vector time, zero-vector time is included in a resonant cycle. However, it is reducing the efficiency of an inverter. In topology T1, the zero-voltage period of time is extended and the inductor current free wheels through a diode and inverter switches. The freewheeling inductor current is gradually reduced by the voltage drops of line resistance, diode and inverter switches. The considerable part of stored energy in an inductor is wasted as conduction losses. So the level of the turn-OFF current is increased, otherwise the inverter input voltage will not reach the dc-link source voltage. The increase in a turn-OFF current and freewheeling inductor current produces substantial losses in an inverter. For low modulation index, a longer zero-voltage period is needed. The losses during the freewheeling period are very high and efficiency of the inverter is reduced to a very low value. These effects are observed in [26]. So a lossless variable zero-voltage duration is necessary for high efficiency of a QRDCL inverter.

A quasi resonant dc-link inverter with lossless variable zero-voltage duration is presented in [28]. An additional switch can be added to the negative dc-link, so that complete separation of the inverter from dc-link is possible. The added lower dc-link switch can be opened only when the inductor current is zero. So, for some time during mode M3, the CM voltage is not zero, but $-V_{\rm dc}/2$. In conclusion, this circuit cannot be adopted for motor-friendly application to reduce the CM voltage. A novel QRDCL inverter with lossless variable zero-voltage duration

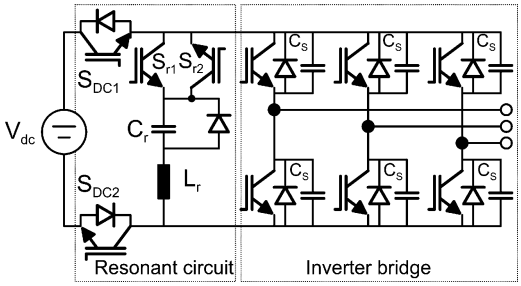

Fig. 10. Circuit diagram of proposed quasi-resonant dc-link inverter.

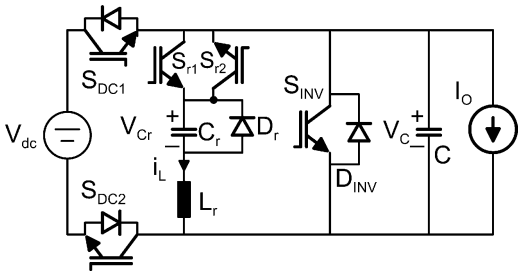

Fig. 11. Simplified circuit during a switching period.

is introduced in this section. This inverter works in a similar fashion as of topology T1 except during the zero-voltage period.

B. Resonant Circuit (T2)

Fig. 10 shows a new QRDCL inverter. It will be further called topology "T2." The lossless variable zero-voltage duration is accomplished by only controlling the switch $S_{r\,2}$. The proposed resonant circuit consists of three additional switches, passive elements L_r, C_r, and C_s. The resonant switches $S_{r\,1}$ and $S_{r\,2}$ are the reverse blocking antiparallel IGBTs. The energy of the resonant circuit is zero in the steady state. In order to analyze the QRDCL inverter, the resonant circuit different modes are discussed here. To simplify the descriptions of operations of this circuit, the assumptions given in Section II are also valid here. For a switching period, the simplified equivalent circuit is shown in Fig. 11. The related operational waveforms are shown Fig. 12 and different operating modes in Fig. 13.

The following notations are used in the subsequent equations:

$$C_{\rm sum} = C + C_r, \quad a = \frac{C_r}{C_{\rm sum}}, \quad b = \frac{C}{C_{\rm sum}}, \quad \omega_0 = \frac{1}{\sqrt{L_r C_r}}$$

$$\omega_1 = \sqrt{\frac{C + C_r}{LCC_r}}, \quad \omega_2 = \frac{1}{\sqrt{L_r C}}, \quad Z_0 = \sqrt{\frac{L_r}{C_r}},$$

$$Z_1 = \frac{1}{\omega_1 C}, \quad Z_2 = \omega_1 L, \quad Z_3 = \frac{1}{\omega_1 C_r},$$

$$Z_4 = \frac{1}{\omega_1 C_{\rm sum}}, \quad Z_5 = \sqrt{\frac{L_r}{C}}. \tag{3}$$

Mode M0 [t_0]: The resonant circuit is in the steady state. In the steady state, the resonant tank energy is zero. $S_{\rm DC1}$ and $S_{\rm DC2}$ are closed. $S_{r\,1}$ and $S_{r\,2}$ are open:

$$i_L\,(t_0) = 0 \tag{4}$$

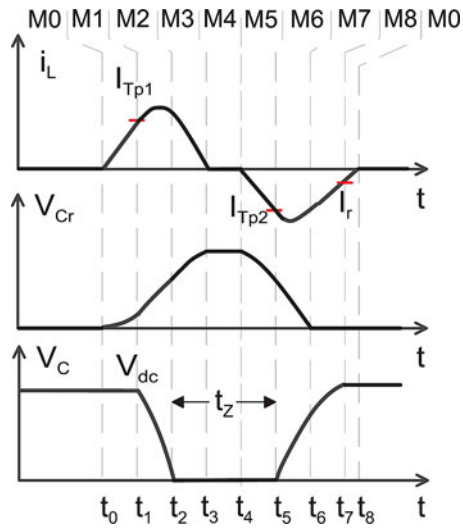

Fig. 12. Typical waveforms.

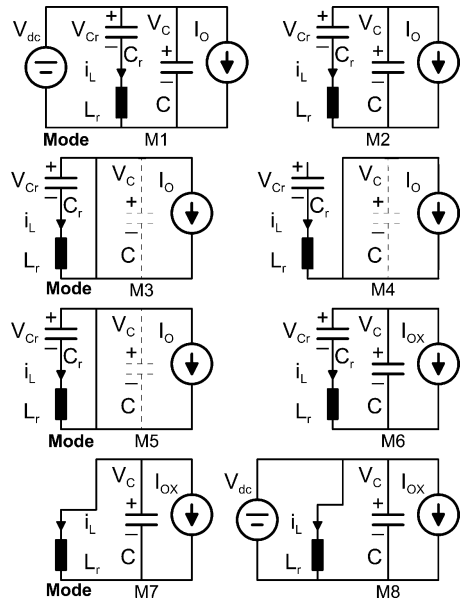

Fig. 13. Operating modes during a resonant cycle.

$$V_{Cr}\,(t_0) = 0 \tag{5}$$

$$V_C\,(t_0) = V_{\rm dc}. \tag{6}$$

Mode M1 [t_0, t_1]: When a switching in PWM inverter is needed, the switch $S_{r\,1}$ is turned ON. Then, the current i_L starts flowing through resonant elements L_r and C_r. Because the switches $S_{\rm DC1}$ and $S_{\rm DC2}$ are closed, voltage across the inverter bridge V_C remains equal to dc-link voltage $V_{\rm dc}$. The energy needed to complete a resonant cycle is stored in resonant inductor L_r and resonant capacitor C_r:

$$\theta = \omega_0\,(t - t_0)$$

$$i_L\,(t) = \frac{V_{\rm dc}}{Z_0}\sin\theta \tag{7}$$

$$V_{Cr}\,(t) = V_{\rm dc}\,(1 - \cos\theta) \tag{8}$$

$$V_C\,(t) = V_{\rm dc} \tag{9}$$

$$\text{At } t = t_1,\ i_L\,(t_1) = I_{Tp1} \ \Rightarrow\ \cos\theta = \frac{\sqrt{V_{\rm dc}^2 - (I_{Tp1}Z_0)^2}}{V_{\rm dc}} \tag{10}$$

$$\text{At } t = t_1,\ V_{Cr}\,(t_1) = V_{\rm dc} - \sqrt{V_{\rm dc}^2 - (I_{Tp1}Z_0)^2}. \tag{11}$$

Mode M2 [t_1, t_2]: When the current i_L reaches the trip current level I_{Tp1}, dc-link switches $S_{\rm DC1}$ and $S_{\rm DC2}$ are opened. Then, the inverter bridge is separated from the dc-link, and voltage V_C decreases resonantly from $V_{\rm dc}$ to zero. The voltage falling time is decided by resonant elements and load current

$$\theta = \omega_1\,(t - t_1)$$

$$i_L\,(t) = (aI_O + i_L\,(t_1))\cos\theta + \frac{V_{\rm dc} - V_{\rm Cr}\,(t_1)}{Z_2}\sin\theta - aI_O \tag{12}$$

$$V_{Cr}\,(t) = b\,(V_{Cr}\,(t_1) - V_{\rm dc})\cos\theta + Z_3\,(aI_O + i_L\,(t_1))\sin\theta + bV_{\rm dc} + aV_{\rm Cr}\,(t_1) - \frac{I_O\,(t - t_1)}{C_{\rm sum}} \tag{13}$$

$$V_C\,(t) = a\,(V_{\rm dc} - V_{Cr}\,(t_1))\cos\theta - Z_1\,(aI_O + i_L\,(t_1))\sin\theta + bV_{\rm dc} + aV_{\rm Cr}\,(t_1) - \frac{I_O\,(t - t_1)}{C_{\rm sum}} \tag{14}$$

$$\text{At } t = t_2,\ V_C\,(t_2) = 0 \Rightarrow V_{Cr}\,(t_2) = \frac{Z_2}{Z_1}\left(V_{\rm dc} - a\sqrt{V_{\rm dc}^2 - (I_{Tp1}Z_0)^2} - \frac{I_O\,(t - t_1)}{C_{\rm sum}}\right) \tag{15}$$

$$i_L\,(t_2) = \sqrt{\frac{V_{\rm dc}^2 - (I_{Tp1}Z_0)^2}{Z_2^2} + (aI_O + i_L\,(t_1))^2 - \left(\frac{V_{Cr}\,(t_2)}{Z_2}\right)^2} - aI_O. \tag{16}$$

Mode M3 [t_2, t_3]: When the dc-link voltage V_C reaches zero, all inverter switches are turned ON. In terms of the simplified equivalent circuit, $S_{\rm INV}$ is turned on under zero-voltage condition. So the voltage V_C remains zero. Due to resonance between C_r and L_r, the inductor current i_L reaches zero and voltage V_{Cr} reaches its maximum value

$$\theta = \omega_0\,(t - t_2)$$

$$i_L\,(t) = i_L\,(t_2)\cos\theta - \frac{V_{\rm Cr}\,(t_2)}{Z_0}\sin\theta \tag{17}$$

$$V_{\rm Cr}\,(t) = V_{\rm Cr}\,(t_2)\cos\theta + Z_0 i_L\,(t_2)\sin\theta \tag{18}$$

$$V_C\,(t) = 0 \tag{19}$$

$$i_L\,(t_3) = 0 \tag{20}$$

$$V_{Cr}\,(t_3) = \sqrt{(V_{Cr}\,(t_2))^2 + (Z_0 i_L\,(t_2))^2}. \tag{21}$$

Mode M4 [t_3, t_4]: The current i_L remains at zero and cannot change its direction until the switch S_{r2} is turned ON. The switch S_{r1} can be turned OFF at zero current. The duration of this mode is controllable and the switch S_{r2} can be turned ON at any time. Now, the total energy to bring the inverter input voltage to dc-link source voltage is stored in the resonant capacitor C_r. The voltage V_{Cr} is constant.

In case of topology T1, this energy is stored in a resonant inductor L_r, and the current i_L free wheels through the inverter switches and diode D_{r1}. The conduction losses occur in the inverter switches and diode D_{r1}, decreasing the efficiency of an inverter

$$i_L\,(t) = 0 \tag{22}$$

$$V_{Cr}\,(t) = V_{Cr}\,(t_3) \tag{23}$$

$$V_C\,(t) = 0. \tag{24}$$

Mode M5 [t_4, t_5]: To apply a new switching status to the inverter and to bring back the inverter voltage to dc-link voltage, the switch S_{r2} has to be turned ON. A path for current i_L is built up and capacitor C_r starts discharging. The capacitor voltage V_{Cr} decreases and the inductor current i_L increases in a reverse direction

$$\theta = \omega_0\,(t - t_4)$$

$$i_L\,(t) = i_L\,(t_3)\cos\theta - \frac{V_{Cr}\,(t_3)}{Z_0}\sin\theta \tag{25}$$

$$V_{Cr}\,(t) = V_{Cr}\,(t_3)\cos\theta + Z_0 i_L\,(t_3)\sin\theta \tag{26}$$

$$V_C\,(t) = 0 \tag{27}$$

$$i_L\,(t_5) = I_{Tp2}. \tag{28}$$

Mode M6 [t_5, t_6]: When the inductor current i_L is equal to second trip current I_{Tp2}, switch $S_{\rm INV}$ is turned OFF under zero-voltage condition, i.e., a new switching status is applied to the inverter. The capacitor voltage V_{Cr} falls to zero as a result of resonance between C, C_r, and L_r. At this point, diode D_r becomes forward biased and starts conducting, which avoids charging of the resonant capacitor in a reverse direction

$$\theta = \omega_1\,(t - t_5)$$

$$i_L\,(t) = (aI_O + i_L\,(t_5))\cos\theta - \frac{V_{Cr}\,(t_5)}{Z_2}\sin\theta - aI_{OX} \tag{29}$$

$$V_{Cr}\,(t) = bV_{Cr}\,(t_5)\cos\theta + Z_3\,(aI_O + i_L\,(t_5))\sin\theta + aV_{Cr}\,(t_5) - \frac{I_{OX}\,(t - t_5)}{C_{\rm sum}} \tag{30}$$

$$V_C\,(t) = aV_{Cr}\,(t_5)\,(1 - \cos\theta) - Z_1\,(aI_{OX} + i_L\,(t_5))\sin\theta - \frac{I_{OX}\,(t - t_5)}{C_{\rm sum}} \tag{31}$$

$$\text{At } t = t_6,\ V_{Cr}\,(t_6) = 0$$

$$V_C\,(t_6) = \frac{Z_2}{Z_3}\left(a\,V_{Cr}\,(t_5) - \frac{I_{OX}\,(t - t_5)}{C_{\rm sum}}\right) \tag{32}$$

$$i_L\,(t_6) = \sqrt{(aI_{OX} + i_L\,(t_5))^2 + \left(\frac{V_{Cr}\,(t_5)}{Z_2}\right)^2 - \left(\frac{V_C\,(t_6)}{Z_2}\right)^2} - aI_{OX}. \tag{33}$$

Mode M7 [t_6, t_7]: Due to resonance between C_r and L_r, the inverter voltage V_C reaches the dc-link source voltage $V_{\rm dc}$. Then, the switches $S_{\rm DC1}$ and $S_{\rm DC2}$ can be turned ON under zero-voltage condition

$$\theta = \omega_2 \left(t - t_6\right)$$

$$i_L(t) = \left(i_L\left(t_6\right) + I_{OX}\right)\cos\theta + \frac{V_C\left(t_6\right)}{Z_5}\sin\theta - I_{OX} \tag{34}$$

$$V_{Cr}\left(t\right) = 0 \tag{35}$$

$$V_C\left(t\right) = V_C\left(t_6\right)\cos\theta - Z_5\left(I_{OX} + i_L\left(t_6\right)\right)\sin\theta \tag{36}$$

$$\text{At } t = t_7,\ V_C\left(t_7\right) = V_{\rm dc} \Rightarrow i_L\left(t_7\right)$$

$$= -\sqrt{\left(I_{OX} + i_L\left(t_6\right)\right)^2 + \left(\frac{V_C\left(t_6\right)}{Z_5}\right)^2 - \left(\frac{V_{dc}}{Z_5}\right)^2} - I_{OX}. \tag{37}$$

Mode M8 [t_8, t_9]: In this mode, the remaining energy stored in the inductor is fed back to the dc-link. The inductor current i_L goes back to zero from a negative value

$$i_L\left(t\right) = i_L\left(t_8\right) + \frac{V_{\rm dc}}{L_r}\left(t - t_8\right) \tag{38}$$

$$V_{Cr}\left(t\right) = 0 \tag{39}$$

$$V_C\left(t\right) = V_{\rm dc}. \tag{40}$$

C. Calculation of Turn-OFF Currents

In order to successfully control the inverter, the relation between turn-OFF currents (I_{Tp1} and I_{Tp2}) and inverter bridge input currents (I_O and I_{OX}) should be calculated. The calculation of the optimal turn-OFF currents is important in order to reduce the stress on the semiconductor devices and passive elements. The resonant circuit of topology T2 operates in a similar fashion as of topology T1, except during zero-voltage period. So for the calculation of turn-OFF currents and design considerations, we can bring an analogy between topology T1 and topology T2. The first two modes and last three modes are similar in both the topologies. For these modes, in both the topologies, all the state variables (i_L, V_{Cr}, and V_C) are having the same initial and final values.

The turn-OFF currents for topology T1 are derived in [24]. If we observe the derivation, the zero-voltage period equations are not used in the calculation of turn-OFF currents. Turn-OFF currents indicate the energy stored in a resonant inductor and capacitor. A sufficient energy should be stored to bring the inverter voltage return to dc-link voltage. During zero-voltage period, this energy is stored in inductor L_r for topology T1 and in capacitor C_r for topology T2. For the calculation of turn-OFF currents, it is not important where the energy is stored. But it is important how much the energy need to be stored. So for the given resonant circuit elements and inverter input currents, the required turn-OFF currents are equal in both the topologies T1 and T2. If the switch S_{r2} is closed forever, the topology T2 works in a similar way of topology T1.

Equations (4)–(40) need to be solved for turn-OFF currents (I_{Tp1} and I_{Tp2}). An analytical solution for the turn-OFF currents turned out to be highly complicated. It is due to the complex modes and three passive elements L_r, C_r, and C. Therefore, we solved the problem in two steps: first, the solution is derived for a simpler resonant circuit which has only one instead of two capacitors, and simpler modes. The topology presented in [14] uses an inductor L_r and a capacitor C as resonant elements and operates in similar fashion as present topology (T2). Initially, the energy stored in resonant elements during mode M1 of [14] is calculated. Second, storing the same amount of energy during mode M1 of the target topology T2, allows us to calculate the turn-OFF current I_{Tp1}. In a similar way, I_{Tp2} can be found.

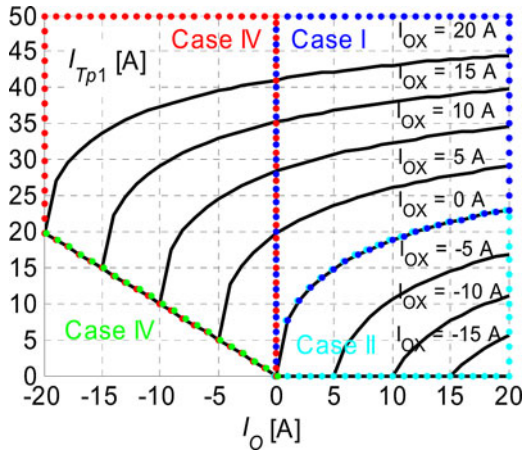

Fig. 14. Variation in turn-OFF current I_{Tp1} according to the present load current I_O and next load current I_{OX}.

Cases from I to IV are classified by the direction of load current [13]. For case I, the inverter input current before switching and also after switching is positive, i.e., I_O and I_{OX} are positive. For case I, the deriving equations for turn-OFF current I_{Tp1} are given as follows:

$$\frac{1}{2}C_r V_{Cr1}^2 + \frac{1}{2}L_r I_{Tp1}^2 = \frac{1}{2}L_r I_i^2, \quad \text{where}$$

$$I_i = \sqrt{\left(\frac{V_{\rm dc}}{Z_5} + I_O + I_{OX}\right)^2 - \left(\frac{V_{\rm dc}}{Z_5}\right)^2} - I_O. \tag{41}$$

From (10), (11), and (41), we have

$$I_{Tp1} = \sqrt{\left(\frac{V_{\rm dc}}{Z_0}\right)^2 - \left(\frac{V_{\rm dc}}{Z_0} - \frac{I_i^2 Z_0}{2V_{\rm dc}}\right)^2}. \tag{42}$$

Fig. 14 shows the relation between turn-OFF current I_{Tp1}, present load current I_O, and next load current I_{OX} for designed parameters. Fig. 15 shows the relation between the turn-OFF current I_{Tp2}, present load current I_O, and next load current I_{OX}.

D. Design Considerations

The inverter is designed to achieve the voltage gradient of 600 V/μS intended for low overvoltage at the end of a 34-m motor cable. The design specifications are given in [24]. The voltage rising mode and falling mode are similar in both the topologies T1 and T2. The current i_L reaches its positive peak current during voltage falling mode. During the zero-voltage

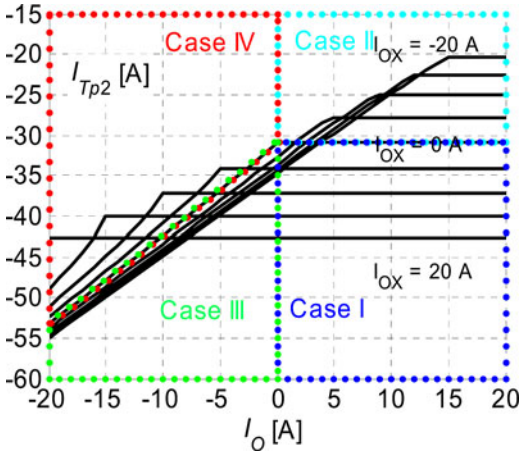

Fig. 15. Variation in turn-OFF current I_{Tp2} according to the present load current I_O and next load current I_{OX}.

period, resonant capacitor voltage reaches its peak value and remains at this value until the switch S_{r2} is turned ON. This peak current and voltage are also same in both topologies. Ultimately, the design criterion is also same for both the topologies. For the given specifications, the selected parameters are same and are as follows: resonant inductor $L_r = 30$ μH, resonant capacitor $C_r = 0.47$ μF, and capacitor $C = 0.141$ μF.

For the reduction of the CM voltage level during zero-voltage period, a complete separation of inverter and dc-link is possible with an additional switch S_{DC2}. The modulation scheme used is similar to the one discussed in Section II, [25]. As for the semiconductor devices, for dc-link switch, CoolMOS selected in [23] can be used. But for the resonant switches S_{r1} and S_{r2}, reverse blocking antiparallel IGBTs are required. The discrete reverse blocking IGBTs (RB-IGBT) commercially available are from one company IXYS and can be connected in parallel. Results of the investigation in [29] point out that RB-IGBTs have superior conduction properties, but they suffer from unduly large reverse recover losses during switching. Using state-of-the-art devices, the RB-IGBTs are an advantage at low switching frequencies and are not suitable in place of resonant switches S_{r1} and S_{r2}. An equivalent circuit for antiparallel IGBTs is given in Fig. 16. The RB-IGBTs are not necessary for this representation. The selected fourth-generation IGBTs in [23] can be used. This structure increases losses due to additional two diodes, which carry the resonant current. However, for the current state of the art, the series connected IGBT–diode pairs have much smaller overall losses for the given application. If the reverse recovery characteristics of RB-IGBT are improved, it has an advantage of low power loss and smaller size compare to the series connected IGBT-diode pair. So the proposed resonant circuit will give good benefits with the future reverse blocking anti parallel IGBTs. The diode in parallel to the capacitance C_r should have a low reverse leakage current.

E. Simulation of the Proposed Quasi-Resonant Inverter

To verify the proposed QRDCL inverter for zero-voltage switching and a lossless variable zero-voltage duration, it has

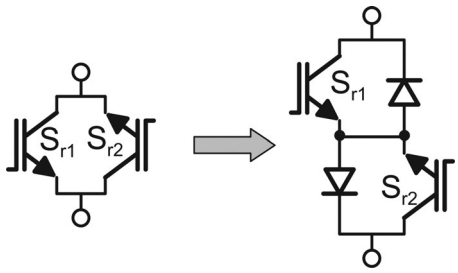

Fig. 16. Equivalent switch.

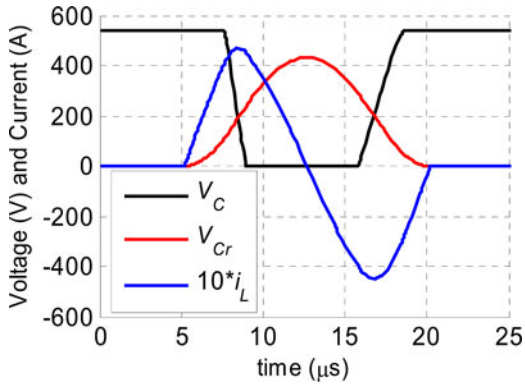

Fig. 17. Simulated resonant circuit waveforms.

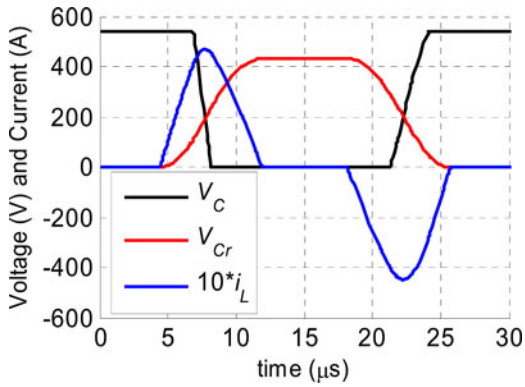

Fig. 18. Simulated waveforms for extended zero-voltage period.

been simulated in Simplorer network simulation software. In Fig. 17, the switch S_{r2} is closed with no delay. Then, the resonant circuit works in similar fashion as of topology T1 and the waveforms are akin to the presented in Fig. 6. The inverter bridge switches change their status when the inverter input voltage V_C is zero. For the designed resonant parameters, the peak capacitor voltage V_{Cr} is always less than the dc-link voltage. The resonant waveforms for extended resonant cycle are shown in Fig. 18. During zero-voltage period, the resonant capacitor voltage charged to its peak value and remained at this voltage until the switch S_{r2} is turned ON. At the same time, the inductor current i_L is zero. This zero-voltage period is controllable and continues until the switch S_{r2} is turned ON. Because the current i_L is zero, no current is freewheeling through the inverter devices. So a lossless variable zero-voltage duration can be achieved by the proposed resonant inverter. For given

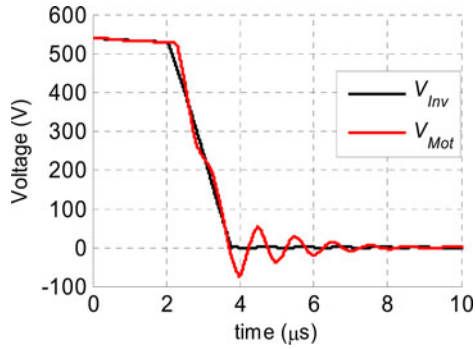

Fig. 19. Simulated overvoltage reflections.

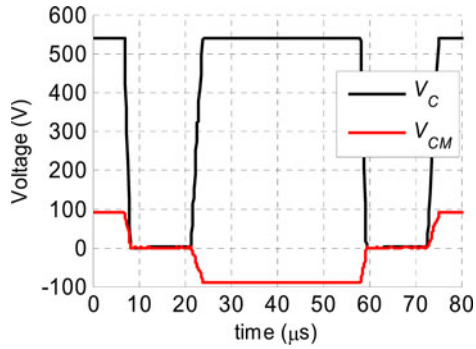

Fig. 20. Simulated common-mode voltage.

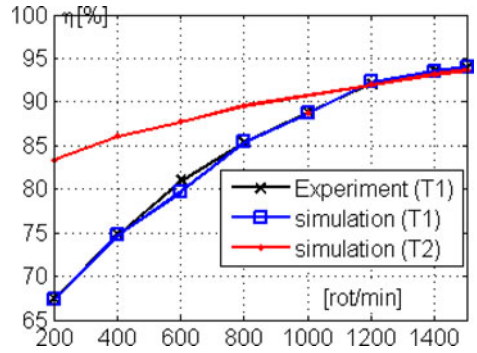

Fig. 21. Efficiency plot (Torque = 10 Nm).

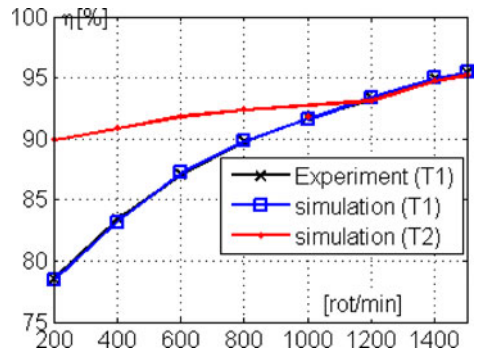

Fig. 22. Efficiency plot (Torque = 20 Nm).

operating conditions, average value of the inductor current is less in topology T2 compared to topology T1.

Motor-friendly characteristics like reduced output voltage gradients and reduced CM voltages can also be achieved by the proposed resonant inverter. The designed resonant circuit passive elements and load current decide the voltage gradient. Fig. 19 shows the waveforms of a line-to-line voltage at the inverter and motor terminals for maximum load current. The overvoltage at motor terminals remains under 17% when using a 34-m-long cable. Here, the long cable simulation model is taken from [30]. The CM voltage waveform is given in Fig. 20. The CM voltage level is reduced from $\pm V_{\rm dc}/2$ to zero. The slope of the CM voltage is also reduced.

To compare the two topologies T1 and T2, efficiencies of both QRDCL inverters are determined through simulations. Munk-Nielsen *et al*. [31] describe how to estimate power losses from simulation using ideal switches combined with measured power loss data and information from datasheets. For different speed and load torques, the input power, output power, output phase current, and inductor losses are already measured experimentally for T1. In the simulation model of topology T1, the same inductor losses are maintained for given input conditions. The semiconductor devices conduction losses are taken from data sheets. The turn-ON and turn-OFF energy losses provided in data sheets are for HS condition. All inverter bridge switches and dc-link switches ($S_{\rm DC1}$ and $S_{\rm DC2}$) are turned OFF under ZVS but not under ZCS condition. For soft-switching condition, i.e., ZVS turn-OFF or ZCS turn-ON, the switching losses are taken such that the overall simulated losses equal to the experimentally measured losses. After calculating the loss parameters for the simulation model of topology T1, the same parameters are taken for the simulation model of topology T2.

The efficiency is estimated for both the topologies and the efficiency plots are shown in Figs. 21 and 22. The efficiency of topology T2 is higher compared to T1 at low speeds. This can be attributed to the reduction of conduction losses during a resonant cycle's long zero-voltage period. At higher speeds, the efficiency of topology T2 is same as topology T1. Here, the zero-voltage period in resonant cycle is small and topology T2 works in a similar way of topology T1.

The QRDCL inverter does not need an output filter. So it has good dynamics compared to an HS inverter with a sine-wave EMC output filter, and it reduces the size, cost, and weight of the system also. Most importantly, efficiency of the proposed QRDCL inverter is nearly same as the efficiency of an HS inverter with a sine-wave EMC output filter [26].

IV. Conclusion

The QRDCL inverter is aimed for *dv*/*dt* and CM voltage reduction. A modified space-vector PWM is implemented for better utilization of dc-link voltage. For first topology, the reduction of HF parasitic effects is tested experimentally. The experimental results suggest that motor-friendly QRDCL inverter is an alternative to HS inverter with a sine-wave EMC output filter. The reduction of losses during a zero-voltage period helps in improving the efficiency of a QRDCL inverter.

For low-loss operation, a new QRDCL inverter is proposed which provides a lossless variable zero-voltage duration. The circuit operation principle is explained in detail. It is concluded

that the principal of proposed inverter topology is similar to the previous topology except during the zero-voltage period. The design considerations and calculation of turn-OFF currents are similar to the first topology. The new QRDCL inverter is verified through simulations. When the switch S_{r2} is closed forever, the circuit works in a similar way to the first topology. So it is clear that the inverter works under real conditions. The lossless variable zero-voltage duration and motor-friendly characteristics are observed from simulations. The improved efficiency is evaluated through simulations.

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