A New Single-Phase Single-Stage Three-Level Power Factor Correction AC–DC Converter

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***Abstract*—In this paper, a new three-level single-stage power-factor-corrected ac/dc converter is presented. The proposed circuit integrates the operation of a boost power factor correction converter and a three-level dc/dc converter into one converter. It does not have the problem of high component stress due to high rising intermediate bus voltages at light load conditions that other single-stage converters have because of its three-level structure. It can operate over a wider load range with significantly less output inductor current ripple; moreover, its input current has little distortion. In the paper, the operation of the new converter is explained in detail and analyzed, its steady-state characteristics are determined, and its design is discussed. Experimental results obtained from a prototype are presented to confirm the feasibility of the new converter.**

***Index Terms*—AC–DC power conversion, single-stage power factor correction (SSPFC), three level converters.**

I. Introduction

POWER factor correction (PFC) is necessary nowadays for an ac-dc power supply to comply with harmonic standards such as IEC 1000-3-2 [1]. Although it is possible to satisfy these standards by adding passive filter elements to the traditional passive diode rectifier/LC filter input combination, the resulting converter would be very bulky and heavy due to the size of the low-frequency inductors and capacitors [2] [Fig. 1(a)]. For conventional two-stage ac–dc converters with output isolation where an ac–dc conversion (rectifying) stage and an isolated dc–dc conversion stage are used, an ac-dc boost converter is used in the rectifying stage for most applications. The boost converter shapes the input line current so that it is almost sinusoidal, with a harmonic content compliant with agency standards, but the cost and complexity of the overall two-stage converter are increased because an additional switching converter must be implemented [2]. This has led to the emergence of single-stage power-factor-corrected (SSPFC) converters.

There have been numerous publications about SSPFC converters, particularly for low-power ac–dc flyback and forward converters [1]–[16]. These cheaper and simpler converters are widely used in industry and their properties and characteristics have been well established. Research on the topic of higher power ac–dc single-stage full-bridge converters, however, has proved to be more challenging, and, thus there have been much fewer publications [17]–[19].

Previously proposed single-stage ac–dc full-bridge converters have the following drawbacks [Fig. 1(b)–(f)]:

1) Some are current-fed converters with a boost inductor connected to the input of the full-bridge circuit. Although they can achieve a near-unity input power factor, they lack an energy-storage capacitor across the primary-side dc bus, which can result in the appearance of high voltage overshoots and ringing across the dc bus. It also causes the output voltage to have a large low-frequency 120-Hz ripple that limits their applications.
2) Some are resonant converters [17], [20], [21] that must be controlled using varying switching-frequency control, which makes it difficult to optimize their design (especially their magnetic components) as they must be able to operate over a wide range of switching frequency.
3) Some converters have two converters stages [22] that allow for a portion of the power that is transferred from the input to the output to be processed only once. It is for this reason that they are considered by some to be single-stage converter, but the fact is they have two converter stages and thus have the cost and complexity associated with two-stage converters.
4) Most are voltage-fed, single-stage, pulse-width modulation (PWM) converters with a large energy-storage capacitor connected across their primary-side dc bus. These converters do not have the drawbacks of resonant and current-fed SSPFC converters. They operate with fixed switching frequency, and the bus capacitor prevents voltage overshoots and ringing from appearing across the dc bus and the 120-Hz ac component from appearing at the output. Voltage-fed converters, however, have the following drawbacks:
    a) The primary-side dc bus voltage of the converter may become excessive under high-input-line and low-output-load conditions. This is because SSPFC converters are implemented with just a single controller to control the output voltage, and the dc bus voltage left unregulated; it is dependent on the converter's input line and output load operating conditions and component values. The high dc bus voltage results in the need for higher voltage rated devices and very large bulk capacitors for the dc bus. For example, the converter in [19] has a dc bus voltage of 600 V [2], [17]–[19], [21].
    b) The input power factor of a single-stage voltage-fed converter is not as high as that of current-fed

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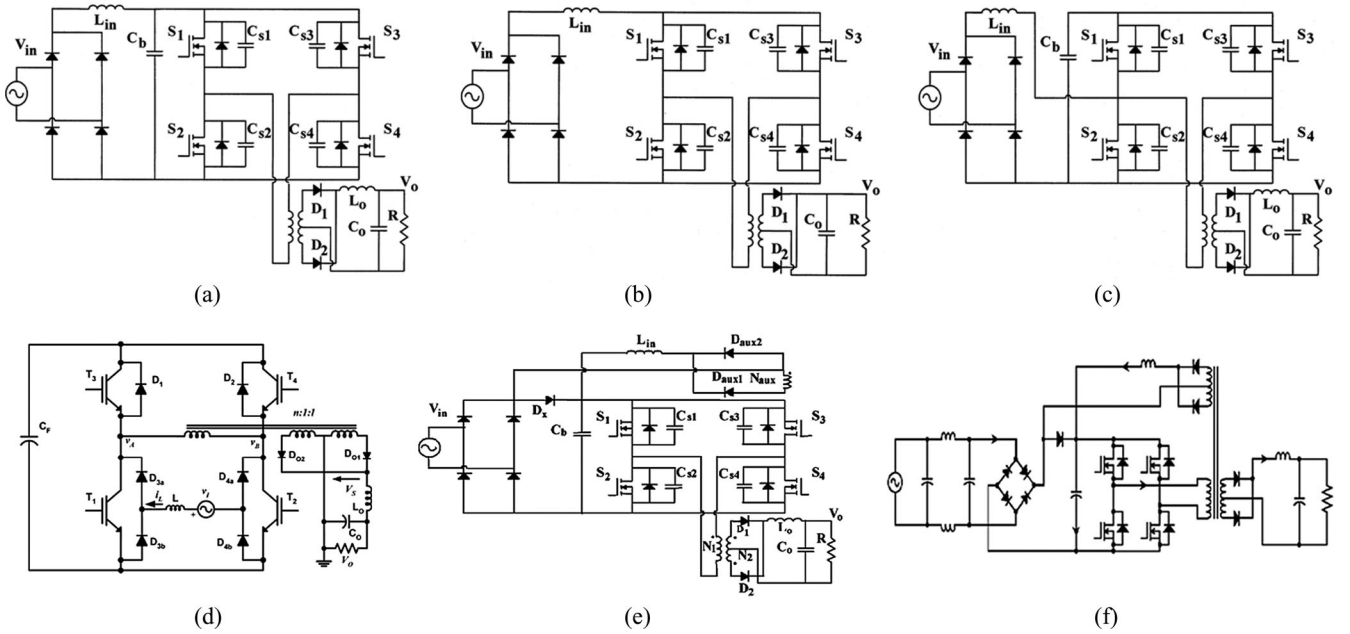

Fig. 1. Various power factor correction ac–dc full-bridge converters. (a) Two-stage ac–dc PWM converter with diode rectifier/*LC* filter front. (b) Boost-based current-fed ac–dc PWM integrated full-bridge converter [2]. (c) Voltage-fed PWM full-bridge converter [2]. (d) Voltage-fed PWM full-bridge converter [31]. (e) Voltage-fed PWM full-bridge converter with auxiliary winding [18]. (f) Voltage-fed PWM full-bridge converter with auxiliary winding [18], [19].

converters. For example, the converter proposed in [18] has an input current that is neither continuous nor discontinuous, but is "semicontinuous" with a considerable amount of distortion.

c) The converter is made to operate with an output inductor current that is discontinuous for all operation conditions, to try to prevent the dc bus voltage from becoming excessive; output inductor current and dc bus voltage are related, as shown in [21]. Doing so results in the need for components that can handle high peak currents, and additional output filtering to remove ripple.

Multilevel converters have been proposed to try to reduce the peak voltage stresses of the converter devices [23]–[29], as the switch voltage is limited to half the dc-bus voltage. There are some multilevel voltage-fed SSPFC converters which have been presented in [17], [23], and [29] and still have many of the problems of previously proposed SSPFC converters; stated above, include distorted input currents, discontinuous output current, and the use of variable switching frequency.

To date, there has been no higher power voltage-fed SSPFC that can operate with universal input voltage range (90–265 $V_{\rm rms}$), wide output load variation (from 10% of full load to a full load that is greater than 500 W), PWM control, excellent pf, a continuous output inductor current, without its components being exposed to excessive peak voltage stresses. A new voltage-fed SSPFC that has all these features is proposed in this paper. To the best of the authors' knowledge, the proposed converter is the only voltage-fed converter that does so. In the paper, the operation of the new voltage-fed converter is explained in detail and analyzed, its steady-state characteristics are determined, and its design is discussed. Experimental results obtained from a prototype are presented to confirm the feasibility of the new converter and its ability to meet IEC 1000-3-2 standards for electrical equipment.

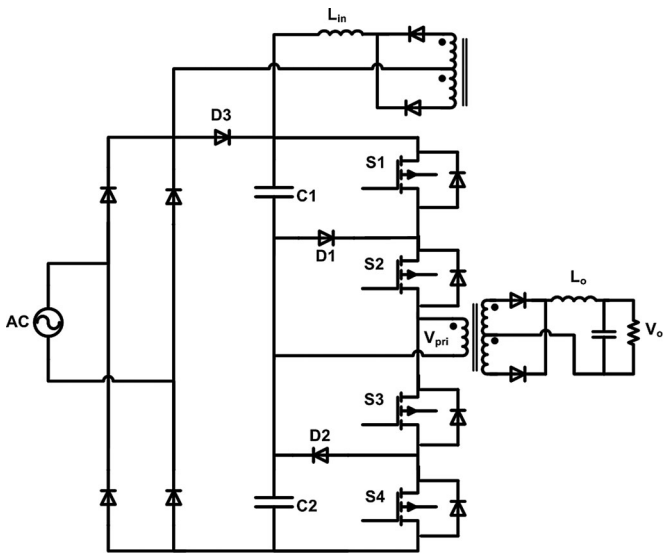

Fig. 2. Proposed single-stage three-level converter.

II. Operation of the Proposed Converter

The proposed converter is shown in Fig. 2. It consists of an ac input section, a three-level dc-dc converter, and dc link circuitry that is based on auxiliary windings taken from the main power transformer and that contains an inductor $L_{\rm in}$ and two diodes. Diode D_3 only conducts current to charge the dc bus capacitor

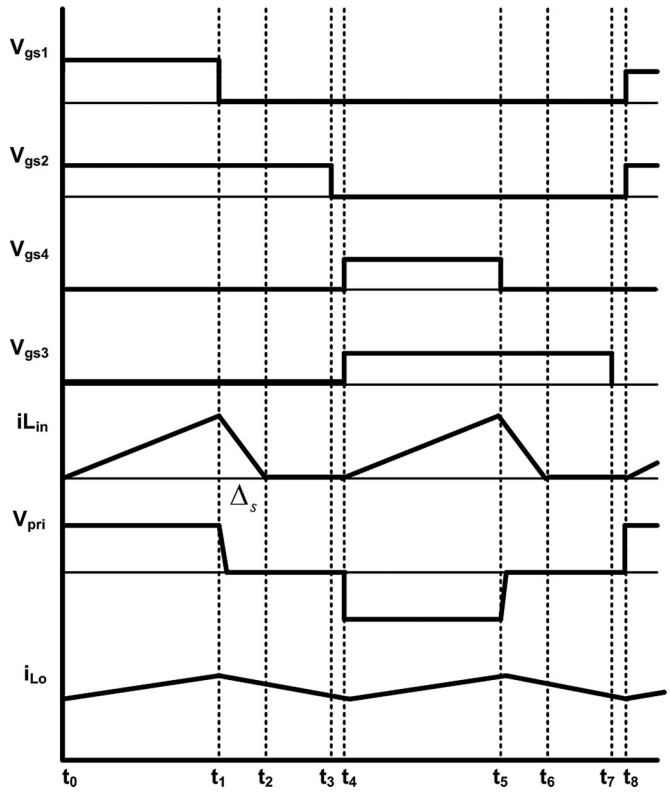

Fig. 3. Typical waveforms describing the modes of operation.

when the converter starts up; it is not in operation when the converter is in steady-state.

The dc link circuit acts like the boost switch in an ac-dc PFC boost converter. Whenever two converter switches are ON, a voltage is impressed across each auxiliary winding so that the voltage across one of the windings cancels out the voltage across the dc link capacitors (sum of the voltage across C_1 and C_2). This is analogous to the boost switch being ON and current in $L_{\rm in}$ (which can be considered to be the boost inductor) rises. Whenever only one converter switch is ON, no voltage is impressed across any of the auxiliary windings so that there is no voltage cancellation of the dc link voltage. This is analogous to the boost switch being OFF and current in $L_{\rm in}$ falls. If the converter is designed so that it operates with a constant duty cycle and a discontinuous $L_{\rm in}$ current throughout the line cycle, then input PFC can be achieved without introducing any significant low frequency component to the output as the peak current in $L_{\rm in}$ tracks the sinusoidal wave shape of the rectified supply voltage.

Typical converter waveforms are shown in Fig. 3, and equivalent circuit diagrams that show the converter's modes of operation are shown in Fig. 4 with the diode rectifier bridge output replaced by a rectified sinusoidal source and thick lines representing the paths of current conduction. The converter has the following modes of operation. It should be noted that the dc bus voltage is assumed to be fixed even though the dc bus capacitor has some ripple due to the 120 Hz component of the diode bridge rectifier output for the purpose of simplicity, as this ripple is negligible compared to the dc component of the bus voltage.

Mode 1 ($t_0 \le t \le t_1$): During this mode, switches S_1 and S_2 are ON and energy from the dc-link capacitor C_1 flows to the output load. Since the auxiliary winding generates a voltage that is equal to the total dc-link capacitor voltage (sum of C_1 and C_2), the voltage across the auxiliary inductor is the rectified supply voltage. This allows energy to flow from the ac mains into the auxiliary inductor during this mode, and the auxiliary inductor current increases, according to

$$i_{L_{{\rm in},k}}(t) = \frac{|v_{s,k}|}{L_{\rm in}} \cdot t \tag{1}$$

where $|v_{s,k}|$ is the rectified ac supply voltage during switching cycle interval k. The supply voltage can be considered to be constant within a switching cycle as the switching frequency is much higher than the line frequency. The current in the auxiliary inductor $L_{\rm in}$ at the end of Mode 1 is

$$i_{L_{{\rm in},k,{\rm max}}}(t) = \frac{|v_{s,k}|}{L_{\rm in}} \cdot \frac{D}{2f_{\rm sw}}. \tag{2}$$

Duty cycle, D, is defined as the time when S_1 and S_2 are both ON during the first half cycle or when S_3 and S_4 are both ON during the second half cycle. These two cases correspond to energy transfer modes of operation. Since D is defined with respect to a half switching cycle $T_{\rm sw}/2$ or $1/2f_{\rm sw}$, (where $f_{\rm sw}$ is the switching frequency) the duration that is used in (2) is $D/(2f_{\rm sw})$.

Similarly, the output inductor current can be expressed as

$$i_{L_o}(t) = \frac{(V_{\rm bus}/2N) - V_L}{L_o} \cdot t \tag{3}$$

where $V_{\rm bus}$ is the average dc-link voltage, V_L is the load voltage and N is the transformer ratio between input and output ($N = N_{\rm pri}/N_{\rm sec}$). If the output inductor current is continuous then peak ripple current can be expressed as

$$\Delta i_{L_o} = \frac{(V_{\rm bus}/2N) - V_L}{L_o} \cdot \frac{D}{2f_{\rm sw}} \tag{4}$$

Mode 2 ($t_1 \le t \le t_2$): S_1 is OFF and S_2 is ON during this mode. The energy stored in $L_{\rm in}$ during the previous mode is completely transferred into the dc-link capacitor. The amount of stored energy in the auxiliary inductor depends upon the rectified supply voltage. This mode is a freewheeling mode as the primary current freewheels through S_2 and D_1 and the output inductor current freewheels through both secondary diodes. This mode ends when the current in $L_{\rm in}$, $i_{\rm Laux}$, reaches zero.

Since the voltage across $L_{\rm in}$ during this mode is $|V_{s,k}| - V_{\rm bus}$, $i_{\rm Lin}$ can be expressed as

$$i_{L_{{\rm in},k}}(t) = i_{L_{{\rm in},k,{\rm max}}} - \frac{V_{\rm bus} - |v_{s,k}|}{L_{\rm in}} \cdot t. \tag{5}$$

The duration of this mode can be expressed as $\Delta_{s,k}/2f_{\rm sw}$. Using this expression along with (2) and (5) with $i_{\rm Lin} = 0$ gives

$$\Delta_{s,k} = \frac{|v_{s,k}|}{V_{\rm bus} - |v_{s,k}|} \cdot D. \tag{6}$$

Equation (6) shows that the duration of this mode is time varying along one ac supply period. In order to assure a discontinuous input current, $\Delta_{s,k}$ must satisfy the expression $D +$

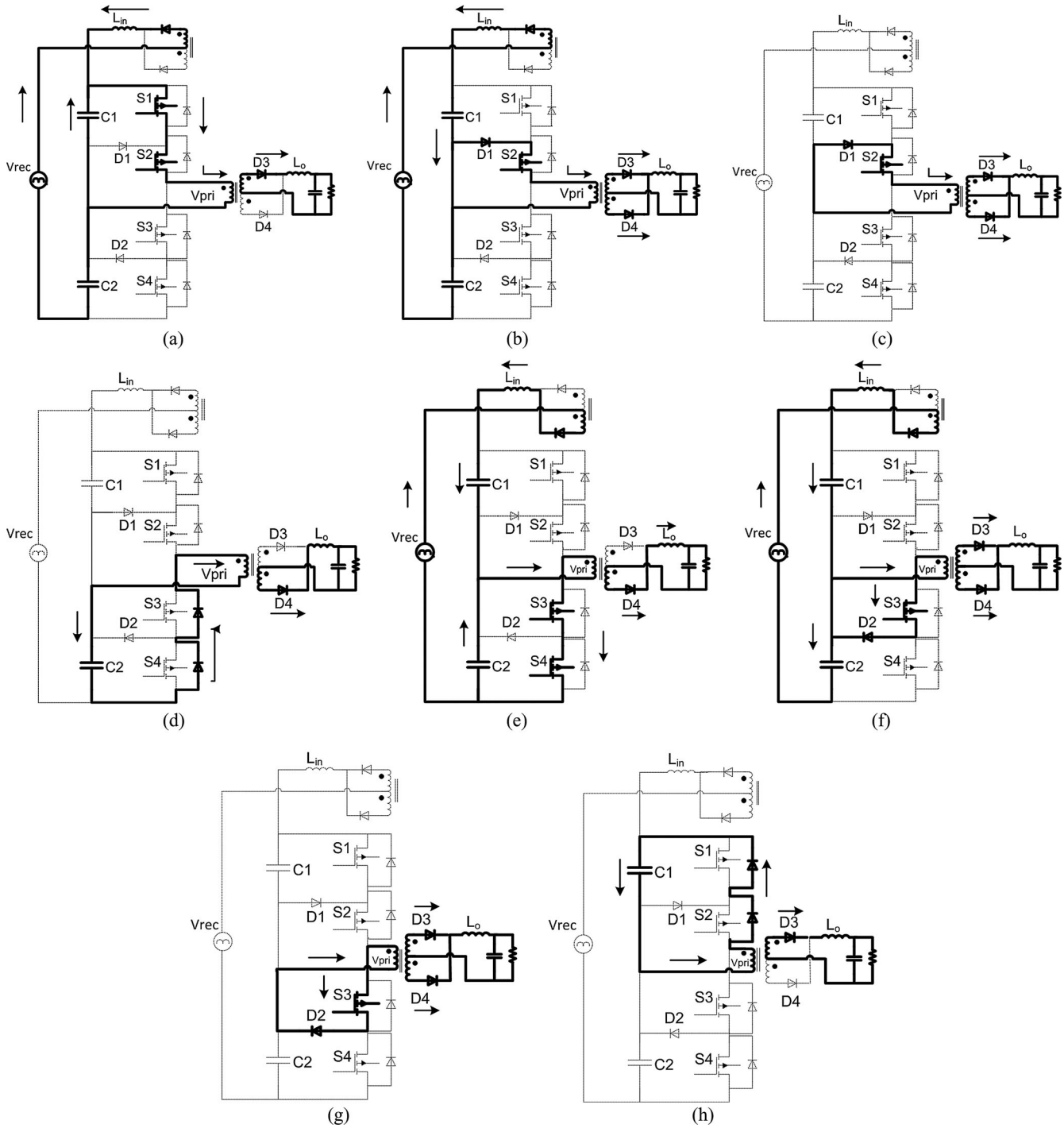

Fig. 4. Equivalent circuits for each operation stage for the converter. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7, and (h) Mode 8.

$\Delta_{s,k} < 1$ at any interval k and load conditions. Using (6), this constraint can be written as

$$V_{\text{bus}} > \frac{|v_{s,k}|}{1-D}. \tag{7}$$

An expression for the output inductor current can be obtained by noting that the voltage across the output inductor is equal to $-V_L$; this current can be expressed as

$$i_{Lo}(t) = i_{L_o,\max} - \frac{V_L}{L_o} \cdot t. \tag{8}$$

The peak output ripple current can be expressed as

$$\Delta i_{L_o} = -\frac{V_L}{L_o} \cdot \frac{1-D}{2f_{\text{sw}}} \tag{9}$$

and the following can be obtained from (4) and (9):

$$V_o = \frac{V_{\rm bus}}{2N} \cdot D \tag{10}$$

Mode 3 ($t_2 \le t \le t_3$): S_2 is the only switch that is ON during this mode. There is no current flowing through $L_{\rm aux}$ and the converter remains in a freewheeling mode.

Mode 4 ($t_3 \le t \le t_4$): No converter switch is ON during this mode as the current in the transformer primary charges capacitor C_2 through the body diodes of S_3 and S_4. This mode ends when switches S_3 and S_4 are switched on and a symmetrical half-period begins. The output inductor current continues to freewheel in the secondary of the transformer during this mode.

Mode 5($t_4 \le t \le t_5$): This mode is the same as Mode 1 except that S_3 and S_4 are ON and energy flows from capacitor C_2 into the load.

Mode 6 ($t_5 \le t \le t_6$): This mode is the same as Mode 2 except that S_3 is ON.

Mode 7 ($t_6 \le t \le t_7$): This mode is the same as Mode 3 except that the primary current circulates through S_3 and diode D_2.

Mode 8 ($t_7 \le t \le t_8$): This mode is the same as Mode 1 except that the current in the primary of the transformer charges capacitor C_1 through the body diodes of S_1 and S_2. This mode ends when the S_1 and S_2 are turned ON and the converter reenters Mode 1.

III. Steady State Analysis

The key parameter that must be derived from an analysis of any integrated converter is the dc-link voltage because it is only then that other parameters such as input current can be determined. Unlike a conventional two-stage converter, this voltage is not regulated by a separate ac–dc boost PFC stage and varies considerably, depending on the line and load; however, it can be determined for any set of operating conditions by noting that an energy equilibrium must exist for the dc-link capacitors when the converter is in steady-state operation. The energy pumped into the capacitors from the input section must be equal to the energy that they provide to the output, so that the net dc current flowing in and out of must be zero during a half-line cycle.

This energy equilibrium, however, cannot be determined using equations with closed-form solutions due to the various possible combinations of input and output modes of operation; it must instead be determined using a computer program. If it is assumed that the converter has ideal semiconductors and an ideal transformer with no leakage inductance and negligible magnetizing current, then the dc-link voltage can be determined for any operating point with a given input voltage $V_{\rm in}$, output voltage V_L, switching frequency $f_{\rm sw}$, input inductor $L_{\rm in}$, output inductor L_o, transformer turns ratio $N = N_{\rm pri}/N_{\rm sec}$, and output current I_o can be determined as follows:

1) Assume a duty cycle D as an initial "guess" (i.e., $D = 0.5$).
2) Assume that the output current is continuous then use (10) to find $V_{\rm bus}$

$$V_{\rm bus} = \frac{2V_o N}{D}. \tag{11}$$

With this value of $V_{\rm bus}$, verify that the output current is continuous by seeing that the peak output current ripple does not exceed the average current I_o

$$\frac{1}{2}\frac{(V_{\rm bus}/2N) - V_o}{L_o} \cdot \frac{D}{2f_{\rm sw}} < \frac{P_o}{V_o}. \tag{12}$$

If this relation is satisfied, then $V_{\rm bus}$ is equal to the value determined in (11). If not, then the output current is discontinuous and $V_{\rm bus}$ must be determined using (13), which has been derived for DCM

$$V_{\rm bus} = 2N \cdot \frac{V_o + \sqrt{V_o^2 + (16P_o \cdot L_o \cdot f_{\rm sw}/D^2)}}{2}. \tag{13}$$

With $V_{\rm bus}$ known, find the average current that flows out of the capacitors during a half-line cycle using either (14) for CCM or (15) for DCM

$$I_{C_{\rm bus,out\text{-}avg}} = \frac{I_o \cdot D}{2N} \tag{14}$$

$$I_{C_{\rm bus,out\text{-}avg}} = \frac{D^2}{4N \cdot L_o \cdot f_{\rm sw}} \cdot \left(\frac{V_{\rm bus}}{2N} - V_o\right). \tag{15}$$

Determine the average current that is fed from the input to the capacitors during a half-line cycle using

$$I_{C_{\rm bus,in\text{-}avg}} = 2f_{\rm in} \cdot \sum_{k=0}^{m} \int_{t^*}^{t_k} \left[\frac{v_{{\rm in},k} - V_{\rm bus}}{L_{\rm in}}(t - t^*) + I^*_{{\rm in},k}\right] \cdot d \tag{16}$$

$I^*_{{\rm in},k}$ is the peak input current value during a switching cycle k. If (16) is equal to (14) or (15), then the converter is confirmed to be operating under steady-state conditions and the value of $V_{\rm bus}$ that has been calculated is valid. If not, then the operating point for which is to be determined is not a valid operating point and the procedure must be repeated for a different value of D. The flowchart shown in Fig. 5 shows the full analysis procedure.

This procedure can be repeated to determine $V_{\rm bus}$ (or any other parameter) for multiple operating points so that graphs of steady-state characteristic curves can be generated for design purposes. The converter operating characteristics for any given input and output voltage are dependent on three key parameters—transformer turns ratio N, input inductance $L_{\rm in}$, and output L_o. The effect that each of these parameters has on $V_{\rm bus}$ can be seen with graphs of characteristic curves that have been generated with a computer program based on the procedure described above, varying the parameter while keeping the others fixed. Such graphs are shown in Fig. 6. The following observations can be made based on these graphs:

1) It can be seen in Fig. 6(a) that $V_{\rm bus}$ decreases as the transformer turns ratio N is decreased and all the other parameters are kept constant.
2) It can be seen in Fig. 6(b) that $V_{\rm bus}$ decreases as $L_{\rm in}$ is increased and all other parameters are kept constant.
3) It can be seen from Fig. 6(c) that $V_{\rm bus}$ rises as L_o is increased and all the other parameters are kept constant.

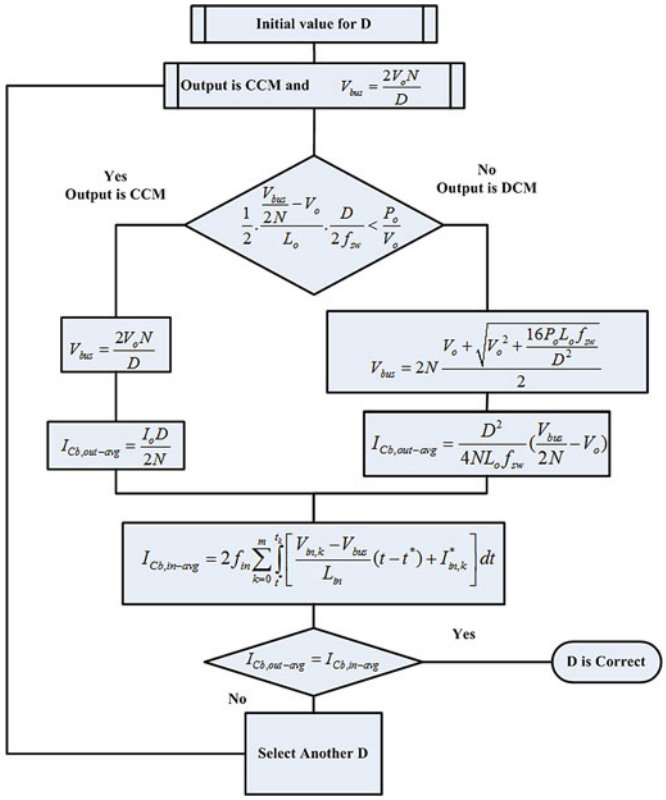

Fig. 5. The procedure of steady state analysis for determining the dc bus voltage.

Varying L_o has a slight effect on $V_{\rm bus}$ for higher output loads when the output is operating in CCM, but has a more pronounced effect at lower output loads when the output is in DCM.

Fig. 6(d) shows the effect of input voltage on the dc-link voltage. As can be seen, increasing the input voltage increases the dc-link voltage as well. These characteristics are consistent with those of most single-stage ac–dc converters. A detailed explanation as to why the converter has these particular characteristics can be found in [2].

It should be noted that since the converter is a multilevel converter, that the dc bus voltage can be split equally among the capacitors so that the capacitors and the converter switches are not exposed to the full dc bus voltage, but are exposed to half of it. This allows from greater flexibility in the design of the converter as there is less need to constrain the dc bus voltage, as will be shown in the next section of this paper. It is the greater flexibility in the converter design that allows for improvements in the performance of a single-stage full-bridge converter.

Since the converter is a multilevel converter, it should be implemented with some sort of capacitor voltage balancing technique to ensure the voltage across each bus capacitor is the same. Various such techniques have been proposed in the literature, including techniques that sense the capacitor voltages and adjust the duty cycle of the converter switches appropriately. For this work, an auxiliary circuit that is composed of a transformer with a turns ratio of $N_{\rm aux1}/N_{\rm aux2}=1$ and two diodes $D_{\rm aux1}$ and $D_{\rm aux2}$ was used, as shown in Fig. 7(a) [30]. This circuit is very simple, small, and handles only a small fraction of the overall power that is processed by the converter. It should be noted that any other voltage balancing technique could have been used.

The basic principle behind the auxiliary circuit is that if the voltage across one capacitor begins to be greater than the other by more than a diode drop, then one of the diodes begins to conduct as energy is transferred away from the capacitor with the higher voltage. Since the auxiliary circuit does not allow for large differences in bus capacitor voltage, the amount of energy that needs to be transferred away at any given time is small. When the auxiliary circuit is added to the main circuit, it is most likely to come into play during Modes 1 and 5 of operation as this is when the most current will flow through one of the bus capacitors. The auxiliary circuit works as follows during these modes:

Mode 1 ($t_0 \le t \le t_1$) (Fig. 7(b)): During this mode, switches S_1 and S_2 are ON and energy from the dc-link capacitor C_1 flows to the output load. Since the auxiliary winding generates a voltage that is equal to the total dc-link capacitor voltage (sum of C_1 and C_2), the voltage across the auxiliary inductor is the rectified supply voltage. This allows energy to flow from the ac mains into the auxiliary inductor during this mode, and the auxiliary inductor current increases.

At the beginning of this interval, if there exists any unbalance between the voltages of the two dc-bus capacitors, such that $V_{C1} > V_{C2}$, the auxiliary circuit starts conducting through diode $D_{\rm aux2}$ to balance the voltage difference across the C_1 and C_2.

Mode 5($t_4 \le t \le t_5$) (Fig. 7(c)): This mode is the same as Mode 1 except that S_3 and S_4 are ON and energy flows from capacitor C_2 into the load. Similarly, in Mode 5, when $V_{C2} > V_{C1}$, the auxiliary circuit starts conducting through diode $D_{\rm aux1}$ to balance the voltage difference across the capacitors.

IV. Converter Design

A procedure for the design of the converter is presented in this section and is demonstrated with an example. The following criteria should be considered when trying to design the converter:

1) The energy-storage capacitor voltage $V_{\rm bus}$ should not be excessive. The value of $V_{\rm bus}$ should be kept to below 800 V (400 V for each capacitor) if possible so that the use of bulkier, more expensive capacitors can be avoided.
2) Excessive peak output and input currents should be avoided if possible.
3) The input line current must satisfy the necessary regulatory agency requirements of harmonic content such as IEC1000-3-2.

A design procedure for the selection of converter components based on the characteristic curves presented in the previous sections of this paper is given along with an example to illustrate how the converter can be designed. The converter is to be designed with the following parameters for the example:

1) Input voltage: $V_{\rm in} = 90{-}265\ V_{\rm rms}$
2) Output voltage: $V_o = 48$ V
3) Maximum output power: $P_o = 1000$ W
4) Switching frequency: $f_{\rm sw} = 1/T_{\rm sw} = 50$ kHz
5) Maximum capacitor voltage: 400 V for each capacitor

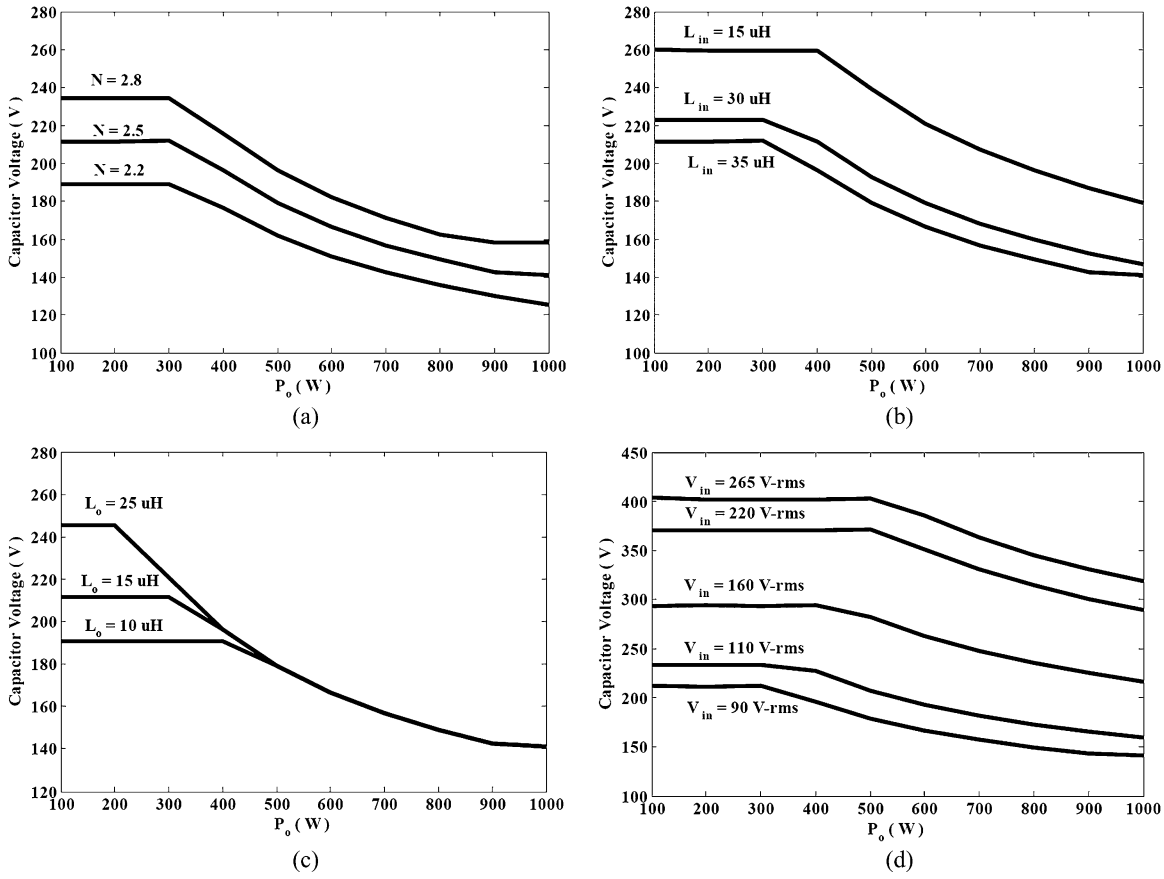

Fig. 6. Steady-state characteristic curves ($V_{\rm in} = 90\ V_{\rm rms}$, $V_o = 48$ V, $f_{\rm sw} = 50$ kHz). (a) Effect of transformer ratio value N on dc bus voltage ($L_{\rm in} = 35\ \mu$H, $L_o = 15\ \mu$H). (b) Effect of input inductor value $L_{\rm in}$ on dc bus voltage ($N = 2.5$, $L_o = 15\ \mu$H). (c) Effect of output inductor value L_o on dc bus voltage ($N = 2.5$, $L_{\rm in} = 35\ \mu$H). (d) Effect of input voltage $V_{\rm in}$ on dc bus voltage ($N = 2.5$, $L_{\rm in} = 35\ \mu$H, $L_o = 15\ \mu$H).

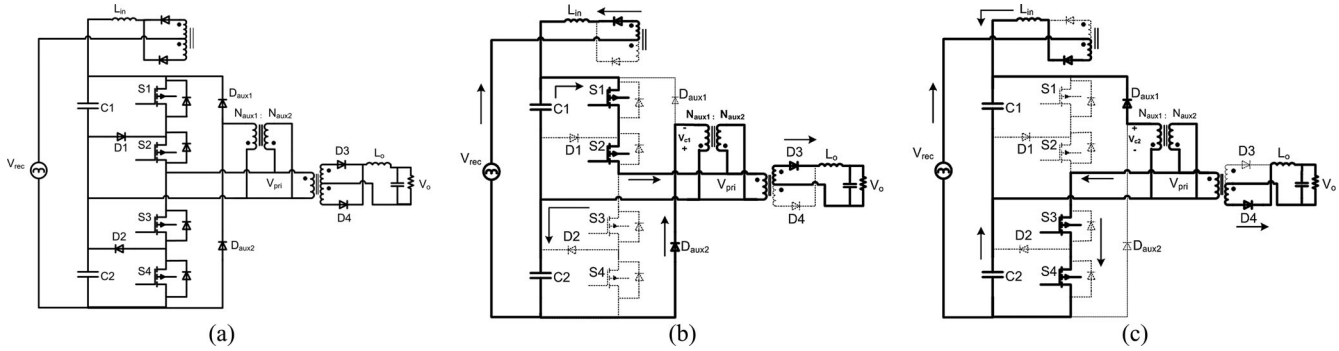

Fig. 7. Proposed single-stage three-level converter with auxiliary circuit and modes of operation. (a) Proposed single-stage three-level converter with auxiliary circuit. (b) Mode 1 with auxiliary circuit. (c) Mode 5 with auxiliary circuit.

6) Input current harmonics: IEC1000-3-2 for Class D electrical equipment.

It should be noted that the design procedure is iterative and only the last iteration is shown here.

Step 1: Determine Value for Turns Ratio of Main Transformer N

N is an important parameter as it affects the amount of reflected load current that is available at the transformer primary to discharge the bus capacitors. Fig. 6(a) is an example of how the value of N affects the primary-side dc bus voltage. If N is very low, then there is little reflected load current available to discharge the bus capacitors, which can result in an extremely high dc bus voltage. If N is high, then the primary current may be very high as there will be a high amount of current circulating in the transformer primary, which will create significant conduction losses. A tradeoff between high values of N and low values of N, therefore, must be considered when selecting a value of N.

Selecting a value of N, however, cannot be done with a simple equation and must be done using some other method. One way of doing so is to use the computer program described in the previous section of this paper to examine a wide range of potentially valid combinations of L_o and $L_{\rm in}$—combinations that allow the converter to work for the two most extreme line and load conditions: high line, light load and low line, and full load. For this particular design example, numerous graphs of characteristic curves for different values of N were generated by the authors (not shown here due to lack of space) and based on these graphs, a value of $N = 2.5$ is selected as an appropriate value.

As a check to see if this value makes sense, (10)—which shows the relation between $V_{\rm bus}, D, V_o$ and N—can be used. For this check, the operation of the converter at minimum input line when it operates with minimum primary-side dc bus voltage $V_{\rm bus,min}$ and maximum duty cycle $D_{\rm max}$ should be considered. If the converter can produce the required output voltage and can operate with discontinuous input and continuous output currents in this case, then it can do so for all cases. Substituting $V_{\rm bus,min}$ and maximum duty cycle $D_{\rm max}$ into (10) gives

$$V_{\rm bus,min} = \frac{2V_o}{D_{\rm max}} \cdot N. \tag{17}$$

Substituting $V_o = 48$, $N = 2.5$, and $D_{\rm max} = 0.8$ (0.8 has been selected as a conservative $D_{\rm max}$ to provide some margin) gives

$$V_{\rm bus,min} = \frac{2(48)}{0.8} \cdot (2.5) = 300\,{\rm V}. \tag{18}$$

A bus voltage of $V_{\rm bus,min} = 300\,{\rm V}$ or $V_{\rm bus}/2 = 150\,{\rm V}$ is acceptable. If a very low value of $V_{\rm bus,min} = 100\,{\rm V}$ or a value of $D_{\rm max} > 1$ would have been found based on (17), then the value of N under consideration would have been unacceptable and another value would have to be considered. It should be noted that the dc bus voltage has not been determined yet. All that has been determined thus far is a value of N that can operate with an acceptable duty cycle for an acceptable minimum dc bus voltage.

Step 2: Determine Value for Inductor $L_{\rm in}$

The value for $L_{\rm in}$ should be low enough to ensure that the input current is fully discontinuous under all operating conditions, but not so low as to result in excessively high peak currents. This can be done using the computer program with the following equations, which are based on the descriptions given in Section III.

For the case where $L_{\rm in}$ is such that the input current remains discontinuous for all operating conditions, the average input power can be expressed as

$$P_{\rm in} = \frac{1}{T_{\rm su}} \int_0^{T_{\rm su}} |v_{s,k}| \cdot i_{s,k} d_{w_k}\, t = \frac{1}{f_{\rm sn}} \sum_{k=0}^{f_{\rm sn}-1} |v_{s,k}| \cdot i_{s,k} \tag{19}$$

where $f_{\rm su}$ is the input ac frequency and $f_{\rm sn} = 2f_{\rm sw}/f_{\rm su}$ and

$$i_{s,k} = \frac{(D+\Delta_s)}{2} \cdot i_{L_{\rm in,max}} = \frac{1}{4} \cdot \frac{D^2}{L_{\rm in} \cdot f_{\rm sw}} \cdot \frac{|v_{s,k}|}{1-(|v_{s,k}|/V_{\rm bus})} \tag{20}$$

By substituting the value of $i_{s,k}$ in (20), $P_{\rm in}$ can be expressed as

$$\begin{aligned} P_{\rm in} &= \frac{1}{f_{\rm sn}} \sum_{k=0}^{f_{\rm sn}-1} |v_{s,k}| \cdot i_{s,k} \\ &= \frac{D^2}{8 \cdot L_{\rm in} \cdot f_{\rm sw}} \cdot \frac{1}{f_{\rm sn}} \sum_{k=0}^{f_{\rm sn}-1} \frac{|v_{s,k}|^2}{1-(|v_{s,k}|/V_{\rm bus})}. \end{aligned} \tag{21}$$

By assuming that $P_{\rm in} = P_o$, the following equation can be derived:

$$\begin{aligned} L_{\rm in} &= \frac{1}{f_{\rm sn}} \sum_{k=0}^{f_{\rm sn}-1} |v_{s,k}| \cdot i_{s,k} \\ &= \frac{D^2}{8 \cdot P_o \cdot f_{\rm sw}} \cdot \frac{1}{f_{\rm sn}} \sum_{k=0}^{f_{\rm sn}-1} \frac{|v_{s,k}|^2}{1-(|v_{s,k}|/V_{\rm bus})}. \end{aligned} \tag{22}$$

The worst case to be considered is the case when the converter operates with minimum input voltage and maximum load since if the input current is discontinuous under these conditions, it will be discontinuous for all other operating conditions and thus an excellent power factor will be achieved. $V_{\rm in} = 90\ V_{\rm rms}$ and $V_{\rm bus} = 300\,{\rm V}$ as calculated in Step 2 are used to determine $L_{\rm in}$ at the boundary condition for the input section with $D = D_{\rm max} = 0.8$ and $P_{\rm in} = P_o = 1000\,{\rm W}$. As a result, a value of $L_{\rm in} = 38.5\ \mu{\rm H}$ can be found. For this design, $L_{\rm in} = 35\ \mu{\rm H}$ is used.

Step 3: Determine Value for Output Inductor L_o

Ideally, the output inductor L_o should be designed so that the output current is made to be continuous under most operating conditions. The reality, however, is doing so may result in an excessive dc bus voltage. As a compromise, the value of L_o should be such that the output inductor current is continuous when the converter is operating with heavy loads and discontinuous when the converter is operating with light loads.

Fig. 6(c) shows a graph of curves of bus capacitor voltage ($V_{\rm bus}/2$) versus load for various values of L_o, with $N = 2.5$ and $L_{\rm in} = 35\ \mu{\rm H}$, which are the values of N and $L_{\rm in}$ that were selected in the previous steps. This graph shows the effect that L_o has on the bus capacitor voltage. When the converter is operating with heavy load, it does not matter what the value of L_o is if the output inductor current is continuous. It is when the load is reduced that the capacitor voltage becomes different with different L_o as the current in L_o start becoming discontinuous. The flat portion of each curve in Fig. 6(c) represents the load range where the current through L_o is discontinuous while the curved or "nonflat" region is the region where the current through L_o is continuous. It can be seen from Fig. 6(c) that the boundary point between continuous current mode (CCM) and discontinuous current mode (DCM) output inductor current occurs at a lighter load as L_o is increased.

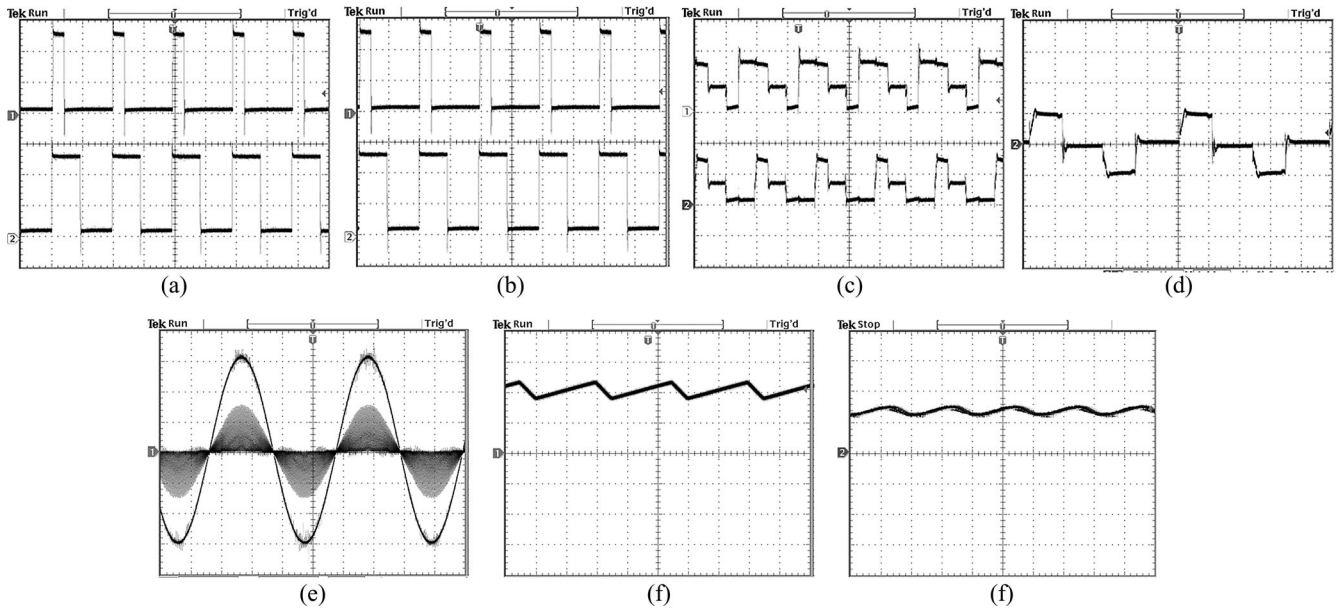

Fig. 8. Experimental results. (a) Switch gating pulses $V_{\rm gs1}$, $V_{\rm gs2}$ (V: 5 V/div., t: 10 μs/div.). (b) Switch gating pulses $V_{\rm gs4}$, $V_{\rm gs3}$ (V: 5 V/div., t: 10 μs/div.). (c) Top switch voltages $V_{\rm ds1}$ and $V_{\rm ds2}$ (V: 100 V/div., t:10 μs/div.). (d) Primary voltage of the main transformer (V: 150 V/div., t: 4 μs/div.). (e) Input current and voltage (V: 50 V/div, I: 25 A/div). (f) Output inductor current (I: 10 A/div., t: 4 μs/div.). (g) Voltage of dc bus capacitors V_c1, V_c2 (V: 100 V/div., t: 4 ms/div.).

The value of L_o should be the largest value that allows the converter to operate with nonexcessive capacitor voltages, nonexcessive being defined as less than 450 V, which is a standard definition for two-level converters. The worst case for this is when the input is at maximum line and thus a graph of capacitor voltage versus load for the values of N and $L_{\rm in}$ selected in the previous steps, $N = 2.5$ and $L_{\rm in} = 35$ μH and the value of L_o under consideration is needed. Such a graph for $L_o = 15$ μH is shown in Fig. 6(d).

It can be seen from this graph that the maximum bus capacitor voltage is approximately 400 V. Since a higher value of L_o would probably result in the bus capacitor voltage exceeding 450 V or being close to 450 V without margin, a value of $L_o = 15$ μH is, therefore, chosen for the output inductor.

As a final check, the value of $V_{\rm bus,min}$ should be looked at given the importance of this parameter as explained in Steps 1 and 2 of this procedure. It can be seen from Fig. 6(d) that $V_{\rm bus,min}/2$ occurs when the line voltage is 90 $V_{\rm rms}$ (low line) and the load is at its maximum and that this value is approximately 150 V or $V_{\rm bus,min} = 300$ V. The chosen combination of N, $L_{\rm in}$, L_o, therefore, is acceptable and the design procedure can be ended. It should be noted that a value of $L_o = 15$ μH is considerably higher than what is typically found in most other single-stage full-bridge converters, which must operate with very low output inductor values to prevent the dc bus voltage from becoming excessive [2], [14], [17]–[19], [21].

V. Experimental Results

An experimental prototype of the proposed converter was built to confirm its feasibility. The prototype was designed according to the following specifications:

1) Input voltage $V_{\rm in} = 90$–265 $V_{\rm rms}$
2) Output voltage $V_o = 48$ V
3) Output power $P_o = 1000$ W
4) Switching frequency $f_{\rm sw} = 50$ kHz.

The main switches were FDL100N50F, and the diodes were UF1006DICT. The input inductance is $L_{\rm in} = 35$ μH, $L_o = 15$ μH and dc-Bus capacitors, C_1, $C_2 = 2200$ μF. The auxiliary transformer ratio was 1:2 and the main transformer ratio was 2.5:1. Typical converter waveforms are shown in Fig. 8.

Fig. 8(a) and (b) shows the gating signals of the four switches; the converter works like a standard dc–dc multilevel full-bridge converter. Fig. 8(c) shows typical voltage waveforms of the top switches and Fig. 8(d) shows the typical voltage waveforms of the bottom switches. The multilevel converter provides the capability of operating at reduced voltage stresses across the switches, as the switch voltage is limited to half the dc-bus voltage. Fig. 8(e) shows the voltage across the primary side of the main transformer, which is the same as that of a full-bridge converter. Fig. 8(f) shows the input voltage and input current before filtering; it can be seen that the input current has no deadbands. Fig. 8(g) shows the voltage across each capacitor. It can be seen that the voltage waveforms are identical as the figure seems to show only one waveform.

Fig. 9 shows the experimental efficiency at different value of output power and Fig. 10 shows the experimental efficiency at value of input voltages. Fig. 11 shows the dc bus voltage at different value of output power. Input power factor at different values of output power is shown in Fig. 12. Figs. 13 and 14 show input current harmonic at $V_{\rm in} = 230$ $V_{\rm rms}$ and $V_{\rm in} = 100$ $V_{\rm rms}$, respectively, and can meet the IEC1000-3-2 Class A standard for electrical equipment.

As can be seen from the experimental results and characteristic graphs, the proposed converter is a higher power voltage-fed SSPFC that can operate with universal input voltage range (90–265 $V_{\rm rms}$), wide output load variation (from 10% of full load to

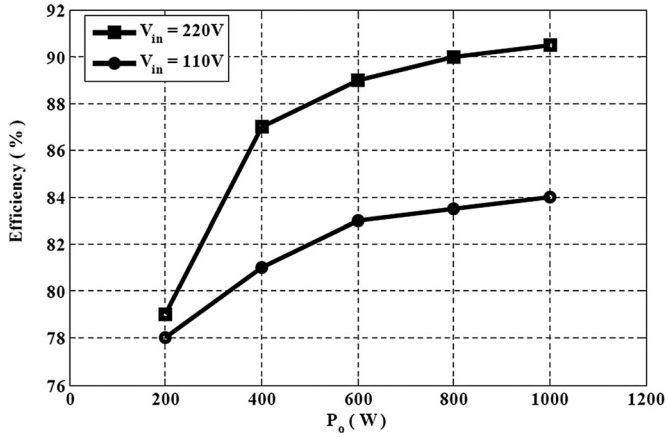

Fig. 9. Experimental efficiency at different value of output power.

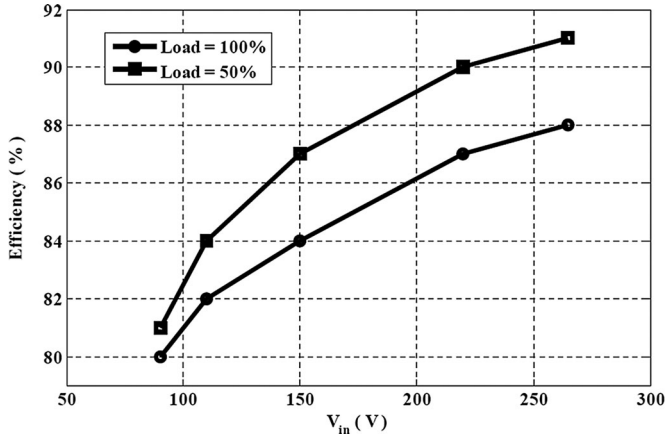

Fig. 10. Experimental efficiency at different value of input voltage.

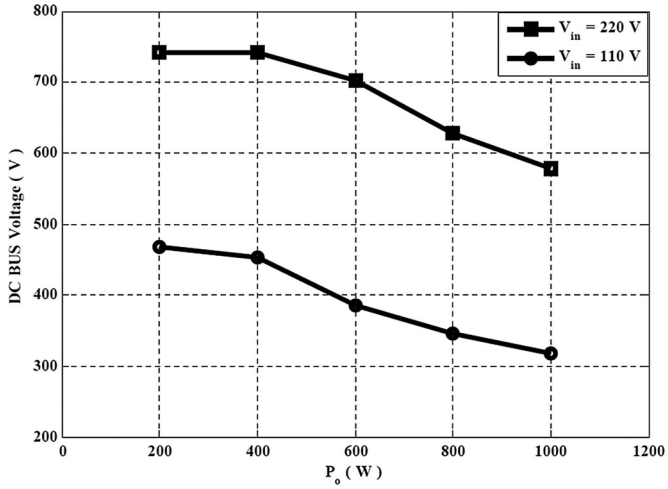

Fig. 11. Experimental dc bus voltage at different value of output power.

a full load that is greater than 500 W), PWM control, excellent power factor, a continuous output inductor current, without its components being exposed to excessive peak voltage stresses.

To the best of the authors' knowledge, it is the only existing voltage-fed SSPFC that has all these features. The superior performance of the proposed converter can be clearly seen when

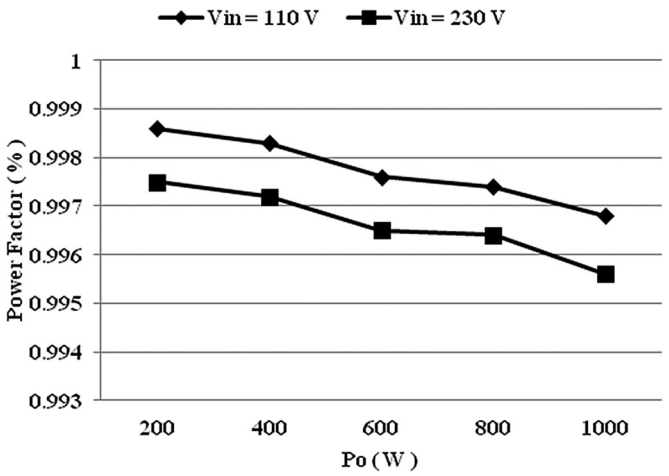

Fig. 12. Input power factor at different values of output power.

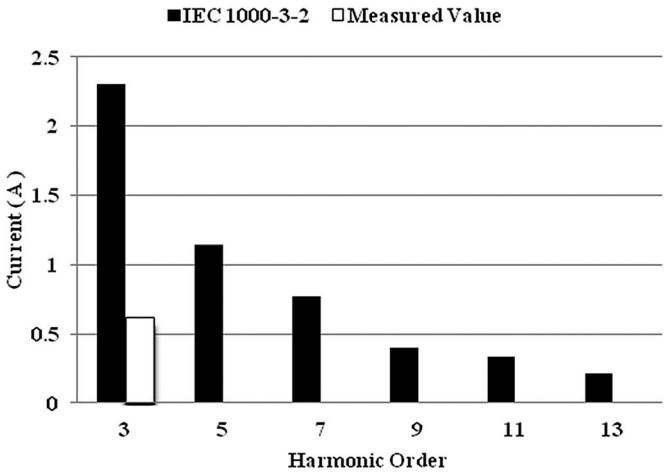

Fig. 13. Input current harmonic at $V_{\rm in} = 230\ V_{\rm rms}$, $P_o = 1000$ W compared to IEC1000-3-2 Class A.

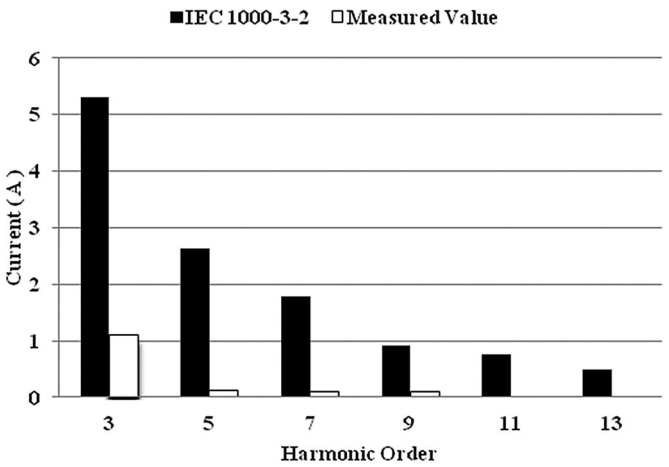

Fig. 14. Input current harmonic at $V_{\rm in} = 100\ V_{\rm rms}$, $P_o = 1000$ W compared to IEC1000-3-2 Class A.

compared to the converters that were presented in [31], which reviewed and compared the performance of a number of SSPFC converters operating at 30 kHz. When comparing the proposed converter with the converters reviewed in that paper, it can be seen that the proposed converter operates with similar converter efficiency even though its switching frequency was almost two times higher, and with higher dc bus capacitor voltages, which increases the peak voltage stresses of the converter switches. It should be mentioned that although the proposed converter may seem complex to power supply designers who are unfamiliar with three-level converter topologies, it has a significantly better performance that two-level SSPFCs with just, at most, two additional clamping diodes and a small passive auxiliary voltage balancing circuit that handles a small fraction of the main converter power.

VI. Conclusion

A new three-level, voltage-fed, single-stage, single-phase, power-factor-corrected (SSPFC) ac/dc PWM converter that operates with a single controller was presented in this paper. The proposed converter can operate with universal input voltage (90– 265 $V_{\rm rms}$) and with a better efficiency, less distorted input current, wider load operating range, and less output inductor current ripple than previously proposed SSPFC converters. The advantageous features of the proposed converter are due to the fact that it is a three-level converter that allows the uncontrolled primary-side dc bus voltage to be higher than what can be allowed for two-level converters so that it does not have the design restrictions that these converters have.

In the paper, the operation of the new converter was explained in detail and analyzed, its steady-state characteristics were determined. The converter's design was discussed and a design procedure was established and demonstrated with an example. Experimental results obtained from a prototype confirmed the feasibility of the new converter and its ability to meet IEC 1000-3-2 standards for electrical equipment.

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