A Novel DC-Side Zero-Voltage Switching (ZVS) Three-Phase Boost PWM Rectifier Controlled by an Improved SVM Method

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***Abstract*—A novel active clamping zero-voltage switching three-phase boost pulsewidth modulation (PWM) rectifier is analyzed and a modified minimum-loss space vector modulation (SVM) strategy suitable for the novel zero-voltage switching (ZVS) rectifier is proposed in this paper. The topology of the novel ZVS rectifier only adds one auxiliary active switch, one resonant inductor, and one clamping capacitor to the traditional hard-switched three-phase boost PWM rectifier. With the proposed SVM strategy, the novel ZVS rectifier can achieve ZVS for all the main and auxiliary switches. In addition, the antiparallel diodes can be turned OFF softly, so the reverse recovery current is eliminated. Besides, the voltage stress of all the switches is equal to the dc-link voltage. The operation principle and soft-switching condition of the novel ZVS rectifier are analyzed. The design guidelines of the soft switched circuit parameters are described in detail. A DSP controlled 30 kW prototype is implemented to verify the theory.**

***Index Terms*—Efficiency, space vector modulation (SVM), soft-switching condition, three-phase pulsewidth modulation (PWM) rectifier, zero-voltage switching (ZVS).**

I. Introduction

THE three-phase six-switch boost pulsewidth modulation (PWM) rectifier as shown in Fig. 1, due to its remarkable features of high power quality and low electromagnetic interference (EMI) emissions, is widely chosen for medium and high power industrial applications [1]. However, during the commutation from diode to transistor, the antiparallel diodes of the rectifier experience reverse recovery process, which will cause severe switching losses and EMI problems due to high *di*/*dt* and *dv*/*dt*. Considering these problems, the switching frequency of PWM converters is usually confined, which may result in higher current total harmonic distortion, larger passive components, and high switching noise [2].

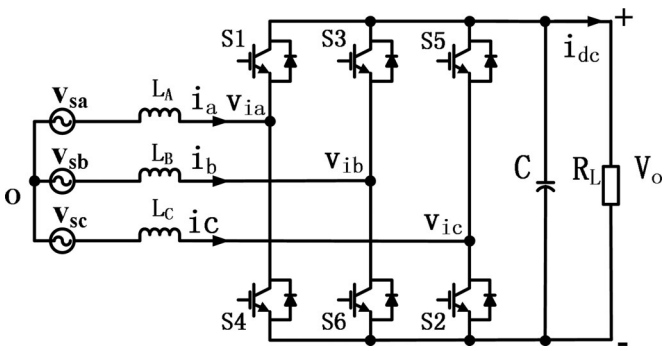

Fig. 1. Topology of the three-phase boost PWM rectifier.

The soft-switching technique can make switches be turned ON and OFF under zero-voltage or zero-current condition, which will resolve the diode reverse recovery problems and reduce switching losses. Meanwhile, the rising and falling edges of switch current and voltage waveforms can be shaped so the *di*/*dt* and *dv*/*dt* are reduced as well.

Many soft-switching techniques for three-phase PWM converter have been investigated. The general methodology is to add auxiliary resonant circuit to decrease or eliminate the overlap between voltage and current at switching transitions. According to the placement of auxiliary circuit, the soft-switching three-phase PWM converters can be divided into two classes: the dc-side soft-switching converter and the ac-side soft-switching converter [2].

The dc-side soft-switching converter uses one group of auxiliary circuits placed on the dc-side of the converter to produce high-frequency pulsating voltage across the main switch bridge. The switches are commutated at the instants when the bridge voltage is zero so the corresponding devices can be zero-voltage switching (ZVS) switched.

Among the various dc-side soft-switching topologies in [3]–[11], the resonant dc-link (RDCL) converter in [3] has the simplest topology, but it imposes 2–2.5 times voltage stress on all the switches. The active clamped RDCL (ACRDCL) converter in [4] added one extra auxiliary clamping switch to decrease the device voltage stress by 1.4–1.8 times. However, the

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RDCL and ACRDCL converters are both controlled by discrete pulse modulation (DPM), which will produce subharmonics in the ac-side current waveforms [5]. A partial PWM control technique for the RDCL and ACRDCL converters has been proposed in [6] to overcome the drawbacks of the DPM but the device turn-off loss is increased and meanwhile the PWM range is limited. To apply real PWM control techniques, many approaches have been presented in [7]–[11]. These converters provide zero-voltage intervals in the switch bridge of the PWM converter whenever the switch transition is needed but the circuits are much more complex compared to the ACRDCL converter. The parallel resonant dc-link (PRDCL) converter with unity voltage stress proposed in [7] needs three additional switches. The quasi-resonant dc-link (QRDCL) converter proposed in [8] requires only two auxiliary switches and the auxiliary switch can be turned off under zero-current condition. The QRDCL inverter with coupled inductive feedback proposed in [9] further simplifies the circuit, which only needs one auxiliary switch, one diode, and one coupled inductor with two additional coils. The drawback is the voltage stress of the clamping diode is too high (4.3–11 p.u.). To overcome this problem, a new QRDCL inverter with some changes to the circuit in [9] is proposed in [10], which still only needs one auxiliary switch and can ensure soft-switching for all the switches. The device voltage stress is (1.01–1.10) times the dc-link voltage under all load conditions but the circuit requires a separate low-voltage dc source. The dc-rail zero-voltage-transition (ZVT) and zero-current-transition (ZCT) three-phase voltage source inverter proposed in [11] can be controlled by a modified SVM and provides ZVT or ZCT for the switches. However, the converter topology consists of three additional switches.

On the other hand, the ac-side soft-switching converters usually have much more complex topology compared to dc-side soft-switching converters, which can offer the advantages of PWM control and soft-switching without additional voltage or current stress in primary devices [12]–[24]. The auxiliary resonant circuit is added at the ac side for each phase and the resonant transitions occur separately when the corresponding main switch needs switching. The auxiliary resonant commutated pole converter proposed in [12] features zero-voltage switching for main switches and zero-current switching for auxiliary switches without affecting the standard PWM control. However, the midpoint voltage provided by split capacitors is susceptible to drift which may affect the operation of the resonant circuit. A transformer-assisted PWM ZVS pole inverter proposed in [13] adds one transformer for each phase leg to avoid using split capacitors but the auxiliary transformer may cause manufacturing penalty and complexity. A new ZVS PWM single-phase full-bridge inverter using a simple ZVS-PWM commutation cell without floating mid-point voltage is proposed in [14]. The main switches operate at ZVS and the auxiliary switches operate at ZCS. The ZVS inverters using coupled magnetics proposed in [15] can also avoid the capacitor voltage unbalance issue with the advantage of less current stress of the auxiliary switch and faster demagnetization. The ZVS timing requirement is also satisfied over the full load range by using the variable timing control [16], [17].

The ZVT topology with six auxiliary switches and three coupled resonant inductors achieves zero-voltage turn-on for main switches and zero-current turn-off for auxiliary switches [18], [19]. Three-phase can be independently controlled without any modification of SVM technique and the auxiliary switches only need to carry half of the phase current. However, the circuit topology is complicated and requires much more space. There have been several research works devoted to developing ZVT topologies with less than six switches [20], [21]. These topologies decrease the cost and space with fewer components but lead to some critical disadvantages which are not in the ZVT topology with six auxiliary switches. The ZCT converter proposed in [22] and [23] can achieve zero-current switching for all of the main and auxiliary switches and their antiparallel diodes, so the turn-off loss and diode reverse recovery related loss are almost eliminated. The only drawback is the requirement of six auxiliary switches and three *LC* resonant tanks. A simplified three-phase ZCT converter proposed in [24] uses only three auxiliary switches and can achieve zero-current turn-off for all the main and auxiliary switches and provide soft commutation for the diodes. The execution of ZCT requires no modifications to normal PWM algorithms but the resonant tank current stress is higher. A novel frequency inverter with a "sinus switch" to solve the EMI noise in conventional PWM inverter is proposed in [25]. A special ZVS control scheme with a variable switching frequency is proposed to control the inverter.

To combine the advantages of both dc-side and ac-side soft-switching converters, the authors proposed a ZVS-SVM-controlled three-phase PWM rectifier in [26] which has a similar topology to the ACRDCL converter. In contrast, the rectifier can be controlled by a modified SVM scheme proposed by the authors and can realize ZVS for both the main and auxiliary switches and soft turn-off of their antiparallel diodes. The auxiliary switch has the same fixed switching frequency as the main switches. However, the voltage stress of all the switches is still a little higher than the dc-link voltage.

Nowadays, SiC power electronic devices have superior performance. The SiC Schottky diode has almost no reverse-recovery process compared to Si diodes. The Si insulated gate bipolar transistor (IGBT) with antiparalleled SiC diode has been shown with very high efficiency [27]. In the future, SiC MOSFET will be used to realize higher efficiency converter. Soft-switching converter is one alternative. Besides the efficiency, soft-switching is also helpful for lower EMI. It is possible that the advantages of wide band gap devices may further be exploited by using soft-switching technology.

In this paper, a novel active clamping ZVS three-phase boost PWM rectifier is analyzed and a modified SVM strategy suitable for the novel ZVS rectifier is proposed. With the proposed SVM strategy, the novel rectifier can achieve ZVS for both the main and auxiliary switches. All the antiparallel diodes can be turned OFF softly, so the reverse recovery current is eliminated. Moreover, the voltage stress of both main and auxiliary switches is equal to the dc-link voltage. The turn-on losses of IGBTs and reverse recovery losses of antiparallel diodes can be avoided. But for ZVS switching, the turn-off losses of IGBTs can only partly be avoided because of the existence of the tail current [28].

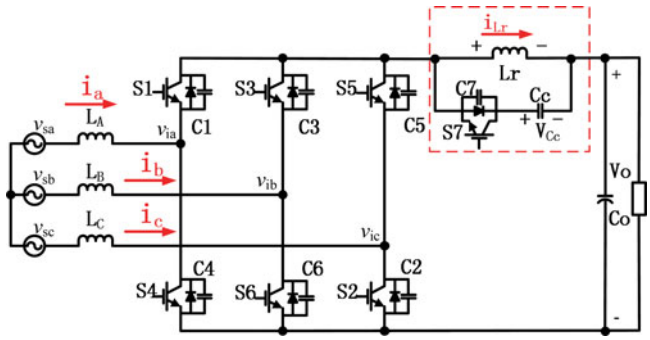


Fig. 2. Topology of the ZVS-SVM controlled three-phase PWM rectifier proposed in [26].

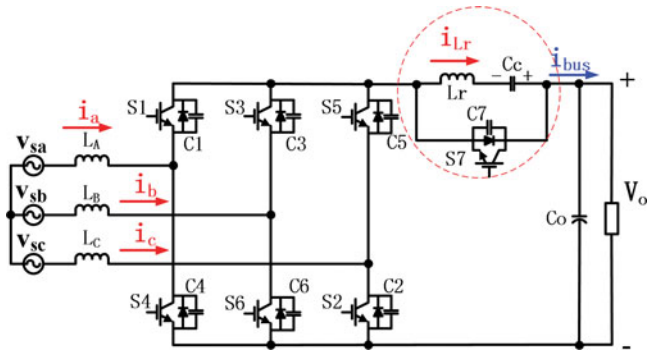


Fig. 3. Novel active clamping ZVS three-phase boost PWM rectifier.

The operation principle and design guidelines are described in detail. The experimental results of a 30 kW hardware prototype are presented to verify the theory in this paper.

II. Converter Topology and Operation Analysis

A. Converter Topology Derivation

Fig. 2 shows the topology of the ZVS-SVM-controlled three-phase PWM rectifier proposed in [26], which consists of a standard PWM rectifier and an auxiliary resonant branch. The auxiliary branch consists of an auxiliary active switch S_7, a resonant inductor L_r, and a clamping capacitor C_c. The auxiliary switch S_7 is conducting for most of the switching period. When the auxiliary switch S_7 is turned OFF, the energy stored in the resonant inductor L_r will discharge the parallel capacitors of the main switches. When the voltage of the capacitors paralleled with the main switches is discharged to be zero, the main switches can be turned ON under ZVS condition. Meanwhile, the current of the antiparallel diodes can be linearly decreased with the existence of L_r. Therefore, the reverse recovery current of the antiparallel diodes is effectively suppressed.

For the topology shown in Fig. 2, the voltage stress of the main and auxiliary switches is clamped to $V_o + V_{Cc}$, which will increase with the load power. With circuit parameter optimization, the voltage stress can be confined within 1.1 times of the dc-link voltage. To further decrease the voltage stress of the main and auxiliary switches, a novel active clamping ZVS three-phase boost PWM rectifier, as shown in Fig. 3 controlled by minimum voltage active clamping SVM method, is proposed in [29]. Compared with the topology shown in Fig. 2, only the position of the clamping capacitor C_c is changed, which will decrease the device voltage stress to the dc-link voltage. In [29], the existing ZVS-SVM control method proposed in [26] is adopted to control the rectifier shown in Fig. 3. But there still exists some problems in the soft-switching condition. This paper will further discuss the rectifier shown in Fig. 3 and find the solution.

B. Operation Analysis With Existing Modulation Scheme

Since the novel topology shown in Fig. 3 is very similar to the topology shown in Fig. 2, this paper will first discuss the operation principle of the novel ZVS rectifier adopting the existing ZVS-SVM control method proposed in [26].

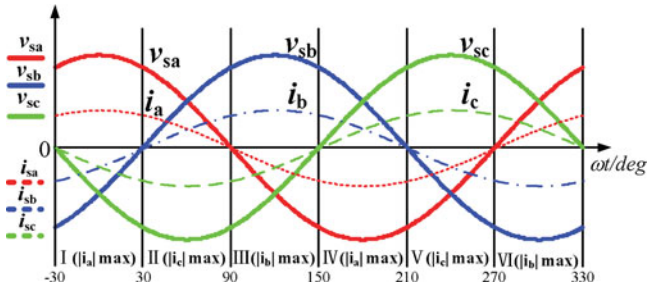


Fig. 4. Grid voltage and current waveforms.

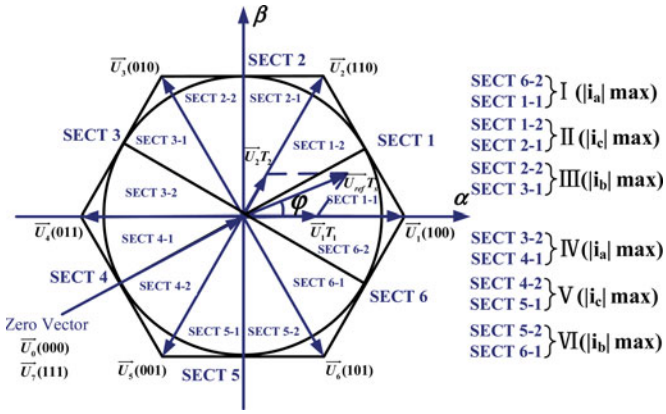


Fig. 5. Three-phase voltage space vectors diagram.

The rectifier always works with unit power factor, so the three-phase grid voltage and current waveforms can be shown in Fig. 4. Based on the analysis in [26], the traditional six voltage sectors can be further divided into 12 different smaller sectors according to the peak of grid current waveforms, as shown in Fig. 5. For example, sector SECT1 can be divided into SECT1-1 and SECT1-2. In SECT1-1, the current of phase A is the largest among three phases, and the switching status of phase A in the selected nonzero-vectors is "1" so that $\mathbf{U}_7(111)$ is chosen as the zero-vector to make sure there is no commutation of phase A in one switching cycle. In SECT1-2, the current of phase C is the smallest among three phases, and the switching status of phase C in the selected nonzero-vectors is "0" so that $\mathbf{U}_0(0\ 0\ 0)$ is chosen as the zero-vector to make sure there is no commutation of phase C in one switching cycle.

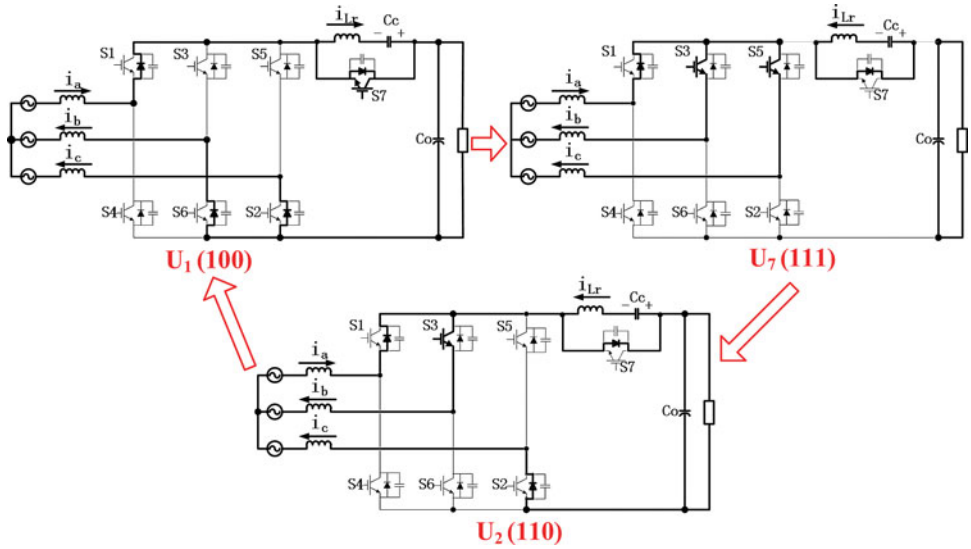


Fig. 6. Three switching states in the SECT1-1.

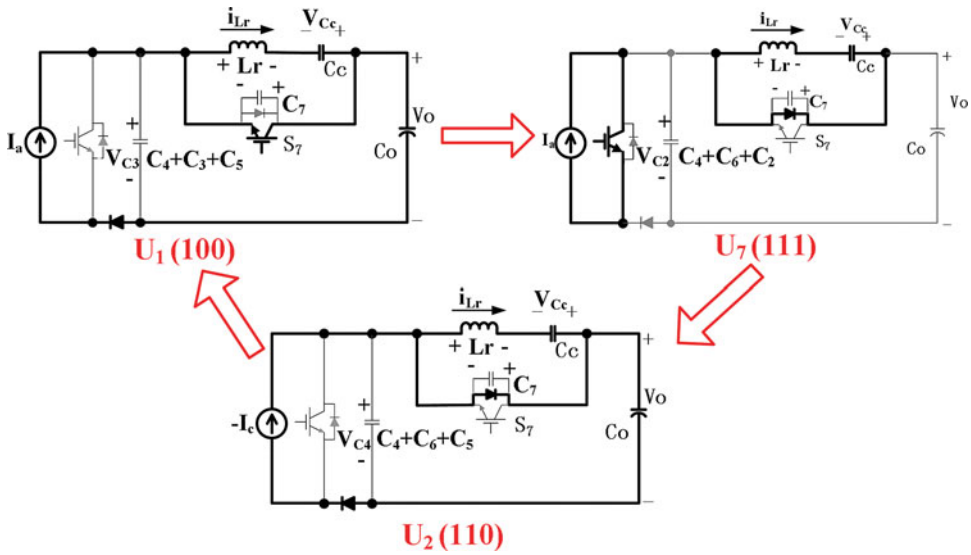


Fig. 7. Equivalent circuits of three switching states in the SECT1-1.

The auxiliary branch only operates once in each switching cycle to realize the ZVS of the main and auxiliary switches. Taking SECT1-1 as an example, the zero-vector $\mathbf{U}_7(1\ 1\ 1)$ should be placed after $\mathbf{U}_1(1\ 0\ 0)$, and $\mathbf{U}_2(1\ 1\ 0)$ follows $\mathbf{U}_7(1\ 1\ 1)$, as shown in Fig. 6.

As shown in Fig. 6, the antiparallel diode of switch S_1 in phase A is always conducting, while the switches in the other two phases are controlled in PWM manner. There are two kinds of commutations: one is from transistor to diode and the other is from diode to transistor. The switching state changing from $\mathbf{U}_7(1\ 1\ 1)$ to $\mathbf{U}_2(1\ 1\ 0)$ and from $\mathbf{U}_2(1\ 1\ 0)$ to $\mathbf{U}_1(1\ 0\ 0)$ are the former, in which the commutations are normally soft-switching and the auxiliary branch needs not act. Much more attention should be taken to the switching state changing from $\mathbf{U}_1(1\ 0\ 0)$ to $\mathbf{U}_7(1\ 1\ 1)$, which is the commutation from diode to transistor and needs to activate the auxiliary branch to realize ZVS.

The three switching states shown in Fig. 6 can be simplified as shown in Fig. 7. The three-phase grid current can be represented by a current source during one switching cycle, and the equivalent circuits of switching states $\mathbf{U}_1(1\ 0\ 0)$, $\mathbf{U}_7(1\ 1\ 1)$, and $\mathbf{U}_2(110)$ can be shown in Fig. 7.

With the existing ZVS-SVM control method proposed in [26], the operation principle of the novel ZVS rectifier in SECT1-1 is given as follows.

1) The auxiliary switch S_7 is in conduction during most of the time in one switching cycle. When the switching state changes from $\mathbf{U}_1(1\ 0\ 0)$ to $\mathbf{U}_7(1\ 1\ 1)$, the auxiliary switch S_7 is turned OFF first and then the resonance between L_r, $C_4 + C_3 + C_5$, and C_7 is initiated.
2) The energy in the resonant inductor L_r will discharge the parallel capacitor of the switches S_4, S_3, and S_5, and

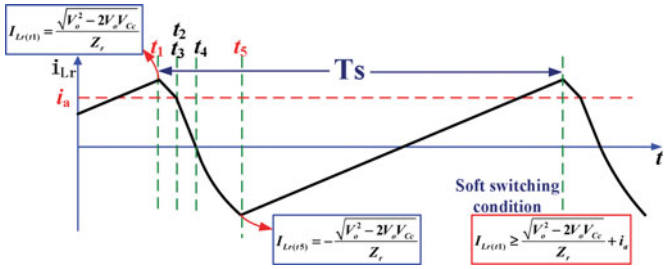


Fig. 8. Current waveform of the resonant inductor under existing modulation scheme.

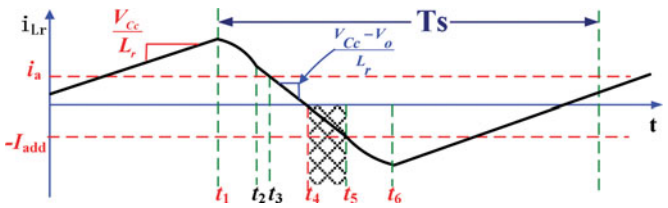


Fig. 9. Current waveform of the resonant inductor under proposed modulation scheme.

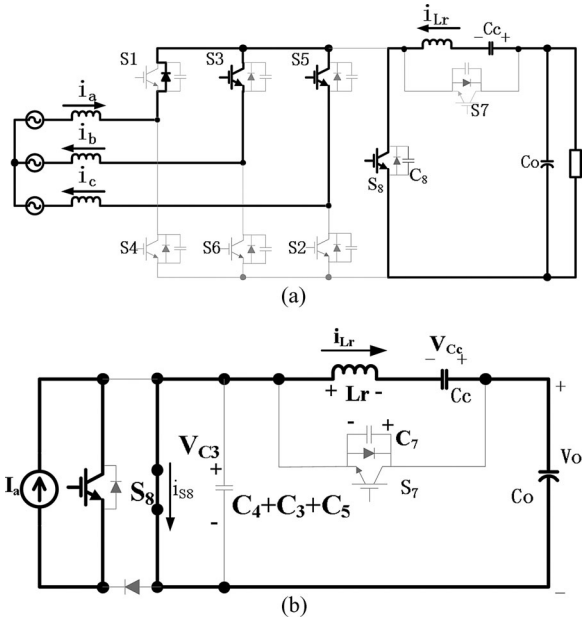


Fig. 10. Novel ZVS rectifier and its equivalent circuit. (a) Novel ZVS rectifier with one additional switch. (b) Equivalent circuit of the novel rectifier.

make the bridge voltage resonant to zero so that S_3 and S_5 can be ZVS turned ON.

3) And L_r can suppress the reverse recovery currents of S_6's and S_2's antiparallel diodes. After these switch antiparallel diodes finish the reverse recovery, the current of the resonant inductor starts to flow through the antiparallel diode of the auxiliary switch S_7. So the auxiliary switch S_7 is turned ON under ZVS condition.

The previous description is designed through qualitative analysis. Through quantitative analysis [29], the current waveform of L_r in one switching cycle and related soft-switching condition will be shown as Fig. 8.

In Fig. 8, it can be seen that the current of L_r in time t_1 is not large enough to satisfy the ZVS condition, which means the energy stored in the resonant inductor L_r is not enough to discharge the parallel capacitors of the switches and make the main switching bridge voltage resonant to zero.

III. Proposed Modulation Scheme and Operation Analysis

A. Proposed Suitable Modulation Scheme

In order to realize the ZVS condition, the energy stored in the resonant inductor L_r must be increased. The solution proposed in this paper is shown in Fig. 9, in which one additional stage (t_4–t_5) is inserted after stage 4 to make the current of L_r decrease linearly to a minus value $-I_{\rm add}$.

To realize the additional stage (t_4–t_5), one additional switch S_8 is paralleled across the main switch bridge, as shown in Fig. 10(a), which can be simplified as shown in Fig. 10(b). At t_4, the additional switch S_8 is turned ON and the voltage of the resonant inductor is clamped to $V_{Cc} - V_o$. Then, the energy stored in the resonant inductor L_r can be increased.

SECT1-1 is taken as an example to analyze. The additional stage is numbered stage 5 (t_4–t_5) as shown in Fig. 11(e). The stage analysis based on the equivalent circuit of the novel rectifier is shown in Fig. 11.

Assume the voltage of the clamping capacitor C_c is constant during one switching cycle, and the detailed sequences are explained as follows.

Stage 1 (t_0–t_1): The rectifier is in switching state $\mathbf{U}_1(1\ 0\ 0)$. In the auxiliary branch, the voltage of L_r is clamped by V_{Cc} and its current increases linearly. This stage ends when the auxiliary switch S_7 is turned OFF.

Stage 2 (t_1–t_2): At t_1, the auxiliary switch S_7 is turned OFF, which initiates the resonance between L_r, $C_4 + C_3 + C_5$, and C_7. The resonant inductor L_r discharges $C_4 + C_3 + C_5$ and charges C_7.

Stage 3 (t_2–t_3): At t_2, the voltage on $C_4 + C_3 + C_5$ drops to zero, and the antiparallel diodes of those main switches start to conduct. The resonance is stopped and the voltage of L_r is clamped by $V_{Cc} - V_o$.

Stage 4 (t_3–t_4): At t_3, the main switches S_3 and S_5 are turned ON under ZVS condition. The resonance is stopped and the voltage of L_r is clamped by $V_{Cc} - V_o$. As shown in Fig. 11(d), the diode is in series with the resonant inductor L_r, so the diode current decreases linearly. This stage ends when the current of the diode decreases to zero.

Stage 5 (t_4–t_5): At t_4, the antiparallel diodes of S_6 and S_2 are turned OFF and the current of L_r is equal to zero. To store much more energy in the resonant inductor L_r, S_8 is turned ON at t_4 under ZVS condition, so the main switch bridge is in short circuit. The voltage of L_r continues to be clamped by $V_{Cc} - V_o$.

Stage 6 (t_5–t_6): At t_5, S_8 is turned OFF, which starts the resonance between L_r, $C_4 + C_6 + C_2$, and C_7. The voltage on $C_4 + C_6 + C_2$ starts to increase and the voltage on S_7 starts to decrease. This stage ends when the voltage on S_7 decreases to zero and the antiparallel diode of S_7 starts to conduct.

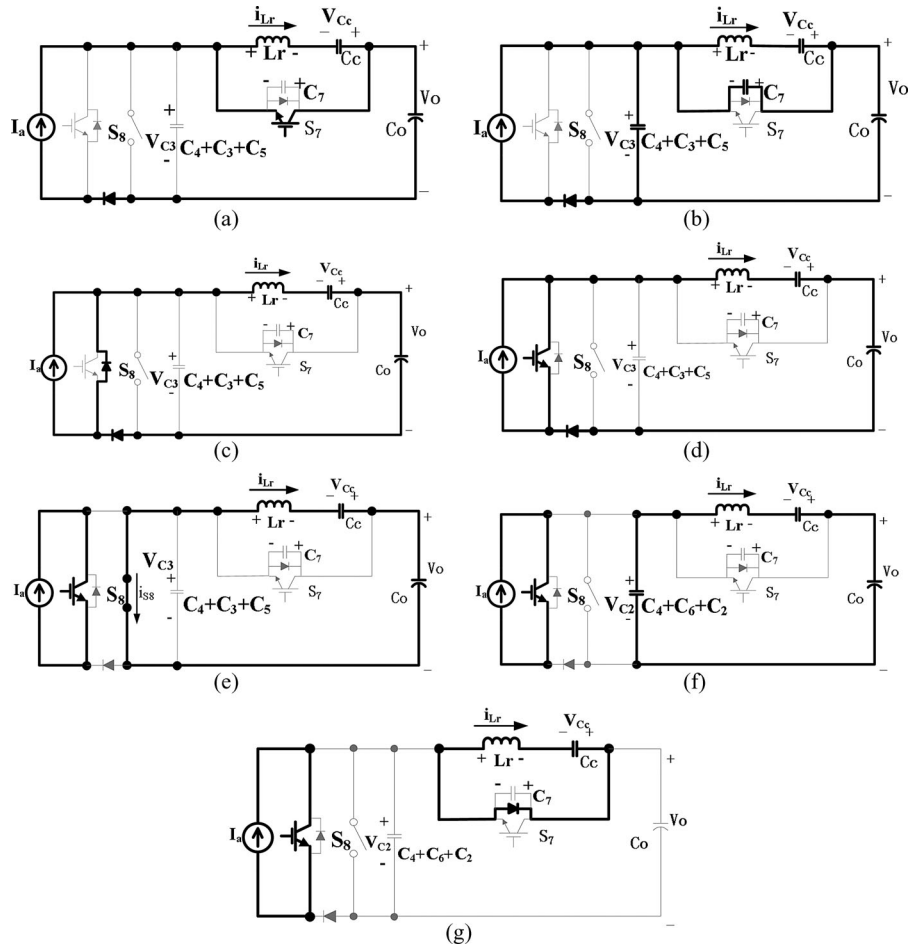


Fig. 11. Operation stages of the novel ZVS rectifier based on the equivalent circuit. (a) Stage 1 (t_0–t_1). (b) Stage 2 (t_1–t_2). (c) Stage 3 (t_2–t_3). (d) Stage 4 (t_3–t_4). (e) Stage 5 (t_4–t_5). (f) Stage 6 (t_5–t_6). (g) Stage 7 (t_6–t_7).

Stage 7 (t_6–t_7): At t_6, the main switches S_1, S_3, S_5 and the auxiliary switch S_7 are ON. The resonance between L_r, $C_4 + C_6 + C_2$ and C_7 stops and then the rectifier enters switching state $\mathbf{U}_7$(1 1 1).

Looking at Fig. 10, the additional switch S_8 can be replaced by making the main switch bridge in short circuit. Then, the traditional modulation scheme should be modified as shown in Fig. 13. At t_4, turning ON one or two or all of the three main switches S_4, S_6, S_2 can make the main switch bridge in short circuit to replace the function of the additional switch S_8.

B. Operation Principle With the Proposed Modulation Scheme

With the proposed modulation scheme shown in Fig. 13, the three-phase rectifier stage analysis is given as follows. SECT1-1 is still taken as an example to analyze. The operation stages and key waveforms of the novel three-phase ZVS rectifier during a whole switching cycle are shown in Figs. 12 and 13 separately.

It is assumed that the voltage of the clamping capacitor C_c is constant during one switching cycle. From Fig. 12, the complete circuit operation in one switching cycle can be divided into ten stages.

Stage 1 (t_0–t_1): The rectifier is in switching state $\mathbf{U}_1$(1 0 0). The main switches S_1, S_2, S_6 and the auxiliary switch S_7 are conducting. The voltage of L_r is clamped by V_{Cc} and its current increases at the rate of

$$\frac{di_{Lr}}{dt} = \frac{V_{Cc}}{L_r}. \tag{1}$$

This stage ends when the auxiliary switch S_7 is turned OFF.

Stage 2 (t_1–t_2): At t_1, the auxiliary switch S_7 is turned OFF, which initiates the resonance between L_r, C_4, C_3, C_5, and C_7. During this resonant stage, the resonant inductor L_r discharges C_4, C_3, C_5, and charges C_7. This stage ends when the voltage of C_4, C_3, and C_5 decreases to zero, which makes the antiparallel diodes of main switches S_4, S_3, S_5 conduct.

Stage 3 (t_2–t_3): At t_2, the antiparallel diodes of main switches S_4, S_3, S_5 start to conduct and the resonance is stopped. The voltage of L_r is clamped by $V_{Cc} - V_o$, so the current of L_r decreases at the rate of

$$\frac{di_{Lr}}{dt} = \frac{V_{Cc} - V_o}{L_r}. \tag{2}$$

This stage ends when the current of the antiparallel diodes decreases to zero.

Stage 4 (t_3–t_4): At t_3, the main switches S_3 and S_5 are turned ON under ZVS condition, so the voltage of L_r is clamped by $V_{Cc} - V_o$. As shown in Fig. 12(d), with the existence of the

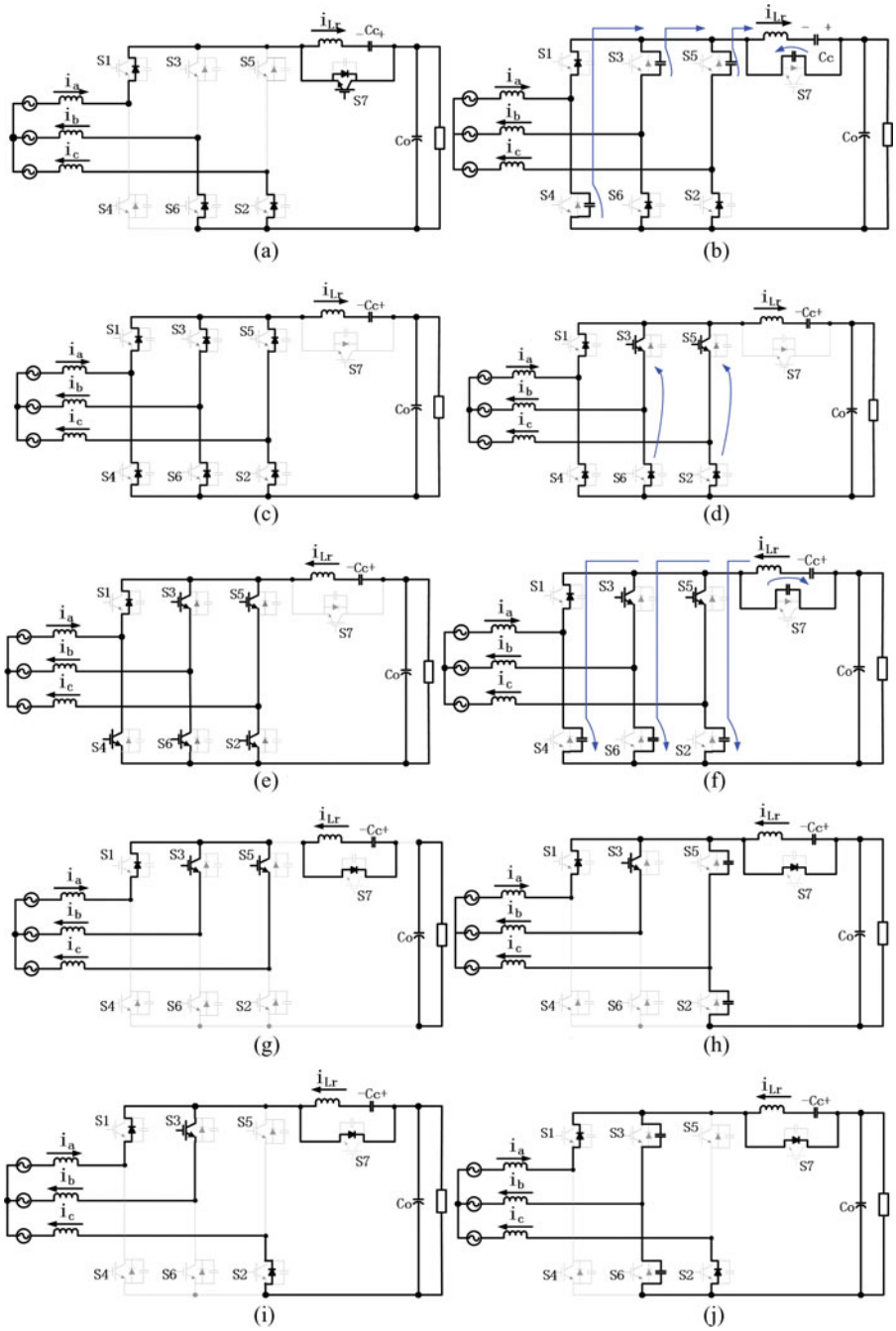


Fig. 12. Operation stages of soft-switching rectifier. (a) Stage 1 (t_0–t_1). (b) Stage 2 (t_1–t_2). (c) Stage 3 (t_2–t_3). (d) Stage 4 (t_3–t_4). (e) Stage 5 (t_4–t_5). (f) Stage 6 (t_5–t_6). (g) Stage 7 (t_6–t_7). (h) Stage 8 (t_7–t_8). (i) Stage 9 (t_8–t_9). (j) Stage 10 (t_9–t_{10}).

resonant inductor L_r, the antiparallel diodes of S_6 and S_2 current will decrease linearly with a slope of (2). When this slope is less than 100 A/μs, the diode reverse recovery will be eliminated. This stage ends when the current of the diodes decreases to zero and meanwhile the resonant inductor L_r current decreases to zero too.

Stage 5 (t_4–t_5): At t_4, when the voltage of the main switch bridge is still zero, one or two or three of the three switches S_4, S_6, and S_2 is turned ON under ZVS condition, so the switch bridge is in short circuit. The voltage of L_r is continuing to be clamped by $V_{Cc} - V_o$, and L_r current changes at the rate of (2). This stage ends when S_4, S_6, and S_2 are turned OFF.

Stage 6 (t_5–t_6): At t_5, S_4, S_6, and S_2 are turned OFF, which starts the resonance between L_r, C_4, C_6, C_2, and C_7. The voltage on C_4, C_6, and C_2 starts to increase and the voltage on C_7 starts to decrease. This stage ends when the voltage on C_7 decreases to zero and the antiparallel diode of S_7 starts to conduct.

Stage 7 (t_6–t_7): At t_6, the main switches S_1, S_3, S_5 and the auxiliary switch S_7 are ON. The resonance between L_r, C_r, and C_7 stops and then the rectifier enters switching state

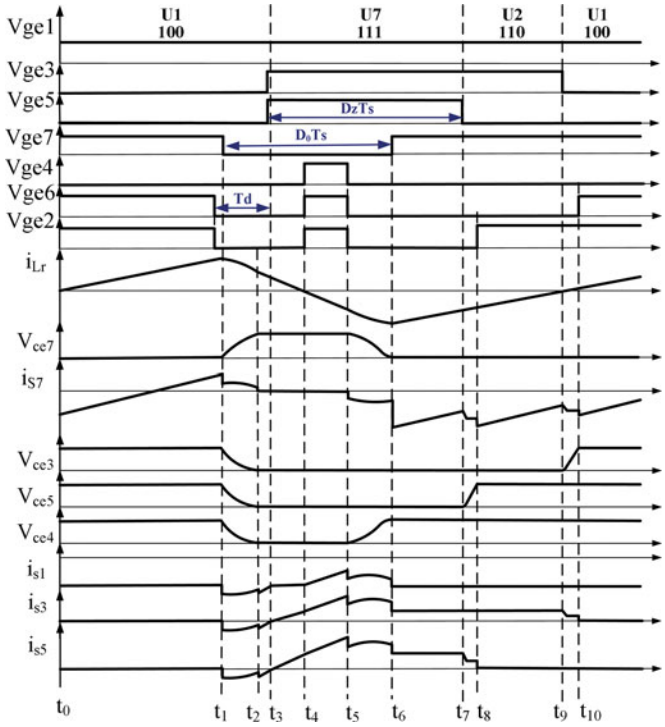


Fig. 13. Operation stage waveforms of the ZVS rectifier in one switching cycle of SECT1-1.

$\mathbf{U}_7$(1 1 1). The resonant inductor is clamped by V_{Cc}, and its current increases at the rate of (1). This stage ends when the main switch S_5 is turned OFF.

Stage 8 (t_7–t_8): At t_7, S_5 is turned OFF. Because of the existence of C_5 and C_2, the voltage of C_5 is slowly rising. When the voltage of C_5 increases to V_o, this stage ends.

Stage 9 (t_8–t_9): At t_8, the main switch S_1, S_3, S_2 and the auxiliary switch S_7 are ON. The circuit enters the state $\mathbf{U}_2$(1 1 0). The resonant inductor is clamped by V_{Cc} and its current increases at the rate of (1). This stage ends when the main switch S_3 is turned OFF.

Stage 10 (t_9–t_{10}): At t_9, S_3 is turned OFF. Because of the existence of C_3 and C_6, the voltage of C_3 is slowly rising. When the voltage of C_3 increases to V_o, this stage ends and the circuit enters state $\mathbf{U}_1$(1 0 0), which repeats the next switching cycle.

IV. Theoretical Analysis of the Novel ZVS Rectifier

A. Resonant Process Analysis

To find the ZVS soft-switching condition, the resonant stage 2 (t_1–t_2) and stage 6 (t_5–t_6) should be analyzed. Suppose that $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C$ and define three parameters

$$\begin{cases} C_r = 3C + C_7 \\ Z_r = \sqrt{\dfrac{L_r}{C_r}} \\ \omega = \dfrac{1}{\sqrt{L_r C_r}}. \end{cases} \tag{3}$$

The first resonant process is in stage 2 (t_1–t_2) as shown in Fig. 12(b), and the equivalent circuit is shown in Fig. 11(b). Making t_1 as the initial time, the loop differential equation and initial condition can be represented as

$$\begin{cases} C_r \dfrac{dv_{C_3}}{dt} = I_a - i_{Lr} \\ L_r \dfrac{di_{Lr}}{dt} = v_{C_3} - V_o + V_{Cc} \\ \begin{cases} v_{C_3}(0) = V_o \\ i_{Lr}(0) = I_{Lr(t_1)}. \end{cases} \end{cases} \tag{4}$$

By solving (4), the voltage across the main switch S_3 and the current of the resonant inductor L_r will be

$$\begin{cases} v_{C_3}(t) = V_o - V_{Cc} + V_{Cc}\cos\omega t + \left(i_a - I_{Lr(t_1)}\right)\cdot Z_r \sin\omega t \\ i_{Lr}(t) = i_a + \dfrac{V_{Cc}}{Z_r}\sin\omega t - \left(i_a - I_{Lr(t_1)}\right)\cos\omega t. \end{cases} \tag{5}$$

In the resonant stage 2, the main switches can realize ZVS only when the voltage of C_3 crosses zero. From (5), the ZVS condition of the main switches can be represented as

$$\begin{cases} I_{Lr(t_1)} \geq \dfrac{\sqrt{V_o^2 - 2V_o V_{Cc}}}{Z_r} + i_a \\ i_a = I_m \cos\phi, \quad 0 \leq \phi \leq \dfrac{\pi}{6}. \end{cases} \tag{6}$$

According to the aforementioned stage analysis, at t_4, the resonant inductor L_r current i_{Lr} is equal to zero. In stage 5, the voltage of L_r is clamped by $V_{Cc} - V_o$, so at t_5, the additional current of L_r will be

$$I_{Lr(t_5)} = -I_{\text{add}} = \frac{V_{Cc} - V_o}{L_r}(t_5 - t_4). \tag{7}$$

The second resonant process is in stage 6 (t_5–t_6) as shown in Fig. 12(f) and the equivalent circuit is shown in Fig. 11(f). Assuming t_4 as the initial point, the loop differential equation and initial condition can be represented as

$$\begin{cases} (3C + C_7)\dfrac{dv_{C_2}}{dt} = -i_{Lr} \\ L_r \dfrac{di_{Lr}}{dt} = v_{C_2} - V_o + V_{Cc} \\ \begin{cases} v_{C_2}(0) = 0 \\ i_{Lr}(0) = I_{Lr(t_5)}. \end{cases} \end{cases} \tag{8}$$

By solving (8), the voltage across the main switch S_2 and the current of the resonant inductor L_r will be

$$\begin{cases} v_{C_2}(t) = (V_{Cc} - V_o)\cos\omega t - I_{Lr(t_5)} Z_r \sin\omega t + V_o - V_{Cc} \\ i_{Lr} = \dfrac{V_{Cc} - V_o}{Z_r}\sin\omega t + I_{Lr(t_5)}\cos\omega t. \end{cases} \tag{9}$$

At t_6, the voltage of C_7 decreases to zero and the voltage of C_2 arrives to V_o. From (9), the current of L_r in t_6 can be

calculated as

$$I_{Lr(t_6)} = i_{Lr}(t_6) = -\frac{\sqrt{V_o^2 - 2V_oV_{Cc} + (Z_rI_{Lr(t_5)})^2}}{Z_r}. \quad (10)$$

From Fig. 12(f), the voltage of C_7 can be represented as

$$v_{C_7}(t) = V_{Cc} + (V_o - V_{Cc})\cos\omega t + I_{Lr(t_5)}Z_r\sin\omega t. \quad (11)$$

The ZVS condition of S_7 is the voltage of C_3 represented as (11) crosses zero.

B. Soft-Switching Condition Analysis

When in steady state, according to the theory of magnetic flux balance of the resonant inductor L_r, the mean voltage of the resonant inductor will be zero

$$\begin{aligned}\int_0^{T_s} u_{Lr}dt &= \int_{t_0}^{t_1} u_{Lr}dt + \int_{t_1}^{t_2} u_{Lr}dt + \int_{t_2}^{t_5} u_{Lr}dt \\ &\quad + \int_{t_5}^{t_6} u_{Lr}dt + \int_{t_6}^{t_{10}} u_{L_1}dt \\ &\approx V_{Cc}(1-D_0)T_s - (V_o - V_{Cc})D_0T_s = 0. \quad (12)\end{aligned}$$

Here, the short-lived state (t_1–t_2), (t_5–t_6) have been ignored, and D_0 is the auxiliary switch turn-off duty cycle, then the voltage of the clamping capacitor C_c is

$$V_{Cc} = D_0V_o. \quad (13)$$

Since the auxiliary switch turn-off duty cycle $D_0 \ll 1$, the clamping capacitor voltage $V_{Cc} \ll V_o$. Then, according to (11), it is easy for the voltage across S_7 to decrease to zero. So, the auxiliary switch is always turned ON under ZVS condition.

On the other hand, according to the theory of the charge balance of the clamping capacitor C_c, the mean current of the clamping capacitor will be zero

$$\begin{aligned}\int_0^{T_s} i_{Cc}dt &= -I_{Lr(t_6)}T_s - \frac{V_{Cc}}{L_r}(1-D_0)D_0T_s^2 \\ &\quad + \frac{V_o - V_{Cc}}{2L_r}(D_0T_s)^2 - \frac{V_{Cc}}{2L_r}(1-D_0)^2T_s^2 = 0.\end{aligned} \quad (14)$$

By solving (14), the auxiliary switch turn-off duty cycle D_0 will be

$$D_0 \approx \frac{2L_r\sqrt{(V_o/Z_r)^2 + (V_o - V_{Cc}/L_r)^2(t_5-t_4)^2}}{V_oT_s}. \quad (15)$$

As Fig. 3 shows, the resonant inductor L_r is in series with the clamping capacitor C_c, so the mean value of resonant inductor L_r current i_{Lr} will be zero too. Based on that and (10), the current of L_r in t_1 can be calculated as

$$I_{Lr(t_1)} = -I_{Lr(t_6)} = \frac{\sqrt{V_o^2 - 2V_oV_{Cc} + (Z_rI_{Lr(t_5)})^2}}{Z_r}. \quad (16)$$

Combining (6), (7), and (16), the ZVS condition for the main switches will be

$$(t_5 - t_4) \geq \frac{L_r}{V_o - V_{Cc}}\sqrt{\frac{2I_m\sqrt{V_o^2 - 2V_oV_{Cc}}}{Z_r} + I_m^2}. \quad (17)$$

In (17), I_m is the maximum value of the input phase current. From (17), in order to realize the ZVS condition of the main switches, the duration time of stage 5 must be long enough to store enough energy in the resonant inductor.

C. Discussion of Three Different Modulation Schemes

In stage 5 (t_4–t_5), as shown in Fig. 12(e), three main switch legs are all in short circuit to store enough energy in the resonant inductor L_r. However, choosing any one of the three switching legs to be in short circuit will satisfy the requirement, which generates different modulation schemes. Three different modulation schemes are discussed and compared as follows.

1) Modulation 1 (one switch leg fixed in short circuit): In every sector, the main switch leg of phase A is always chosen to be in short circuit in stage 5 (t_4–t_5). This method only modifies the driving signal of phase A and is very easy to realize. However, the main switch current stress of phase A will be increased by the additional resonant inductor current $I_{\rm add}$. According to grid current waveforms shown in Fig. 4 and (7), the current stress of the main switches of phase A can be derived as

$$I_{Sa\_\max} = \frac{\sqrt{3}}{2}I_m + \frac{V_o - V_{Cc}}{L_r}(t_5 - t_4). \quad (18)$$

2) Modulation 2 (three switch legs all in short circuit): As shown in Fig. 12(e), three switch legs are all chosen to be in short circuit in stage 5. Taking SECT1-1 as an example, the maximum current of S_2 is i_c added by 1/3 of the additional resonant inductor current $I_{\rm add}$. Since the operation is symmetrical in every sector, the current stress of the main switches will be the maximum value of i_c in SECT1-1 added by 1/3 of the additional resonant inductor current $I_{\rm add}$. According to grid current waveforms shown in Fig. 4 and (7), the current stress of the main switches can be derived as

$$I_{S\_\max} = \frac{\sqrt{3}}{2}I_m + \frac{V_o - V_{Cc}}{3L_r}(t_5 - t_4). \quad (19)$$

3) Modulation 3 (one of three switch legs taking turns in short circuit): According to the extreme of grid current waveforms shown in Fig. 4, when the absolute value of phase A current is the largest among three phases, S_1 and S_4 of phase A switch leg is chosen in short circuit. When the absolute value of phase B current is the largest, S_3 and S_6 of phase B switch leg is chosen in short circuit. When the absolute value of phase C current is the largest, S_5 and S_2 of phase C leg is chosen in short circuit.

For example, in SECT1-1, the absolute value of phase A current is the largest among three phases, so S_1 and S_4 of phase A switch leg is chosen in short circuit in stage 5 (t_4–t_5). The equivalent circuit of stage 5 (t_4–t_5) can be shown as Fig. 14(a). The current waveforms of the main switches S_1 and S_4 are shown in Fig. 14(b). From Fig. 14(b), the maximum current of S_4 is the additional resonant inductor current $I_{\rm add}$ and the

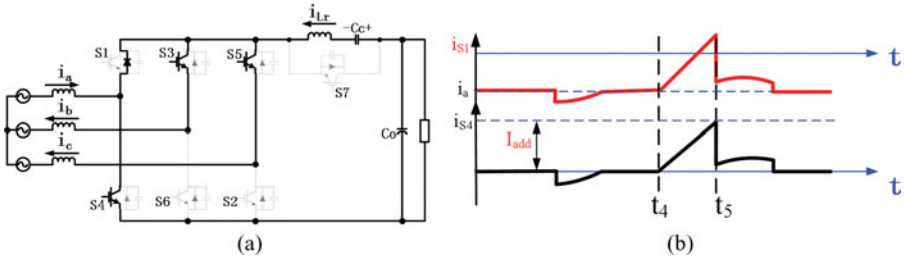


Fig. 14. Current stress of the main switches under one of three switch legs taking turns in short circuit. (a) Stage 5 (t_4–t_5). (b) Current waveforms of the main switches of phase A.

maximum current of S_1 is the maximum phase current I_m. Since the operation of the converter is symmetrical in every sector, the current stress of the main switches will be the maximum value of I_m and $I_{\rm add}$, which can be represented as

$$I_{S\_\max} = \max\left(I_m, \frac{V_o - V_{Cc}}{L_r}(t_5 - t_4)\right). \tag{20}$$

V. Design Guidelines

A. Resonant Parameters Optimization

In the novel ZVS three-phase boost PWM rectifier shown in Fig. 3, the resonant parameters include the inductance of the resonant inductor L_r, the resonant capacitors $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C$, and C_7. These parameters have much influence on the efficiency of the rectifier and must be optimized.

Base on the previous theoretical analysis, the design guidelines of the novel ZVS three-phase boost PWM rectifier are presented as follows.

1) Choosing resonant cycle T_r according to dead time $t_{\rm dead}$. According to the switch driving signals shown in Fig. 13, the duration time of stage 2 (t_1–t_2) $t_{\rm stage2}$ should be less than dead time $t_{\rm dead}$.
2) According to Fig. 12(d), to effectively suppress the reverse recovery current of the antiparallel diodes, the *di/dt* of the diodes must be confined to less than 100 A/μs in stage 4, which requires the resonant inductor be large enough.
3) According to (17), the duration time of stage 5 must be larger than a value to realize ZVS of the main switches. On the other hand, the duration time of stage 5 also determines the additional current of the resonant inductor $I_{\rm add}$ represented as (7), which should be minimized to decrease the turn-off losses of the main switches at t_5. The resonant tank impedance Z_r is also determined to minimize current $I_{\rm add}$.
4) According to the switch driving signals shown in Fig. 13, the auxiliary switch turn-off duty cycle D_0 should be less than the duty cycle of zero-vector in a PWM period D_z. Otherwise, D_0 will occupy the duty cycle of nonzero-vector, which will distort the input current waveforms.
5) Combining all the aforementioned conditions, a feasible parameters region will be obtained. Considering turn-off loss reduction, C_r is selected to be the maximum value of the feasible region. Then, a group of optimized resonant parameters will be confirmed.

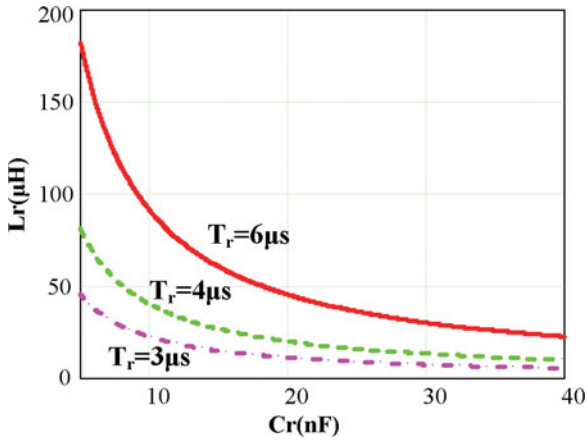


Fig. 15. Resonant cycle T_r versus C_r and L_r.

The working condition of the novel ZVS three-phase boost PWM rectifier designed in this paper is given as follows.

1) input phase voltage V_{sa}: 220 $V_{\rm rms}$;
2) output dc voltage V_o: 700 V;
3) switching frequency f_s: 16 kHz;
4) maximum output power $P_{\rm omax}$: 30 kW.

Following the optimization steps mentioned previously, the resonant parameters can be designed as follows.

1) The dead time $t_{\rm dead}$ is selected to be 3 μs, which is about 5% of the switching period. From the stage analysis, the maximum duration time of stage 2 (t_1–t_2) will be

$$t_{\rm stage2(max)} = \frac{1}{4}T_r = \frac{\pi}{2}\sqrt{L_r(3C + C_7)}. \tag{21}$$

Considering $t_{\rm stage2}$ should be less than dead time $t_{\rm dead}$, the resonant cycle T_r is confined to be less than 6 μs. The relationship between the resonant cycle T_r and the resonant parameters can be seen in Fig. 15, in which the parameter C_r is defined in (3).
2) According to Fig. 12(d), the *di/dt* of the resonant inductor should be lower than 100 A/μs to suppress the reverse recovery of the antiparallel diodes. Since the output voltage is 700 $V_{\rm DC}$, the inductance of L_r should be larger than 7 μH.
3) According to the ZVS condition shown in (17), the duration time of stage 5 should be as long as possible to store enough energy in the resonant inductor. However, lengthening the duration time of stage 5 will increase the

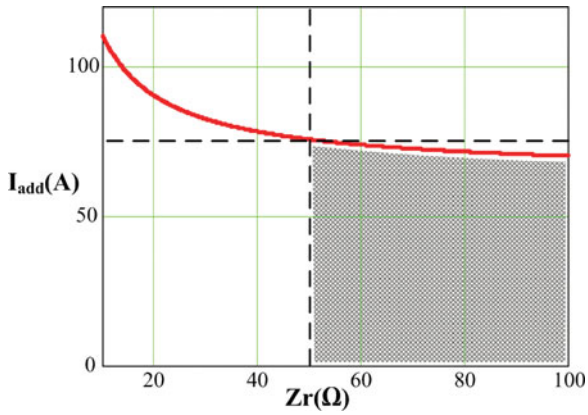


Fig. 16. Additional current $I_{\rm add}$ versus Z_r.

additional current of the resonant inductor $I_{\rm add}$, which will lead to higher turn-off loss of the main switches.

To optimize the efficiency of the novel ZVS three-phase rectifier, the duration time of stage 5 should be chosen to be the minimum value that can realize ZVS of the main switches. Then, based on (17) and (7), the additional current of L_r will be

$$I_{\rm add} = \sqrt{\frac{2I_m\sqrt{V_o^2 - 2V_oV_{Cc}}}{Z_r} + I_m^2} \qquad (22)$$

where the resonant tank impedance Z_r is defined in (3).

From (22), the additional current $I_{\rm add}$ decreases when the resonant tank impedance Z_r increases. When $P_o = 30\,\text{kW}$, $V_o = 700\,\text{V}_{\rm DC}$, the relationship between Z_r and additional current $I_{\rm add}$ is shown in Fig. 16. As reducing the current $I_{\rm add}$ is useful to decrease the turn-off loss of the main switches at t_5, the resonant tank impedance Z_r is chosen to be larger than 50 Ω, after which the $I_{\rm add}$ value decreases little.

4) For SVM strategy, the duty cycle of zero-vector in a PWM period D_z can be expressed as

$$D_z = 1 - \frac{\sqrt{6}V_{sa}}{V_o}\sin\left(\frac{\pi}{3} + \phi\right), \quad 0 \le \phi \le \frac{\pi}{6}. \qquad (23)$$

When the input phase voltage $V_{sa} = 220\ \text{V}_{\rm rms}$, $V_o = 700\,\text{V}_{\rm DC}$, the minimum value of D_z is about 0.23. When the duration time of stage 5 is chosen to be the minimum value that can realize ZVS of the main switches, combining (17) and (15), the auxiliary switch turn-off duty cycle D_0 will be

$$D_0 \approx \frac{(I_m + V_o/Z_r)\,2L_r}{T_sV_o}. \qquad (24)$$

Based on (24), the relationship between the auxiliary switch turn-off duty cycle D_0 and resonant parameters L_r, C_r is shown in Fig. 17. In order to make sure the auxiliary switch turn-off duty cycle D_0 is smaller than the zero-vector duty cycle D_z, the resonant inductance L_r should be less than 50 μH.

5) Based on the previous analysis, the feasible solution of the resonant parameters will be confined to a small region

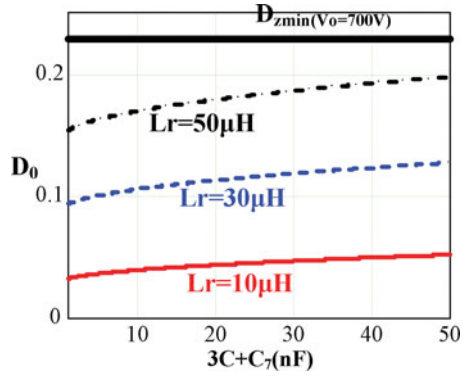


Fig. 17. Additional current D_0 versus L_r and C_r.

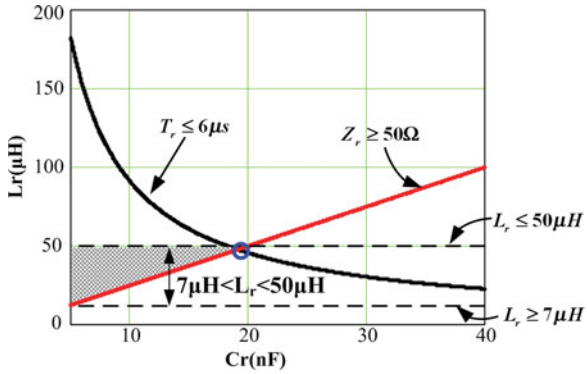


Fig. 18. Feasible solution of the resonant parameters.

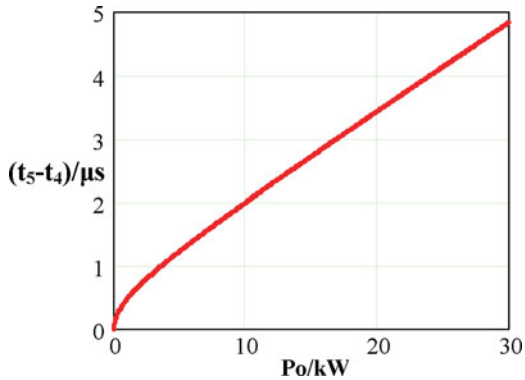


Fig. 19. Duration time of stage 5 versus P_o.

shown in Fig. 18. For the novel ZVS three-phase rectifier shown in Fig. 3, larger capacitance of the resonant capacitor C_r is good for decreasing the turn-off losses of the switches. So the optimized resonant parameters can be selected as follows: $L_r = 45\ \mu$H and $C_r = 19$ nF.

B. Some Results Under Optimized Parameters

Taking the optimized parameters to (17), the minimum duration time of stage 5 at different output power can be drawn as in Fig. 19. From Fig. 19, the duration time of stage 5 should be increased by the output power of the rectifier.

Taking the optimized parameters to (18)–(20), the main switch current stress under three different modulations discussed

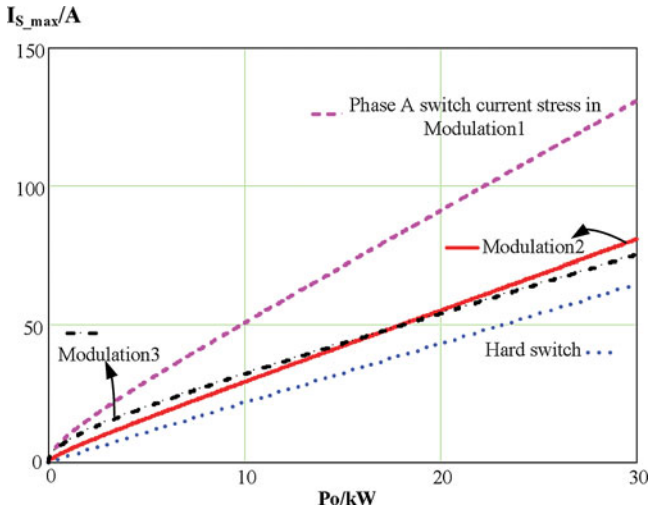


Fig. 20. Current stress of the main switches under three modulation schemes versus P_o.

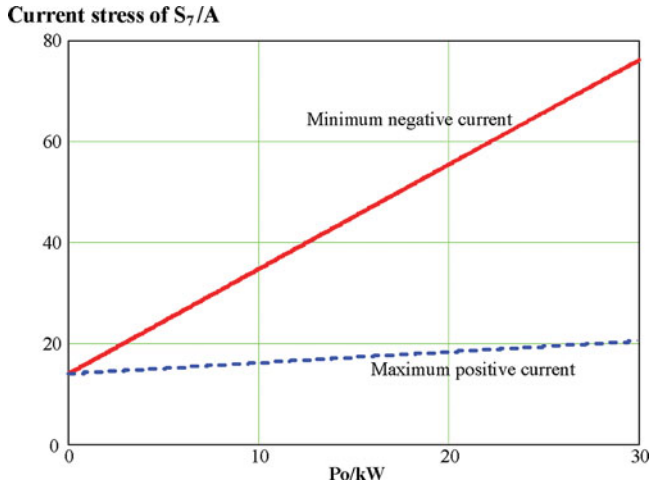


Fig. 21. Current stress of auxiliary switch S_7 versus P_o.

previously can be drawn as in Fig. 20. From Fig. 20, in modulation 1, the main switch current stress of phase A is about two times that in hard switch condition. In modulations 2 and 3, the main switch current stress is about 1.2 times that in hard switch condition.

According to the current waveform of the auxiliary switch i_{S7}, shown in Fig. 13, the antiparallel diode of S_7 is flowing current for most of the one switching cycle. From (16) and (22), when in the optimized ZVS condition, the maximum positive current flowing in the IGBT of S_7 in t_1 will be

$$i_{S_7(t_1)} = \frac{\sqrt{V_o^2 - 2V_oV_{Cc}}}{Z_r} + I_m - \frac{\sqrt{3}}{2}I_m. \qquad (25)$$

From i_{S7} waveform shown in Fig. 13, the minimum negative current of S_7 is equal to the resonant inductor current in t_6. Then, based on (10) and (22), when in optimized ZVS condition, the minimum negative current flowing the antiparallel diode of S_7 in t_6 will be

$$i_{S_7(t_6)} = i_{Lr(t_6)} = -\frac{\sqrt{V_o^2 - 2V_oV_{Cc}}}{Z_r} - I_m. \qquad (26)$$

Taking the optimized parameters to (25) and (26), the current stress of the auxiliary switch S_7 at different output power can be drawn as in Fig. 21. In Fig. 21, the minimum negative current is much larger than the maximum positive current due to the power flow of the rectifier.

VI. Simulation Verification

To verify the theory discussed previously, a simulation model based on Orcad software is built. The input and output voltage is 220 V_{AC} and 700 V_{DC}. The switching frequency is 16 kHz. The resonant capacitor $C_1 = C_2 = \cdots = C_6 = C = 5.7$ nF, $C_7 = 2$ nF. The resonant inductor $L_r = 45$ μH. The clamping capacitor $C_c = 100$ μF.

Based on the previous discussion, there are three different modulation schemes suitable for the novel ZVS rectifier. Modulation 1 will be implemented in the experiment later. The simulation results of modulations 2 and 3 will be given here. Based on modulation 2, all the three switch legs are in short circuit in stage 5, the waveforms of CE voltage and C→E current of the main switch S_1 are shown in Fig. 22. From Fig. 22, the main switch is turned ON under ZVS condition.

Based on modulation 3, making one switch leg flowing the extreme phase current in short circuit in stage 5, the waveforms of CE voltage and C→E current of the main switch S_1 are shown in Fig. 23(a). From Fig. 23(a), the main switch is turned ON under ZVS condition. At that moment, the absolute value of phase C current is the largest, so S_5 and S_2 of phase C leg is chosen to be in short circuit. The waveform of C→E current of the main switch S_5 and S_2 is shown in Fig. 23(b). The additional current $I_{\rm add}$ is larger than the maximum phase current I_m, so the current stress will be $I_{\rm add}$ according to (20).

The waveform of the auxiliary switch current and voltage is shown in Fig. 24, which is the same in all the three modulations. From Fig. 24, the antiparallel diode is in conduction before the auxiliary switch is turned ON, so the auxiliary switch can be turned ON under ZVS condition.

VII. Experimental Results

A 30 kW prototype of the novel ZVS three-phase boost PWM rectifier, as shown in Fig. 25, is built to verify the theory. It is controlled by DSP (TMS320F2407A). The input and output voltage is 220 V_{AC} and 700 V_{DC}. The input filter inductor $L_A = L_B = L_C = 0.3$ mH. The switching frequency is 16 kHz. The resonant capacitor $C_1 = C_2 = \cdots = C_6 = C = 5.7$ nF, $C_7 = 2$ nF. The resonant inductor $L_r = 45$ μH. The clamping capacitor $C_c = 100$ μF. Main and auxiliary switches S_1–S_7 are IGBT module CM200DU-24NFH (1200 V/200 A).

According to (13) and (15), the clamping capacitor voltage V_{Cc} is determined by the resonant parameters, output voltage, and output power. So the voltage V_{Cc} does not need a control loop to control. When the circuit is started up, the voltage V_{Cc} is built up automatically according to the output voltage.

The control algorithm of the novel ZVS rectifier is the same as hard-switching, which consists of outer voltage loop and

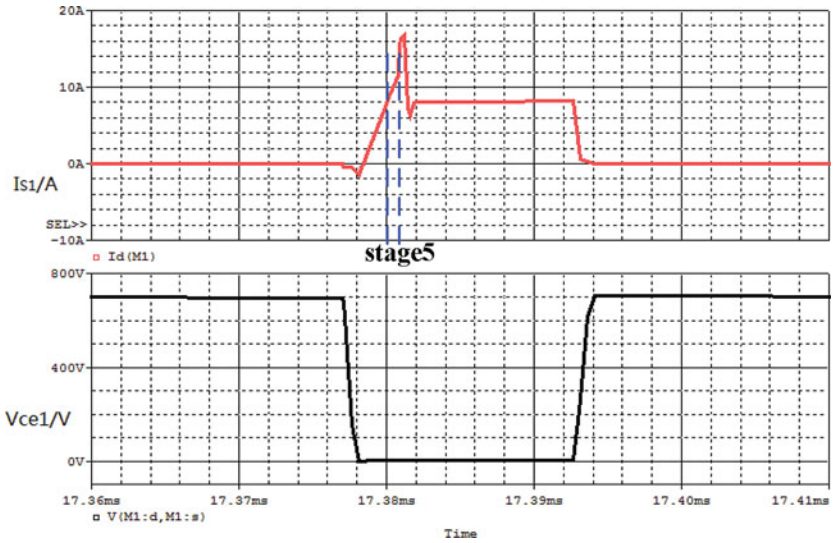
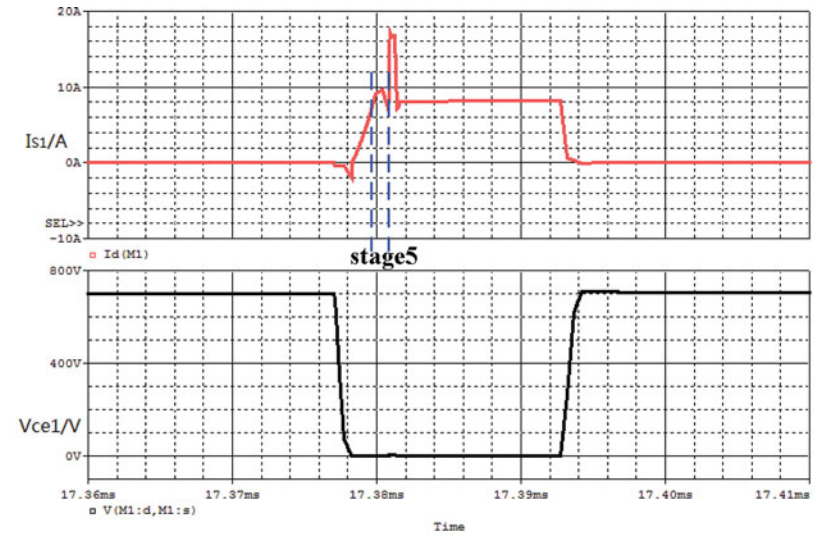
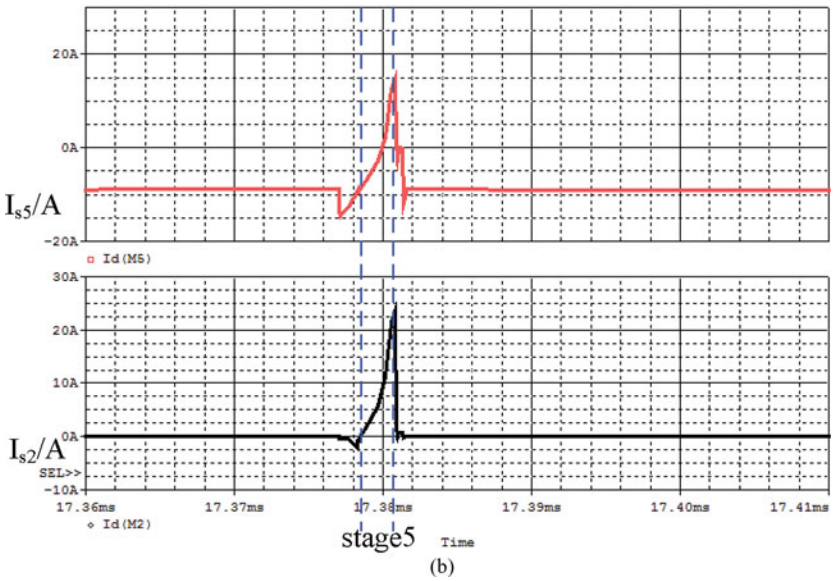


Fig. 22. CE voltage and C→E current of S1 (modulation 2).



(a)



(b)

Fig. 23. CE voltage and current waveforms of modulation 3. (a) CE voltage and C→E current of S1. (b) Current waveforms of the main switches in phase C.

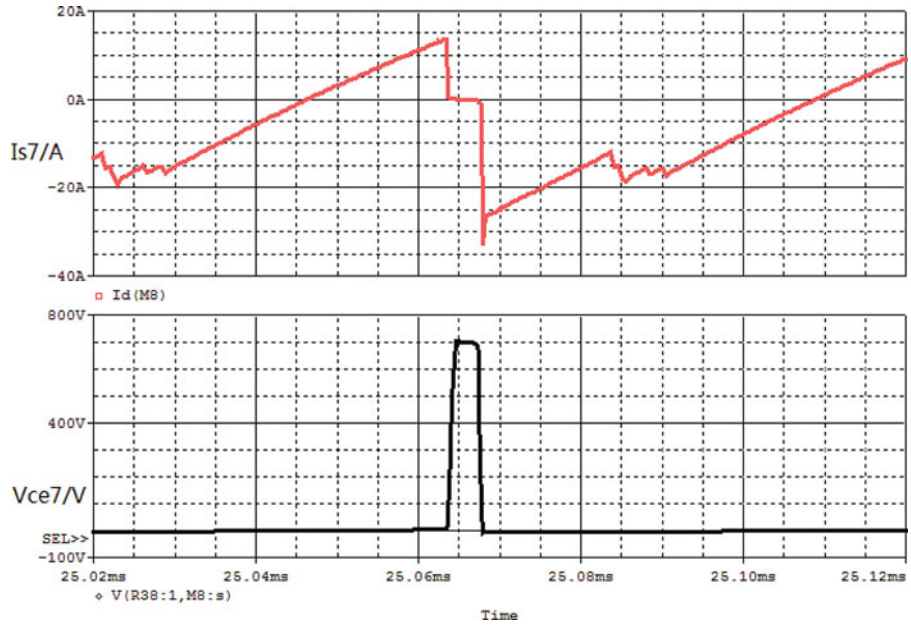


Fig. 24. CE voltage and C→E current of S_7.

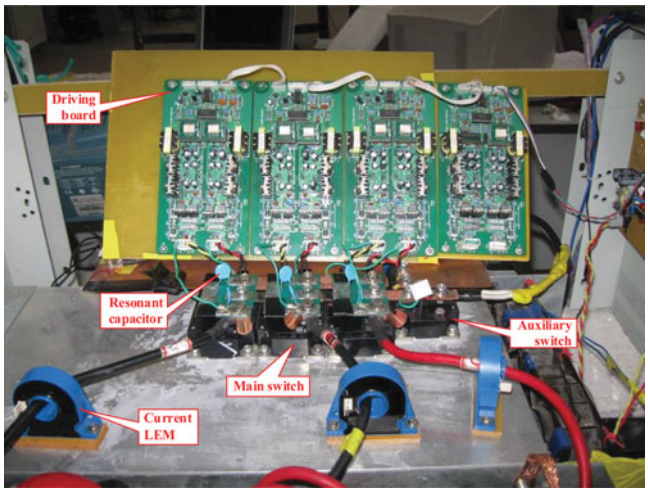


Fig. 25. Photo of 30 kW novel ZVS three-phase boost PWM rectifier prototype.

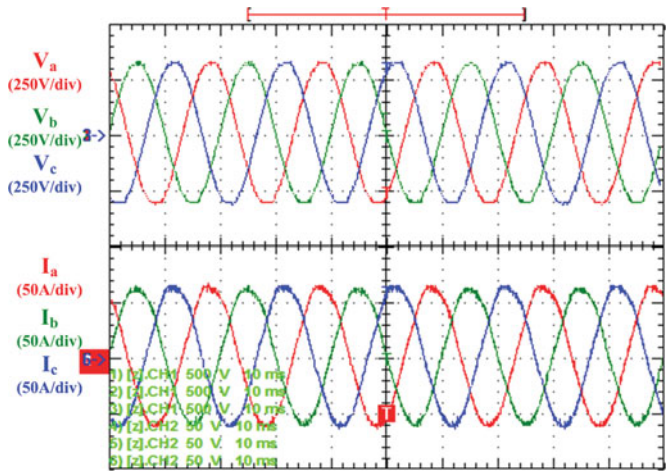


Fig. 26. Input voltage and current waveforms (time: 10 ms/div).

inner current loop using PI regulators in *dq* synchronous rotating frame. The outer voltage PI regulator generates the active current reference while the inner current PI regulators determine the ac-side command voltages of the rectifier. The output voltage is controlled by the outer dc-voltage loop and the output voltage error is determined by the PI controller. The proposed soft-switching SVM method has almost no influence on the output voltage error.

Based on the previous discussion, there are three different modulation schemes suitable for the novel ZVS rectifier. In modulation 1, only the main switch leg of phase A is chosen to be in short circuit in stage 5, so it is very easy to implement. This paper will show the experimental results based on modulation 1. The duration time of stage 5 is chosen according to Fig. 19, which increases by the output power of the rectifier. The three-phase input voltage and current waveforms of the ZVS rectifier are shown in Fig. 26.

Based on modulation 1, only phase A is chosen to be in short circuit in stage 5. The driving signal of main switches S_1 and S_4 is shown in Fig. 27, in which the driving signals of S_1 and S_4 are both high to make the main switch leg of phase A in short circuit in stage 5. The duration time of stage 5 shown in Fig. 27(b) is suitable for 10 kW, which should be about 2 μs according to Fig. 19.

When the output power is 20 kW, the waveform of CE voltage and C→E current of the main switch S_1 in SECT3-1 is shown in Fig. 28. It can be seen from Fig. 28 that before the main switch is turned ON, the CE voltage across the main switch is equal to zero, so the main switch is turn ON under ZVS condition. When the main switch S_1 flows the phase current, the additional

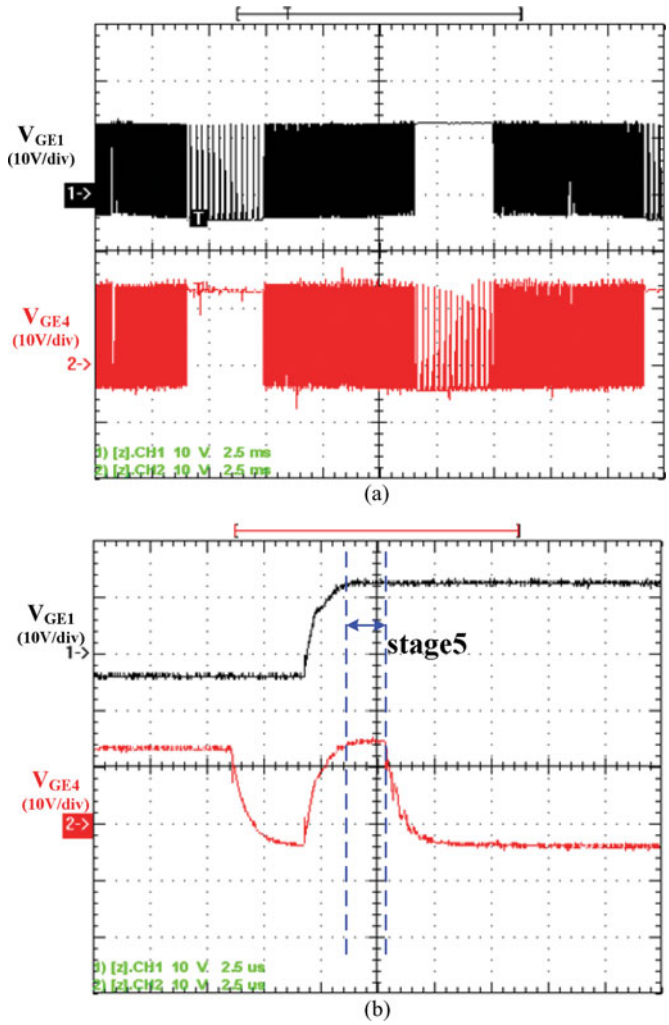


Fig. 27. Driving signal of main switches S1 and S4. (a) Time: 2.5 ms/div. (b) Time: 2.5 μs/div.

energy storage stage 5 is inserted and switch S_1 will carry the additional current $I_{\rm add}$.

When the output power is 20 kW, the waveform of CE voltage and C→E current of the main switch S_1's antiparallel diode in SECT1-2 is shown in Fig. 29. When the current of the diode decreases to zero, the IGBT of switch S_1 is turned ON to make the switch leg of phase A in short circuit and switch S_1 will carry the additional current $I_{\rm add}$.

The waveform of the auxiliary switch current and voltage is shown in Fig. 30, from which it can be seen that the antiparallel diode conducts before the auxiliary switch is turned ON. So the auxiliary switch is turned ON under ZVS condition.

The waveforms of voltage across the clamping capacitor and current flowing through the resonant inductor are shown in Fig. 31, from which it can be seen that V_{Cc} is stable and less than 80 V.

The efficiency curves of traditional hard-switching and novel ZVS soft-switching rectifier analyzed in this paper are shown in Fig. 32, from which it can be seen that the efficiency of the novel ZVS soft-switching rectifier is higher than that in the traditional hard-switching rectifier. According to Section V, the maximum

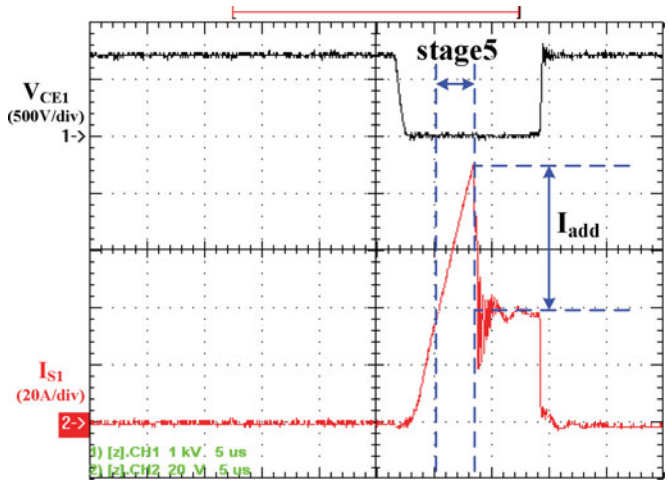


Fig. 28. CE voltage and C→E current of S_1 (time: 5 μs/div).

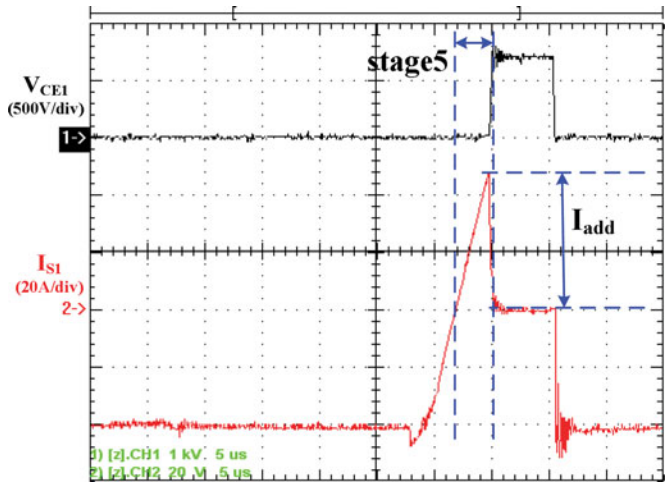


Fig. 29. CE voltage and C→E current of S_1's antiparallel diode (time: 5 μs/div).

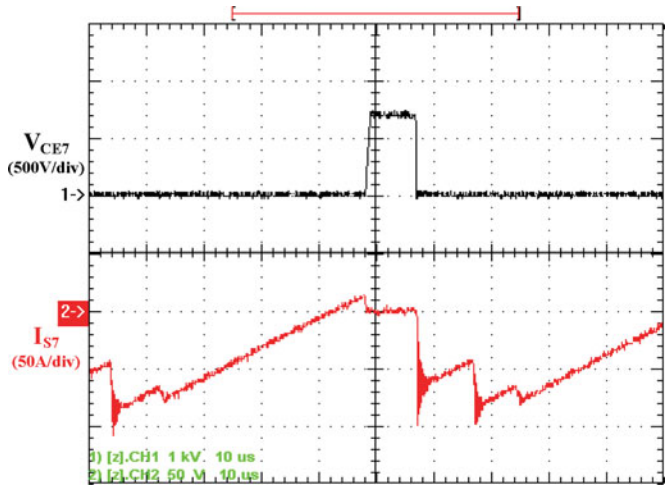


Fig. 30. CE voltage and current of S_7 (time: 10 μs/div).

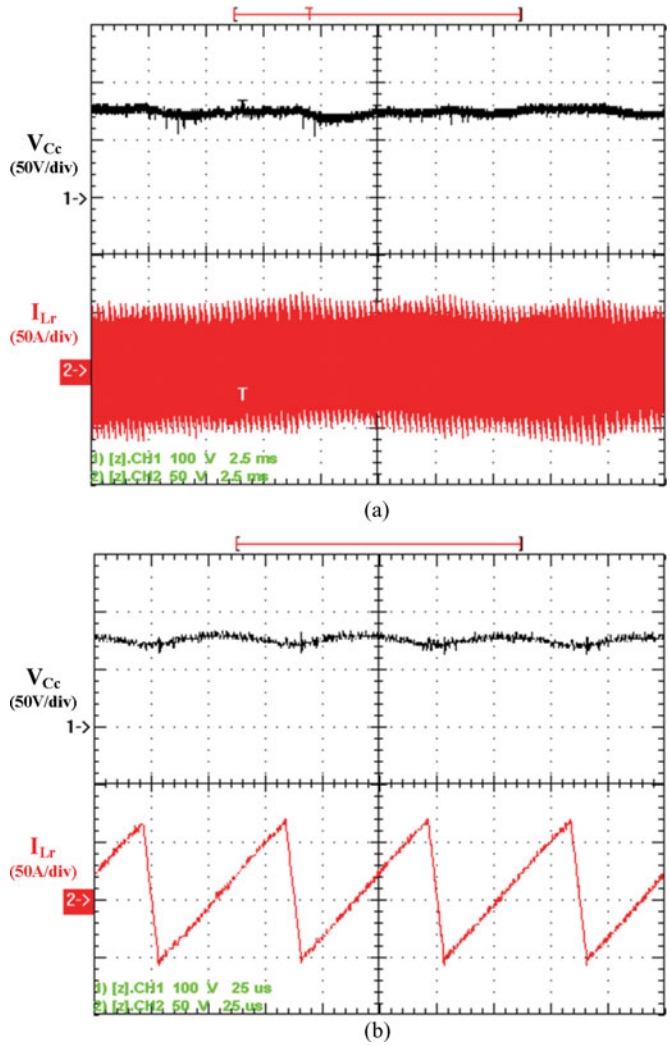


Fig. 31. Current flowing L_r (i_{Lr}) and voltage across C_c (V_{Cc}). (a) Time: 2.5 ms/div. (b) Time: 25 μs/div.

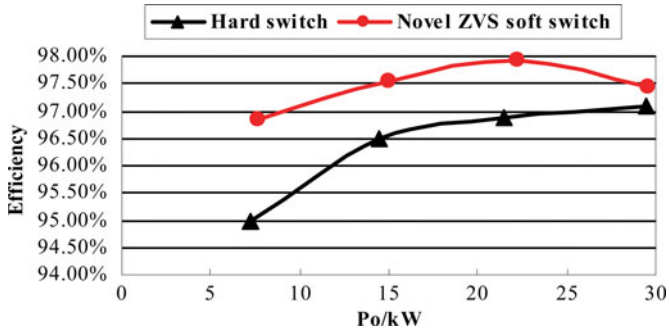


Fig. 32. Efficiency curves of hard-switching and the novel ZVS soft-switching rectifier.

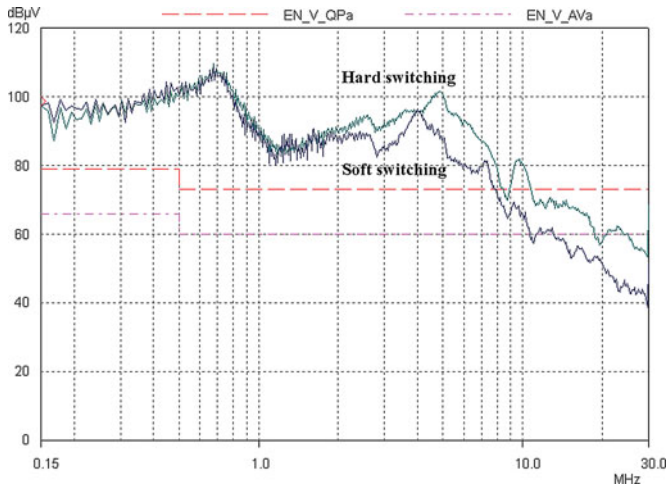


Fig. 33. Comparison of conducted EMI in hard-switching and novel ZVS soft-switching conditions.

output power for parameters optimization is set to 30 kW. The reason for the efficiency decreasing after the output power over 22 kW is due to parameters optimization.

In traditional three-phase PWM rectifier, the high *dv*/*dt* and *di*/*dt* due to the hard-switching of IGBT will cause serious EMI problems. In the novel ZVS soft-switching rectifier analyzed in this paper, all the switches can work under ZVS condition, so the *dv*/*dt* and *di*/*dt* could be decreased and brings lower EMI noise. The conducted EMI noise spectrum of the hard-switching and soft-switching three-phase PWM rectifier is measured and the results are shown in Fig. 33. The upper curve is the conducted EMI noise in hard-switching condition, and the lower curve is obtained in soft-switching condition. It can be seen from the figure that the EMI noise of the converter in soft-switching condition is lower than that in hard-switching condition when the noise frequency is higher than 2 MHz. The lower noise level for frequencies higher than 2 MHz does not allow us to reduce the EMI filter size. However, it affects radiation noise level. The authors sought to show the EMI differences between hard switching and the novel ZVS soft-switching rectifier.

VIII. Conclusion

This paper analyzed a novel active clamping ZVS soft-switching three-phase boost PWM rectifier. A modified SVM strategy suitable for this novel topology was proposed to realize the ZVS condition of the main switches. From theoretical analysis and experimental verifications, the following promising features have been demonstrated:

1) Compared with conventional hard-switching converter, it adds only one auxiliary switch, one resonant inductor, and one clamping capacitor. Extra components are employed and the auxiliary switch required cooling on does not match with the main switches. It is much more complicated compared with hard-switching. However, it is relatively simple compared with the existing soft-switching topologies and still achieves desirable soft-commutation performance.
2) The control scheme required little modification to the traditional minimum switching-loss SVM algorithm. The auxiliary switch is operating at the same switching frequency as the main switches. All main switches and auxiliary switches are turned ON under zero-voltage condition. Meanwhile, all the antiparallel diodes are soft

turned off and have no reverse recovery current. Furthermore, the voltage stress across all the main and auxiliary switches is clamped to the dc-link voltage.

3) Three different modulations are discussed and compared. In modulation 1, the switch current stress of phase A is about two times that in hard switch condition and the switch current stress of the other two phases is not changed. In modulations 2 and 3, the main switch current stress is about 1.2 times that in hard switch condition. The auxiliary switch carries the load power and its current stress is close to the main switch current stress in modulations 2 and 3.
4) The duration time of stage 5 should be varied by the load power of the rectifier. The load power can be represented by the input current, which is already available from general rectifier control functions. So no additional sensors are required.
5) The special SVM scheme proposed in this paper is not symmetric, which causes a little increase of the harmonic current around the switching frequency. However, it makes ZVS operation simple and the auxiliary switch needs to operate once each switching cycle.
6) To realize ZVS for all time in one utility cycle, a minimum length of zero-vector duty cycle is required to realize ZVS condition. On the other hand, for partial ZVS operation in one utility cycle, the modulation ratio will not be restricted.

A 30 kW prototype has been built and realizes desirable ZVS soft-switching features together with unit power factor rectifier functions. The full-power closed-loop test has verified the efficiency superiority of the soft-switching rectifier compared to the hard-switching rectifier. The EMI noise of the novel ZVS rectifier is reduced compared to the hard-switching rectifier.

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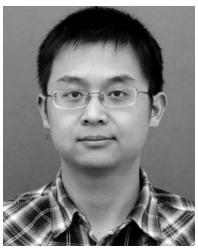

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