A Novel Integrated DC/AC Converter With High Voltage Gain Capability for Distributed Energy Resource Systems

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***Abstract*—In this paper, a novel high voltage gain single-stage dc/ac converter is proposed for distributed energy resources. A flyback-type auxiliary circuit is integrated with an isolated Ćuk-derived voltage source inverter to achieve a much higher voltage gain. It is seen that through this integration, the capacitors of the flyback and the Ćuk circuits are paralleled for charging and in series for discharging automatically. Due to the capacitive voltage dividing, the dc-side switch voltage stress can be reduced and the losses can be reduced as well. Besides, the low influence of coupling coefficient of flyback-type auxiliary circuit on the inverter characteristic renders the proposed inverter design rather flexible and easy. Steady-state characteristics, performance analysis, simulation and experimental results are given to show the merits of the proposed integrated inverter. Finally, based on the same integration concept, a family of different topologies is also presented for reference.**

***Index Terms*—Ćuk-derived voltage source inverter (VSI), distributed energy resource (DER), high voltage gain, single-stage inverter.**

I. Introduction

RECENTLY, public concern about global warming and climate change has caused much efforts being devoted to the development of environment friendly distributed generation (DG) technologies [1]–[3]. In particular, DG resources such as photovoltaic and fuel cell systems have been widely promoted and deployed in many countries. These DG systems are used either to deliver electrical power to the utility grid [4]–[7] or used as stand-alone power supplies in remote areas [8]–[10]. To cope with the applications, battery storage systems or ultracapacitors are often required for achieving stable operation of the DG systems. Since solar cells or fuel cells, batteries, and ultracapacitors are low-voltage dc sources, hence, a high voltage gain dc/ac power conversion interface is essential and many dc/ac converter topologies have been proposed and reviewed recently [8], [11]–[36]. Naturally, the simplest way of solution is to use a high turn-ratio isolation transformer. However, this will induce both voltage/current spikes and rather high losses due to the existence of leakage inductance and stray capacitance [37]. As such, a two-stage approach is proposed to solve this problem [7], [9], [10], [12]. Nevertheless, as far as the total system efficiency is concerned, the resulting efficiency of a two-stage dc/ac converter will be degraded. Hence, many single-stage dc/ac converter topologies such as Z-source/modified Z-source [11], [16], [19]–[25], Sepic, Ćuk, or Zeta-derived dc/ac converters are proposed recently [27]–[34]. However, very few existing dc/ac converters can achieve a high voltage gain while maintaining rather good efficiency.

In view of the aforementioned considerations, in this paper, the authors propose a novel high voltage gain single-stage inverter for distributed energy resources (DERs). A flyback-type auxiliary circuit is integrated with an isolated Ćuk-derived voltage source inverter (VSI) to achieve a much higher voltage conversion ratio. It is seen that through this integration, the capacitors of the flyback and the Ćuk circuits are paralleled for charging and in series for discharging automatically. Due to the capacitive voltage dividing, the dc-side switch voltage stress can be reduced, and lower voltage rating devices can be used to further reduce both switching and conduction losses to enhance the conversion efficiency. The proposed inverter indeed achieves a much higher voltage gain than that can be achieved by the conventional isolated Ćuk-derived VSI, making the proposed inverter rather suitable for low-voltage DER applications.

The remaining content of this paper is organized as follows. First, for completeness, a brief review of Ćuk-derived buck-boost inverter is given in Section II. The topology and operation principle of the proposed integrated inverter are presented in Section III. Detailed steady-state characteristics are then analyzed in Section IV to show the merits of the proposed inverter. Based on the same integration concept, a family of different topologies is also given in Section V for reference. In Section VI, some simulation and experimental results are also given for verifying the validity of the proposed inverter. Finally, some conclusions are offered in the last section.

II. Review of a Ćuk-Derived Single-Phase Inverter

For easy explanation of the proposed single-stage inverter, the conventional Ćuk-derived inverter as shown in Fig. 1 will be briefly reviewed first [27]–[31]. From Fig. 1, one can see

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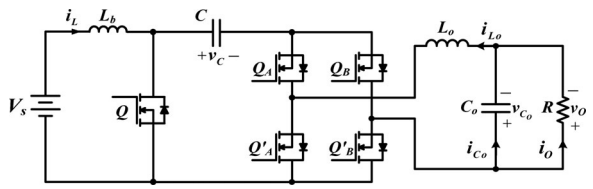

Fig. 1. Ćuk-derived single-phase inverter.

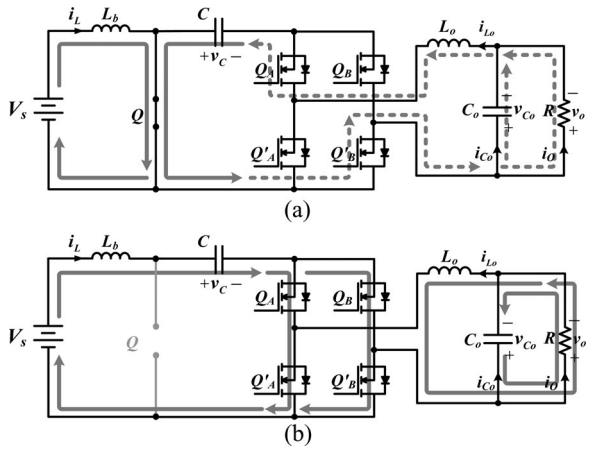

Fig. 2. Equivalent circuits of a Ćuk-derived inverter: when dc-side switch Q is (a) turned ON, and (b) turned OFF.

that this inverter basically belongs to an integration of a boost converter with a full-bridge inverter. One special merit of this inverter is that its output voltage can be either stepped up or down by adjusting the duty ratio of dc-side switch Q.

Since the operation principles of boost and full-bridge inverter are well known, the operation principle of this single-stage inverter can be roughly explained with the following two modes. The first mode is the charging mode as shown in Fig. 2(a) when switch Q is turned ON. During this period, the input energy is stored in inductor L_b at dc-side and the capacitor voltage v_C serves as an equivalent dc input voltage for the full-bridge inverter at the ac-side. The dash line loop at the ac-side only represents one operation mode of the familiar conventional inverter operation modes when v_o is greater than zero. The second operation mode occurs when switch Q is turned OFF as shown in Fig. 2(b). From this equivalent circuit, one can see that the stored energy in L_b is now released to capacitor C. At the same time, the conventional inverter is operated in the free-wheeling mode. It is worth mentioning that, for this inverter, there does not exist the shoot-through problem as that exists in a conventional VSI.

Based on the aforementioned circuit descriptions, the voltage conversion ratio of the inverter can be calculated according to the volt–second balance principle of inductor L_b, and capacitor voltage v_C can be obtained as

$$\frac{V_s}{L} \cdot k = \frac{v_C - V_s}{L} \cdot (1-k)T_s \tag{1}$$

$$v_C = \frac{1}{(1-k)} \cdot V_s \tag{2}$$

where k and T_s represent the duty cycle of Q and the switching period, respectively.

Since v_C is the voltage across the full-bridge inverter input when switch Q is turned ON, therefore, the peak ac output voltage V_o can be derived as

$$V_o = M v_C = \frac{M}{1-k} \cdot V_s \tag{3}$$

where M represents the modulation ratio of the ac-side single-phase VSI. Although (3) indicates that the Ćuk-derived inverter can theoretically attain an infinite gain, practical parasitic imperfections generally limit its maximum gain to a finite value. Hence, the circuit topology can only operate in a limited range in practical applications and suffer degradation in the overall efficiency [30]–[33].

III. Operation Principle of the Proposed Integrated Inverter Topology

In order to achieve a higher voltage gain, a flyback-type auxiliary circuit is integrated with the previous Ćuk-derived inverter [27]–[31] as shown in Fig. 3. From Fig. 3, one can see that the output capacitor of the flyback circuit is placed in series with the secondary side capacitor of Ćuk converter. Also, through this capacitor voltage divider, the voltage stress of dc-side switch will be reduced significantly.

The major symbols in Fig. 3 are described as follows. V_s and L_b, respectively, denote the dc input voltage and input inductor; C_p and C_s represent capacitors in the primary and secondary sides of the isolated transformer T_c, respectively. C_f is the secondary energy storing capacitor of the flyback-type auxiliary circuit. Q is the dc-side switch of the proposed inverter, and Q_A, Q_B, Q'_A, Q'_B are the ac-side full-bridge switches. L_o, C_o denote the output filter and R is the output load.

The operation principle can be described by considering the modulation scheme and key waveforms of the proposed high step-up ratio inverter shown in Figs. 4 and 5, respectively.

For sake of simplicity, assume that all the components in Fig. 3 are ideal and under steady-state condition, with exception of the coupling inductor of the flyback-type auxiliary circuit. The coupling coefficient α of transformer T_f is defined as

$$\alpha = \frac{L_m}{(L_k + L_m)}. \tag{4}$$

According to the modulation scheme shown in Fig. 4, the inverter boosts its input voltage to the dc-link voltage by controlling the duty cycle of dc-side switch Q. Depending on the ON/OFF status of the active switches, there are five operation modes. The operating principle of the proposed inverter can be explained briefly as follows.

Mode I: Switches Q, Q'_A, and Q'_B are turned OFF; switches Q_A and Q_B are turned ON. Diodes D_s and D_f are forward-biased. The corresponding equivalent circuit is shown in Fig. 6(a). Energy stored in boost inductor L_b and the primary side leakage L_k is now released to capacitors in the primary and secondary sides of the isolated transformer T_c. At the same time, the input power is delivered to the secondary side through isolated transformer T_f to charge capacitor C_f. Meanwhile, the

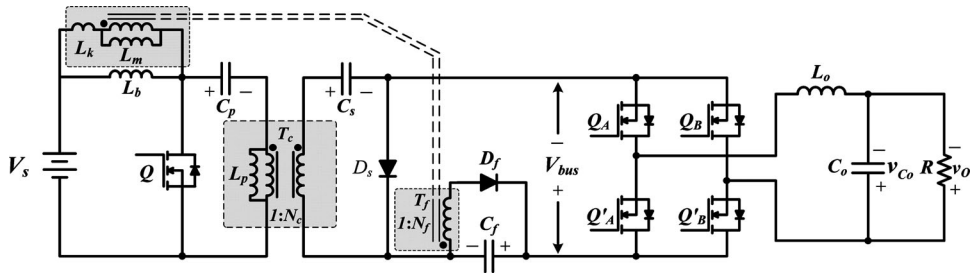

Fig. 3. Circuit configuration of the proposed single-stage inverter.

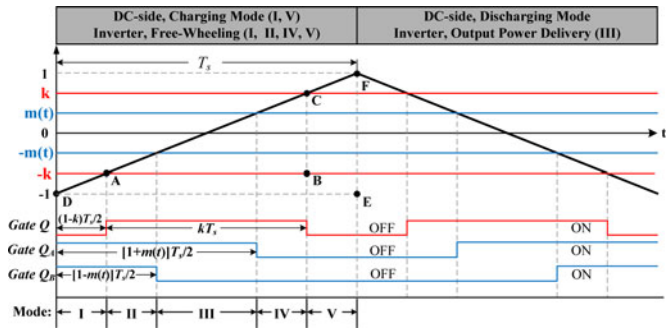

Fig. 4. Modulation scheme of the proposed inverter.

output power is supplied from the output filter. The corresponding state equations of Mode I can be listed as

$$\begin{cases} L_b \dfrac{di_{Lb}}{dt} = V_s - v_{Cp} - \dfrac{v_{Cs}}{N_c} \\ L_p \dfrac{di_{Lp}}{dt} = \dfrac{v_{Cs}}{N_c} \end{cases} \tag{5}$$

$$\begin{cases} L_m \dfrac{di_{Lm}}{dt} = -\dfrac{v_{Cf}}{N_f} \\ L_k \dfrac{di_{Lk}}{dt} = V_s - v_{Cp} + \dfrac{v_{Cf}}{N_f} - \dfrac{v_{Cs}}{N_c} \\ L_o \dfrac{di_{Lo}}{dt} = -v_{Co} \end{cases} \tag{6}$$

$$\begin{cases} C_p \dfrac{dv_{Cp}}{dt} = i_{Lb} + i_{Lk} \\ C_s \dfrac{dv_{Cs}}{dt} = \dfrac{(i_{Lb} + i_{Lk} - i_{Lp})}{N_c} \end{cases} \tag{7}$$

$$\begin{cases} C_f \dfrac{dv_{Cf}}{dt} = \dfrac{i_{Lm} - i_{Lk}}{N_f} \\ C_o \dfrac{dv_{Co}}{dt} = i_{Lo} - \dfrac{v_{Co}}{R}. \end{cases} \tag{8}$$

Mode II: Switches Q, Q_A, and Q_B are turned ON, Q'_A and Q'_B are turned OFF. Diodes D_f and D_s are reverse-biased. The corresponding equivalent circuit is shown in Fig. 6(b). The magnetizing inductor L_m and input boost inductor L_b are charged by the input voltage source V_s. At the same time, the output power is still supplied from the output filter. The corresponding

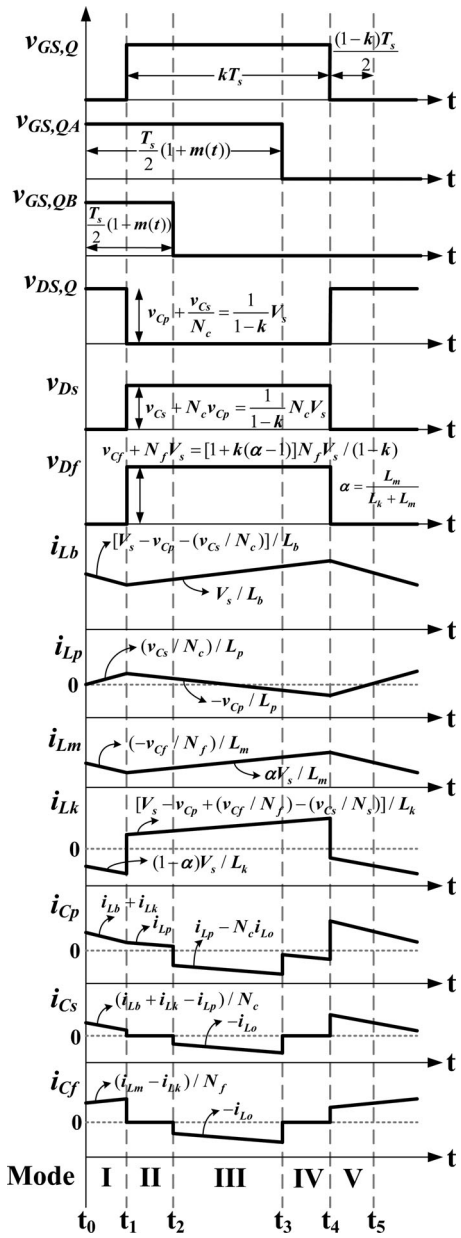

Fig. 5. Key waveforms of the proposed converter.

state equations for this operating mode are given as follows:

$$\begin{cases} L_b \dfrac{di_{Lb}}{dt} = V_s \\ L_p \dfrac{di_{Lp}}{dt} = -v_{Cp} \end{cases} \tag{9}$$

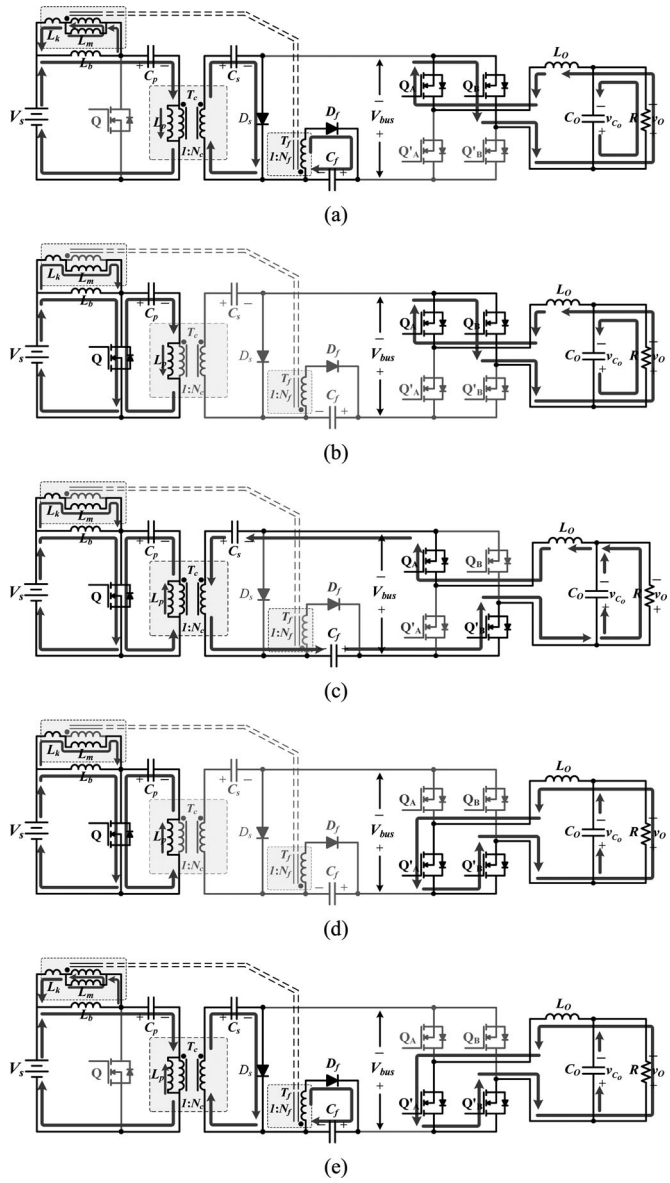

Fig. 6. Equivalent circuits for different inverter operating modes. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

$$\begin{cases} L_m \dfrac{di_{Lm}}{dt} = \alpha V_s \\ L_k \dfrac{di_{Lk}}{dt} = (1-\alpha)V_s \\ L_o \dfrac{di_{Lo}}{dt} = -v_{Co} \end{cases} \tag{10}$$

$$\begin{cases} C_p \dfrac{dv_{Cp}}{dt} = i_{Lp} \\ C_s \dfrac{dv_{Cs}}{dt} = 0 \end{cases} \tag{11}$$

$$\begin{cases} C_f \dfrac{dv_{Cf}}{dt} = 0 \\ C_o \dfrac{dv_{Co}}{dt} = i_{L_o} - \dfrac{v_{Co}}{R}. \end{cases} \tag{12}$$

Mode III: Switches Q, Q_A, and Q'_B are turned ON, and Q'_A and Q_B are turned OFF. Diodes D_f and D_s are reverse-biased. The corresponding equivalent circuit is shown in Fig. 6(c). In this mode, i_{Lb} and i_{Lm} are still increasing to store energy in boost inductor L_b and magnetizing inductor L_m, respectively. In addition, capacitors C_s and C_f are connected in series to give a dc-link voltage ($v_{\rm bus} = v_{Cs} + v_{Cf} + N_c v_{Cp}$) to deliver energy through switches Q_A and Q'_B to the externally connected ac load. The corresponding state equations can be represented as follows:

$$\begin{cases} L_b \dfrac{di_{Lb}}{dt} = V_s \\ L_p \dfrac{di_{Lp}}{dt} = -v_{Cp} \end{cases} \tag{13}$$

$$\begin{cases} L_m \dfrac{di_{Lm}}{dt} = \alpha V_s \\ L_k \dfrac{di_{Lk}}{dt} = (1-\alpha)V_s \\ L_o \dfrac{di_{Lo}}{dt} = v_{Cs} + N_c v_{Cp} + v_{Cf} - v_{Co} \end{cases} \tag{14}$$

$$\begin{cases} C_p \dfrac{dv_{Cp}}{dt} = -(N_c i_{Lo} - i_{Lp}) \\ C_s \dfrac{dv_{Cs}}{dt} = -i_{Lo} \end{cases} \tag{15}$$

$$\begin{cases} C_f \dfrac{dv_{Cf}}{dt} = -i_{Lo} \\ C_o \dfrac{dv_{Co}}{dt} = i_{Lo} - \dfrac{v_{Co}}{R}. \end{cases} \tag{16}$$

Mode IV: As seen in Fig. 6(d), switches Q, Q'_A, and Q'_B are turned ON, and Q_A and Q_B are turned OFF. Diodes D_s and D_f are reverse-biased. Input boost inductor L_b and magnetizing inductor L_m are charged by the input voltage source V_s. Meanwhile, the ac-side of the inverter enters free-wheeling operation mode, and the output power is supplied from the output filter. The corresponding state equations of the proposed inverter are the same as those for Mode II.

Mode V: As shown in Fig. 6(e), switches Q'_A and Q'_B are turned ON, while Q, Q_A, and Q_B are turned OFF. Diodes D_s and D_f are forward-biased. Energy stored in boost inductor L_b and the primary side leakage L_k is now released to capacitors C_p and C_s. At the same time, partial input power is delivered to the secondary side through isolated transformer T_f to charge capacitors C_f. The ac-side of the inverter remains in free-wheeling operation mode, and the output power is still supplied from the output filter. The corresponding state equations of the proposed inverter are the same as those for Mode I.

IV. Analysis of Steady-State Characteristics

From Fig. 4, one can see that a double-slope carrier signal is chosen for increasing the ripple frequency. Assume T_s is the switching period of dc-side switch Q, k is the duty ratio of Q, and $m(t)$ is the modulation index of the ac-side inverter. It is seen from Fig. 4 that triangles ΔABC and ΔDEF are similar.

Hence, one can obtain that the turn-ON period of switch is kT_s, and the corresponding turn-OFF period of Q is $(1-k)T_s$. It follows from Fig. 4 that the time period of mode I is equal to $(1-k)T_s/2$. By using the same procedure, one can find that the weighting factors for the remaining four operation modes are $[k-m(t)]/2$, $m(t)$, $[k-m(t)]/2$, and $(1-k)/2$ in sequence, respectively.

Based on the aforementioned operation modes, the voltage conversion ratio of the proposed inverter can be calculated according to the volt–second balance principle of inductors. The volt–second balance equation for inductor L_b becomes

$$\left(V_s - v_{Cp} - \left(\frac{v_{Cs}}{N_c}\right)\right)(1-k) + V_s(k-M) + V_s M = 0 \tag{17}$$

$$V_s = (1-k)\left(v_{Cp} + \frac{v_{Cs}}{N_c}\right) \tag{18}$$

where M represents the peak value of modulation index *m(t)* of ac output reference.

The volt–second balance equation for equivalent inductance L_p in the primary side of the isolated transformer can be described as

$$\frac{v_{Cs}(1-k)}{N_c} - v_{Cp}(k-M) - v_{Cp}M = 0. \tag{19}$$

It turns out that

$$v_{Cs} = \frac{k}{1-k} N_c v_{Cp}. \tag{20}$$

Thus, from (18) and (20), the respective voltages across capacitors C_p and C_s of the proposed inverter can be obtained as follows:

$$v_{Cp} = V_s \tag{21}$$

$$v_{C_s} = \frac{k}{1-k} N_c V_s. \tag{22}$$

Similarly, the volt–second balance equation for inductor L_m becomes

$$\frac{-v_{Cf}(1-k)}{N_f} + \alpha V_s(k-M) + \alpha V_s M = 0. \tag{23}$$

As a result, the voltage across capacitor C_f of the proposed inverter can be obtained as

$$v_{Cf} = \frac{\alpha k}{1-k} N_f V_s. \tag{24}$$

The volt–second balance equation for output inductor L_o takes the following form:

$$-v_{Co}(1-k) - v_{Co}(k-M) + (v_{Cs} + N_c v_{Cp} + v_{Cf} - v_{Co})M = 0. \tag{25}$$

Therefore, the peak ac output voltage can be directly derived as follows:

$$V_{Co} = V_o = M(v_{Cs} + N_c v_{Cp} + v_{Cf}). \tag{26}$$

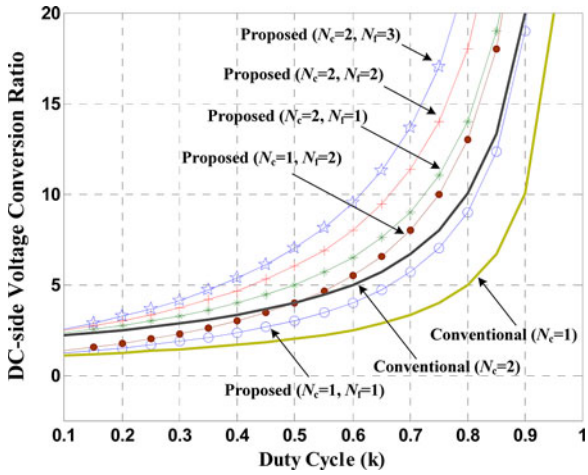

Fig. 7. DC-side voltage conversion ratio for different duty cycle k ($\alpha = 1$).

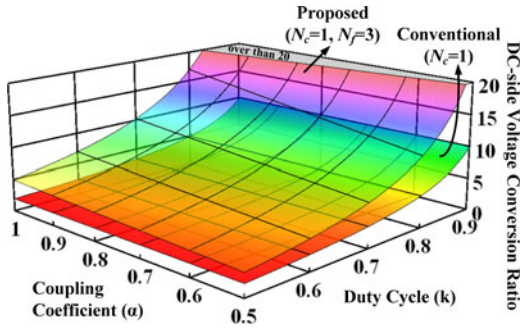

Fig. 8. DC-side voltage conversion ratio versus duty cycle k and coupling coefficient α.

From (21), (22), and (24), the resulting peak ac output voltage can be expressed as

$$V_{Co} = V_o = \left(\frac{1}{1-k}N_c + \frac{\alpha k}{1-k}N_f\right) M V_s. \tag{27}$$

Accordingly, the voltage conversion ratio G_V of the proposed inverter becomes

$$G_{V,\text{proposed}} = \left.\frac{V_o}{V_s}\right|_{\text{proposed}} = \left(\frac{1}{1-k}N_c + \frac{\alpha k}{1-k}N_f\right) M. \tag{28}$$

For convenient comparison, the voltage conversion ratio of the conventional isolated Ćuk-derived VSI is also repeated as follows [27]–[31]:

$$G_{V,\text{conventional}} = \left.\frac{V_o}{V_s}\right|_{\text{conventional}} = \left(\frac{1}{1-k}N_c\right) M \tag{29}$$

From (28) and (29), it is seen that an additional voltage gain $\alpha k M N_f/(1-k)$ can be obtained for the proposed inverter as compared with the conventional isolated Ćuk-derived VSI. The proposed inverter is, therefore, rather suitable for use in those required high step-up ratio applications.

For clearly showing the variation of the dc-side voltage conversion ratio, namely V_{bus}/V_s, with k, N_c, and N_f, the common factor M is not included in Figs. 7–9. Fig. 7 shows the ideal dc-side voltage conversion ratio characteristic as a function of duty

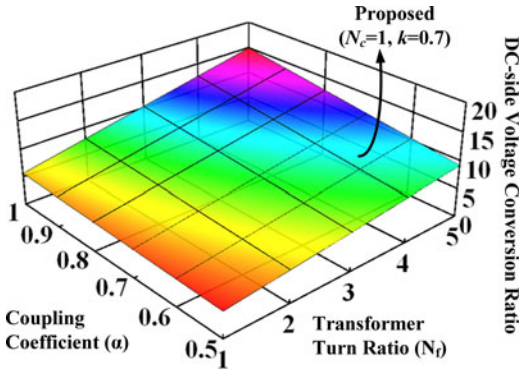

Fig. 9. DC-side voltage conversion ratio versus transformer turn ratio N_f and coupling coefficient α.

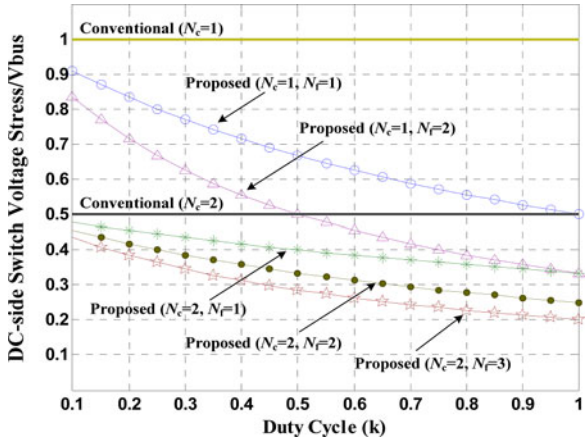

Fig. 10. DC-side switch voltage stress for different duty cycle k ($\alpha = 1$).

cycle k under $\alpha = 1$ condition for both conventional isolated Ćuk-derived VSI and the proposed inverter [27]–[31]. It is seen from Fig. 7 that higher turn ratio N_c and N_f of the proposed converter can also be chosen to obtain even higher voltage gain.

To provide a better understanding of the relationships among the dc-side voltage conversion ratio, duty cycle k, turn ratio N_f, and coupling coefficient α, Fig. 8 provides a 3-D plot of the ideal dc-side voltage conversion ratio as a function of duty cycle k and coupling coefficient α, for both conventional isolated Ćuk-derived VSI and the proposed inverter [27]–[31], respectively. Fig. 9 shows the dc-side voltage conversion ratio versus transformer turn ratio N_f and coupling coefficient α of the proposed inverter. It is seen from Fig. 9 that due to very limited influence of coupling coefficient and other parasitic effects, turn ratio N_f indeed provides a rather flexible design degree of freedom to achieve high voltage gain and renders the inverter design rather easy.

In addition, from the equivalent circuits shown in Fig. 6, the open-circuit voltage stress of dc-side switch Q can be obtained directly as follows:

$$V_{Q,\max} = v_{Cp} + \frac{v_{Cs}}{N_c} = \frac{1}{1-k} V_s. \tag{30}$$

For convenient comparison, the dc-side switch voltage stress divided by the dc bus voltage for the proposed inverter and the conventional isolated Ćuk-derived VSI are also provided as follows:

$$\left.\frac{V_{Q,\max}}{V_{\text{bus}}}\right|_{\text{proposed}} = \frac{1}{N_c + \alpha k N_f} \tag{31}$$

$$\left.\frac{V_{Q,\max}}{V_{\text{bus}}}\right|_{\text{conventional}} = \frac{1}{N_c} \tag{32}$$

Following (31) and (32), the dc-switch voltage stress divided by the dc bus voltage versus duty cycle k under $\alpha = 1$ condition for both inverters is shown in Fig. 10. From Fig. 10, one can see that the proposed inverter can achieve much lower dc-switch voltage stress. As a result, given a proper design, the proposed inverter can adopt lower voltage rating switch to achieve higher efficiency.

V. Topology Variations of the Proposed Integrated Inverter

The proposed concept can also be applied to other single-phase integrated inverters. Fig. 11 shows some variations for reference. Table I also summarizes the voltage conversion ratios of these topologies. In addition, as seen from Table I, all of these converters can easily achieve high step-up voltage gains by automatically capacitive charging in parallel and discharging in series without increasing dc-side switch voltage stress.

VI. Simulation and Experimental Results

To facilitate understanding the merits and to serve as a verification of the effectiveness of the proposed inverter, a 200 W rating laboratory prototype with the following system specifications is constructed as an example:

1) input voltage (dc) V_s: 30 V;
2) output voltage (ac) V_o: 156 $V_{(\text{peak})}$;
3) rated output power P_o: 200 W;
4) switching frequency f_s: 40 kHz;
5) duty cycle of dc-side switches k: 0.7;
6) peak modulation index M: 0.65.

To make the conversion efficiency performance comparison, a conventional isolated Ćuk-derived dc/ac converter with the same power rating and system specification is also constructed. The corresponding circuit parameters of the proposed integrated converter and conventional isolated Ćuk-derived dc/ac converter prototypes are presented in Tables II and III for reference, respectively.

Figs. 12 and 13 show the simulation and experimental waveforms of MOSFET driving signals, diode voltage V_{Df}, and diode voltage V_{Ds}, respectively, from one can see the corresponding operating modes of the proposed converter. To check the validity of (26)–(28), both simulation and experimental results are recorded as shown in Fig. 14. It can be seen that, with the input voltage $V_s = 30$ V, the 156 V peak ac output voltage can be achieved easily with a duty cycle of dc-side switch being equal to 0.7 and a peak modulation index of 0.65. The maximum value of line voltage V_{AB} is about 242 V. It confirms that the dc-link voltage, $v_{\text{bus}} = v_C + v_{Cf} + N_c v_{Cp}$, is now boosted to 242 V

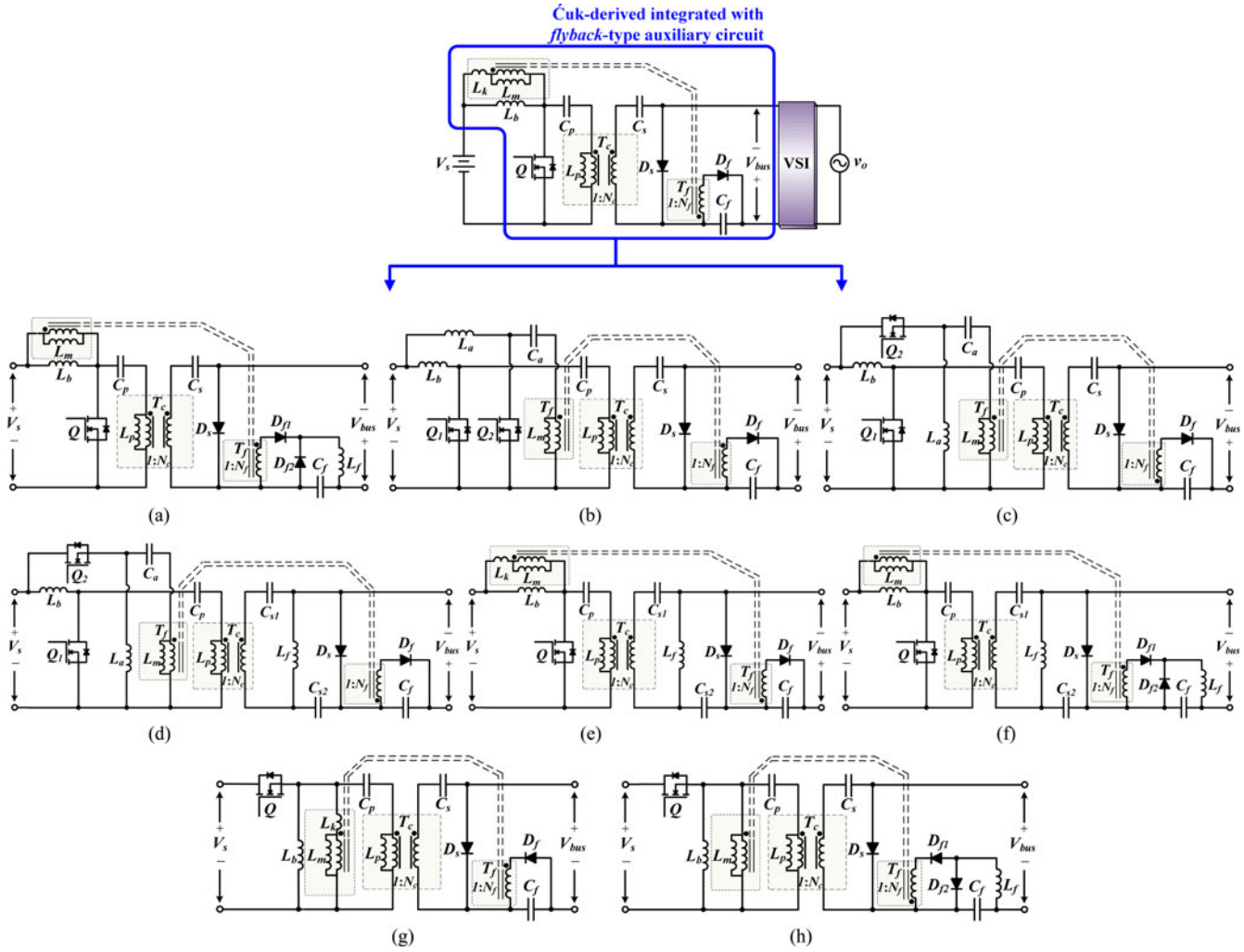

Fig. 11. Topology variations for the proposed inverter. (a) Ćuk-derived integrated with *forward-type*. (b) Ćuk-derived integrated with *Sepic-type*. (c) Ćuk-derived integrated with *Zeta-type*. (d) Sepic-derived integrated with *Zeta-type*. (e) Sepic-derived integrated with *flyback-type*. (f) Sepic-derived integrated with *forward-type*. (g) Zeta-derived integrated with *flyback-type*. (h) Zeta-derived integrated with *forward-type*.

TABLE I
VOLTAGE CONVERSION RATIOS OF THE VARIATION TOPOLOGIES

Voltage Gain (V_o/V_s) / Auxiliary Circuits	Integrated single-phase inverters		
	Ćuk-derived	Sepic-derived	Zeta-derived
***flyback*-type**	$(\frac{1}{1-k}N_c+\frac{\alpha k}{1-k}N_f)M$		
***forward*-type**	$(\frac{1}{1-k}N_c+k\cdot N_f)M$		
***Zeta*-type**	$(\frac{1}{1-k}N_c+\frac{k}{1-k}N_f)M$		
***Sepic*-type**	$(\frac{1}{1-k}N_c+\frac{k}{1-k}N_f)M$		
***Ćuk*-type**	$(\frac{1}{1-k}N_c+\frac{k}{1-k}N_f)M$		

under the discharging mode. In addition, from Fig. 14, it can be seen that the simulation results are in close agreement with the corresponding experimental results.

Similarly, to check the correctness of (21)–(24), both simulation and experimental results are made and shown in Fig. 15. From Fig. 15, one can observe that both results are in very close agreement as well. In the proposed topology, voltage across capacitor C_p is charged to 30 V, and voltages across capacitors C_s and C_f are charged to 86 and 118 V, respectively. Both capacitors indeed can share most of the output voltage for reducing the voltage stress of dc-side active switches.

Both simulation and experimental results of dc-side switch voltage are shown in Fig. 16. From Fig. 16, one can observe that the voltage spike of the measured waveform is caused by the leakage inductance of the power transformer T_f when the switch is turned OFF. However, the steady-state voltage stress of the dc-side active switch is about 98 V, which is also very close to that calculated from (30). In addition, it is worth mentioning that the voltage stress is much smaller than the peak value of dc-link voltage and enables one to adopt lower voltage rating devices for reducing the conduction loss as well as switching loss

The measured efficiency of the proposed converter is shown in Fig. 17. For comparison, the measured efficiency of the

TABLE II
CIRCUIT PARAMETERS OF THE PROTOTYPE (PROPOSED DC/AC CONVERTER)

Parameters		Symbol	Value/Part no.
Input boost inductor		L_b	300μH
Transformer (T_f, T_c)	Turn ratio	N_f	1.72
		N_c	1.23
	Leakage inductance	$L_{k,Tf}$	1.2μH
		$L_{k,Tc}$	1.2μH
	magnetizing inductance	$L_{m,Tf}$	500μH
		$L_{m,Tc}$	800μH
DC-side capacitor		C_p	33μF/100VAC
Energy storing capacitors		C_s, C_f	560μF/200VDC
Output filter inductor		L_o	1mH
Output filter capacitor		C_o	2.2μF/250VAC
DC-side switch		Q	IXFH120N20P
AC-side switches		Q_A, Q_B, Q'_A, Q'_B	IXTQ30N60P
Diodes		D_s, D_f	15S2TH06FP

TABLE III
CIRCUIT PARAMETERS OF THE PROTOTYPE (CONVENTIONAL ISOLATED ĆUK-DERIVED DC/AC CONVERTER)

Parameters		Symbol	Value/Part no.
Input boost inductor		L_b	225μH
Transformer (T_c)	Turn ratio	N_c	2.46
	Leakage inductance	$L_{k,Tc}$	1.5μH
	magnetizing inductance	$L_{m,Tc}$	876μH
DC-side capacitor		C_p	33μF/100VAC
Energy storing capacitor		C_s	560μF/200VDC
Output filter inductor		L_o	1mH
Output filter capacitor		C_o	2.2μF/250VAC
DC-side switch		Q	IXTQ88N28T
AC-side switches		Q_A, Q_B, Q'_A, Q'_B	IXTQ30N60P

conventional isolated Ćuk-derived dc/ac converter [27]–[31] is also shown in the same figure. It should be mentioned that to achieve equal output voltage for comparison, an isolation transformer with a turn ratio of 2.46 is inserted to the nonisolated Ćuk-derived dc/ac converter as shown in Fig. 1. Also, a high precision power meter Yokogawa-WT500 is adopted for measuring the conversion efficiency. For reference, photograph of the constructed prototype is shown in Fig. 18.

From Fig. 17, it is seen that an efficiency of 92.3% at 40% load can be achieved. In addition, the efficiency at 40 W light load of the proposed converter is about 90.92%. With the increase of the output load, the conversion efficiency is decreased due to the relatively larger primary side conduction losses and switching losses caused by the more injected input current. Note

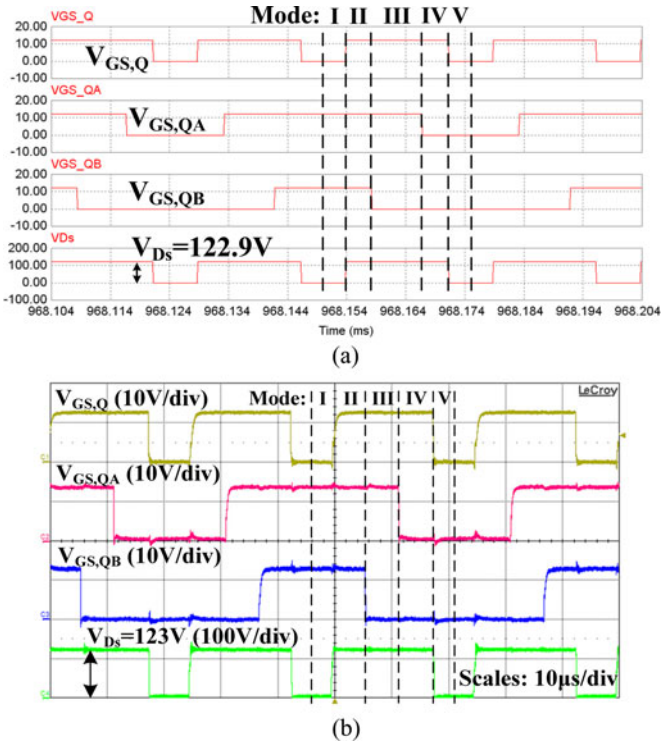

Fig. 12. Waveforms of MOSFET driving signals and diode voltage V_{Ds}. (a) By simulation. (b) By experiment.

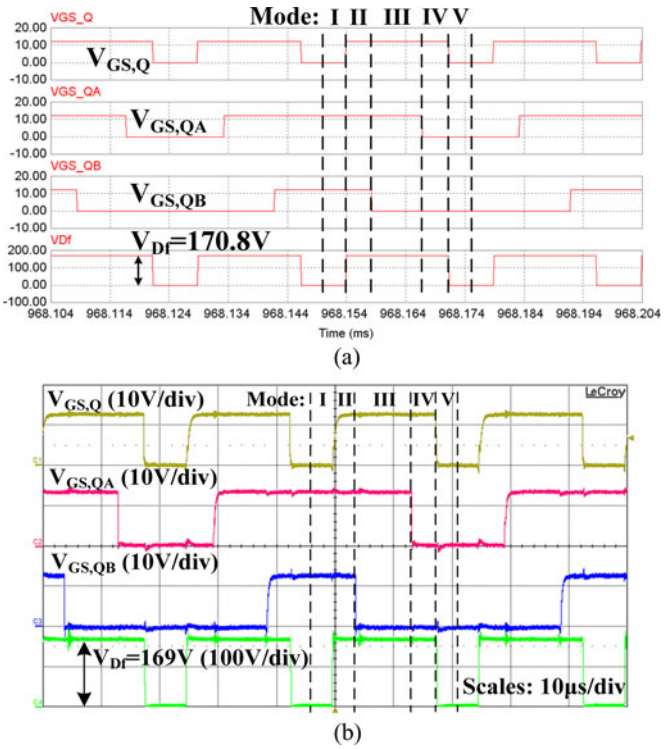

Fig. 13. Waveforms of MOSFET driving signals and diode voltage V_{Df}. (a) By simulation. (b) By experiment.

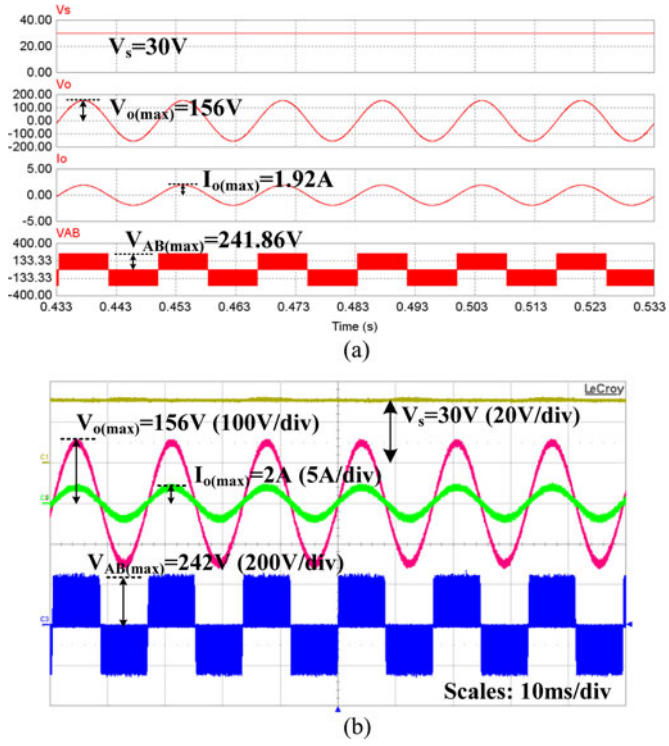

Fig. 14. Waveforms of input voltage, output voltage/current, and line voltage. (a) By simulation. (b) By experiment.

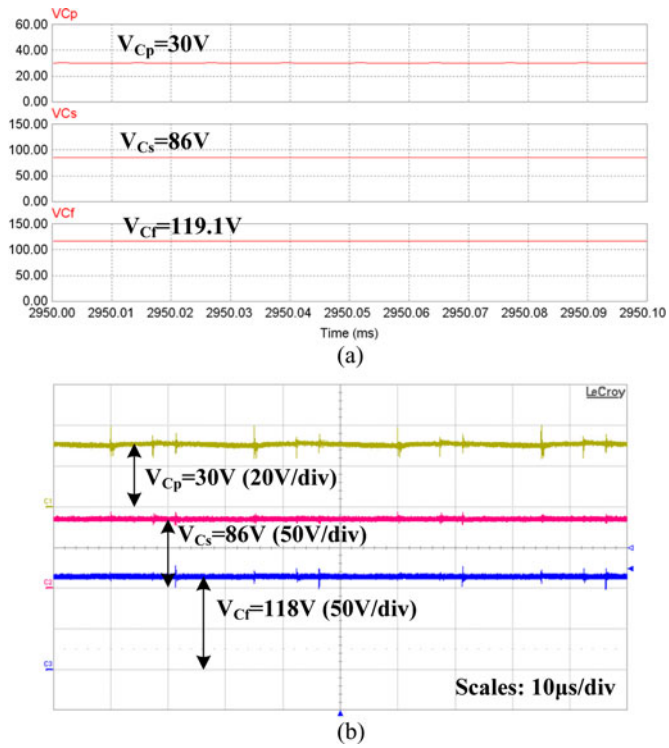

Fig. 15. Waveforms of capacitor voltage. (a) By simulation. (b) By experiment.

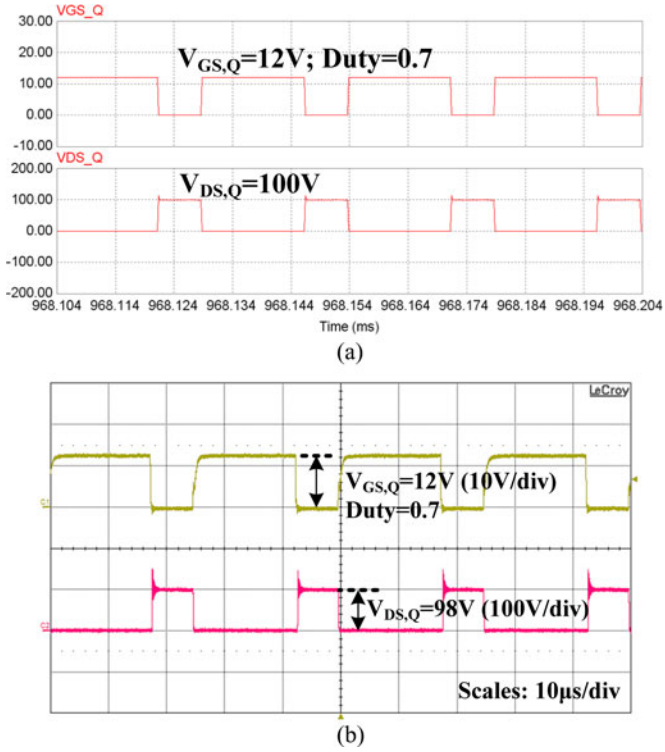

Fig. 16. Waveforms of dc-side MOSFET driving signal and switch voltage. (a) By simulation. (b) By experiment.

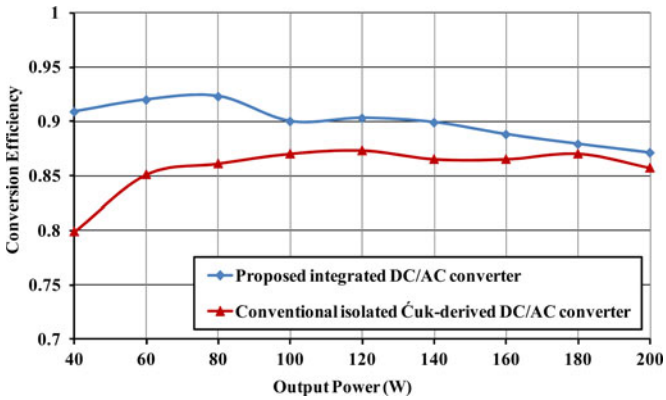

Fig. 17. Measured efficiencies of the proposed converter and the conventional isolated Ćuk-derived converter.

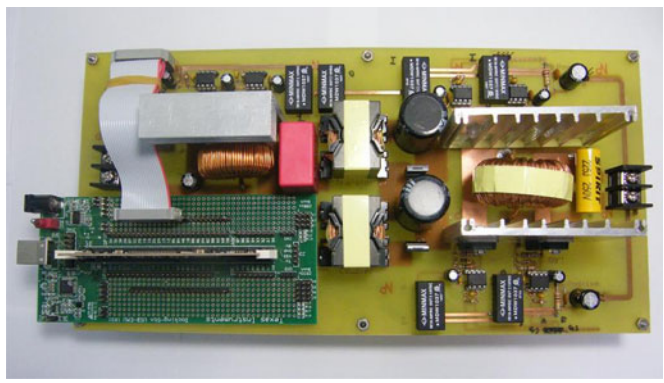

Fig. 18. Constructed integrated dc/ac converter prototype.

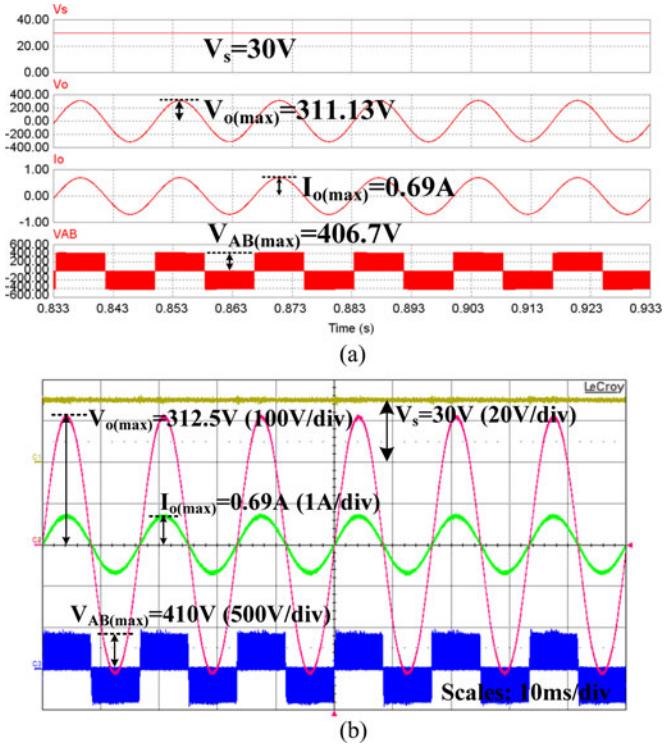

Fig. 19. Waveforms of input voltage, output voltage/current, and line voltage with 220 $V_{\rm rms}$ output voltage condition. (a) By simulation. (b) By experiment.

that the similar efficiency curves can also be observed in the high step-up energy conversion topologies [38]–[41]. From the same figure, one can also observe that there is approximately 10% improvement in efficiency at light load as compared with the conventional isolated Ćuk-derived converter. Also, it indicates that nearly 3% and 1.4% improvement in efficiency can be achieved by the proposed integrated converter, under 120 W and 200 W load conditions, respectively.

The proposed converter naturally can also be applied for 220 $V_{(\rm rms)}$ ac-output voltage. For completeness, the previous prototype is redesigned to meet this specification, namely, V_s: 30 V, V_o: 220 $V_{(\rm rms)}$, k: 0.8, M: 0.77, and f_s: 40 kHz. The corresponding replaced components of power stage are listed as follows for reference: 1) transformers—N_f: 1.75, N_c: 1.31, magnetizing inductances $L_{m,Tf}$: 486 μH, $L_{m,Tc}$: 1.26 mH; 2) energy storing capacitors—C_s, C_f: 330 μF/450 $V_{\rm DC}$; (3) dc-side switch—IXTQ88N28T; (4) diodes D_s, D_f—D16S60 C. Typical waveforms of the constructed prototype for 220 $V_{(\rm rms)}$ output voltage are shown in Fig. 19. It is seen from Fig. 19 that both simulation and experimental results indeed agree with each other very closely. Also, one can see that now the maximum value of line voltage V_{AB} is about 410 V, which would generate an ac-output voltage of 220 $V_{(\rm rms)}$.

VII. Conclusion

In this paper, a novel high voltage gain single-stage inverter is proposed for DER applications. A flyback-type auxiliary circuit is integrated with an isolated Ćuk-derived VSI to achieve a much higher voltage gain. The dc-side switch voltage stress of the proposed inverter can be reduced and the losses can be reduced as well. Besides, the low influence of coupling coefficient of flyback-type auxiliary circuit on the inverter characteristic renders the proposed inverter design rather flexible and easy. Steady-state characteristics, performance analysis, simulation and experimental results are given to show the merits and validity of the proposed inverter. Finally, based on the same integration concept, a family of different topologies is also presented for reference.

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