A Novel Valley-Fill SEPIC-derived Power Supply Without Electrolytic Capacitors for LED Lighting Application

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***Abstract*—The high-brightness white light-emitting diode (LED) has attracted a lot of attention for its high efficacy, simple to drive, environmentally friendly, long lifespan, and compact size. The power supply for LED also requires long life, while maintaining high efficiency, high power factor, and low cost. However, a typical power supply design employs an electrolytic capacitor as the storage capacitor, which is not only bulky, but also with a short lifespan, thus hampering performance improvement of the entire LED lighting system. In this paper, a novel power factor correction (PFC) topology is proposed by inserting the valley-fill circuit in the single-ended primary inductance converter (SEPIC)-derived converter, which can reduce the voltage stress of the storage capacitor and output diode under the same power factor condition. This valley-fill SEPIC-derived topology is then proposed for LED lighting applications. By allowing a relatively large voltage ripple in the PFC design and operating in the discontinuous conduction mode (DCM), the proposed PFC topology is able to eliminate the electrolytic capacitor, while maintaining high power factor and high efficiency. Under the electrolytic capacitor-less condition, the proposed PFC circuit can reduce the capacitance of the storage capacitor to half for the same power factor and output voltage ripple as comparing to its original circuit. To further increase the efficiency of LED driver proposal, a twin-bus buck converter is introduced and employed as the second-stage current regulator with the PWM dimming function. The basic operating principle and analysis will be described in detail. A 50-W prototype has been built and tested in the laboratory, and the experimental results under universal input-voltage operation are presented to verify the effectiveness and advantages of the proposal.**

***Index Terms*—Electrolytic capacitor, light-emitting diode (LED), multiple lighting LED lamps, power factor correction (PFC), pulse width modulation (PWM) dimming, single-ended primary inductance converter (SEPIC)-derived, valley-fill circuit.**

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I. Introduction

With the potential of high efficacy, long lifetime, environmental friendliness, and compact size over the conventional lighting devices, the light-emitting diodes (LEDs) have emerged as a promising lighting technology to replace the energy-inefficient incandescent lamps and mercury-based fluorescent lamps [1]–[6]. To promote more energy saving, some countries have introduced measures to phase out incandescent lamps [2].

Presently, the power ratings of individual LED devices are a few watts, and their typical efficacies are about 90 and 75 lm/W for cool and warm white LEDs, respectively [7], [8]. Hence, multiple LED lamps have to be connected in parallel or series to obtain sufficient luminance. The general photo-electro-thermal (PET) theory also indicates that a distributed LED system based on a plurality of relatively low-power LEDs can have advantages over a concentrated system consisting of a small number of high-power LEDs for the same system power [9], [10]. Therefore, paralleling LED strings has been a common practice.

Driving multiple LED lamps from an offline power source poses challenges in many aspects of power converter design. High power factor and low input-current harmonics are becoming the mandatory design criteria for switching power supplies. In lighting equipment, the input current of ballasted lamps exceeding 25 W is required to comply with stricter requirements as stated in IEC 61000-3-2-Class C [11]. Energy Star requires the input power factor higher than 0.9 for commercial luminaries [12].

Much research has been directed toward power factor correction (PFC) topologies and control schemes [13]–[28] in LED application over the past decades. Fig. 1(a) shows a typical solution using the "classical" two-stage PFC circuit and postcurrent regulators [13]–[16]. Although such a two-stage configuration of the PFC circuit can help LEDs achieve good operating performance, too many components, large size, low efficiency, and relatively high cost are its main drawbacks. As shown in Fig. 1(b), another candidate for driving multiple lighting LED lamps is to employ the single-stage PFC circuit to eliminate the additional dc–dc stage. State-of-the-art LED drivers using the single-stage PFC topology have been published in [17]–[27]. The circuit choices

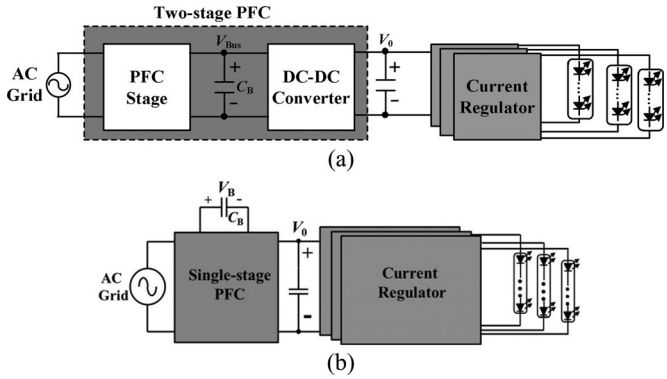

Fig. 1. Traditional solutions for driving multiple lighting LED lamps. (a) Traditional three-stage structure for driving multiple lighting LED lamps. (b) Traditional two-stage structure for driving multiple lighting LED lamps.

involved flyback [17], [18], [24], single-ended primary inductance converter (SEPIC) [18]–[22], buck-flyback [23], boost-flyback [25], resonance-assisted buck [7], [8], buck-boost [27], etc. In [21], the authors compared several offline PFC topologies for driving LEDs, including boost, SEPIC, forward, flyback, and half-bridge. These topologies are suitable for different power level and customer requirements.

No matter what kind of PFC converter, to balance the difference between instantaneous input power and output power, the intermediate capacitor has to be large enough to absorb the energy difference. Therefore, the electrolytic capacitor with large capacitance is usually used as the energy buffer. Unfortunately, the lifetime of the electrolytic capacitor is limited to several thousand hours under rated operating conditions, which is much shorter than the lifetime of LEDs that is generally higher than 50 000 h. In [31], several lighting management institutions have expressed their needs to have LED drivers with lifetime over 10 years.

In order to prolong the overall lifetime of LED lighting products, it is necessary to reduce the storage capacitance so that nonelectrolytic capacitors can be adopted. A third harmonic injection into the input current to reduce the storage capacitance of continuous conduction mode (CCM) boost PFC and the corresponding implementation circuit is presented in [28]. The major shortcoming with the third harmonic injection is that the current ripple flowing into the LEDs is too large, reducing luminous efficacy of the LEDs. This approach is also used to reduce the peak-average ratio of LED current, but the LED current is controlled as rectified sinusoidal type with zero valley value and 120-Hz frequency, which may also cause noticeable luminous variation and color variation to human eyes [29]. An approach based on load modularization is reported for removing the electrolytic capacitor [30]. The efficiency with this approach is too low, and also the performance depends on the count of the LED load strings. The LED ballast with a dual noncascading structure is proposed [16]. In this design, the short-lifetime high-voltage storage capacitor at the primary is replaced by a long-lifetime low-voltage capacitor at the secondary, thus extending the overall system's lifetime. However, this proposal has two major drawbacks: 1) dimming cannot be achieved with

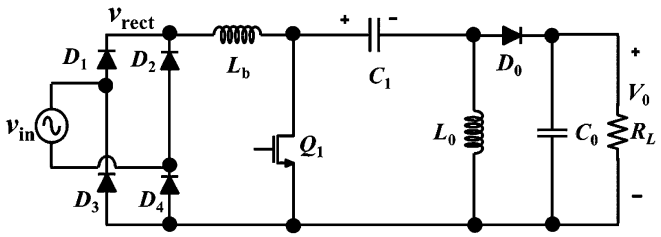

Fig. 2. Conventional SEPIC-derived PFC.

the pulse width modulation (PWM) current control and 2) excessively large secondary capacitance (6.9 mF), requiring parallel of a large amount of capacitors. A passive LED driver for offline applications is presented based on the valley-fill circuit in [31]. Unlike the previous use of the valley-fill circuit targeting for improving the input power factor [32], [33], the major function of the proposed usage of the valley-fill circuit is to reduce the output voltage ripple so as to reduce the size of the output-filter inductor. This solution features circuit simplicity, reliability, and long lifetime because it does not use any power electronic switches, auxiliary power supply, and control boards; however, large size is its disadvantage as the passive PFC circuit.

On the other aspect, dimming control is often needed to regulate lighting levels for human needs, as well as to achieve energy saving, and it is usually implemented by a current regulator stage. According to the circuit topology of the current regulator stage and dimming methods, there are four kinds of LED driving circuits: 1) analog dimming with linear regulators [34]; 2) PWM dimming with linear regulators [22], [35]; 3) analog dimming with switching regulators [19], [20]; and 4) PWM dimming with switching regulators [36]– [40],]. In the analog dimming methods, the LED current level of each string is regulated by adjusting the reference level of the individual current feedback loop. This method is simple and cost effective, but it can also cause color variation. To adjust the LED brightness without color variation over the full dimming range, PWM dimming methods have been widely used because of its high-efficiency operation.

Compared with various topologies, the SEPIC is a better solution for low-power LED lighting application [21]. Fig. 2 shows the conventional SEPIC PFC circuit. It can operate in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) for PFC. The DCM operation can be classified into two forms, which are defined as DCM I and DCM II. DCM I is defined according to the sum of inductor current $i_{\rm Lb}$ and i_{L0}, or the output diode current i_{D0} in the SEPIC topology. This operation mode for LED lamp applications has been discussed in several papers [19]–[22]. It should be noted that the bus voltage still follows the ac input voltage $v_{\rm rect}$ as the CCM operation. Thus, the output capacitor C_0 has to employ an electrolytic capacitor with large capacitance to meet the output voltage ripple's requirement. In DCM II, both the inductor currents i_{Lb} and i_{L0} reduce to zero in one switch cycle, and $i_{\rm Lb}$ reaches to zero before the current i_{L0} reduces to zero. By employing this operation mode, the low-frequency loop consisting of inductors L_b and L_0, and bus capacitor C_1 can be broken. Thus,

the bus capacitor voltage no longer follows the input voltage $v_{\rm rect}$, which helps decouple and balance the difference between pulsating instantaneous input power and constant output power. The isolated version of this circuit with DCM II can be also derived by operating both boost input current shaper (ICS) and the dc/dc converter of boost integrated with flyback rectifier/energy storage/dc–dc converter (BIFRED) in the DCM, while removing the diode inserting between the inductor L_b and the bus capacitor C_1. However, the fast recovery diode must be adopted in the rectified bridge of the modified BIFRED. This concept and conclusion have been presented in [41]–[44]. In this paper, the DCM SEPIC-derived PFC only represents DCM II.

Based on the description made earlier, this DCM SEPIC-derived PFC is very suitable for the low-power LED lighting application because of the ease of the control, the bus capacitor voltage is independent of load, and low cost. However it still has some drawbacks 1) The high voltage rating of active switch Q_1, bus capacitor voltage C_1, and output diode D_0 for achieving high power factor under universal input. Furthermore, in isolation version, with the effect of the leakage inductance of the transformer, the voltage stress of these components becomes even higher. 2) When allowing a relatively large voltage ripple in the PFC design to eliminate electrolytic capacitor, the voltage stress of the output diode D_0 and the bus capacitor will become higher to achieve the high power factor [42]. Additionally, as discussed in [41], [43], and [44], the bus capacitor still adopts the bulky electrolytic capacitor with large capacitance, which do not satisfy the long lifetime requirement of the LED driver.

In this paper, the valley-fill circuit within the SEPIC-derived converter along with PWM dimming is adopted for electrolytic capacitor-less LED lighting applications. Unlike the previous usage of the valley-fill circuit for improving the power factor and reducing the output voltage ripple, the major function of the valley-fill circuit is to break the low frequency loop in the SEPIC converter and to reduce the voltage stress of the intermediate capacitor and output diode. By allowing a relatively large voltage ripple in the PFC design, hence, the film capacitor with small capacitance can be used to replace the electrolytic capacitor. Meanwhile, the current regulator with the PWM dimming function is adopted with a noncascading structure, which is named as "twin-bus buck converter." The detailed operating principle and analysis are described in Sections II and III, respectively. In Section IV, we describe the design procedure. Experimental results for a 50-W prototype are included in Section V. In Section VI, we provide the overall summary of the circuit features based on the implementation results.

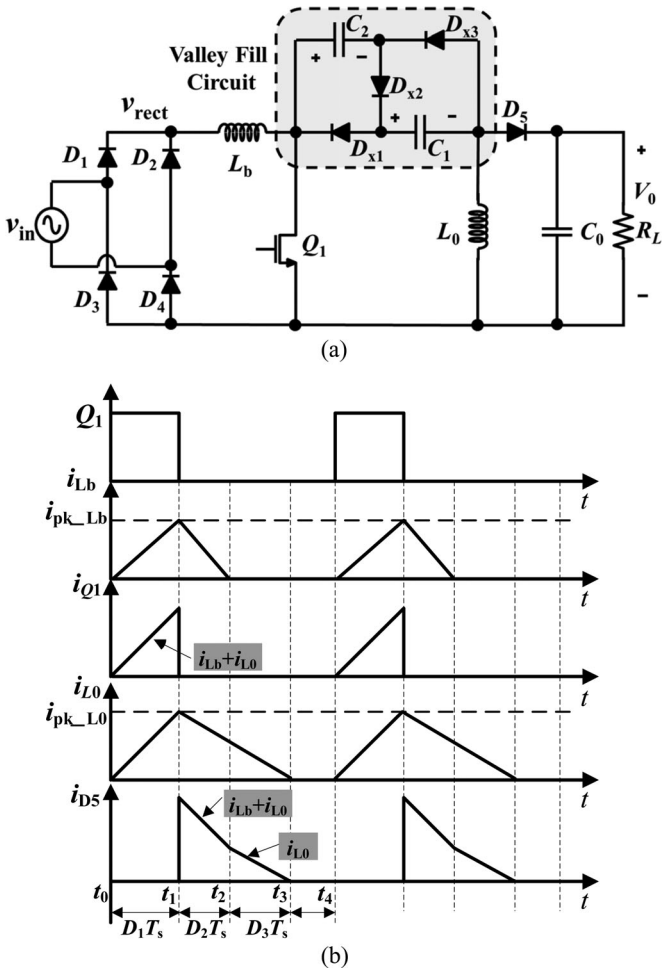

Fig. 3. Proposed topology and its main current waveforms during switching period T_S. (a) Proposed valley-fill SEPIC-derived PFC circuit. (b) Theoretical waveforms in a switch cycle.

II. Operation Principle

Although the isolated version is used in the final implementation, to describe the circuit operation principle, the nonisolated version of the proposed PFC topology shown in Fig. 3(a) is adopted to simplify the circuit analysis. The following assumptions are made throughout the overall analysis.

1) The rectified input voltage, i.e., $v_{\rm rect} = V_m \sin(\omega_l {\rm t})$, is an ideal sine wave, where V_m is the peak amplitude and ω_l is the line angular frequency.
2) The converter is operating at the steady state and all components are ideal.
3) The switching frequency f_s is much higher than the ac line frequency f_l so that the input voltage can be considered constant during one switching period T_s.
4) Capacitors C_1, C_2, and C_0 are large enough so that voltages V_{C1}, V_{C2}, and V_0 can be considered constant during the switching cycle T_s. Moreover, V_{C1} is equal to V_{C2}.
5) Both inductors L_b and L_0 operate in the DCM. Furthermore, the inductor current $i_{\rm Lb}$ reaches zero level prior to the inductor current i_{L0}.

Based on the assumptions made earlier, the circuit operation during one switching cycle can be divided into four distinct intervals. The main current waveforms during a switching period are plotted in Fig. 3(b), while the corresponding equivalent circuits at different operation intervals are shown in Fig. 4. The converter analysis starts at the instant t_0.

Interval [t_0, t_1]: Prior to this interval, the currents through L_b and L_0 are at zero level. When switch Q_1 is turned ON at t_0, diode D_5 is reverse biased. Diode D_{x2} of the valley-fill circuit is also reverse biased. Therefore, capacitors C_1 and C_2 are in

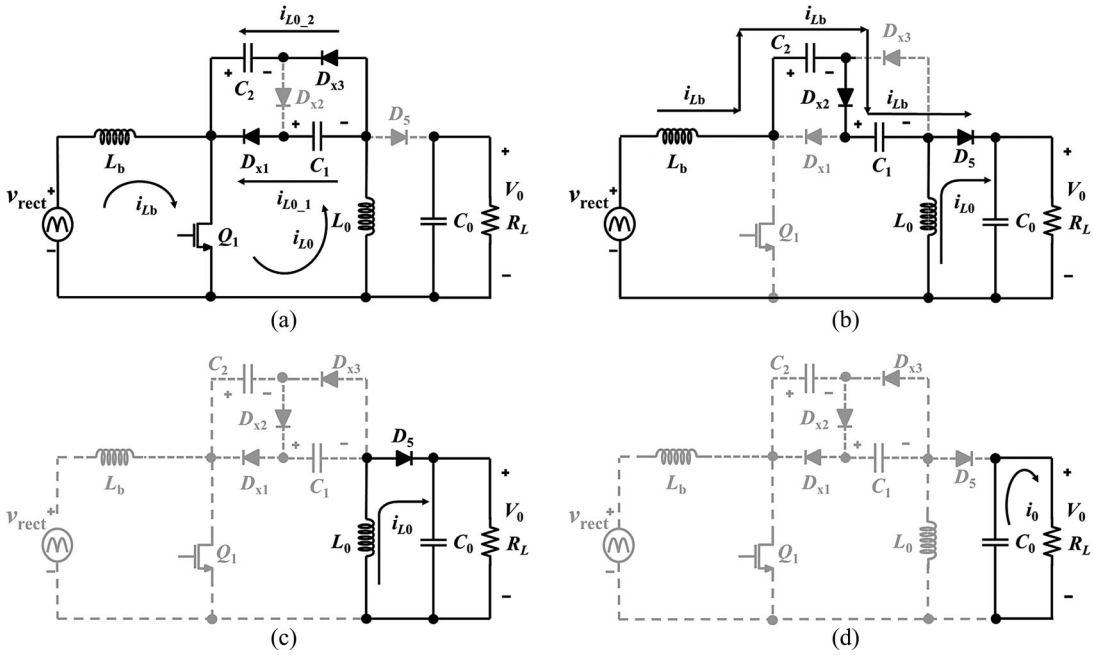

Fig. 4. Equivalent circuits during the different modes: (a) interval $[t_0, t_1]$, (b) interval $[t_1, t_2]$, (c) interval $[t_2, t_3]$, and (d) interval $[t_3, t_4]$.

parallel and serve as the charging power supply of inductance L_0. The equivalent circuit is shown in Fig. 4(a). Hence, currents $i_{\rm Lb}$ and i_{L0} begin to increase linearly as shown in Fig. 3(b). This interval ends when switch Q_1 is turned OFF, initiating the next interval. In this interval, inductor currents $i_{\rm Lb}$ and i_{L0} and switch current $i_Q 1$ can be derived approximately as

$$i_{L_b}(t) = \frac{v_{\rm rect}}{L_b} t \tag{1}$$

$$i_{L_0}(t) = \frac{V_{C_1}}{L_0} t \tag{2}$$

$$i_{Q_1} = i_{L_b}(t) + i_{L_0}(t) = \left(\frac{v_{\rm rect}}{L_b} + \frac{V_{C_1}}{L_0}\right) t. \tag{3}$$

Interval [t_1, t_2]: When switch Q_1 is turned OFF, diode D_{x2} of the valley-fill circuit is forward biased, and D_{x1} and D_{x3} are reverse biased. Thus, capacitors C_1 and C_2 are in series and absorb the discharged energy from inductor L_b. Meanwhile, the output diode D_5 becomes forward biased carrying the sum of i_{Lb} and i_{L0}. Thus, currents $i_{\rm Lb}$ and i_{L0} decrease linearly at the rates proportional to $(2V_{C1}+V_0-v_{\rm rect})$ and V_0, respectively. The corresponding current waveforms are shown as D_2T_S in Fig. 3(b). Fig. 4(b) shows the equivalent circuit at this interval. This interval does not end until current $i_{\rm Lb}$ reaches zero. Both inductor currents i_{Lb} and i_{L0}, and diode current i_{D5} can be described as follows:

$$i_{L_b}(t) = \frac{v_{\rm rect}}{L_b} D_1 T_s + \frac{v_{\rm rect} - 2V_{C1} - V_0}{L_b} t \tag{4}$$

$$i_{L_0}(t) = \frac{V_{C_1}}{L_0} D_1 T_s - \frac{V_0}{L_0} t \tag{5}$$

$$i_{D_5}(t) = \left(\frac{v_{\rm rect}}{L_b} + \frac{V_{C_1}}{L_0}\right) D_1 T_s + \frac{v_{\rm rect} - 2V_{C1}}{L_b} t - \left(\frac{V_0}{L_0} + \frac{V_0}{L_b}\right) t. \tag{6}$$

Interval [t_2, t_3]: In this interval, current i_{L0} continues to decrease through the freewheeling diode D_5. This interval ends when the current of D_5 reaches zero. The corresponding equivalent circuit is plotted in Fig. 4(c).

Interval [t_3, t_4]: This interval is a resting stage, where all switches and diodes are OFF and all branch currents are zero. The converter stays in this state until switch Q_1 is turned ON again.

According to the description made earlier, it is not difficult to understand that capacitors C_1 and C_2 work as the bus capacitor together in the proposed valley-fill SEPIC-derived PFC. Compared with the conventional DCM SEPIC-derived PFC, to achieve the same power factor under the same output voltage V_0 and input voltage, the bus capacitor voltage should have the same voltage value, i.e., $V_{C1\_\rm convential} = V_{C1\_\rm valley} + V_{C2\_\rm valley}$, where $V_{C1\_\rm convential}$ represents the voltage of bus capacitor C_1, $V_{C1\_\rm valley}$ and $V_{C2\_\rm valley}$ are the voltages of capacitors C_1 and C_2, respectively. Thus, one high-voltage bus capacitor in the conventional SEPIC-derived PFC can be replaced by two capacitors with half voltage rating. Meanwhile, when switch Q_1 is turned ON, capacitors C_1 and C_2 are in parallel, thus, the voltage rating of output diode D_5 becomes $V_{C1\_\rm valley} + V_0$, which is far less than that of the conventional DCM SEPIC-derived PFC.

III. Analysis of the Proposed PFC Topology

A. Calculation of the Power Factor Value

For simplicity, based on the same assumptions described in Section II, the input voltage is defined as $v_{\rm in} = V_m \sin(\omega_l t)$. Then, the rectified voltage is $v_{\rm rect} = V_m \sin(\omega_l t)$. Based on the current waveform of inductor L_b in a switching cycle when the

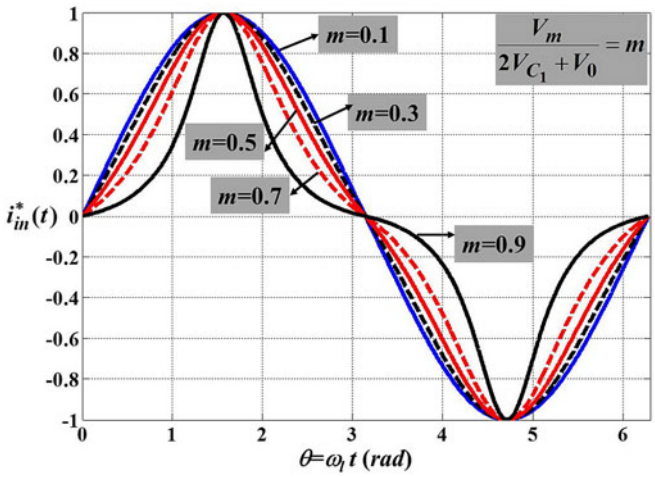

Fig. 5. Normalized input current waveform $i^*_{\rm in}(t)$ in a line cycle.

converter operates at the DCM, the average inductor current in a switching cycle can be derived as follows:

$$i_{\rm Lb\_ave}(t)=\frac{1}{2}i_{Lb\_pk}(D_1+D_2)=\frac{V_m D_1^2}{2L_b f_s}\times\frac{|\sin\omega_l t|}{1-V_m/(2V_{C1}+V_0)\,|\sin\omega_l t|}. \tag{7}$$

Here, D_1, f_s, and V_o are the duty cycle, the switching frequency, and the output voltage, respectively. D_2 is the duty cycle corresponding to the reset time of the inductor current $i_{\rm Lb}$. Therefore, the input current is achieved as

$$i_{\rm in}(t)=\frac{V_m D_1^2}{2L_b f_s}\frac{\sin\omega_l t}{1-V_m/(2V_{C1}+V_0)\,|\sin\omega_l t|} \tag{8}$$

when D_1 is considered constant. By choosing a base current of $I_{\rm base}=(V_m/2L_b f_s)D_1^2/(1-V_m/(2V_{C1}+V_0))$, the normalized input current, i.e., $i^*_{\rm in}(t)=i_{\rm in}(t)/I_{\rm base}$, becomes

$$i^*_{\rm in}(t)=\left(1-\frac{V_m}{2V_{C1}+V_0}\right)\frac{\sin\omega_l t}{1-V_m/(2V_{C1}+V_0)\,|\sin\omega_l t|}. \tag{9}$$

Fig. 5 shows the normalized input current $i^*_{\rm in}(t)$ under different values $m=V_m/(2V_{C1}+V_0)$. It can be seen that the shape of the input current is only dependent on m, and the smaller the m, the closer to sinusoidal the current shape. This can be explained as follows. As the peak value of the inductor current is in the sinusoidal shape, and the duty cycle is constant in a line cycle, the average value of the inductor current in the rising interval is sinusoidal. However, the falling time of the inductor current depends on the value of $(2V_{C1}+V_0-v_{\rm rect})$; so; the average value of the inductor current in the falling interval is not sinusoidal. Thus, the average value of the inductor current in a switching cycle is not sinusoidal. For a smaller m, the inductor current falling time is shorter, and the inductor current wave shape is closer to sinusoidal.

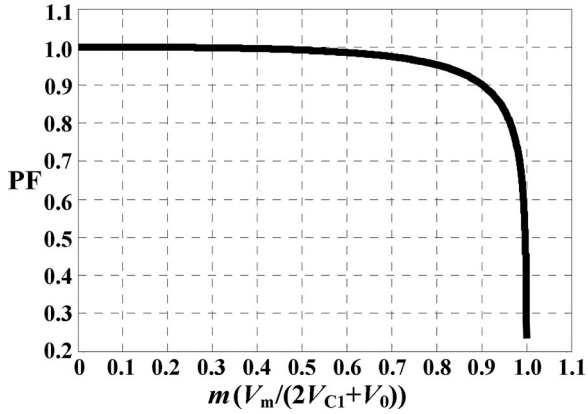

Fig. 6. Power factor as a function of m.

The average input power in a half line cycle can be calculated as

$$P_{\rm in}=\frac{1}{T_{\rm line}/2}\int_0^{T_{\rm line}/2}v_{\rm in}(t)i_{\rm in}(t)dt=\frac{1}{2}\frac{V_m^2}{L_b f_s}D_1^2\frac{1}{\pi}\int_0^{\pi}\frac{\sin^2\omega_l t}{1-V_m/(2V_{c1}+V_0)\,|\sin\omega_l t|}d\omega_l t. \tag{10}$$

The power factor PF is achieved as

$$\mathrm{PF}=\frac{P_{\rm in}}{V_{\rm rms}\times I_{\rm rms}}=\frac{P_{\rm in}}{(1/\sqrt{2})V_m\times\sqrt{(1/\pi)\int_0^{\pi}i_{\rm in}^2 d\omega_l t}}=\frac{\sqrt{2/\pi}\int_0^{\pi}[\sin^2\omega_l t/(1-V_m/(2V_{C1}+V_0)\,|\sin\omega_l t|)d\omega_l t}{\sqrt{\int_0^{\pi}[\sin\omega_l t/(1-V_m/(2V_{C1}+V_0)\,|\sin\omega_l t|)]^2\,d\omega_l t}}. \tag{11}$$

The PF as function of m is plotted in Fig. 6. The result indicates that a larger m yields a poorer PF, consistent with the waveform distortion shown in Fig. 5.

Assuming that the efficiency of the converter is 100%, i.e., $P_{\rm in}=P_0$, duty cycle D_1 can be calculated as

$$D_1=\frac{1}{V_m}\sqrt{\frac{2\pi L_b f_s P_0}{\int_0^{\pi}[\sin^2\omega_l t/(1-V_m/(2V_{C1}+V_0)\,|\sin\omega_l t|)d\omega_l t}}. \tag{12}$$

Using the aforementioned equation, Fig. 7 can be plotted to show the relationship between the voltage conversion ratio M and duty cycle D_1 based on the given inductance ratio (L_b/L_0 = 1.6) and selected the inductor L_b (L_b = 350 μH), where M is defined as the ratio of the output voltage V_0 and the peak value of ac input voltage V_m. Fig. 7 indicates that the voltage conversion ratio M is linearly proportional to duty cycle D_1.

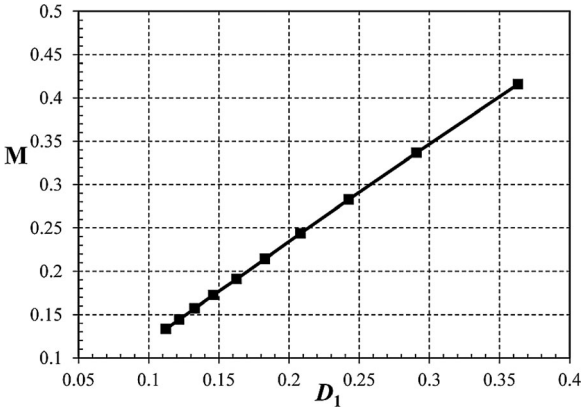

Fig. 7. Voltage-conversion ratio M versus duty cycle D_1.

B. Calculation of Average Voltage and Ripple of Storage Capacitor

During a half line cycle, the energy absorbed from the ac line equals the energy delivered to the load:

$$P_0 = \frac{1}{\pi}\int_0^{\pi}\left[\frac{V_{C1}^2}{2L_0}D_1^2T_s + V_0\cdot\frac{V_m^2\sin^2(\omega_l t)}{2L_b(2V_{C1}+V_0-V_m\,|\sin(\omega_l t)|)}D_1^2T_S\right]d\omega_l t. \tag{13}$$

Let $P_{\rm in} = P_0$, and then, the following can be derived:

$$\frac{2V_m^2}{\pi V_{C1}}\times\int_0^{\pi}\left[\frac{\sin^2\omega_l t}{2V_{C1}+V_0-V_m\,|\sin\omega_l t|}\right]d\omega_l t = \frac{L_b}{L_0} \tag{14}$$

.The aforementioned equation implies that: 1) V_{C1} is independent of the load; 2) when the peak value of the input voltage V_m and output voltage V_0 are certain, V_{C1} is a function of L_b/L_0; 3) when L_b/L_0 is determined, V_{C1} is a nonlinear function of V_m.

The relationship of the storage capacitor and its voltage ripple can be analyzed as following. When the input power factor is unity, the waveform of the input voltage, the input current, the input power, the output power, and the storage capacitor voltage is shown in Fig. 8. The instantaneous input power is

$$P_{\rm in} = v_{\rm in}\times i_{\rm in} = \frac{V_m I_m(1-\cos 2\omega_l t)}{2}. \tag{15}$$

During a half line cycle, the average input power is equal to the output power. As shown in Fig. 8, the instantaneous input power is greater than the output power in the ω_lt = [π/4, 3π/4] interval. Hence, in the ω_lt = [π/4, 3π/4] interval, the total energy change of the capacitor C_1 is

$$\Delta E = \frac{1}{2}\int_{1/4\,\pi}^{3/4\,\pi}\frac{1}{\omega_l}(P_{in}-P_0)d\omega_l t = \frac{P_0}{2\omega_l} \tag{16}$$

.With the relationship of the capacitor energy and its voltage, we obtain

$$\frac{1}{2}C_1(V_{C1\_\rm Max}^2 - V_{C1\_\rm Min}^2) = \Delta E \tag{17}$$

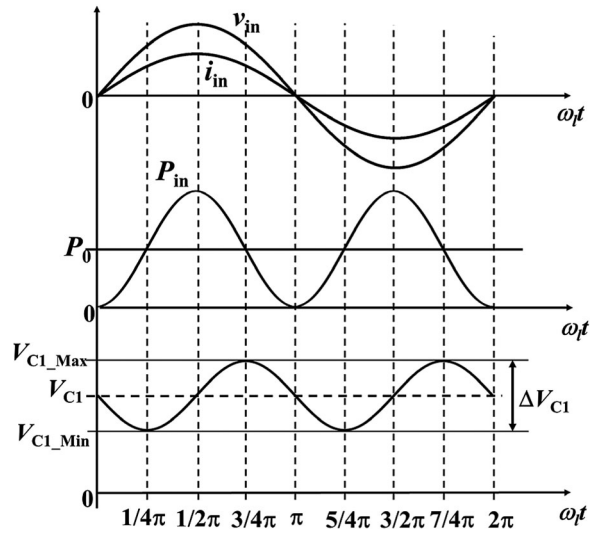

Fig. 8. Theoretical waveforms of storage capacitor when PF = 1.

where C_1 is the storage capacitance, and $V_{C1\_\rm Max}$ and $V_{C1\_\rm Min}$ are the maximum value and the minimum value of the capacitor voltage, respectively. Substituting (16) into (17), the following is obtained:

$$\Delta V_{C1} = \frac{\Delta E}{C_1 V_{C1}} = \frac{P_0}{2\omega_l C_1 V_{C1}} \tag{18}$$

where V_{C1} and ΔV_{C1} are the average value and the peak-to-peak ripple value of the capacitor voltage, respectively.

C. Compared With the Conventional DCM SEPIC-Derived PFC

Consider a well-known boost integrated with the BIFRED circuit; it is not suitable for PWM dimming LED lighting application because its bus voltage is dependent on load. As described in Section I, the DCM SEPIC-derived PFC is considered as a DCM BIFRED. According to the analysis made earlier and (11), the power factor is determined by the average bus capacitor voltage for the same input voltage and output voltage when the ripple is neglected, or when circuit employs the electrolytic capacitor with large capacitance. Because the duty cycle D_1 can be considered as constant, as long as the capacitor value is large enough to meet the small ripple assumption, the proposed valley-fill PFC circuit and the conventional DCM SEPIC-derived PFC will obtain the same power factor.

However, under the electrolytic capacitor-less condition, the ripple of storage capacitor is relatively large. The large ripple will affect the PF value. Meanwhile, the duty cycle D_1 will not be considered as the constant value. The variation of the duty cycle will be the decisive factor of the power factor. From (18), this voltage ripple is determined by the average voltage and capacitor value for same input voltage and output power. Hence, when selecting the appropriate inductor ratio L_b/L_0 to make sure the same average bus voltage, i.e., $V_{\rm C1\_DCM\_sepic} = V_{\rm C1\_valley} + V_{\rm C2\_valley}$, for achieving the same power factor, it is not difficult to know that the variation of the duty cycle D_1 in the proposed PFC circuit is half of the variation of the duty

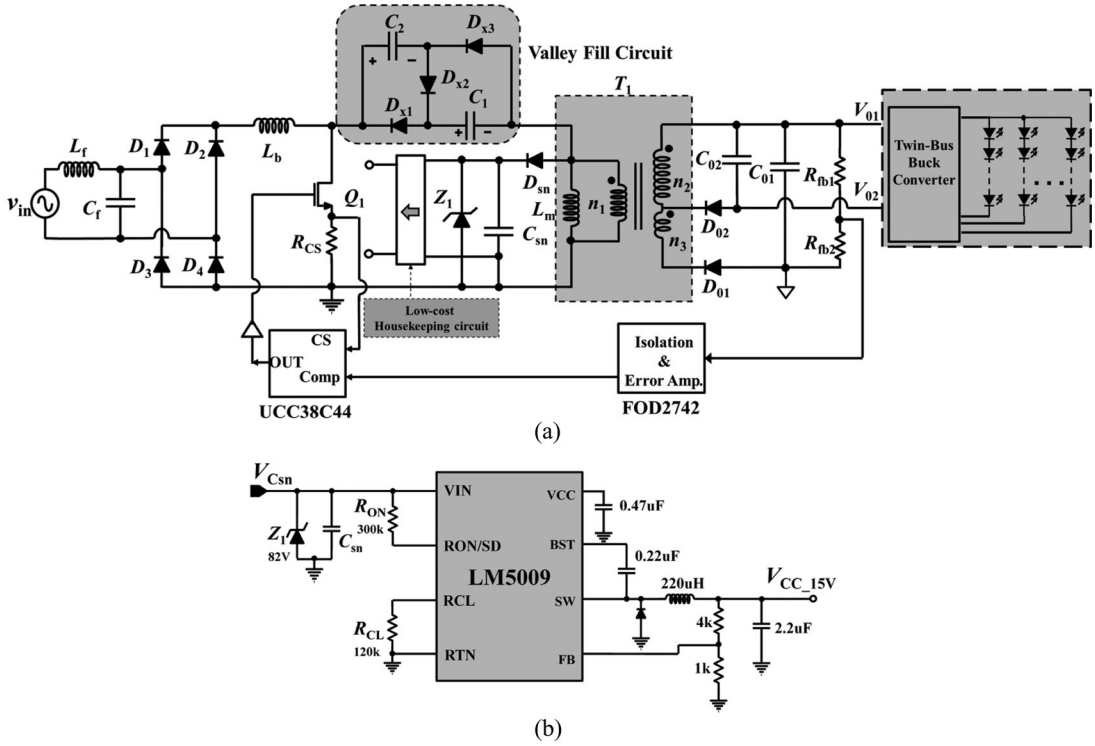

Fig. 9. Proposed offline LED driver without electrolytic capacitor and its auxiliary power supply. (a) Proposed offline LED driver without electrolytic capacitor. (b) Auxiliary power supply for low-voltage control and gate driver circuitry.

cycle D_1 in the DCM SEPIC-derived PFC circuit theoretically. Therefore, the valley-fill SEPIC-derived PFC should select half of capacitance of the DCM SEPIC-derived PFC theoretically to achieve the same duty cycle variation:

$$C_{1\_\text{valley}} = C_{2\_\text{valley}} = 0.5 \times C_{1\_\text{DCM\_SEPIC}} \tag{19}$$

Provided that the same duty cycle variation is obtained under the electrolytic capacitor-less condition, the proposed PFC circuit will have the same power factor and output voltage ripple. Considering the energy amount (CV^2) as the capacitor sizing criterion, the proposed circuit requires only one quarter of the capacitor energy as compared to the DCM SEPIC-derived PFC circuit.

From the viewpoint of size, this result indicates the significant size reduction of LED driver, because of the following reasons.

1) The voltage rating of bus capacitor C_1_valley and C_2_valley is half of the DCM SEPIC-derived PFC.
2) The capacitance in the proposed circuit only is half of that of the conventional DCM SEPIC-derived PFC circuit.

IV. Proposed Circuit for Multiple LED Lighting Lamps

Fig. 9 shows the proposed circuit for driving multiple LED lighting lamps. The complete circuit consists of the proposed isolated valley-fill SEPIC-derived PFC circuit and a twin-bus buck converters. The isolated ac–dc converter produces two dc similar level voltages, i.e., V_{01} and V_{02}, while drawing a high power factor and low harmonic current to meet the standard, such as IEC 61000-3-2 Class C. The twin-bus buck switching converter is employed as a current regulator for the PWM dimming control.

The auxiliary power supply for the valley-fill SEPIC-derived converter can be obtained by recycling the snubber capacitor energy. In Fig. 9(a), D_{sn} and C_{sn} serve as the snubber circuit to clamp the MOSFET voltage spike during turnoff. Fig. 9(b) shows the schematic of the auxiliary power supply. The energy stored in C_{sn} is regulated to 15 V by LM5009 to supply the control and gate drive circuitry. The voltage across the snubber capacitor depends on the power drawn by the control circuit. Because the snubber capacitor C_{sn} is paralleled with zener Z_1, the maximum voltage across capacitor C_{sn} is 82 V. The LM5009 is a step-down switching regulator with the 100-V maximum input voltage and 150-mA output current capability, sufficient to provide the driving power to the entire control circuit.

A. PWM Dimming Design

As shown in Fig. 10(a), a twin-bus buck switching converter is employed as the current regulator and PWM dimming control. V_{01} and V_{02} come from the front-end isolation PFC. The MOSFET Q_{DIM} is the dimming transistor. The voltage across capacitors C_{01} and C_{02} can be treated as two voltage sources, which are the input-voltage source of twin-bus buck converters. Note that the first input voltage is regulated by an ac–dc converter with a level slightly higher than the maximum voltage of the LED strings. The second input voltage can be obtained from a proper turns ratio with a level slightly lower than the minimum voltage of the LED strings at the rated current. The two voltage sources are defined as the twin bus because their voltages

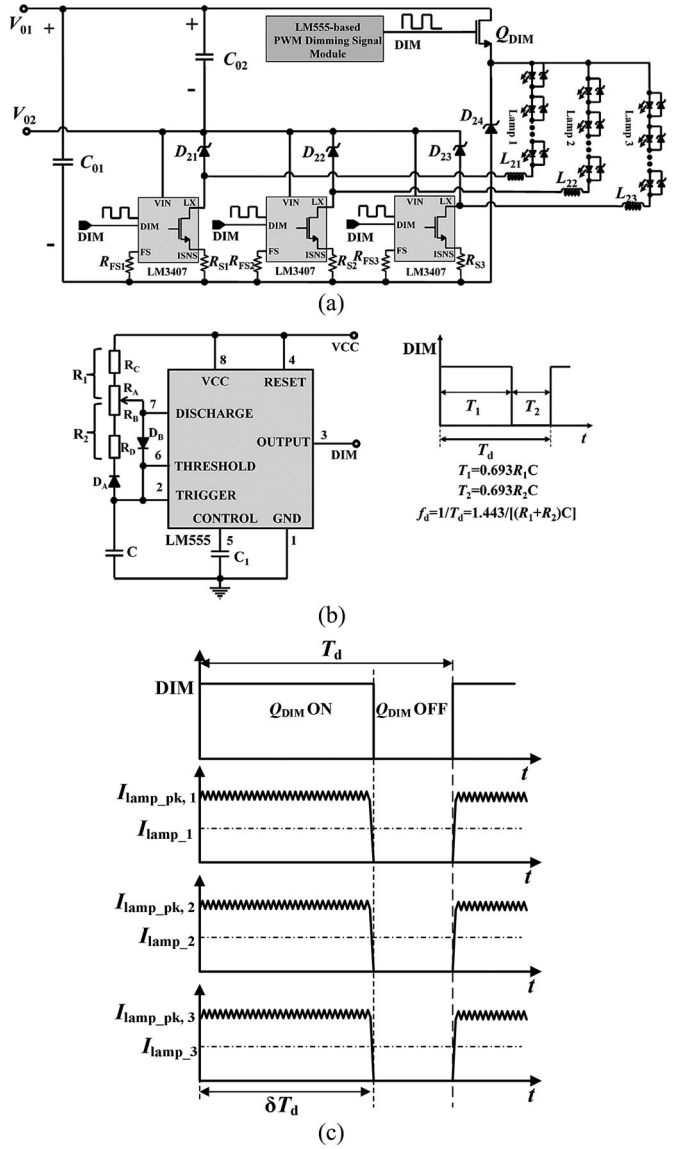

Fig. 10. Current regulator with the PWM dimming function and its theoretical waveform. (a) Current regulator circuit. (b) PWM dimmer circuit. (c) Theoretical waveform of PWM dimmer.

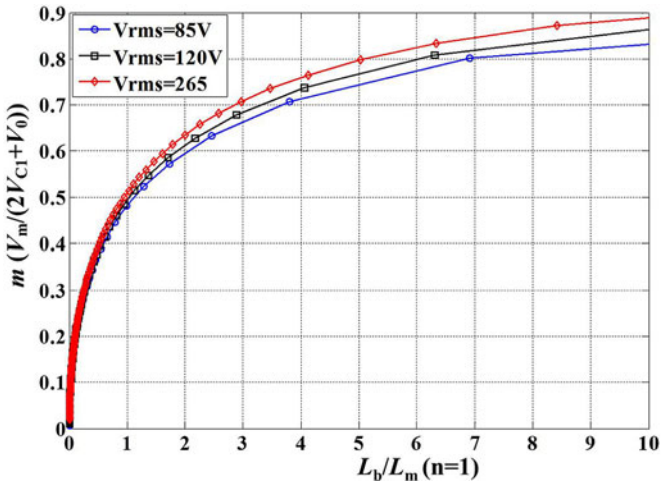

Fig. 11. $m\ (V_m/(2V_{C1}+V_0))$ versus L_b/L_m

are close and shared by the LED strings. When the MOSFET $Q_{\rm DIM}$ is turned ON, inductor L_{2i}, diode D_{2i} (i = 1, 2, 3), the power MOSFET integrated in LM3407, and the twin-bus input voltage source constitute the power stage of the twin-bus buck converter to regulate the LED current at the desired level. The detailed theory can be found in [40].

The operating frequency of the dimming MOSFET is usually higher than 70 Hz, making them perceivable to the human eye. Considering the switching loss for the dimming transistors, the PWM dimming frequency in this paper is designed at 400 Hz. Fig. 10(b) shows the detailed PWM dimming implementation circuit using LM555. The output of PWM dimming circuit DIM is to feed the current regulator LM3407 to add one more stage control for the power *N*-MOSFET that is integrated in LM3407. Note that a driver circuit with the charge pump function is inserted to drive the floating dimming MOSFET $Q_{\rm DIM}$.

Fig. 10(c) shows the theoretical waveforms of the LED dimmer. The average LED lamp current can be represented as

$$I_{{\rm lamp},j} = \delta I_{{\rm lamp\_pk},j}, \quad j = 1, 2, 3 \tag{20}$$

where $I_{{\rm lamp\_pk},j}$ is the peak current value of the LED lamp j, and δ is the duty ratio of the dimming MOFET $Q_{\rm DIM}$. The peak current of the LED lamp j can be set by selecting the sense resistor $R_{{\rm s}j}$. As shown in Fig. 10(c), each LED lamp average current $I_{{\rm lamp},j}$ is regulated by adjusting the duty ratio δ.

In addition, any LED failure will result in the extinguishment of the corresponding LED lamp. As shown in Fig. 10(a), each LED is connected in parallel with a zener diode. When a LED fails, the voltage across the failed LED reaches the breakdown voltage of the zener diode. The LED current can flow through the parallel-connected zener diode, and the LED array will not be extinguished.

B. Optimal Design Flow of the Proposed Valley-Fill SEPIC-Derived PFC Without an Electrolytic Capacitor

According to the analysis in Section III, the design of the two inductors L_b and L_0 is the key for ensuring the proper operation mode. As shown in Fig. 6 and (11), the power factor is determined directly by the ratio $V_m/(2V_{C1} + V_0)$. Meanwhile, the voltage V_{C1} is the function of the ratio of L_b and L_0 for the known input voltage according to (14). However, they are very difficult to solve directly. Hence, the design must depend on the numerical calculation software. Fig. 11 shows $V_m/(2V_{C1}+V_0)$ as a function of L_b/L_0 at the different input-voltage condition, where n is the turns ratio of the transformer. This figure indicates that the ratio of L_b and L_0 can be selected according the known input voltage and power factor requirement. Once the ratio of L_b and L_0 is determined, the corresponding parameter will be calculated based on the DCM operation condition of both inductors.

The results of the analysis made earlier and the design approach are based on the assumptions that the voltage of the capacitor of valley-fill circuits C_1 and C_2 is considered as constant. Since the film capacitor with small capacitance is employed here

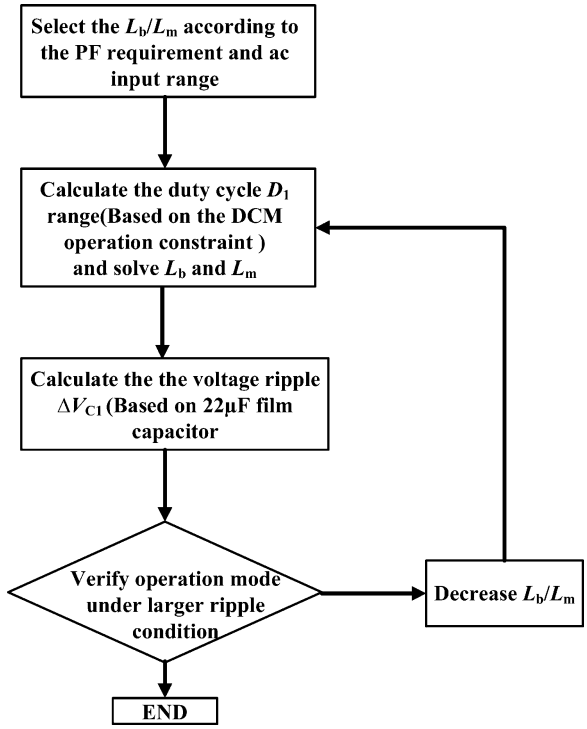

Fig. 12. Proposed optimal design flow of solving the inductances

to replace the bulk electrolytic capacitor, the capacitor voltage is no longer constant, and the design becomes much more difficult. Hence, an optimal design process is proposed to solve the inductor L_b and L_0. The optimal design flow chart is shown in Fig. 12, and the procedure is described as follows.

Step 1: Select the ratio of inductor L_b and L_0 according to the requirement of the power factor and input voltage range. For a given input voltage range, according to Figs. 6 and 11, the ratio of L_b and L_0 can be selected to meet the power factor requirement.

Step 2: Calculate the duty cycle D_1. Once the ratio of L_b and L_0 is determined, the average voltages of the capacitor of valley-fill circuit V_{C1} and V_{C2} can be calculated under different input voltages. Then, the duty cycle D_1 range can be solved based on the DCM operation constraint under different input voltages. Note that inductance L_b can be calculated based on the DCM operation constraint and need to be determined through iterations with different input voltages. L_0 can then be obtained based on the selected ratio of L_b and L_0.

Step 3: Calculate the voltage ripple ΔV_{C1}. The results of the calculation performed earlier are suitable for the condition that V_{C1} and V_{C2} are constant during the line period. If the capacitance is reduced, its voltage ripple will become larger consequentially. Due to the large variation of the capacitor voltage in a line cycle, it is difficult to determine the valley-fill capacitor voltage. However, the average capacitor voltage and its ripple can still be estimated from the calculation results of (14) and (18). It should be noted that a larger voltage ripple tends to decrease the efficiency under the same ac input voltage. The complete design thus needs a tradeoff among voltage ripple, efficiency, average voltage, and power factor. In the proposed design case, a 22-μF film capacitor is chosen.

Step 4: Verify if both inductors work in the DCM. As mentioned earlier, the design of L_b and L_0 is based on the assumption that ΔV_{C1} is small enough. L_b and L_0 may not work in the proper mode under the large ripple condition. Hence, it must be verified that L_b and L_0 both work in the DCM under the minimum value of the capacitor voltage $V_{C1\_\min}$. Meanwhile, simulation verification is also necessary. If the verification result shows the satisfactory DCM operation, the design process is finished. Otherwise, the ratio of L_b and L_0 must be reduced and return to Step 2 until the condition in Step 4 is satisfied. Note that for the isolated version, the inductor L_0 is realized by the magnetic inductance L_m.

C. Components' Stress

The voltage and current stresses are analyzed in the following section. To achieve high power factor and high efficiency under universal input voltage (85–265 V), the inductance values of L_b and L_0 are selected as 350 and 220 μH, respectively.

1) Voltage Stress of Bus Capacitors C_1 and C_2: According to the basic circuit operation principle, the voltage stress should be calculated under the maximum ac input voltage condition. From (14), the voltage rating of bus capacitors C_1 and C_2 is 290 V. According to (18), the ripple is about 35 and 10 V under 85- and 265-V input voltages, respectively.

2) Voltage and Current Stress of Active Switch Q_1 and Output Diode D_{01}: In the designed example case, the turns ratio of transformer is selected as 1 to be compatible with the nonisolation case. According to the operating principle described in Section II, switch Q_1 and diode D_{01} alternately conduct, leading to the fact that the conducting device carries its maximum current, while the nonconducting counterpart bears its maximum voltage stress. Therefore, the maximum voltage stress of active switch Q_1 can be estimated as

$$V_{Q_1\_\max} = V_{C_1\_\max} + V_{C_2\_\max} + V_0 = 2V_{C_1\_\max} + V_0 = 630 \text{ V} \quad (21)$$

where $V_{C_1\_\max}$ and $V_{C_2\_\max}$ are the maximum voltage stress of bus capacitors C_1 and C_2, respectively.

However, output diode D_{01} only bears the sum of bus capacitor voltage $V_{C_1\_\max}$ and output voltage V_0:

$$V_{D_{01}\_\max} = V_{C_1\_\max} + V_0 = 290 + 50 = 340 \text{ V}. \quad (22)$$

Furthermore, both Q_1 and D_{01} carry the peak current of i_{Lb} and i_{L0}. Thus, the maximum current stresses on Q_1 and D_{01}, i.e., $I_{Q1\_\max}$, and $I_{D01\_\max}$, can be calculated based on the minimum input voltage:

$$I_{Q_1\_\max} = I_{D_{01}\_\max} = D_{1\_\min} T_s \left(\frac{V_{m\_\min}}{L_b} + \frac{V_{C1\_\min}}{L_0} \right) \quad (23)$$

where $D_{1\_\min}$, $V_{m\_\min}$, and $V_{C1\_\min}$ refers to the duty cycle, peak input voltage, and bus capacitor under the minimum input voltage condition, respectively. From (15), duty cycle $D_{1\_\min}$

is 0.35, and thus

$$I_{Q_1\_\max} = I_{D_{01}\_\max} = 0.35 \times \frac{1}{53\times 10^3} \times \left(\frac{85\times\sqrt{2}}{350\times 10^{-6}} + \frac{100}{220\times 10^{-6}}\right) = 5.2\text{A}. \quad (24)$$

3) Voltage and Current Stress of Valley-Fill Circuit's Diode D_{x1}, D_{x2}, and D_{x3}: It is not difficult to know that voltage ratings of diodes D_{x1}, D_{x2}, and D_{x3} are identical, which are equal to the bus capacitor voltage V_{C1}. Current ratings of diode D_{x1} and D_{x3} are the same and are equal to half of $i_{\text{pk\_L0}}$. The current rating of diode D_{x2} is equal to the peak current $i_{\text{pk\_Lb}}$, where i_{pk_L0} and $i_{\text{pk\_Lb}}$ are the peak values of inductor currents i_{L0} and i_{Lb}, respectively. The current rating of valley-fill diodes, i.e., $I_{Dx1\_\max}$, $I_{Dx2\_\max}$, and $I_{Dx3\_\max}$, are estimated as follows:

$$I_{D_{x1}\_\max} = I_{D_{x3}\_\max} = \frac{1}{2}D_{1\_\min}T_s\left(\frac{V_{C1\_\min}}{L_0}\right) = \frac{1}{2} \times 0.35 \times \frac{1}{53\times 10^3}\left(\frac{100}{220\times 10^{-6}}\right) = 1.5\text{ A} \quad (25)$$

$$I_{D_{x2}\_\max} = D_{1\_\min}T_s\left(\frac{V_{m\_\min}}{L_b}\right) = 0.35 \times \frac{1}{53\times 10^3} \times \left(\frac{85\times\sqrt{2}}{350\times 10^{-6}}\right) \approx 2.3\text{ A}. \quad (26)$$

V. Experimental Results and Verification

In order to verify the validity of the proposed circuit operation without an electrolytic capacitor for driving multiple LED lamps, a 50-W prototype has been built and tested in the laboratory. The specifications of the prototype are as follows:

1) universal input voltage: $v_{\text{in}} = 85$–$265\ v_{\text{ac}}$, 60 Hz;
2) twin-bus output voltage: $V_{01} = 50\ V_{\text{dc}}$, $V_{02} = 45\ V_{\text{dc}}$;
3) rated output power: $P_0 = 50$ W;
4) switching frequency: $f_s = 53$ kHz.

Based on the aforementioned design specifications, the final designed parameters and selected components of the isolated valley-fill SEPIC-derived prototype are listed in Table I.

Three LED lamps are configured with 15 series-connected LUMILEDS emitter-type LEDs, respectively. Each LUMILEDS LED is a 1.1-W high luminance with a nominal voltage of 3.2 V at a rated current of 350 mA. Three constant current control chips LM3407 containing the low-side 0.77-Ω/40-V *N*-channel MOSFET and the peak current mode controllers are used as the independent string current regulators. The other key components are shown in Table II. Resistor R_{FS} with the 40.2-kΩ value is used to set the switching frequency to 1.08 MHz.

Fig. 13 shows the experimental waveform under the lowest input voltage of 85 V and full-load condition. Fig. 13(a) indicates that the input current i_{in} is near-sinusoidal and is in phase with the input voltage v_{in}. The measured power factor is about 0.96. Note that the average valley-fill capacitor voltage V_{C1} and its ripple ΔV_{C1} are 80 and 40 V, respectively, which agree well with the calculation of (14) and (18). The fourth channel in

TABLE I
Components and Parameter Values in the Proposed PFC Prototype

REF	Value	Description
L_f	390μH	2119-RC
C_f	0.1μF	630V ceramic capacitor
D_1~ D_4	STTH3L06U	600V/3A ultra-fast diode
L_b	350μH	ETD 29
D_{x1}, D_{x2}, D_{x3}	STTH3L06U	600V/3A ultra-fast diode
D_{sn}	STTH2L06U	600V/2A ultra-fast diode
C_{sn}	10nF	630V ceramic capacitor
C_1, C_2	22μF	450V metallized polypropylene film capacitor, ESR=5mΩ
Q_1	STB18NM80	800V/17A R_{ds_on}=0.25Ω
T_1	L_m=220uH 20:18:2	PQ32/30
C_{01}, C_{02}	4×10μF	100V multilayer ceramic capacitor
D_{01}, D_{02}	STTH3L06U	600V/3A ultra-fast diode
Control IC	UCC38C44	Current-mode PWM controller

Fig. 13(a) shows the measured waveform of the output voltage V_{01}. As can be seen, the output voltage is regulated well with very small voltage ripple. Fig. 13(b) shows the experimental waveforms of the inductor current i_{Lb}, voltage of switch V_{ds}, and voltage of output diode V_{D01} under the peak value of input line voltage. From Fig. 13(b), it can be seen that the spike of switch Q_1 have been clamped to 240 V by the snubber circuit, and the voltage stress of the output diode D_{01} is equal to V_{C1}, which is less than voltage stress of the output diode presented in [41]–[44]. The inductor L_b always operates in the DCM for automatic power factor correction. Experimental results at the input voltages of 110 and 220 V are shown in Figs. 14 and 15, respectively.

Fig. 16 shows the experimental waveform under the highest input voltage of 265 V and full-load condition. The measured power factor is about 0.962. Similarly, the average valley-fill capacitor voltage V_{C1} and its ripple ΔV_{C1} also agree well with the calculation results using (14) and (18). The fourth channel in Fig. 16(a) shows the measured waveform of the output voltage V_{01}. As can be seen, the output voltage is regulated well with very small voltage ripple. Fig. 16(b) shows the experimental waveforms of inductor current i_{Lb}, voltage of switch V_{ds}, and voltage of output diode V_{D01} under the peak value of input line voltage. From Fig. 16(b), it can be seen that the spike of switch Q_1 has been clamped to 630 V by the snubber circuit, and the voltage stress of output diode D_{01} is equal to V_{C1}, which is about 260 V. In [41]–[44], the voltage rating of the output diode D_{01} is the sum of V_{C1} and V_{C2}, which may exceed 500 V. Hence, the voltage rating of the output diode D_{01} and bus capacitor in the proposed circuit is significantly reduced as compared to the circuit shown in [41]–[44]. The inductor L_b always operates in the DCM for automatic power factor correction. From Figs. 13–16, the circuit works well over the entire universal line input operation.

Fig. 17 depicts the power factor and efficiency under different output power conditions with the 110-V ac input voltage.

TABLE II
COMPONENTS SELECTION IN THE TWIN-BUS CURRENT REGULATOR

REF	Value	Description
Q_{DIM}	FDS3672	22mΩ/100V/7.5A MOSFET
D_{21}~ D_{23}	BAT60A	10V/3A Schottky diode
D_{24}	PDS5100H-13	100V/5A Schottky diode
L_{21}~L_{23}	33uH	Rated current 0.82A SLF7045T-330MR82-PF
R_{FS1}~R_{FS3}	40.2kΩ	1/8W 1% 0805 SMD
R_{S1}~R_{S3}	Two 1.13Ω resistors in parallel	1/8W 1% 0805 SMD

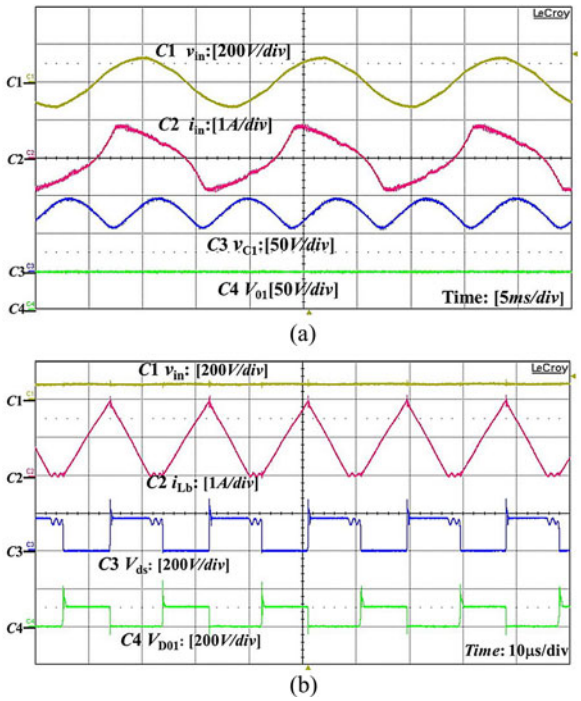

Fig. 13. Measured waveforms under input voltage of 85 V. (a) Measured input voltage v_{in}, input current i_{in}, bus voltage v_{C1}, and output voltage V_{01} waveform. (b) Inductor current i_{Lb}, voltage of the switch V_{ds}, and output diode V_{D01} at input ac peak voltage.

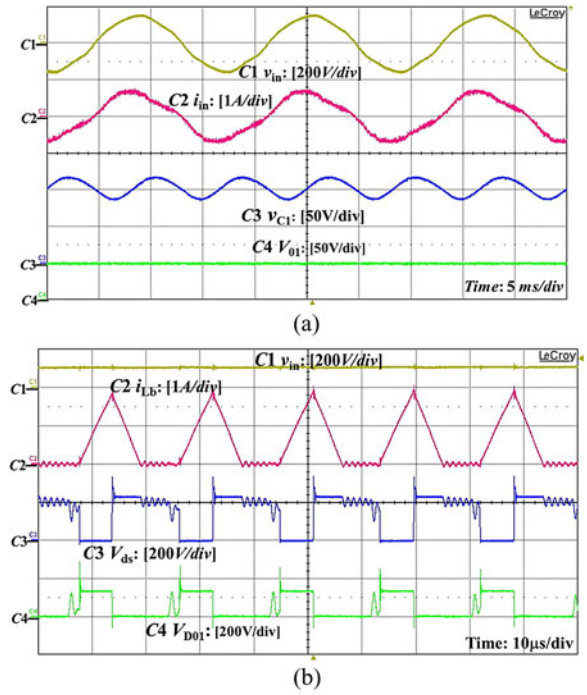

Fig. 14. Measured waveforms under the input voltage of 110 V. (a) Measured input voltage v_{in}, input current i_{in}, bus voltage v_{C1}, and output voltage V_{01} waveform. (b) Inductor current i_{Lb}, voltage of the switch V_{ds}, and output diode V_{D01} at input ac peak voltage.

The full load efficiency and PF are about 90.6% and 0.97, respectively. At 20% load, the power factor is about 0.918, which completely meets the power factor requirement.

Fig. 18 compares the measured input current harmonics under input voltages of 110 and 220 V with the IEC 61000-3-2 class C. The results indicate that individual harmonics are well within the standard limits. Fig. 19 shows the full-load power factor and efficiency variations under the different input voltages. The power factor and efficiency peak at about 140-V input and taper down in both low and high voltages.

The photograph of the experimental prototype is shown in Fig. 20. The figure indicates that the size of the proposed valley-fill SEPIC-derived power factor circuit is 9×15 (W×L) cm^2. The height is limited by the film capacitor of valley-fill circuit, which is about 30 mm. Similar to [29], the magnetic components L_b, transformer T_1, and film capacitors of valley-fill circuit, i.e., C_1 and C_2, occupy 80% of the prototype area. The size of the magnetic components can be reduced by increasing the operation switching frequency. However, as many proposed the LED lighting driver without an electrolytic capacitor, the size of high voltage film capacitor will be still an issue to integrate the driver circuit into LED luminaire, which may be improved by better capacitor technologies in the future. Nevertheless, this solution is still suitable for some special applications, such as street lighting and electronic ballasts (or drivers for the LED lighting system).

Fig. 21 shows the measured LED lamp current and device voltage waveforms at 350-mA average current with the 1.08-MHz operation frequency. V_{Lx} represents the voltage stress of the power switch integrated in LM3407. The LED current is well regulated with less than 10% peak-to-peak ripple. It is worth noting that the stress of the active switch is 5 V,

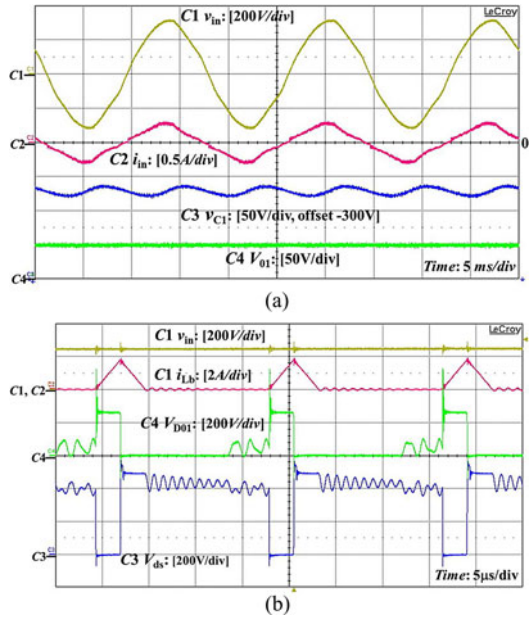

Fig. 15. Measured waveforms under input voltage of 220 V. (a) Measured input voltage $v_{\rm in}$, input current $i_{\rm in}$, bus voltage V_{C1}, and output voltage V_{01} waveform. (b) Inductor current $i_{\rm Lb}$, voltage of the switch $V_{\rm ds}$, and output diode V_{D01} at input ac peak voltage.

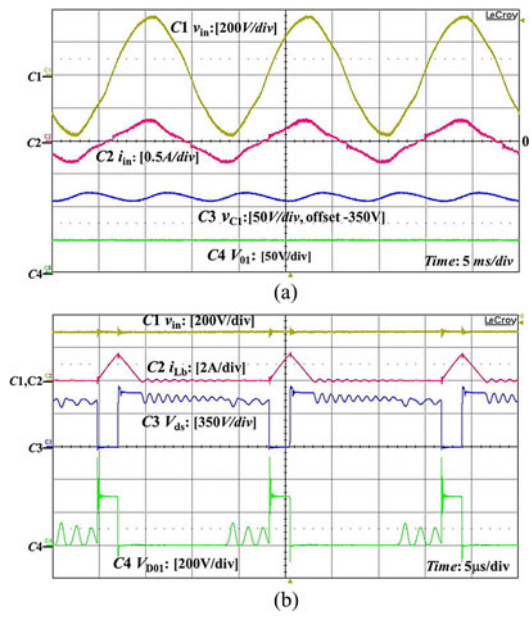

Fig. 16. Measured waveforms under input voltage of 265 V. (a) Measured input voltage $v_{\rm in}$, input current $i_{\rm in}$, bus voltage V_{C1}, and output voltage V_{01} waveform. (b) Inductor current $i_{\rm Lb}$, voltage of the switch $V_{\rm ds}$, and output diode V_{D01} at input ac peak voltage.

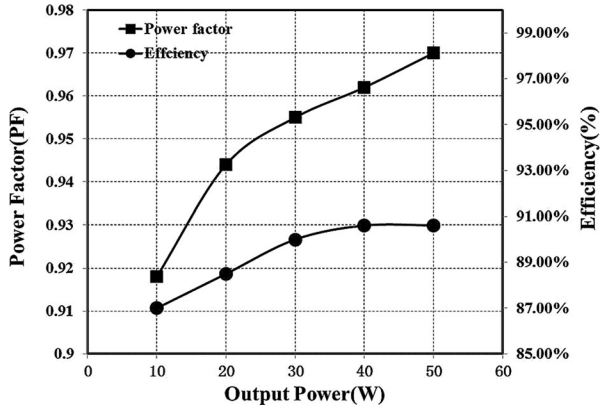

Fig. 17. Measured PF and efficiency against output power at the 110-V input condition.

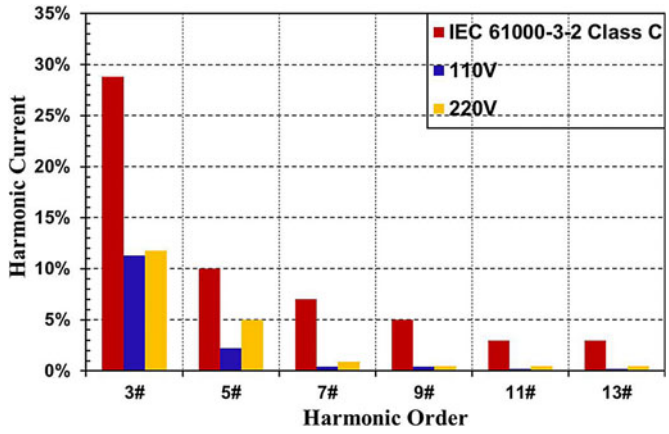

Fig. 18. Measured input current harmonics.

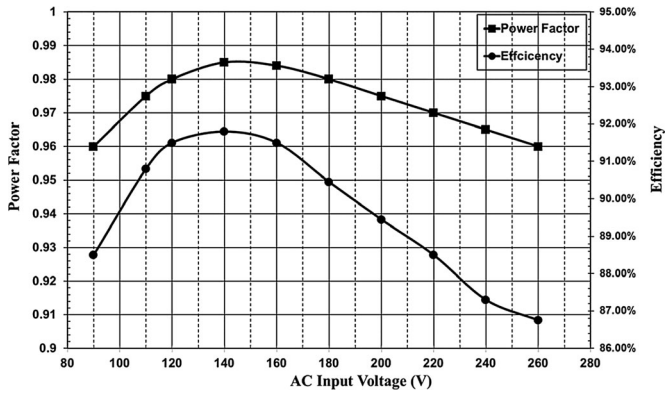

Fig. 19. Measured efficiency and power factor variations under different input-voltage conditions.

which is the difference of the twin-bus voltages V_{01} and V_{02}. Such a low voltage stress allows LED driver stage to operate under the ultrahigh frequency condition.

Fig. 22(a) shows device voltages and LED current waveforms under dimming operation. $V_{\rm DS\_QDIM}$ is the voltage across the dimming switch $Q_{\rm DIM}$. The dimming control frequency is 400 Hz in this case. Fig. 22(b) and (c) shows the detailed LED current falling and rising edges during the dimming operation. The transition response time in both the cases is within 2 μs.

For the individual stage efficiency, the current regulator employing the twin-bus buck converter has a peak efficiency of 98.5% and maintains above 98% for the output power range from 10 to 50 W. The overall system efficiency including the current regulator stage and the PFC stage without an electrolytic capacitor exceeds 90% under the input voltage of 110 V.

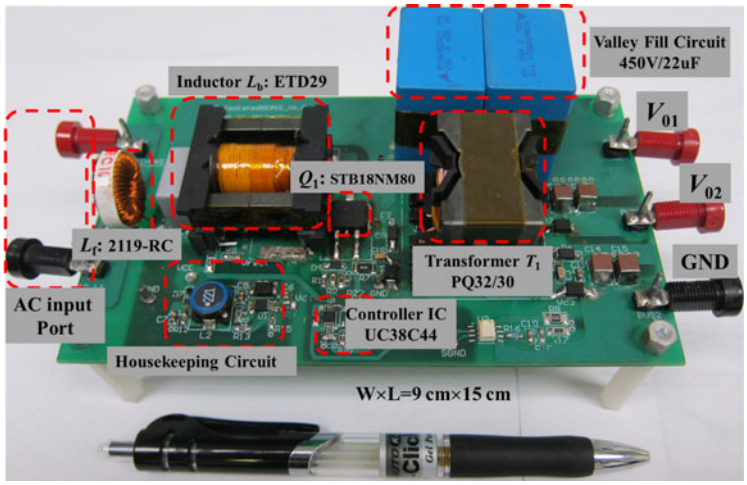

Fig. 20. Photograph of the experimental prototype.

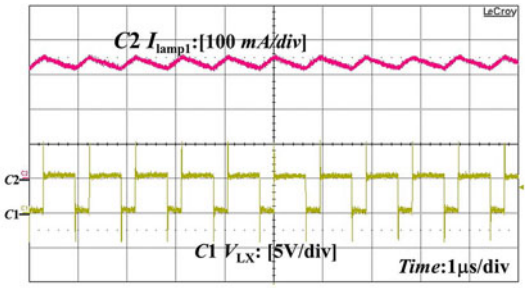

Fig. 21. Measured LED lamp current and the device voltage stress.

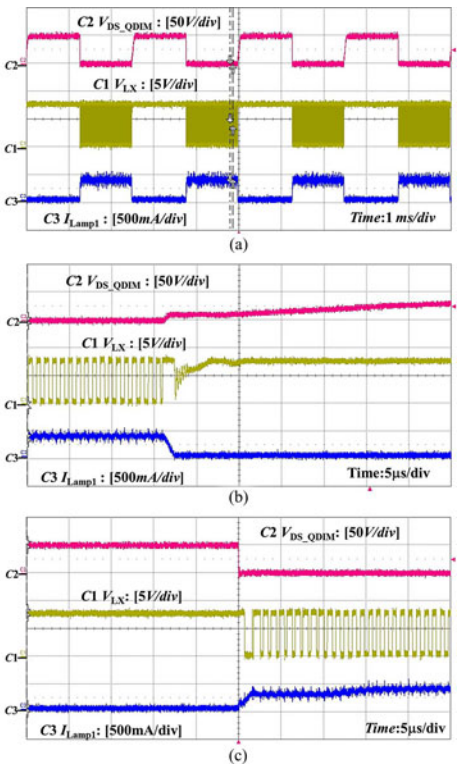

Fig. 22. Experimental device voltages and LED current waveforms under dimming operation. (a) Waveforms under dimming cycles. (b) During the falling interval. (c) During the rising interval.

VI. Conclusion

A novel PFC topology is proposed by inserting the valley-fill circuit into the DCM SEPIC-derived converter. The isolated version of the proposed circuit allows multiple voltage outputs and, thus, is adopted to couple with the twin-bus buck converter for LED lighting applications. The overall circuit design allows elimination of the bulk electrolytic capacitor, while maintaining desired high power factors and low harmonic contents to meet the standards requirements. The key circuit and design features are summarized as follows.

1) Significantly reduce the voltage stress of the output diode and all the energy-storage capacitors in the DCM SEPIC-derived converter with the use of valley-fill circuit, which serves as a voltage divider. Meanwhile, the capacitance of the capacitors in the valley-fill SEPIC-derived PFC circuit only needs to be half of capacitance of the DCM SEPIC-derived PFC to achieve the same power factor and output voltage ripple under the electrolytic capacitor-less condition.
2) DCM operation makes the valley-fill capacitors work as the power decoupling capacitor, thus minimizing the need for the low-frequency decoupling capacitance to allow the elimination of the electrolytic capacitor.
3) Snubber circuit serves as MOSFET voltage spike clamping, as well as the auxiliary power supply. The energy stored in snubber capacitor is recycled for the housekeeping circuit.

The presented topology solves the bus capacitor voltage dependent on the output load issue and avoids high voltage stress in light load. The complete circuit including the valley-fill SEPIC-derived PFC stage and the twin-bus converter LED lighting driver stage has been tested for the universal line operation to demonstrate the claimed features. This paper has described the basic circuit operating principle, device selection, and passive component design procedure to achieve the desired power decoupling and low harmonic contents. Further work is needed to improve the efficiency and to apply to different power levels.

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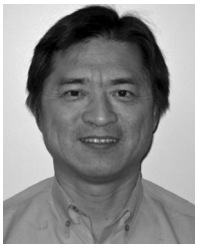

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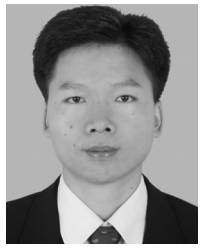

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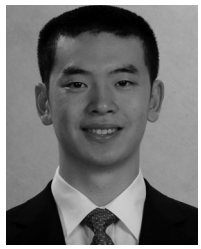

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