# A Novel ZVZCS Full-Bridge DC/DC Converter Used for Electric Vehicles

Majid Pahlevaninezhad, *Student Member, IEEE*, Pritam Das, *Member, IEEE*, Josef Drobnik, *Senior Member, IEEE*, Praveen K. Jain, *Fellow, IEEE*, and Alireza Bakhshai, *Senior Member, IEEE*

***Abstract*—This paper presents a novel ZVZCS full-bridge DC/DC converter, which is able to process and deliver power efficiently over very wide load variations. The proposed DC/DC converter is part of a plug-in AC/DC converter used to charge the traction battery (high voltage battery) in an electric vehicle. The key challenge in this application is operation of the full-bridge converter from absolutely no-load to full-load conditions. In order to confirm reliable operation of the full-bridge converter under such wide load variations, the converter should not only operate with soft-switching from full load to no-load condition with satisfactory efficiency for the full range of operation, but also the voltage across the output diode bridge needs to be clamped to avoid any adverse voltage overshoots arising during turn-OFF of the output diodes as commonly found in regular full bridge converters. In order to achieve such stringent requirements and high reliability, the converter employs a symmetric passive near lossless auxiliary circuit to provide the reactive current for the full-bridge semiconductor switches, which guarantees zero voltage switching at turn-ON times for all load conditions. Moreover the proposed topology is based on a current driven rectifier in order to clamp the voltage of the output diode bridge and also satisfy ZVZCS operation of the converter resulting in superior efficiency for all load conditions. In this paper operation of the converter is presented in detail followed by analytical design procedure. Experimental results provided from a 3KW prototype validate the feasibility and superior performance of the proposed converter.**

***Index Terms*—DC/DC converter, full-bridge converter, lagging leg, leading leg, shoot-through, snubber capacitor, Zero Current Switching (ZCS), Zero Voltage Switching (ZVS), Zero Voltage Zero Current Switching (ZVZCS) .**

## NOMENCLATURE

| | |
|---|---|
| $t_d$ | Dead-time between MOSFET gate signals (s). |
| $L_{AUX1}$ | Leading leg auxiliary inductance (H). |
| $L_{AUX2}$ | Lagging leg auxiliary inductance (H). |
| $C_{s1}$ | Leading leg snubber capacitance (F). |
| $C_{s2}$ | Lagging leg snubber capacitance (F). |
| $C_{so}$ | Switch output capacitance (F). |
| $k$ | Transformer turns ratio (Np/Ns). |
| $L_{leak}$ | Leakage inductance (H). |
| $L_M$ | Magnetizing inductance (H). |
| $L_s$ | Series inductance (H). |
| $L_{seq}$ | Equivalent series inductance (H). |
| $C_f$ | Output filter capacitance (F). |
| $f_s$ | Switching frequency ($H_Z$). |
| $T_s$ | Switching period (s). |
| $I_p$ | Peak current of transformer primary-side (A). |
| $I_{BAT}$ | Battery current (A). |
| $V_{dc}$ | Input DC voltage (V). |
| $V_{BAT}$ | Battery voltage (V). |
| $v_{\rm sec}$ | Secondary voltage of the transformer (V). |
| $g_v$ | Voltage gain of converter. |
| $I_{AUXA}$ | Current of leading leg auxiliary circuit (A). |
| $I_{AUXB}$ | Current of lagging leg auxiliary circuit (A). |
| $I_{PA}$ | Peak current value of leading leg auxiliary circuit (A). |
| $I_{PB}$ | Peak current value of lagging leg auxiliary circuit (A). |
| $I_P$ | Peak value of the series inductance current (A). |
| $I$ | Average value of the series inductance current (A). |
| $E_{AUX}$ | Energy in the auxiliary circuit (J). |
| $E_{Cso}$ | Energy in output capacitors of MOSFETs (J). |
| $i_{DB}$ | Diode bridge current (A). |
| $\omega_s$ | Switching frequency (rad/s). |
| $P_{o,\max}$ | Maximum output power. (W) |
| $I_o$ | DC output current (A). |
| $V_o$ | DC output voltage (V). |
| $V_d$ | Output diode forward voltage drop (V). |
| $\psi$ | Phase-shift between leading leg and lagging leg pulses. |
| $R_e$ | Converter effective load resistance (Ω). |
| $ESR$ | Equivalent series resistance (Ω). |

Manuscript received August 19, 2011; revised October 21, 2011; accepted November 21, 2011. Date of current version March 16, 2012. This work was supported by Freescale Semiconductor, Inc., Austin, TX. Recommended for publication by Associate Editor A. Emadi.

M. Pahlevaninezhad, P. Jain, and A. Bakhshai are with the ePOWER, Electrical and Computer Engineering, Queens University, Kingston, ON K7L 3N6, Canada (e-mail: 7mp@queensu.ca; praveen.jain@queensu.ca; alireza.bakhshai@queensu.ca).

P. Das is with the ePOWER, Electrical and Computer Engineering, Murata Power Solutions, Toronto, ON, Canada (e-mail: pritam.das@queensu.ca).

J. Drobnik is with Freescale Semiconductor Inc. Tempe, Arizona, AZ 85284 USA (e-mail: B15009@freescale.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2011.2178103

## I. INTRODUCTION

POWER conversion systems in electric vehicles (EVs) usually use a high energy battery pack to store energy for the electric traction system [1]. This high energy battery pack is typically charged from the utility AC mains [2]. Energy conversion during the battery charging is performed by an AC/DC converter. Such AC/DC converters, which are used to charge the high-energy battery, usually consist of two stages: input power factor correction (PFC) for AC/DC conversion and DC/DC conversion for battery charging [3]. PFC is used to improve the quality of the input current, which is drawn from the utility, and the

charger which is an isolated DC/DC converter, is used to charge the high voltage battery and provide galvanic isolation between the utility mains and the traction battery [31], [32], [35], [36].

Full-bridge topology is the most popular topology used in the power range of a few kilowatts (1–5 KW) for DC/DC converters. Since the switch ratings are optimized for the full-bridge topology, this topology is extensively used in industrial applications. High efficiency, high power density, and high reliability are the prominent features of this topology [38]–[40].

For applications in the range of a few kilowatts, MOSFETs are mostly used to implement the full-bridge converters. In order to have robust and reliable operation, MOSFETs should be switched under zero voltage. Operation with zero voltage switching (ZVS) has numerous advantages including, for example, reduction of the converter switching losses and a noise-free environment for the control circuit. Zero voltage switching is usually achieved by providing an inductive current flowing out of the full-bridge legs during the switch turn-ON and by placing a snubber capacitor across each switch during the switch turn-OFF. The inductive current can be produced by inserting an inductor in series with the power transformer or by inserting an inductor in parallel with the power transformer [4]–[11]. In a practical full-bridge configuration, the internal drain-to-source capacitor of the MOSFET is usually utilized as the snubber capacitor, the series inductor is usually the leakage inductance of the power transformer, and the parallel inductor is implemented by using the magnetizing inductance of the power transformer. Thus, external passive components are not required, which makes the power circuit very simple and efficient. However, the full-bridge converter with the series inductor loses its ZVS capability at light loads, and the converter with the parallel inductor loses its ZVS under heavy loads. Loss of ZVS implies extremely high switching losses at high switching frequencies and very high EMI due to the high di/dt of the snubber discharge current. Loss of ZVS can also cause a very noisy control circuit, which leads to shoot-through and loss of the semiconductor switches. The ZVS range can be extended by increasing the series inductance. However, having a large series inductance limits the power transfer capability of the converter and reduces the effective duty ratio of the converter.

In battery charger applications, ZVS is vitally important since the converter might be operating at absolutely no-load for a long period of time. In this application, when the battery is charged, the load is absolutely zero and the converter should be able to safely operate under the zero load condition. Since ZVS in conventional full-bridge PWM converters is achieved by utilizing the energy stored in the leakage inductance to discharge the output capacitance of the MOSFETs, the range of the ZVS operation is highly dependent on the load and the transformer leakage inductance. Thus, this converter is not able to ensure ZVS operation for a wide range of load variations [12].

In [11], a novel approach has been adopted to extend the ZVS range in the full-bridge converter. In this approach, an auxiliary inductor is put at the leading leg by deriving an auxiliary winding on the main transformer and confirms ZVS for the leading leg. Although the proposed scheme can effectively extend ZVS of the leading leg MOSFETs, it is not able to guarantee ZVS for the lagging leg of the converter. Thus, when the battery is fully charged, the lagging leg switches may not be switched under ZVS. Moreover, the voltage at the secondary side still suffers from the spikes due to the leakage inductance and voltage-fed rectifier, commonly seen in full-bridge converters.

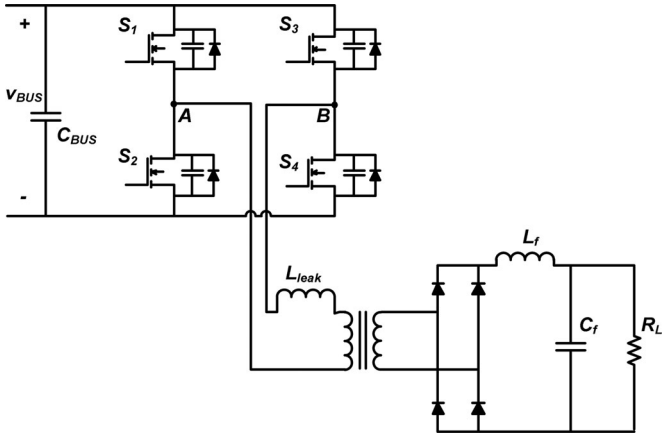


Fig. 1. Conventional full-bridge converter.

A fundamental problem related to the conventional full-bridge phase-shift DC/DC converter is the voltage spikes across the output diodes. Fig. 1 shows the schematic of the conventional full-bridge converter. Basically, the leakage inductance of the transformer causes the voltage spikes across the output diodes. Theses spikes are intensified by increasing the switching frequency of the converter. Thus, the diodes should be designed overrated to be able to withstand the voltage spikes, which leads to higher losses due to the higher forward voltage drop of the diodes and poorer reverse recovery characteristics. In addition, the spikes significantly increase the EMI noise of the converter. This fact makes the topology not very practical for high frequency, high voltage applications. There are quite a few references that proposed solutions for the voltage spikes across the output diodes. Some references tried to decrease the leakage inductance as much as possible though the transformer winding structures, which effectively decreases the peak of the voltage spikes across the output diodes. However, reducing the leakage inductance decreases the ZVS operating range of the full-bridge converter, which results in a very narrow range of ZVS operation. In [13], an R-C-D snubber circuit is used to mitigate the voltage spikes across the diodes. The main problem with the snubber circuit is the amount of losses in the snubber resistor, which considerably degrades the efficiency of the converter especially at higher power and it can only reduce the peak value of the voltage spikes. In [14], an active clamp circuit has been added to the converter to clamp the voltage across the output diodes. This method can effectively clamp the voltage spikes of the output diodes. However, the active clamp circuit increases the complexity of the converter and causes small losses in the clamp circuit. Several energy recovery clamp circuits (ERCCs) have been proposed in [15]–[20]. In [21], an improved ERCC method has been proposed to accommodate the effects of voltage spikes for a wide range of input voltage. Although the ERCC techniques are able to reduce the voltage stress of the output

diodes, the amount of the voltage stress depends on the duty ratio and input voltage of the converter in most of the ERCCs techniques. In addition, using extra semiconductors is inevitable in all these aforementioned methods.

The problem of voltage spikes is essentially related to the voltage-driven output rectifiers. This is due to the fact that the full-bridge inverter produces high frequency voltage pulses across the output diode rectifier, which is connected to the output inductor as shown in Fig. 1. The voltage-driven rectifier works perfectly if there is no leakage inductance in between the output of the full-bridge inverter and the diode rectifier. However, the existence of the leakage inductance makes the rectifier connect two current sources, i.e., leakage inductance and output inductance, together. This connection creates high voltage spikes across the output diodes. In this paper, a new topology is proposed based on a current driven rectifier, which effectively rectifies the voltage stress problems related to the full-bridge DC/DC converter. The proposed topology provides zero current switching (ZCS) for the output rectifiers, which eliminates reverse recovery losses of the output diode rectifiers.

In [37], a new modified current-fed full-bridge is presented in order to reduce the voltage stress arising in the conventional current-fed full-bridge converter. In the current-fed full-bridge in [37], the inductor stores energy as the transformer transmits energy from the DC source to the load. This scheme is able to effectively reduce the voltage spikes at the input-side (full-bridge MOSFETs) of the converter. In addition, the input inductor is replaced by coupled inductors in series with two MOSFETs to reduce the size of the inductor. The fundamental difference between the proposed converter and the converter in [37] is that in the proposed converter, the full-bridge section at the transformer is the conventional voltage-fed topology, while in [37] the input section of the converter is a modified current-fed topology.

In the battery charger applications, the converter should be able to operate from absolutely no-load to full-load condition. In order to achieve zero voltage switching for the whole load range, the proposed converter uses a passive circuit to provide the required inductive current for the power MOSFETs. In [22], the detailed analysis of the auxiliary circuit is given.

This paper is organized as follows: In Section II, the proposed topology is introduced and different operating modes are described. The steady-state operation of the converter is analyzed in Section III. In Section IV, features of the proposed topology are presented. Design procedure for key components of the converter is given in Section V. Section VI shows the experimental results obtained from the converter prototype and finally, Section VII, provides the conclusion.

## II. Proposed Topology

The main problem regarding the conventional full-bridge converter is the series connection of the leakage inductor and output inductor through the diode rectifier. In other words, the diode rectifier at the secondary side of the converter connects two current sources together. This leads to large voltage spikes across the diode rectifier and very lossy commutation of the current in the rectifier diodes. This phenomenon is intensified in high voltage applications due to the inevitable large leakage inductance. This fact forces designers to over design the diode rectifier at the output side. For instance, designers usually use even 1200 V diodes for a 400 V output DC power supply. This phenomenon is usually mitigated by using snubber circuits or clamp circuits. However, the snubber circuits are usually lossy especially for high frequency applications. In addition, the voltage spikes are highly intensified by increasing the load, which makes the snubber circuit a very poor solution for high frequency applications. Basically, this problem exists with all topologies that use transformers with voltage-driven rectifiers. Generally, in converters with voltage-driven rectifiers, there is an inductor at the output of the rectifier and the leakage inductance of the transformer interferes with this inductor.

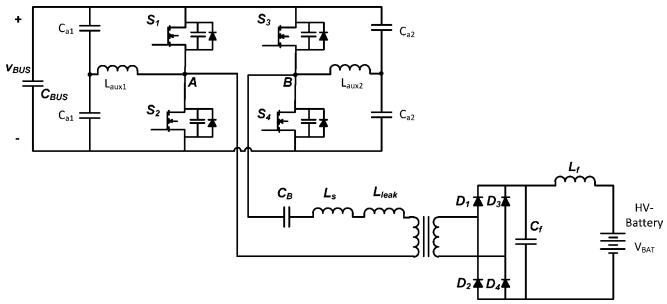


Fig. 2. Proposed converter.

Moreover, in full-bridge DC/DC converters with high output voltages (such as 400 V or higher), the equivalent capacitance viewed from the transformer primary side is not negligible. This is due to the high number of turns at the secondary and to the required high voltage semiconductors with high value of output capacitance. In high frequency applications, these parasitic capacitances resonate with the leakage inductance of the transformer, which leads to a very high resonant current in the primary of the transformer. Therefore, this capacitor completely deteriorates the performance of the converter in high switching frequency applications. The conventional full-bridge topology exhibits very poor performance due to the secondary side components in high frequency high voltage applications.

The topology introduced in this paper presents a novel yet simple solution to this problem. The proposed topology is essentially a ZVZCS type full-bridge converter with a current-driven rectifier. Fig. 2 shows the power circuit of the proposed topology. In this topology, the full-bridge inverter converts the DC-bus voltage to a high frequency quasi-square wave voltage. Then there is an inductor in series with the transformer, which acts as a current source for a current driven rectifier. The current driven rectifier rectifies the output current of the transformer and transfers power to the output. Fig. 3 illustrates the key waveforms of the converter. In one switching cycle, the circuit has 14 modes during steady-state operation. Due to the symmetrical structure, the analysis is only given for half a switching cycle. In half cycle, the steady state behavior of the circuit is divided into the following operating modes:

*Mode I: ($t_0 \leq t \leq t_1$):* At $t_0$, $S_2$ is turned OFF. The output capacitor of $S_1$ is discharging and that of $S_2$ is charging up with the reactive current provided by the auxiliary circuit.

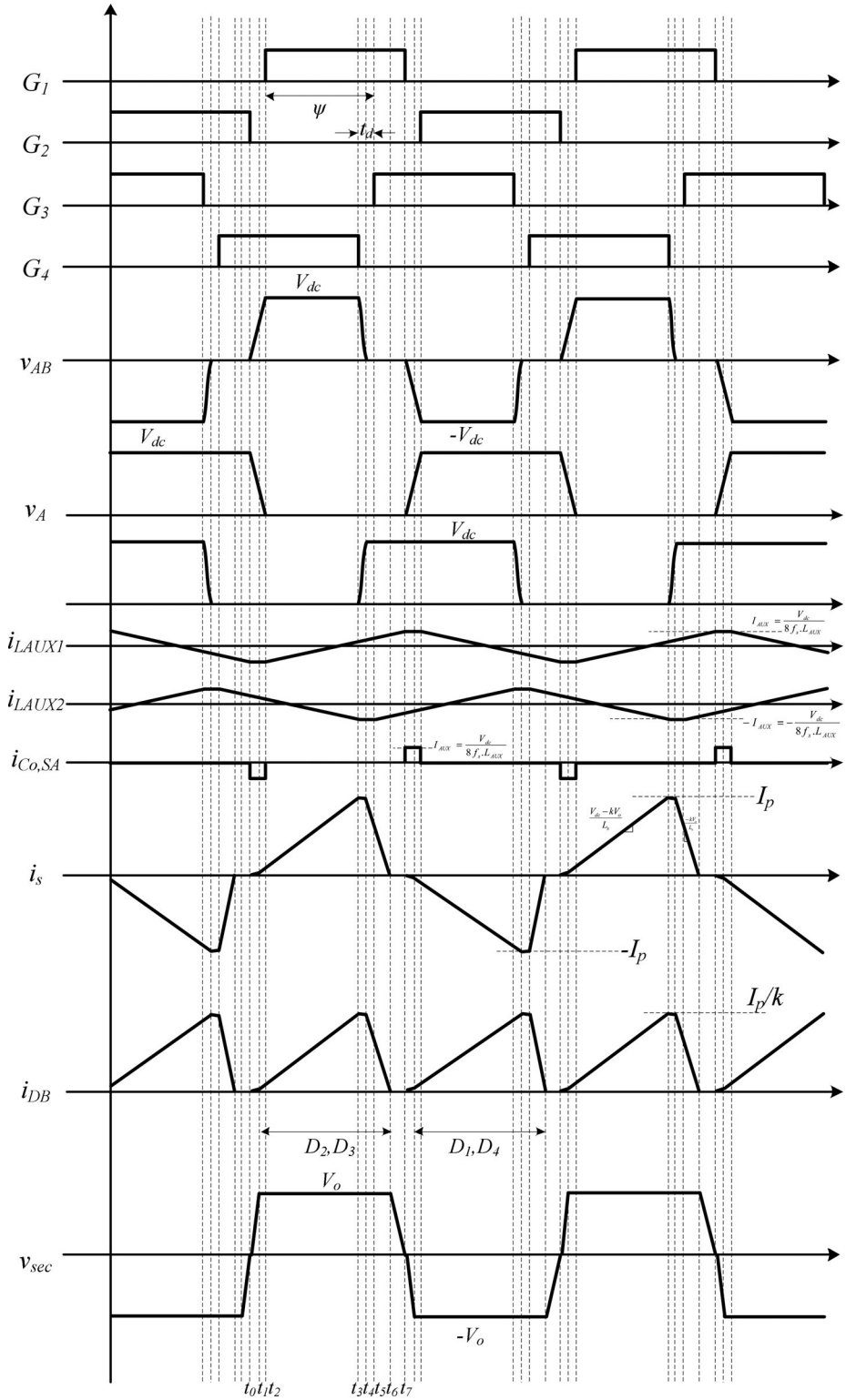


Fig. 3. Ideal waveforms of the converter.

During this interval, the secondary-side diodes are reversed biased and are OFF. Therefore, the rising voltage $v_{AB}$ conducts a very small current through the DC blocking capacitor $C_b$, series inductance $L_s$, leakage inductance $L_{leak}$, and magnetizing inductance $L_M$. Fig. 4(a) shows the active components in this mode of operation. The current through the series inductance $L_s$, is given by

$$i_s(t) = \frac{1}{L_s + L_{leak} + L_M} \int_{t_0}^{t} v_{AB}\, dt. \tag{1}$$

Due to the fact that $L_M$ is large, the amount of current flowing through the primary side of the transformer is much smaller than

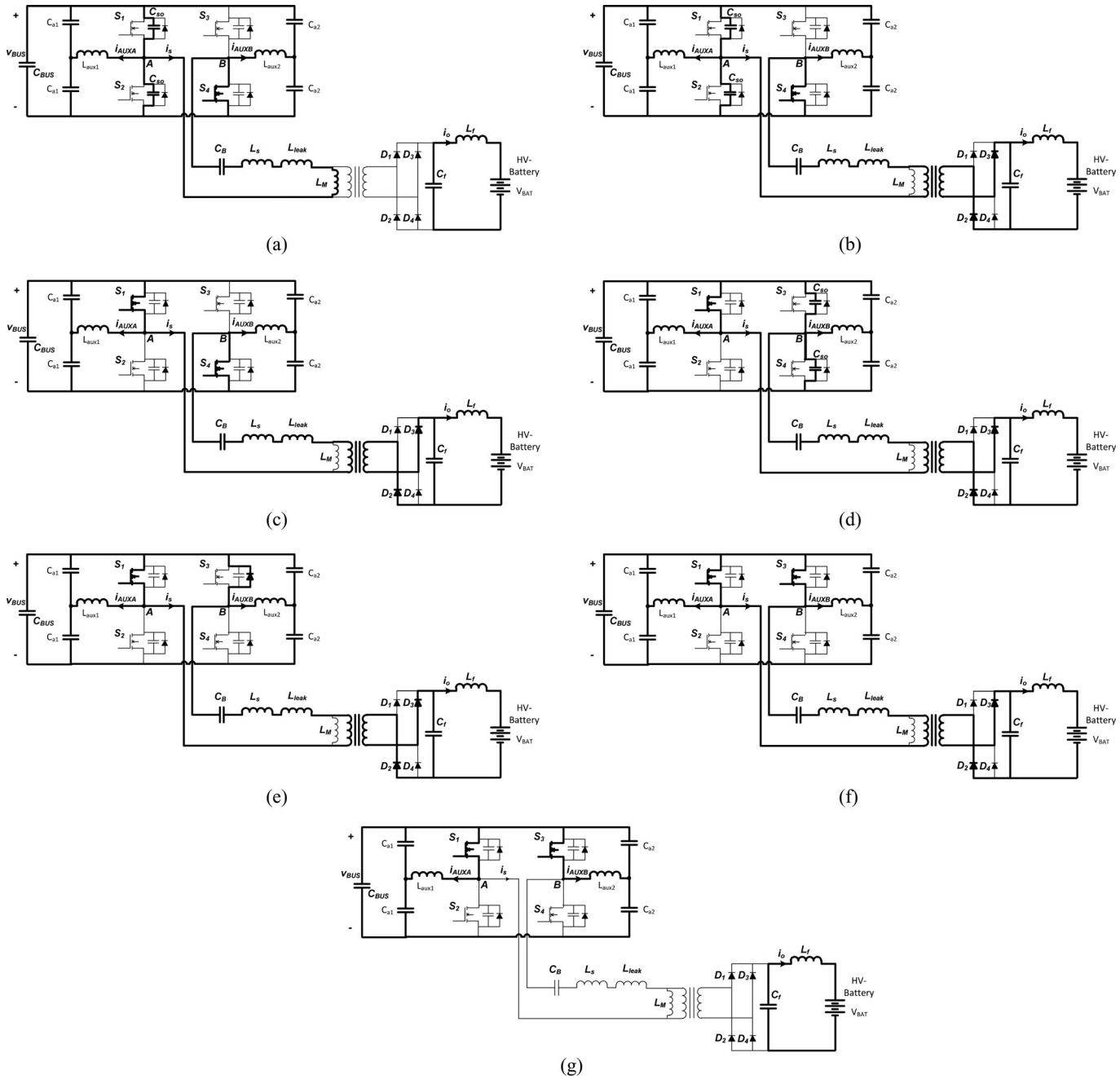


Fig. 4 (a) Active components of Mode I. (b) Active components of Mode II. (c) Active components of Mode III. (d). Active components of Mode IV. (e) Active components of Mode V. (f) Active components of Mode VI. (g) Active components of Mode VII.

the current through the auxiliary circuit $i_{AUXA}$. According to this assumption $v_{AB}$ is calculated as

$$v_{AB}(t) = V_{dc} - v_{Cso}(t) \tag{2}$$

$$v_{Cso}(t) = V_{dc} - \frac{I_{PA}}{2C_{so}}(t - t_0). \tag{3}$$

By using (1)–(3), the equation of the series current is calculated as

$$i_s(t) = \frac{I_{PA}}{4(L_s + L_M + L_{leak}).C_{so}}(t - t_0)^2. \tag{4}$$

This interval ends once the voltage across the secondary reaches the output voltage plus the voltage drops of the diodes to forward bias the output diodes. Thus, $t_1$ is given by

$$t_1 = t_0 + \frac{2k(V_o + 2V_d).(L_s + L_M + L_{leak}).C_{so}}{L_M.I_{PA}}. \tag{5}$$

*Mode II ($t_1 \le t \le t_2$):* This mode starts once the output diodes get forward biased. Fig. 4(b) shows the active components in this mode. According to this figure, the output capacitor of the MOSFET, $S_1$ is still discharging to finally reach zero and that of $S_2$ is charging up to $V_{dc}$. This mode ends once the voltage across this capacitor becomes zero. In this interval, the series

current $i_s$, is calculated as

$$i_s(t) = \frac{1}{L_s + L_{leak}} \int_{t_0}^{t} (v_{AB} - k(V_o + 2V_d))\, dt \quad (6)$$

$v_{AB}$ is given by

$$v_{AB}(t) = \frac{I_{PA}}{2C_{so}}(t - t_1). \quad (7)$$

Placing (7) into (6), $i_s$ is given by

$$i_s(t) = \frac{I_{PA}}{4(L_s + L_{leak}).C_{so}}(t - t_1)^2 - \frac{k(V_o + 2V_d)}{L_s + L_{leak}}(t - t_1). \quad (8)$$

This interval ends once the output capacitor of the MOSFET $S_1$, has discharged completely. Therefore, $t_2$ is calculated using (3) as follows:

$$t_2 = t_0 + \frac{2V_{dc}.C_{so}}{I_{PA}}. \quad (9)$$

*Mode III ($t_2 \le t \le t_3$):* This mode starts once the MOSFET output capacitors have been charged and discharged completely. Fig. 4(c) shows the active components in this mode. During this mode, the output diodes clamp the secondary voltage to the output voltage. Thus, there is a constant voltage across the combination of the series inductance and the leakage inductance. Therefore, the series current ramps up to its peak value. According to Fig. 4(b), the series current $i_s$, is given by

$$i_s(t) = \frac{V_{dc} - k(V_o + 2V_d)}{L_s + L_{leak}}(t - t_2). \quad (10)$$

The peak value $I_p$ of the series current $i_s$ is determined by using (4), (5), (8)–(10), and the amount of phase-shift between the leading leg and the lagging leg of the full-bridge inverter

$$\begin{aligned} I_p = {} & \frac{2k^2.(V_o + 2V_d)^2.(L_s + L_{leak} + L_M).C_{so}}{L_M^2.I_{PA}} \\ & + \frac{I_{PA}}{(L_s + L_{leak}).C_{so}} \\ & \times \left( \frac{V_{dc}.C_{so}}{I_{PA}} - \frac{k(V_o + 2V_d).(L_s + L_{leak} + L_M).C_{so}}{L_M.I_{PA}} \right)^2 \\ & - \frac{2k(V_o + 2V_d)}{L_s + L_{leak}} \\ & \times \left( \frac{V_{dc}.C_{so}}{I_{PA}} - \frac{k(V_o + 2V_d).(L_s + L_{leak} + L_M).C_{so}}{L_M.I_{PA}} \right) \\ & + \frac{V_{dc} - k(V_o + 2V_d)}{L_s + L_{leak}} \left( \frac{\psi}{\omega_s} - t_d \right). \end{aligned} \quad (11)$$

This mode ends once the MOSFET $S_4$, gate voltage becomes zero. The end of this interval $t_3$, is given by

$$t_3 = t_2 + \frac{\psi}{\omega_s} - t_d. \quad (12)$$

*Mode IV ($t_3 \le t \le t_4$):* Fig. 4(d) illustrates the active circuit during this mode. During this interval the output capacitor of $S_3$ is discharging from and that of $S_4$ is charging up to $V_{dc}$. In this interval, the output voltage of the inverter $v_{AB}$, is given by

$$\begin{aligned} v_{AB}(t) = {} & V_{dc} - V_{dc}\mathrm{Sin}\left( \frac{t}{\sqrt{2C_{so}.(L_s + L_{leak})}} - t_3 \right) \\ & - \frac{I_{PB}}{2C_{so}}(t - t_3). \end{aligned} \quad (13)$$

The series current is calculated using (13) as follows:

$$\begin{aligned} i_s(t) = {} & \frac{1}{L_s + L_{leak}} \left[ V_{dc}(t - t_3) + \frac{V_{dc}}{\sqrt{2C_{so}.(L_s + L_{leak})}} \right. \\ & \left. \mathrm{Cos}\left( \frac{t}{\sqrt{2C_{so}.(L_s + L_{leak})}} - t_3 \right) - \frac{I_{PB}}{4C_{so}}(t - t_3)^2 \right] \\ & - \frac{k(V_o + 2V_d)}{L_s + L_{leak}}(t - t_3) + I_p. \end{aligned} \quad (14)$$

This mode ends once the $S_3$ output capacitor got completely discharged and $S_4$ output capacitor got charged to $V_{dc}$. The end of this mode $t_4$ is determined by solving (13) for $v_{AB}(t_4) = 0$.

*Mode V ($t_4 \le t \le t_5$):* Fig. 4(e) shows the active components during this mode of operation. Once this voltage $v_{AB}$, becomes zero this mode commences. During this mode, the output voltage of the inverter is zero and the output diodes clamp the secondary voltage to the output voltage. Thus, a net negative voltage is incident across the series inductor, which is the reflected output voltage at the transformer primary side. This causes the current $i_s$ to ramp down. According to Fig. 4(e), the series current is given by

$$i_s(t) = i_s(t_4) - \frac{k(V_o + 2V_d)}{L_s + L_{leak}}(t - t_4). \quad (15)$$

This interval is part of the dead time between the gating pulses of $S_3$ and $S_4$. Therefore, in this mode the body diode of $S_3$ is conducting. Once the gate pulse of $S_3$ is applied this mode finishes and the current flows through the MOSFET channel.

*Mode VI ($t_5 \le t \le t_6$):* This mode starts when the gate pulse is applied to $S_3$. The active components in this mode are shown in Fig. 4(f). The equivalent circuit is the same as the previous mode except $S_3$ channel is conducting in this mode rather than the body diode of $S_3$. Therefore, the series inductor current is still ramping down to reach zero at the end of this mode. It should be noted that $S_1$ turns off under near zero current switching at the end of this mode. At the end of this mode, the current through the series inductor reaches zero, so that the output diodes $D_2$ and $D_3$ naturally turn off with zero current.

*Mode VII ($t_6 \le t \le t_7$):* Fig. 4(g) shows the active components during this mode of operation. This interval starts once the current through output diodes reaches zero and the diodes naturally turn off with zero current. During this mode, the output capacitor $C_f$ feeds the output load with its stored energy while on the transformer primary side there is no current.

The modes of operation of the converter are slightly different for light loads. In particular, Mode IV is subdivided into two modes for light load conditions due to the small value of peak current $I_p$, in the series inductor. There are basically two sources of current to charge and discharge the MOSFET output

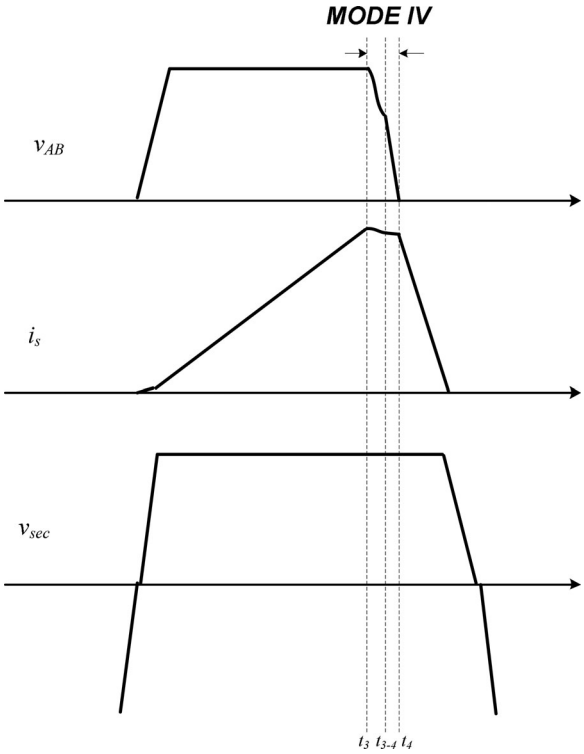


Fig. 5. Submodes of Mode IV.

capacitors. The first is the auxiliary circuit current and the second is the current flowing in the series inductance. In light loads, the latter is not enough to charge and discharge the MOSFET output capacitors. Therefore, the lagging edge of the inverter output voltage has two different slopes at light loads. The first slope is determined by the auxiliary circuit current and $I_p$ while the second slope is determined by the auxiliary circuit current. That is why there are two different modes of operation during Mode IV. Fig. 5 shows the submodes of Mode IV at light loads.

## III. Analysis of Steady-State Operation

In this section, the steady-state operation of the converter is analyzed. The following assumptions are considered for the derivations:

1) The converter losses are neglected, which implies that the input power of the converter equals to the output power.
2) The energy transferred from primary to the secondary side of the transformer during Mode I and Mode II of the operation, which extends from time $t_0$ to $t_2$, is neglected since the series inductance current is negligible during these intervals.
3) The change in the waveform of the series inductor current during Mode IV of operation is neglected since the duration of Mode IV is very small compared to the switching cycle.
4) All passive components are considered to be ideal, which implies the ESRs of inductors and capacitors are neglected.

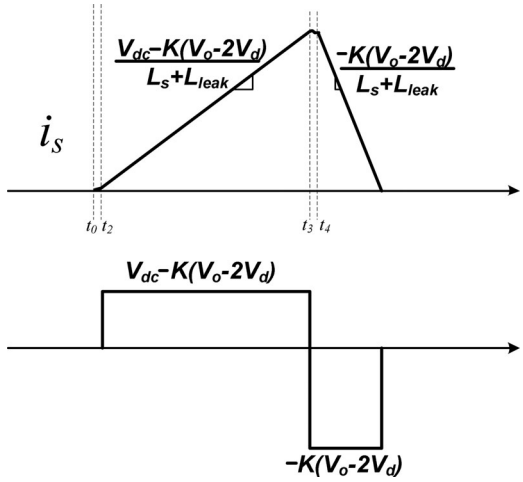


Fig. 6. Series inductor current and voltage waveforms for half a switching cycle.

5) The magnetizing inductance of the transformer is large enough to have a negligible magnetizing current.
6) The voltage ripple across the output filter capacitor is very small considering the application of battery charging.

Fig. 6 illustrates the series inductance current and voltage waveforms. In order to calculate the conversion ratio of the converter, the average value of the series inductance current should be determined. According to Fig. 6 and the aforementioned assumptions, the average value of the series inductance current is given by

$$I = \frac{2}{T_s}\left(\frac{\psi}{\omega_s} - t_d\right)^2 \cdot \left(\frac{V_{dc}}{kV_o}\right) \cdot \left(\frac{V_{dc} - kV_o}{L_s + L_{leak}}\right). \tag{16}$$

In order to find the conversion gain, the power balance equation is used. The power balance is given by

$$k.I.V_o = V_{BAT}.I_{BAT}. \tag{17}$$

By using (16) and (17) the gain of the converter is given by

$$g_v = \frac{V_o}{V_{dc}} = \frac{2}{k + \sqrt{k^2 + \left(\frac{4(L_s + L_{leak})}{T_s.R_e.\left(\frac{\psi}{\omega_s} - t_d\right)^2}\right)}} \tag{18}$$

where $R_e$ is the effective load of the converter and is given by

$$R_e = \frac{V_{BAT}}{I_{BAT}}. \tag{19}$$

Fig. 7 shows the converter gain with respect to the phase-shift angle of the full-bridge inverter for different load conditions. According to this figure, the variations of the gain are more pronounced for light loads in smaller values of phase-shift angle, while the gain varies more consistently for heavier loads. This is due to the fact that the current in the series inductance has a very small peak for light loads; hence, the duration of Mode IV–VI is very short, whereas this duration is significant compared to the switching cycle at heavy loads.

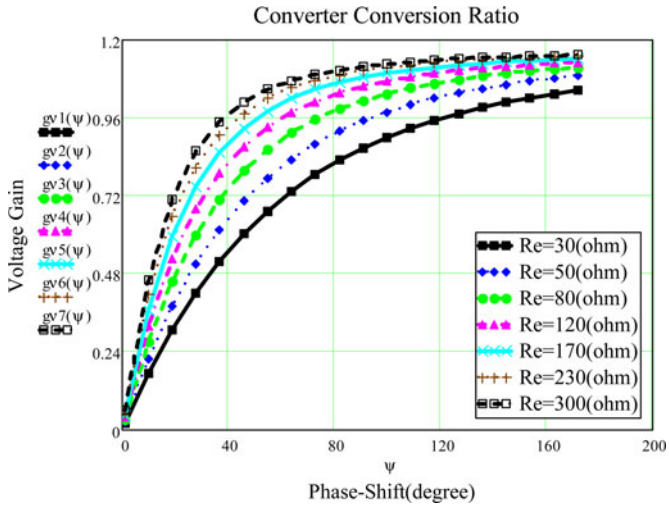


Fig. 7. Converter gain for different load conditions.

## IV. Features of the Proposed Topology

In this section, the salient features of the proposed converter are discussed as follows:

### *A. Zero Voltage Switching (ZVS) of the Full-Bridge Switches From Absolutely No-Load to Full-Load Condition*

In electric vehicle applications, the power converter should be able to operate at absolutely no-load condition for long periods of time. The conventional full-bridge converters lose ZVS at light loads. This limits the use of the conventional full-bridge converter in such applications. Two auxiliary circuits are placed to provide reactive current for ZVS turn–ON of the full-bridge switches independent of the load condition [22], [23]. Although, the auxiliary circuit increases the current of the MOSFETs, this current is essential to ensure reliable operation of the converter in the battery charging application, where the converter operates at no-load for a long period of time. Losing ZVS at no-load implies a significant amount of switching losses especially at high switching frequencies and very noisy control and gate drive circuit, which may cause shoot-through and failure of the power MOSFETs.

### *B. Same Amount of Reactive Current Requirement for Leading Leg and Lagging Leg ZVS Transition*

In [22], it is proven that the amount of reactive current required to guarantee ZVS for the leading leg is higher than the one for lagging leg due to the extra negative current in the transformer leakage inductor, which has to be compensated by the auxiliary circuit. This implies that the leading leg auxiliary inductor should carry much more current than the lagging leg. The extra current in the auxiliary inductor significantly increases the conduction losses in the leading leg switches as well as in the leading leg auxiliary inductor. In the proposed topology, due to the fact that the series inductor current starts from zero during the switching of the leading leg MOSFETs, the auxiliary circuit must only provide just enough reactive current to charge and discharge the leading leg MOSFET output capacitors. This can be concluded from Mode I of the converter operation. Therefore, both the auxiliary inductors only carry small amounts of current, just enough for the ZVS turn–ON of the MOSFETs. Therefore, the two auxiliary circuits are symmetric and, hence, easier to manufacture.

### *C. Near Zero Current Switching (ZCS) of the Leading Leg MOSFETs*

It is evident from Mode I and Mode VII that when the leading leg switches are turned on, the current in the series inductor is zero. The only current in the leading leg switches is the auxiliary circuit current during these modes. Considering the fact that the current in the auxiliary circuit is much smaller than the current in the series inductor it can be concluded that the MOSFETs of the leading leg undergo near ZCS turn-ON.

### *D. Elimination of Voltage Spikes Across the Output Diode and Inherent Voltage Clamping Across the Output Diode*

In the proposed topology, the voltage spikes across the output diodes are eliminated by using a current-driven configuration, which is realized by a series inductance with the main power transformer operating in discontinuous mode ensuring complete energy transfer and a capacitive filter at the output of the diode bridge. The series inductor acts as a current source and the capacitive filter clamps the voltage across the diode bridge.

### *E. Natural Lossless Commutation of Output Diodes*

Due to the current-driven nature of the output rectifier, the output diodes turn off naturally when the current in the series inductance reaches zero. This eliminates any reverse recovery and switching losses in the output diode bridge and guarantees a safe and reliable operation of the secondary side of the converter. Fig. 3 illustrates the lossless commutations of the output diodes.

### *F. Elimination of the Freewheeling Mode in Full-Bridge Inverter and the Output Diode Bridge*

In conventional full-bridge converters, when the output voltage of the inverter rises to $V_{dc}$, the current though the leakage inductance increases to reach the reflected output inductor current. Once it reaches the reflected output inductor current, the voltage at the transformer secondary side rises to $V_{dc}/k$. During this time the output diodes are freewheeling and the transformer secondary voltage is near zero. In this period, the output inductor current is flowing through the output diodes and the leakage inductance current is circulating in the primary side of the converter. The freewheeling operating mode significantly increases the losses of the converter especially for heavy loads. In the proposed topology, the freewheeling mode is completely eliminated due to the current-driven structure at the primary side and capacitive output filter at the secondary side.

### *G. Discontinuous Mode of Conduction of the Series Inductor*

The operation in DCM of the series inductor plays an important role in eliminating the voltage spikes across the diode

rectifier. This allows use of 600 V diodes to implement the output diode bridge. Elimination of the voltage spikes guarantees highly reliable operation of the converter for heavy loads. However, the DCM operation increases the rms and peak values of the series inductor current, which may deteriorate the efficiency at very heavy loads.

### H. Improved EMI

Another main advantage of the proposed method compared to the conventional phase-shift full-bridge controller is very low amount of EMI produced by the proposed converter. In conventional phase-shift full-bridge converter, the voltage spikes of the output diodes and the reverse recovery phenomenon during diode transitions are significant sources of EMI, which deteriorate the performance of the converter in high frequency range. Due to the fact that the converter for traction battery is connected to the utility mains to charge the traction battery, these high frequency voltage spikes are injected to the grid from the converter. Therefore, the converter requires a bulky EMI filter at the input side to suppress the effects of the high frequency voltage ringing present at the output side of the converter. The proposed converter operates without any high frequency spikes at the output diodes as well as the full-bridge DC-bus due to the current driven structure and auxiliary circuits in the primary side.

## V. Design Procedure

In this section, the design procedure of the proposed converter is presented. The main components, which require special considerations while designing, are the auxiliary inductors, series inductor, and output capacitor.

### A. Design of Auxiliary Inductors

Auxiliary inductors are designed based on the amount of reactive power required to guarantee ZVS for the MOSFETs. In other words, the reactive current should be enough to completely charge and discharge the MOSFET output capacitors. In [22], the design procedure of auxiliary circuits for a regular full-bridge converter is explained. However, since there are substantial differences in operating modes for the leading leg, the design procedure is given accordingly. According to the operating modes of the proposed converter, described earlier, the worst case for ZVS operation is no-load. Thus, ZVS should be guaranteed for no-load in order to make sure ZVS operation for all operating conditions. At absolutely no-load, the primary current is zero during the switching transitions of the leading leg. Therefore, the current through auxiliary circuit of the leading leg should only charge and discharge the output capacitors of the MOSFETs. Fig. 8 illustrates the auxiliary circuit waveforms. Considering the operating modes of the proposed converter and the discussion given in the previous section, the auxiliary circuits for this topology are completely symmetric unlike the auxiliary circuits for the regular full-bridge in which the amount of the reactive current should be more for the leading leg. Due to the fact that the auxiliary circuit current remains pretty constant during

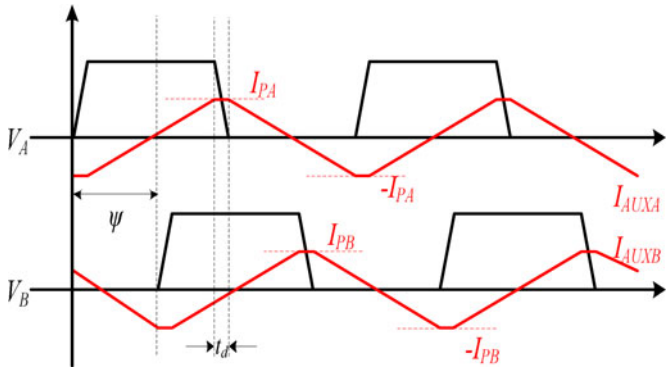


Fig. 8. Auxiliary circuit waveforms.

the dead-time, the auxiliary inductor acts as a constant current source, which discharges the capacitor across $S_1$ and charges the capacitor across $S_2$. According to Fig. 8, the value of this constant current source is derived as

$$I_{PA} = \frac{V_{dc}}{8L_{AUX1}.f_s}. \tag{20}$$

In order to design the inductor for the auxiliary circuits, first the amount of energy required to charge and discharge the output capacitors of the MOSFETs are calculated. Then the amount of dead-time required to allow complete charging and discharging is derived. Therefore, the amount of energy stored in the auxiliary inductor is given by

$$E_{AUX} = \frac{1}{2}.L_{AUX1}.I_{PA}^2. \tag{21}$$

The amount of energy required to charge and discharge the output capacitors of the MOSFETs is given by

$$E_{Cso} = C_{So}.V_{dc}^2. \tag{22}$$

Therefore, the value of the auxiliary inductance is designed as

$$L_{AUX1} = \frac{1}{128C_{So}.f_s^2}. \tag{23}$$

In order to ensure ZVS, the dead-time $t_d$, should be adjusted to allow the output capacitors of the MOSFETs to fully charge and discharge and is given by

$$t_d = \frac{2C_{So}.V_{dc}}{I_{PA}}. \tag{24}$$

It should be noted that the auxiliary inductors are AC inductors. Therefore, the maximum flux density considered for these inductors should be limited to avoid significant core losses. In [22], the design of the auxiliary inductors is explained in detail.

### B. Design of Series Inductor

The series inductor should be designed so that the converter full-load condition corresponds to the critical conduction mode of the series inductor. Fig. 9 shows the critical conduction mode of the series inductance, which is used to design the series

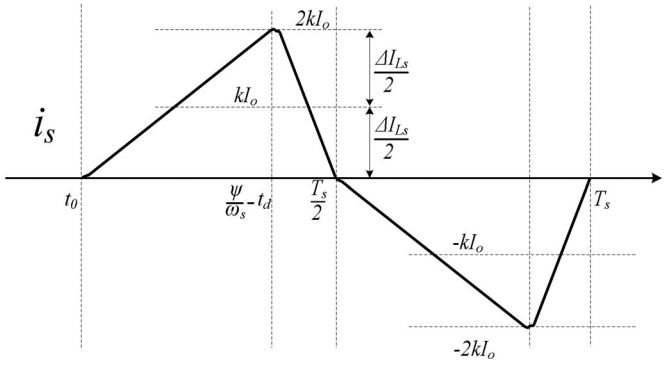


Fig. 9. Critical conduction mode.

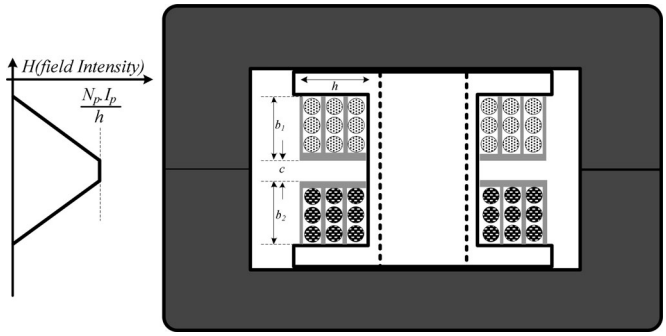


Fig. 10. Transformer winding configuration.

inductor. According to this figure, the reflected output current at the primary side is half of the peak current in the series inductor. Therefore, the value of series inductance is given by

$$L_{seq} = \frac{V_{dc} - kV_o}{2I_o} \cdot \left( \frac{\psi}{\omega_s} - t_d \right) \cdot \frac{T_s}{2} \tag{25}$$

where$L_{seq} = L_s + L_{leak}$.

Replacing the phase-shift from the expression for the gain of the converter given by (18), the series inductance is given by

$$L_{seq} = \left( 1 + k\frac{V_o}{V_{dc}} \right) \frac{V_o^2}{P_{o,\max}} \frac{T_s}{64}. \tag{26}$$

This series inductance $L_{seq}$ plays a major role in the energy transfer from the primary to the secondary side of the transformer. This inductance by nature is an AC inductor. So regular design methods [22], [30] of an AC inductor with air-gap has to be followed if an external inductor is to be designed for the series inductor, $L_s$. This inductance can be integrated as the leakage inductor of the transformer too. Although in that case, a transformer with a precisely designed leakage inductance will be necessary but the advantage of having this integrated series inductance is immense including elimination of an actual physical inductor along with its core and copper losses and the adverse effects of its fringing flux on the EMI and the operation of the surrounding devices on the PCB of the converter.

In order to enjoy the advantages of having an integrated series inductor, design of the transformer leakage is closely studied in this section [24]. In order to calculate the magnetic field in a transformer the following assumptions are made:

1) The winding consists of a large number of turns which are placed close to each other and the cross-sectional area of the wire used for winding is small compared to the winding cross section.
2) The magnetic field intensity inside the ferrite core is uniform and constant.

Although there can be numerous configurations of windings on a bobbin, in this section only the two-winding top-bottom arrangement is considered. This winding structure is shown in Fig. 10. It is evident in this figure that this winding provides excellent isolation between two windings, which is essential for this application. The magnetic flux distribution pattern can be derived by Amper's Law.

The leakage inductances $\ell_1$ and $\ell_2$ of each winding arises due to the magnetic flux which is stored only in the winding and not in the core and the effective leakage inductance of one winding is evaluated by electrically shorting the other winding. For calculating leakage inductance at the primary winding, the secondary winding is shorted. Under such a shorted condition, the field intensity along the cross section of the winding is shown in Fig. 10, with the mutual flux approximately reduced to zero. The leakage inductance $\ell_1$ is calculated by evaluating the following volume integral over the window area of the core occupied by the primary winding

$$\ell_1 = \frac{\mu_o}{I_1^2} \iiint H(\rho^2) dv. \tag{27}$$

Similarly, the reflected leakage inductance of the secondary winding on the primary side is given by

$$\ell_2 = \frac{\mu_o}{I_1^2} \iiint H(\rho^2) dv \tag{28}$$

evaluated over the volume occupied by the secondary winding on the bobbin.

Evaluation of the above integrals gives

$$\ell_1 = \frac{\mu_o}{h} N_1^2 \left( \frac{c}{2} + \frac{b_1}{3} \right) \tag{29}$$

$$\ell_2 = \frac{\mu_o}{h} N_1^2 \left( \frac{c}{2} + \frac{b_2}{3} \right). \tag{30}$$

The equivalent leakage inductance on the primary side is given by

$$\ell_{eq} = \ell_1 + \ell_2 = \frac{\mu_o}{h} N_1^2 \left( c + \frac{b_1 + b_2}{3} \right). \tag{31}$$

From the expression for equivalent leakage inductance it can be realized that for a given winding span and winding volume on the bobbin, the leakage inductance can be fine tuned by variation of the distance $c$ between the two windings. This feature is unique to this type of layout of the windings and cannot be exploited in the common method of laying the windings one on top of each other and just have the insulating material separating them. Moreover, this gap between the windings also ensures proper clearance and henceforth isolation between the windings, which is extremely essential for automotive applications that require strict isolation levels between the high voltage traction

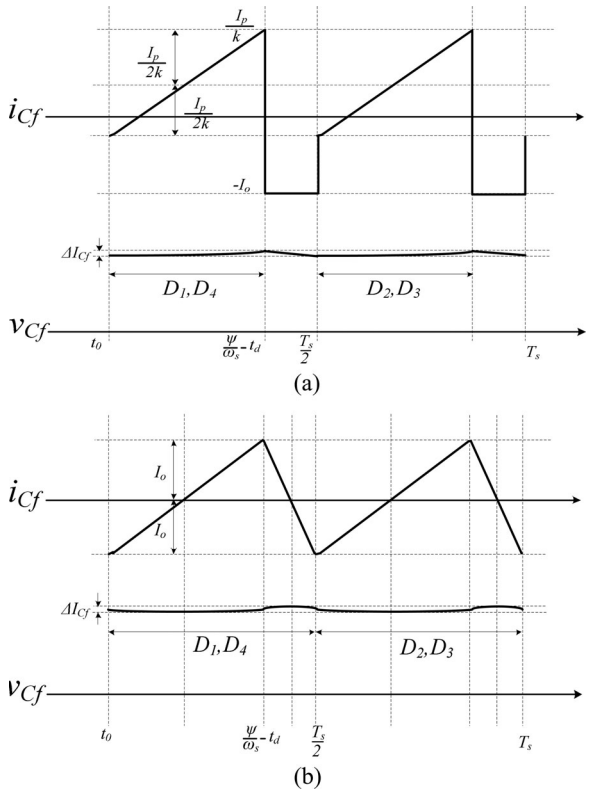


Fig. 11 (a) Output capacitor waveforms for a typical load. (b) Output capacitor waveforms for full-load.

TABLE I
CONVERTER SPECIFICATIONS

| Symbol | Parameter | Value |
|---|---|---|
| *Po* | Output Power | 3KW |
| *Vac* | Input Voltage | 170-267VAC |
| *Vo* | Output Voltage | 235-431VDC |
| $f_{sb}$ | Interleaved boost switching frequency | 50 KHz |
| $f_{sf}$ | Full-Bridge Switching Frequency | 220 KHz |
| $I_{in(max)}$ | Maximum input current | 16A |
| $I_{inrush}$ | Maximum inrush current | 32A |
| *P.F.* | Power Factor | > 99% |

TABLE II
PROPOSED FULL-BRIDGE PASSIVE COMPONENTS

| Symbol | Parameter | Value | Ratings |
|---|---|---|---|
| $L_{AUX,A,B}$ | Auxiliary Inductor | 67uH | 2A(rms) |
| $L_{eq}$ | Series Inductor(integrated in the transformer) | 11.8uH | 12.6A(rms) |
| $C_f$ | Filter Capacitor | 1uF | 400VDC |
| $L_f$ | Filter Inductor | 80uH | 10A(DC) |
| *k* | Transformer Turn's Ratio | 1:1.18 | - |
| $C_{a1}$ | Auxiliary Capacitor | 2.2uF | 300VDC |

battery ground and the input utility mains following the electric car isolation standards [33].

### C. Design of Output Capacitor

Fig. 11(a) shows the voltage and current of the output capacitor for a typical load. This capacitor is designed for the maximum load of the converter. Therefore, the minimum value of the capacitor is designed to assure operation in the critical conduction mode at peak load. The voltage and current waveforms of the capacitor are shown in Fig. 11(b) for the critical conduction mode. According to this figure the value of the capacitor is designed by

$$C_f = \frac{I_o}{8 f_s . \Delta V_{Cf}} \tag{32}$$

where $\Delta V_{Cf}$ is usually considered as 5%–10% of the output voltage. In the implemented prototype of this converter this capacitor value is chosen to be higher than the one given by (32).

## VI. EXPERIMENTAL RESULTS

A 3-KW prototype is implemented to verify the performance of the proposed converter. The designed specifications are shown in Table I. Table II shows the passive components used to implement the proposed full-bridge converter. Fig. 12 illustrates the block diagram of the converter. At the input stage, there is an inrush current protection, which limits the inrush current of the converter. Since there is usually a big capacitor at the output of the PFC, the inrush current to charge the capacitor is very high and a circuit is required to limit this current. The next block is the EMI filter which is designed to comply with the EMI standard (CISPR25/12) for electric vehicles [25], [26]. The following block is the input diode rectifier. It rectifies the input voltage for the two-phase interleaved boost converter. The interleaved boost converts the rectified input voltage to the intermediate DC-bus voltage. The output capacitor of the interleaved boost converter is large (1.4 mF) in order to decrease the second harmonic voltage ripple caused by the power ripple of the input boost PFC converter. In addition, there is a differential-mode (DM) filter at the output of the PFC in order to filter out the differential-mode noise. At the output of this filter, a clean DC-bus voltage is provided to the full-bridge converter. Note that another EMI filter is required at the output of the full-bridge converter in order to provide filtering for the EMI noise injected by the inverter. Since the inverter is connected to the high energy battery, it injects switching noise to the battery charger.

In order to achieve a high power density, the semiconductors are used in the form of power modules. There are two power modules used in the AC/DC converter. The first module shown in Fig. 13(a) consists of the input full-bridge rectifier, the interleaved boost MOSFETs including the driver circuit for the MOSFETs and the output boost diodes designed to be used for the PFC. Another module shown in Fig. 13(b) consisting of the full-bridge MOSFETs along with their driver circuits as well as the output diode rectifier is used to implement the

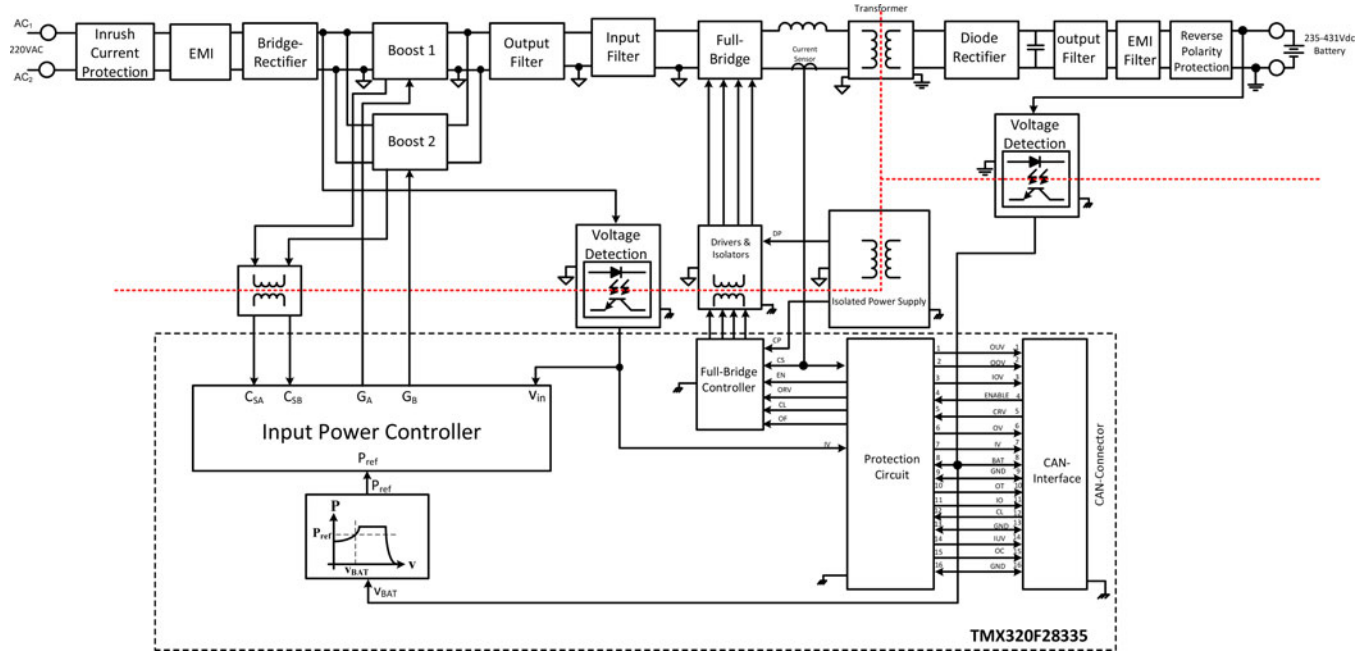


Fig. 12. Converter block diagram.

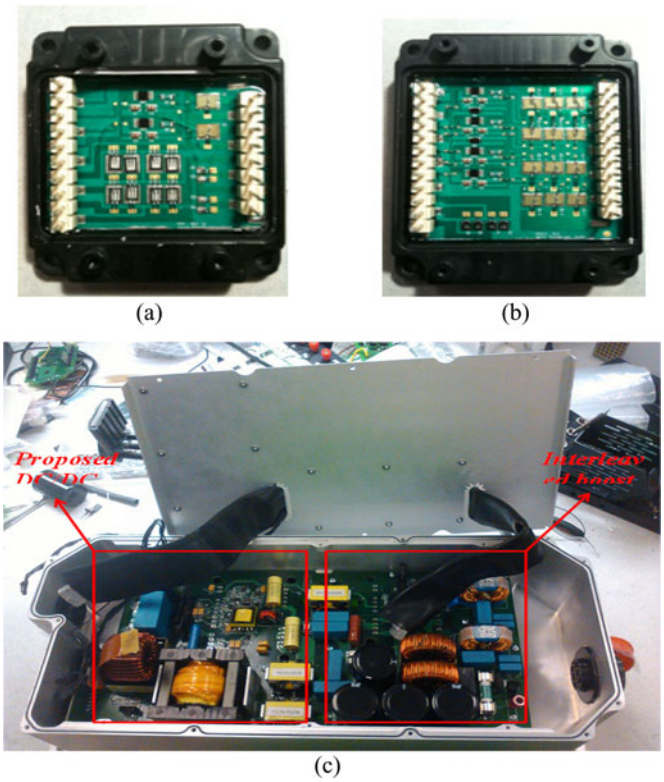


Fig. 13 (a) Interleaved boost power module. (b) DC/DC converter power module.

full bridge converter and its secondary side bridge rectifier. The components, which are used in PFC power module and in full-bridge power module, are shown in Tables III and IV, respectively. Since the semiconductors used in the power modules are in die package, the parasitic components are minimized in-

TABLE III
PFC POWER MODULE COMPONENTS

| Symbol | Parameter | Value | Ratings |
|---|---|---|---|
| *IDR* | Input Rectifier Diodes | 20ETF06pbF | 600VDC, 20ADC |
| $S_{PFC}$ | PFC MOSFETs | STx25NM50N | 500VDC, 25ADC |
| $D_{PFC}$ | PFC Output Diodes | CPW-0600-S010B | 600VDC,10ADC |
| *DR* | MOSFET Drivers | UCC27322D | 9A(peak) |

TABLE IV
FULL-BRIDGE POWER MODULE COMPONENTS

| Symbol | Parameter | Value | Ratings |
|---|---|---|---|
| $D_{FB}$ | Parallel Diodes | CPW-0600-S010B | 600VDC,10ADC |
| $S_{PFC}$ | Full-Bridge MOSFETs | STW77N65M5 | 650VDC, 65ADC |
| $D_{PFC}$ | Output Diodes | CPW-0600-S010B | 600VDC,10ADC |
| *DR* | MOSFET Drivers | UCC27322D | 9A(peak) |

side the module. This leads to superior performance under high switching frequency where resonance in the parasitic components tends to deteriorate the performance of the system. The diode CPW2-0600S010, which is used at the output of the interleaved boost rectifier, is a silicon-carbide diode and it has a zero reverse recovery [34]. The phase-shift full bridge converters usually suffer from the slow body diodes of the MOSFETs. The slow body diode causes voltage spikes due to the reactive current flowing through MOSFETs during the switching times. Due to the inductive path, using a fast diode parallel to the discrete MOSFET does not solve the problem. However, this problem can be solved using dies instead of discrete components; so there are four silicon carbide diodes added in parallel to the power MOSFETs in the full-bridge power module. UCC27322D is selected to drive the MOSFETs. This driver is able to drive 9 A peak current, which speeds up the switching transitions

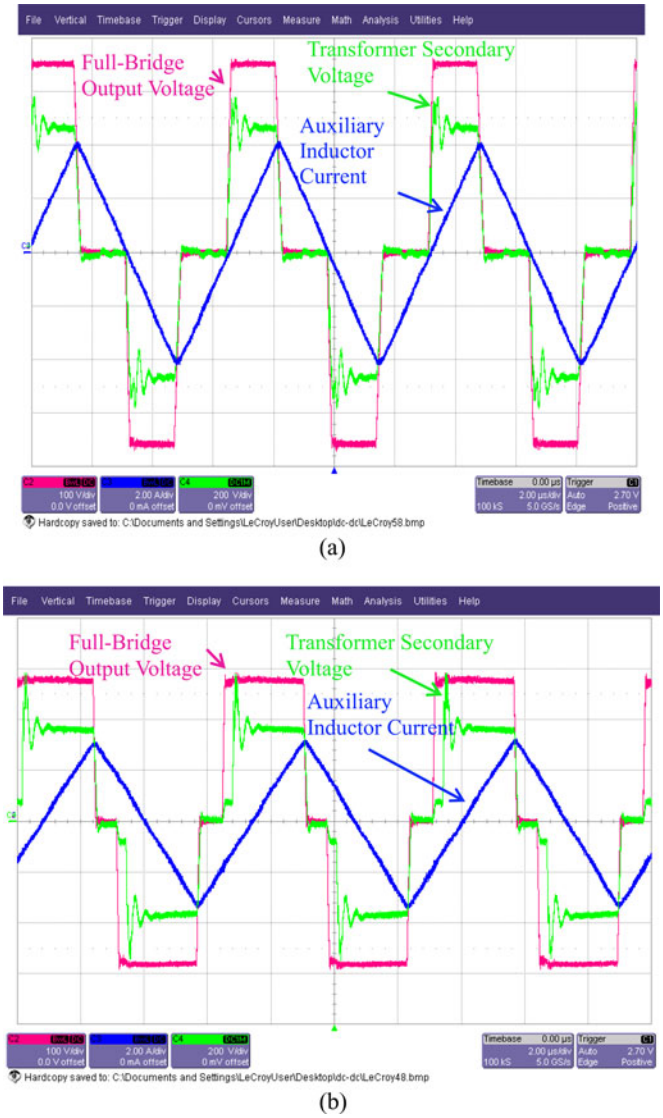


Fig. 14 (a) Waveforms of the conventional full-bridge converter with auxiliary circuit at 10% load. (b) Waveforms of the conventional full-bridge converter with auxiliary circuit at full-load.

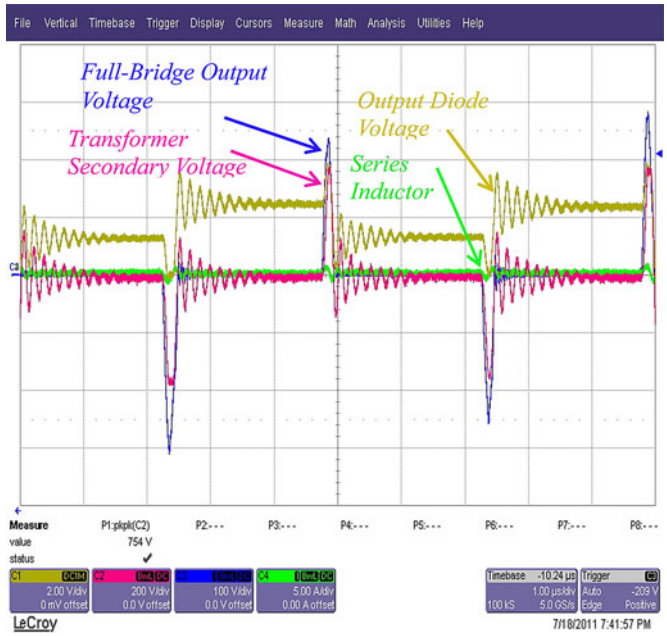


Fig. 15. Proposed converter waveforms at no load.

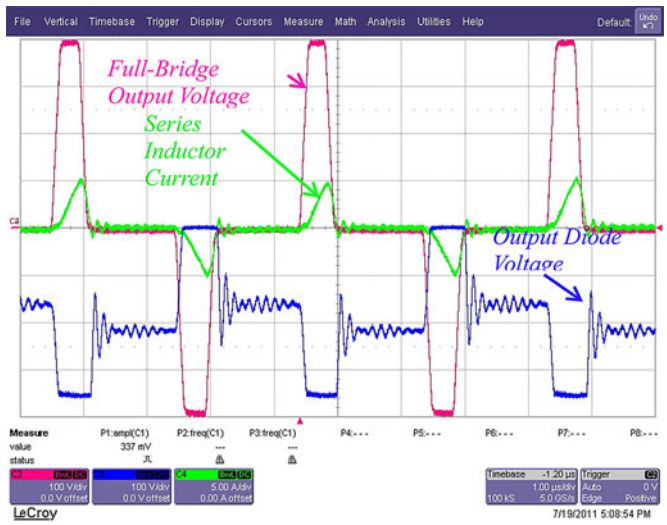


Fig. 16. Proposed converter waveforms at 10% load.

significantly. Fig. 13(c) shows the industrial prototype of the converter inside the water-cooled enclosure.

In order to implement the proposed controller, the TMX320F28335 eZdSP board is employed. This DSP board is a floating-point DSP, which offers a very flexible environment for advanced calculations. This DSP has a 12-bit ADC with a sequencer that is able to convert multiple analog signals sequentially [27]. It also has six EPWM (Enhanced PWM) modules, which can produce the desired PWM signals with a very high degree of flexibility [28]. The EPWM channels can be practically used up to 100 KHz. However, for the higher frequency range, the high resolution EPWM should be used to achieve a high resolution PWM signal and to avoid the limit cycle and instability. The high resolution module is embedded in the DSP [29]. Since the switching frequency is high, the high resolution module should be utilized to produce the PWM pulses.

In order to compare the performance of the proposed converter with the full-bridge converter, a prototype of the full-bridge converter with the same specification in Table I is implemented. Asymmetric auxiliary circuit [22] was added to the conventional full-bridge to be able to operate at light loads. Table V shows the key components of the conventional full-bridge converter.

Fig. 14(a) shows different waveforms of the conventional full-bridge converter operating at 10% load. According to this figure, the secondary voltage of the transformer which is incident across the output diode-bridge shows significant voltage spikes. Fig. 14(b) illustrates the waveforms of the conventional full-bridge converter operating at full-load. This figure shows severe voltage spikes across the transformer secondary voltage.

TABLE V
CONVENTIONAL FULL-BRIDGE PASSIVE COMPONENTS

| Symbol | Parameter | Value |
|---|---|---|
| $L_{AUX,A}$ | Auxiliary Inductor A | 33uH |
| $L_{AUX,B}$ | Auxiliary Inductor B | 67uH |
| $L_{leak}$ | Transformer Leakage Inductor | 1.8uH |
| $C_o$ | Output Capacitor | 140uF |
| $L_f$ | Filter Inductor | 80uH |
| $k$ | Transformer Turn's Ratio | 1:1.18 |
| $C_{a1}$ | Auxiliary Capacitor | 2.2uF |

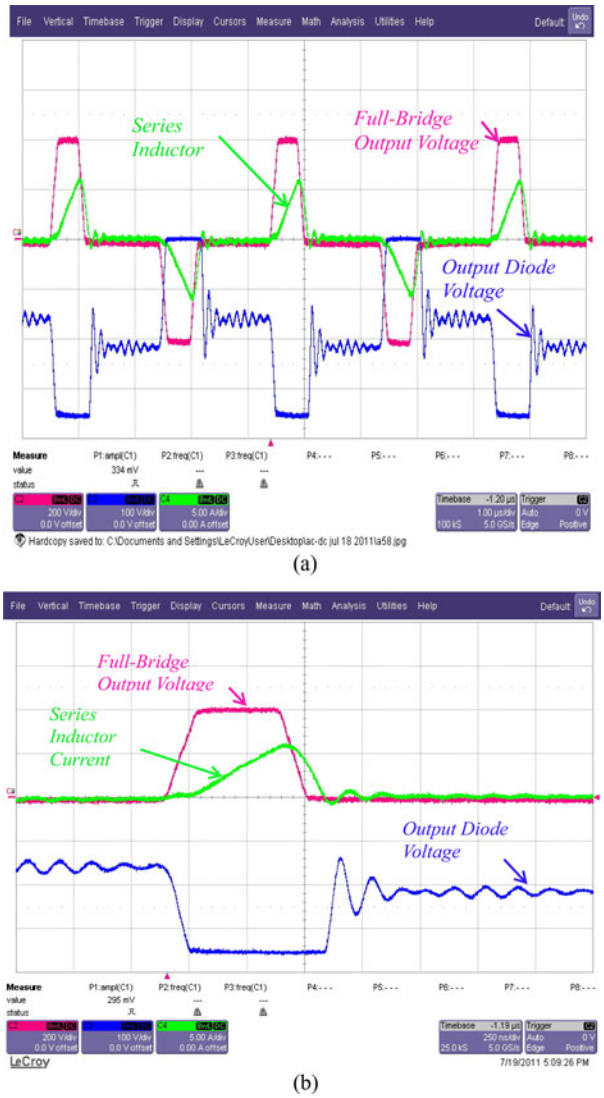


Fig. 17 (a) Proposed converter waveforms at 25% load. (b) Proposed converter enlarged waveforms at 25% load.

The experimental results for the proposed topology are obtained for input voltage of 400 VDC, output voltage of 300 VDC, and output power of 0 to 3 KW. The switching frequency is 220 KHz.

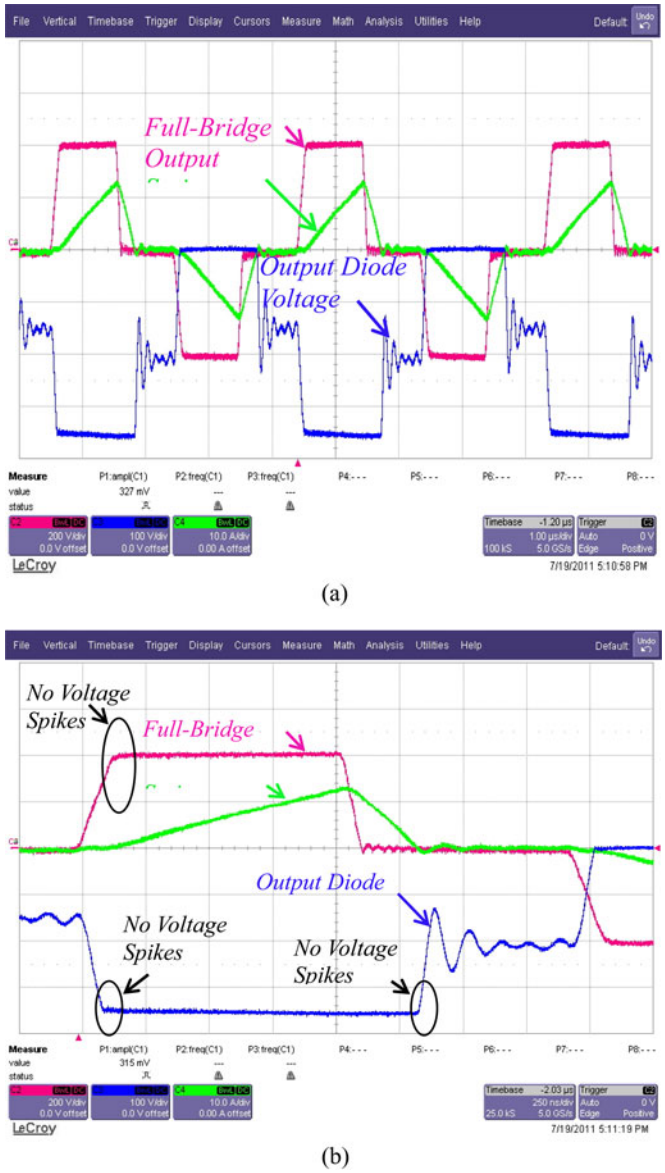


Fig. 18 (a) Proposed converter waveforms at 50% load. (b) Proposed converter enlarged waveforms at 50% load.

Figs. 15–21 show the waveforms of the proposed converter for different load conditions. Fig. 15 shows the waveforms for no-load condition. According to this figure, the converter is able to operate at absolutely no-load without any adverse voltage spikes across any of the semiconductors. Fig. 16 shows the waveforms for 10% load. Comparing Figs. 14(a) and 16, it is concluded that the proposed converter has superior performance over the conventional converter especially in regards to the voltage across the secondary-side diode-bridge. Fig. 17(a) and (b) shows the converter waveforms at 25% load. It can be seen in Fig. 17(b), even at such light loads the full-bridge output voltage has very smooth transitions at the leading and lagging edges; moreover, the series inductor current remains zero during the transition of the leading edge MOSFETs, which confirms that these switches enjoy zero voltage and zero current switching. Also from the

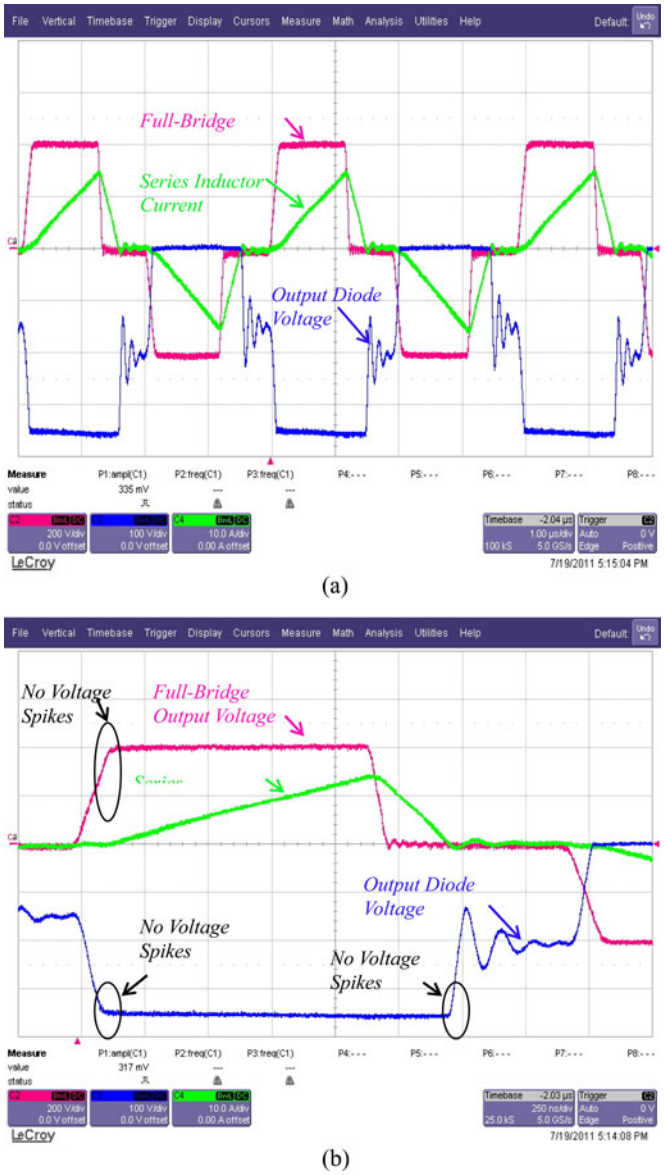


Fig. 19 (a) Proposed converter waveforms at 70% load. (b) Proposed converter enlarged waveforms at 70% load.

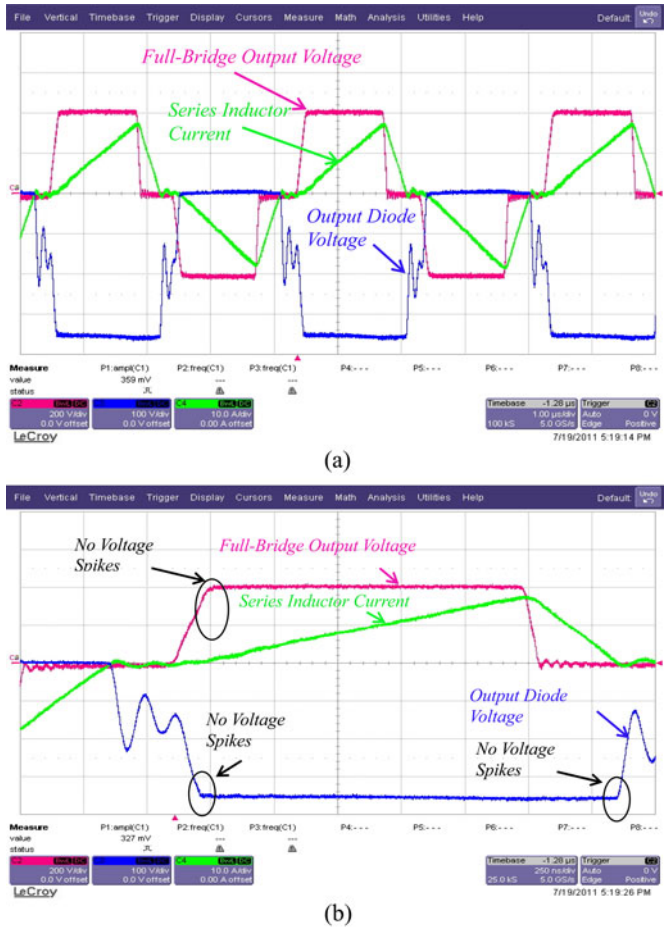


Fig. 20 (a) Proposed converter waveforms at 85% load. (b) Proposed converter enlarged waveforms at 85% load.

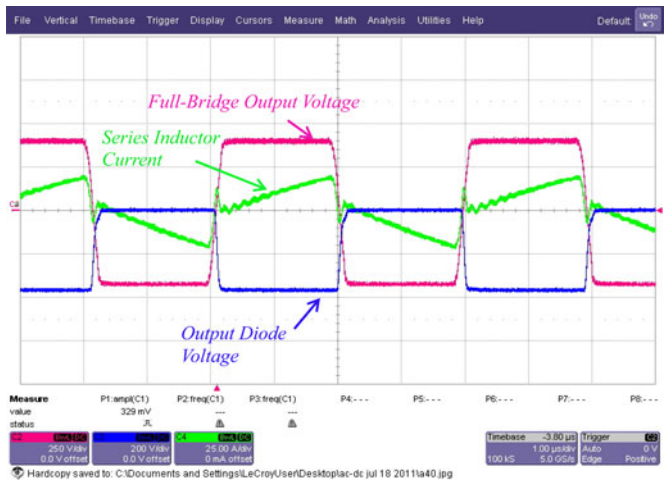


Fig. 21. Proposed converter waveforms at full-load.

output diode-bridge voltage waveform depicted in Fig. 17(b) the voltage clamping effect of the filter capacitor, $C_f$ is appreciated.

Fig. 18(a) and (b) illustrates the waveforms at 50% load. Fig. 19(a) and (b) shows the waveforms for 70% load. Fig. 20(a) and (b) depicts the waveforms for 85% load. From these figures, it is concluded that with increasing load Mode IV–VI gain prominence. Fig. 21 show the waveforms at full-load operation of the converter. The waveforms confirm operation of the converter close to critical conduction mode for the series inductor. It should be appreciated from the waveforms presented in this section that for the whole range of operation, the freewheeling mode of the output diode-bridge is eliminated due to the current driven nature of the output rectifier, which is a unique feature of the proposed topology. Fig. 22(a) and (b) show the auxiliary circuit current along with the other waveforms of the converter for two different loads.

Considering the experimental results of the proposed topology for the output diode bridge, 600 V diodes can be used to implement the output diode bridge rather than 1200 V diodes with higher forward voltage drop and bigger packages as required by the conventional full-bridge converter.

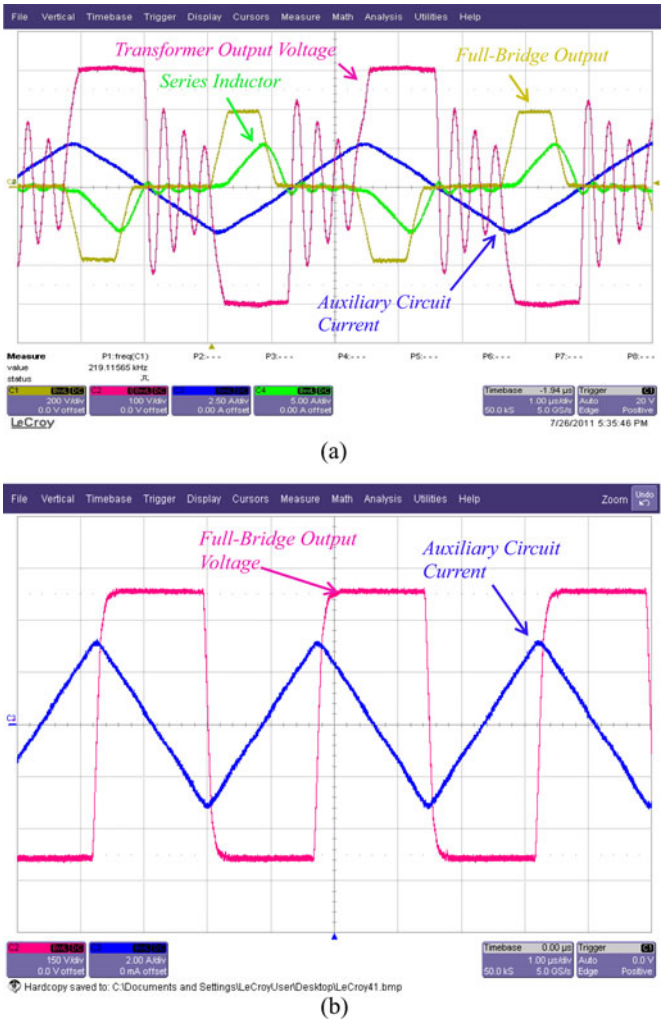


Fig. 22. Current in auxiliary circuit at different loads.

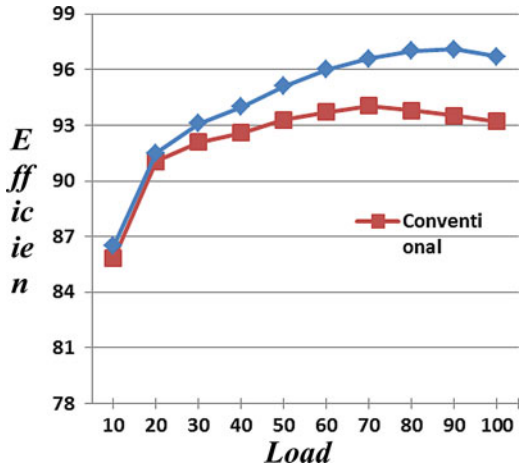


Fig. 23. Efficiency curves of the proposed and conventional full-bridge converter.

Fig. 23 shows the efficiency curves of the proposed and conventional full-bridge converter. This figure confirms the superior performance of the proposed converter over the conventional full-bridge converter with the asymmetric auxiliary circuit. According to this figure the efficiency is higher especially for heavy loads due to the elimination of the freewheeling mode, associated reverse recovery losses of output diodes, ZVZCS switching of the leading leg and ZVS switching of the lagging leg in the proposed topology.

## VII. Conclusion

In this paper, a novel yet simple full-bridge topology is introduced for high voltage battery charging applications in electric vehicles. The proposed converter eliminates the adverse effects of the voltage spikes at the secondary side of the transformer, as well as the freewheeling mode of operation, which are intrinsic to the conventional full-bridge converters. Moreover, the proposed converter assures reliable operation at no load by applying the symmetric auxiliary circuits on both legs of the full-bridge converter. Experimental results and better efficiency of the proposed converter over full range of operation not only validate the operation of the converter but also confirm the superiority of the proposed topology over the conventional full-bridge converter.

## References

[1] S. M. Lukic, J. Cao, R. C. Bansal, F. Rodriguez, and A. Emadi, "Energy storage systems for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2258–2267, Jun. 2008.

[2] L. Young-Joo, A. Khaligh, and A. Emadi, "Advanced integrated bidirectional AC/DC and DC/DC converter for plug-in hybrid electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 58, no. 8, pp. 3970–3980, Oct. 2009.

[3] A. Emadi, Y. J. Lee, and K. Rajashekara, "Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237–2245, Jun. 2008.

[4] G.-B. Koo, G.-W. Moon, and M.-J. Youn, "Analysis and design of phase shift full bridge converter with series-connected two transformers," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 411–419, Mar. 2004.

[5] J. Wang, F. Z. Peng, J. Anderson, A. Joseph, and R. Buffenbarger, "Low cost fuel cell converter system for residential power generation," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1315–1322, Sep. 2004.

[6] M. J. Schutten and D. A. Torrey, "Improved small-signal analysis for the phase-shifted PWM power converter," *IEEE Trans. Power Electron.*, vol. 18, no. 2, pp. 659–669, Mar. 2003.

[7] A. Averberg and A. Mertens, "Analysis of a voltage-fed full bridge DC–DC converter in fuel cell systems," in *Proc. IEEE Power Electron. Spec. Conf., (PESC) IEEE*, Orlando, FL, Jun. 17–21, 2007, pp. 286–292.

[8] W.-J. Lee, C.-E. Kim, G.-W. Moon, and S.-K. Han, "A new phase-shifted full-bridge converter with voltage-doubler-type rectifier for high-efficiency PDP sustaining power module," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2450–2458, Jun. 2008.

[9] Y. Jang and M. M. Jovanovic, "A new family of full-bridge ZVS converters," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 701–708, May 2004.

[10] W. Xinke, J. Zhang, X. Xie, and Z. Qian, "Analysis and optimal design considerations for an improved full bridge ZVS DC DC converter with high efficiency," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1225–1234, Sep. 2006.

[11] R. Ayyanar and N. Mohan, "Novel soft-switching DC–DC converter with full ZVS-range and reduced filter requirement. I. Regulated-output applications," *IEEE Trans. Power Electron.*, vol. 16, no. 2, pp. 184–192, Mar. 2001.

[12] G. Hua, F. C. Lee, and M. M. Jovanovic, "An improved zero-voltage-switched PWM converter using a saturable inductor," in *Conf. Rec. 22nd Annu. IEEE Power Electron. Spec. Conf.*, 1991, pp. 189–194.

[13] L. H. Mweene, C. A. Wright, and M. F. Schlecht, "A 1 kW 500 kHz front-end converter for a distributed power supply system," *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 398–407, Jul. 1991.

[14] J. A. Sabate, V. Vlatkovic, R. B. Ridley, and F. C. Lee, "High-voltage, high-power, ZVS, full-bridge PWM converter employing an active snubber,"

in *Proc. 6th Annu. Appl. Power Electron. Conf. Expo.*, Dallas, TX, Mar. 10–15, 1991, pp. 158–163.
[15] J. G. Cho, J. W. Baek, D. W. Yoo, H. S. Lee, and G. H. Rim, "Novel zero-voltage and zero-current-switching (ZVZCS) full bridge PWM converter using transformer auxiliary winding," in *Proc. 28th Annu. IEEE Power Electron. Spec. Conf., (PESC)*, vol. 1, St. Louis, MO, Jun. 22–27, 1997, pp. 227–232.
[16] E.-S. Kim, K.-Y. Joe, M.-H. Kye, Y.-H. Kim, and B.-D. Yoon, "An improved soft-switching PWM FB DC/DC converter for reducing conduction losses," *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 258–264, Mar. 1999.
[17] E.-S. Kim and Y.-H. Kim, "A ZVZCS PWM FB DC/DC converter using a modified energy-recovery snubber," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1120–1127, Oct. 2002.
[18] A. Bendre, S. Norris, D. M. Divan, I. Wallace, and W. E. Brumsickle, "New high power DC–DC converter with loss limited switching and lossless secondary clamp," in *Proc. 2001 IEEE 32nd Annu. Power Electron. Spec. Conf., (PESC)*, vol. 1, Vancouver, BC, 2001, pp. 321–326.
[19] M. Ilic and D. Maksimovic, "Phase-shifted full bridge DC–DC converter with energy recovery clamp and reduced circulating current," in *Proc. 22nd Annu. IEEE Appl. Power Electron. Conf. (APEC)*, Feb. 25–Mar. 1, 2007, pp. 969–975.
[20] W. Xinke, X. Xiaogao, Z. Chen, Q. Zhaoming, and Z. Rongxiang, "Low voltage and current stress ZVZCS full bridge DC–DC converter using center tapped rectifier reset," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1470–1477, Mar. 2008.
[21] H. Cha, L. Chen, R. Ding, Q. Tang, and F. Z. Peng, "An alternative energy recovery clamp circuit for full-bridge PWM converters with wide ranges of input voltage," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2828–2837, Nov. 2008.
[22] M. Pahlevaninezhad, J. Drobnik, P. Jain, and A. Bakhshai, "A load adaptive control approach for a zero voltage switching DC/DC converter used for electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 920–933, Feb. 2012.
[23] P. K. Jain, W. Kang, H. Soin, and Y. Xi, "Analysis and design considerations of a load and line independent zero voltage switching full bridge DC/DC converter topology," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 649–657, Sep. 2002.
[24] A. D. Abraham, "Modeling and estimation of leakage phenomena in magnetic circuits," Ph.D. dissertation, Dept. Electr. Comput. Eng., California Inst. of Technol. Pasadena, CA, 1986.
[25] K. Raggle, T. Nussbaumer, and J. W. Kolar, "Guideline for a simplified differential-mode EMI filter design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010.
[26] J. Beila, A. Wirthmueller, R. Waespe, M. L. Heldwein, K. Raggl, and J. W. Kolar, "Passive and active hybrid integrated EMI filters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1340–1349, May 2009.
[27] Texas Instrument, "TMS320×2833 Analog-to-Digital Converter (ADC) Module," SPRU812 A, Sep. 2007.
[28] Texas Instrument, "TMS320×2833, 2823× ENHANCED PULSE WIDTH MODULATOR (ePWM) Module," SPRUG04 A, Oct. 2008 (Revised Jul. 2009).
[29] Texas Instrument, "TMS320×2833, 2823× High Resolution Pulse Width Modulator," SPRUG02, Feb. 2009.
[30] F. Krismer and J. W. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar. 2010.
[31] Z. Amjadi and S. S. Williamson, "Power-electronics-based solutions for plug-in hybrid electric vehicle energy storage and management systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 608–616, Feb. 2010.
[32] F. L. Mapelli, D. Tarsitano, and M. Mauri, "Plug-in hybrid electric vehicle: Modeling, prototype realization, and inverter losses reduction analysis," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 598–607, Feb. 2010.
[33] A. Hajimiragha, C. A. Canizares, M. W. Fowler, and A. Elkamel, "Optimal transition to plug-in hybrid electric vehicles in Ontario, Canada, considering the electricity-grid limitations," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 690–701, Feb. 2010.
[34] H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC devices on hybrid electric and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 912–921, Mar./Apr. 2011.
[35] A. Y. Saber and G. K. Venayagamoorthy, "Plug-in vehicles and renewable energy sources for cost and emission reductions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1229–1238, Apr. 2011.
[36] I. Aharon and A. Kuperman, "Topological overview of power-trains for battery-powered vehicles with range extenders," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 868–876, Mar. 2011.
[37] W. Song and B. Lehman, "Current-fed dual-bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 461–469, Mar. 2007.
[38] H. Akagi and R. Kitada, "Control and design of a modular multilevel cascade BTB system using bidirectional isolated DC/DC converters," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2457–2464, Sep. 2011.
[39] J. Kim, H.-S. Song, and K. Nam, "Asymmetric duty control of a dual-half-bridge DC/DC converter for single-phase distributed generators," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 973–982, Mar. 2011.
[40] C.-M. Wang, C.-H. Lin, and T.-C. Yang, "High-power-factor soft-switched DC power supply system," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 647–654, Feb. 2011.

**Majid Pahlevaninezhad** (S'07–M'12) received the B.S. and M.S. degrees in electrical engineering from Isfahan University of Technology, Isfahan, Iran, and the Ph.D. degree from Queens University, Kingston, Canada.

He is currently a Postdoctoral Research Associate with the Department of Electrical and Computer Engineering at Queen's University, Canada. He worked as a technical designer in the Information and Communication Technology Institute (ICTI) at Isfahan University of Technology from 2003 to 2007, where he was involved in design and implementation of high quality resonant converters. He also collaborated with Freescale Semiconductor Inc. where he was the leader of a research team working on the design and implementation of the power converters for a pure electric vehicle from 2008 to 2012. He is the author of more than 32 journal and conference proceeding papers and the holder of 4 U.S. patents. His current research interests include robust and nonlinear control in power electronics, advanced soft-switching methods in power converters, plug-in pure electric vehicles, and PV-micro-inverters.

Dr. Pahlevaninezhad is a member of the IEEE Power Electronics Society and Industrial Electronics Society. He was also the recipient of the distinguished graduate student award from Isfahan University of Technology.

**Pritam Das** (S'09–M'12) was born in Calcutta, India in 1978. He received the Bachelor of Engineering degree in electronics and communication engineering from the University of Burdwan, India. He also received the Master's of Applied Science degree and the Ph.D. degree, both in electrical engineering from the University of Western Ontario, London, ON, Canada in 2005 and 2010 respectively.

From 2010 to 2011, he was a post-doctoral fellow at the Queen's Centre for Energy and Power Electronics Research (ePOWER), Queen's University Kingston, Ontario, Canada. Presently he is with Murata Power Solutions, Markham Ontario. His research interests include high frequency and high efficiency ac-dc and dc-dc power converters, power factor correction, soft switching techniques, design of high frequency magnetic components for power converter and modeling and design of control of ac-dc and dc-dc converters. He is involved in research on modeling and control of high frequency and high efficiency resonant and PWM converters for various applications including electric vehicles, photo-voltaic micro-inverters, data centers, etc. He has published over 33 technical papers in referred journals and conferences.

Dr. Das is also a reviewer of IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS.

**Josef Drobnik** (SM'93) left Czechslovakia, in 1982, for political reasons; since then he has been working in the field of power electronics with steadily increasing responsibilities. From 1982 to 1995, he was in Canada with CVDS, BNR, and Norrtel. In 1995, he relocated to the USA to work for GE Corporate R&D, then with Intel, LL3 Communications, and finally with Freescale Semiconductor. His positions include Chief Engineer, Technical Advisor, and Director. He has published 46 technical papers and is responsible for 33 US and international patents. His professional interests include new power conversion topologies, integrated magnetic, and "after silicon" semiconductors.

**Praveen K. Jain** (S'86–M'888–SM'91–F'02) received the B.E. (Hons.) degree (from the University of Allahabad, India, and the M.A.Sc. and Ph.D. degrees from the University of Toronto, Toronto, ON, Canada, in 1980, 1984, and 1987, respectively, all in electrical engineering.

Currently, he is a Professor and Canada Research Chair at the Department of Electrical and Computer Engineering, Queen's University, Kingston, Canada, and Director of the Queen's Centre for Energy and Power Electronics Research (ePOWER). He has secured cash and in-kind in external research funding to conduct research in the field of power electronics. He has supervised more than 75 graduate students, postdoctoral fellows, and research engineers. He has published more than 350 technical papers (including more than 90 IEEE Transactions papers). He holds more than 50 patents (granted and pending). He is also a founder of CHiL Semiconductor in Tewksbury, MA, and SPARQ System in Kingston, Ontario, Canada. Prior to joining Queen's, he worked as a Professor at Concordia University (1994–2000), Technical Advisor at Nortel (1990–1994), Senior Space Power Electronics Engineer at Canadian Astronautics Ltd (1987–1990), Design Engineer at ABB ((1981), and Production Engineer at Crompton Greaves (1980). In addition, he has consulted with Astec, Ballard Power, Freescale Semiconductor Inc., General Electric, Intel and Nortel.

Dr. Jain is an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS and an Editor of International Journal of Power Electronics. He is also a Distinguished Lecturer of IEEE Industry Applications Society. He is a Fellow of the Engineering Institute of Canada (EIC) and the Canadian Academy of Engineering (CAE). He is the recipient of thee 2004 Engineering Medal (R&D) from the Professional Engineers of Ontario. He is also the recipient of the 2011 IEEEE William Newell Power Electronics Field Award.

**Alireza Bakhshai** (M'04–SM'099) received the B.Sc. and M.Sc. degrees from the Isfahan University of Technology, Isfahann, Iran, in 1984 and 1986, respectively, and the Ph.D. degree from Concordia University, Montreal, QC, Canada, in 1977.

From 1986 to 1993 and from 1998 to 2004, he was in the faculty of the Department of Electrical and Computer Engineering, Isfahan University of Technology. From 1997 to 1998, he was a Postdoctoral Fellow with Concordia University. Currently, he is with the Department of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, Canada. His research interests include high-power electronics and applications in distributed generation and wind energy, control systems, and flexible AC transmission services.