A Three-port Flyback for PV Microinverter Applications With Power Pulsation Decoupling Capability

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***Abstract*—A novel single-stage photovoltaic (PV) microinverter with power decoupling capability is proposed in this paper. The proposed topology is based on three-port flyback with one port dedicated to power decoupling function so as to reduce the decoupling capacitance, thus allowing for long lifetime film capacitor to be used. Operation principle is analyzed in details. Key design considerations, including key parameter selections, predictive control strategy, and the dc voltage balance control across the power decoupling capacitor, are given in this paper. A 100-W microinverter prototype is built to verify the proposed topology. Experimental results show the proposed topology can achieve power decoupling, while maintaining good efficiency.**

***Index Terms*—Flyback, microinverter, predictive control, power decoupling, three-port converter.**

I. Introduction

With the depletion of fossil fuels, renewable sources, generated from natural resources, have caught the eyes in recent years from both the industries and governments all over the world due to their environmental friendliness. Among renewable sources, the photovoltaic (PV) has witnessed the unprecedented growth. The PV market grew by almost 15% in 2009 compared to that in 2008, reaching 7.2-GW capacity, and the accumulative PV power installed in the world raised by 45% up to 22.9 GW [1]. Based on the European Photovoltaic Industry Association (EPIA) optimistic estimation, PV systems could provide up to 12% of European electricity demand by 2020 [2].

Currently, the inverter for the PV system can be categorized into three types: centralized inverter, string inverter, and ac module [3]–[5]. Recently, the ac module has attracted the attention of both the researchers and industry due to its numerous advantages: 1) improved energy harvest, 2) improved system efficiency, 3) lower installation costs, 4) plug-N-play operation, and 5) enhanced flexibility and modularity. Moreover, ac module is designed with mass production in mind, which will lead to competitive cost. With these advantages, the ac module has become the trend for future PV system development. However, low cost, high efficiency, long life expectancy, low profile, and multifunctions are the challenges that still need to be addressed.

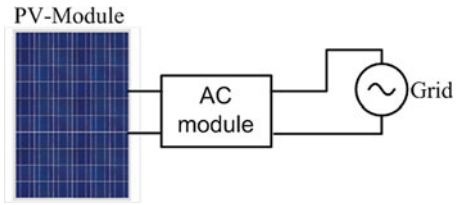

Fig. 1. AC-module PV system.

Fig. 1 shows a typical microinverter-based PV system, where the microinverter is integrated to the PV panel, and feeds the collected solar power directly into the utility grid. Usually, for safety purposes and leakage current in grid-connected applications, a high-frequency transformer is embedded in the ac module due to the reasons of low cost and small size. AC module with a high-frequency transformer can be further grouped into three architectures based on the dc-link configurations: dc link, pseudo-dc link and high-frequency ac [6]. Among these three basic implementations, the architecture with the pseudo-ac link, featuring only one power conversion stage compared to other two implementations, has the potential to achieve the highest efficiency. Typically, the microinverter is connected, and even attached, to a single PV panel, which requires that the microinverter has a lifespan matching the PV panel's ones, namely 25 years [7], and thus long life components have to be used to ensure ac module's long lifespan. However, ac module usually with single-phase grid connection has the disadvantage that the power flow to the grid is time varying, while the power of the PV panel must be constant for maximizing energy harvest. This requires energy storage elements to be placed between the input and output to balance (decouple the unbalance) the different instantaneous input and output power. Capacitor is usually used to serve as a power decoupling element. However, the lifetime of different types of capacitors varies greatly, e.g., electrolytic capacitors typically having 1000–7000-h lifetime at 105 °C

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operating temperature [8]. Most of microinverters use electrolytic capacitors as power decoupling storage elements due to their large capacitance and ease of implementation, which tends to limit their lifespan. For the conventional single-stage ac module, power decoupling capacitor has to be placed at PV side [9], where the dc voltage is relatively low, normally ranging from 25 to 60 V for crystalline PV technology. In this case, a large capacitance is needed to realize the power decoupling (2.6 mF is needed for 100-W single-stage microinverter with 2-V voltage ripple across the 60-V input voltage). To reduce the required power decoupling capacitance, some researchers have explored various ways so as to allow for other longer lifespan capacitor technologies, such as film capacitors, to be used [10]–[18].

A flyback-type single-stage microinverter with a decoupling power circuit is proposed in [10], in which a 40-μF film capacitor was used for a 100-W microinverter design. Given the double conversion process, the projected efficiency is low, as indicated in [10] where the peak efficiency reported was only 70%. A modified topology was proposed by Kjaer and Blaabjerg [11] where the leakage inductance energy is recycled by using a "dual-switch flyback converter," which complicates the topology by adding two more switches. Even with design optimization, the calculated peak efficiency was 86.7%. Another modified topology was proposed in [12] to avoid a double power conversion, resulting in higher conversion efficiency in compared with the one in [10]. However, the topology has two main drawbacks: 1) similar to [10], when the switch S_x turns OFF, there is no releasing pass for leakage inductance, either causing high voltage spikes on S_x or requiring a snubber circuit; 2)when the switch S_x turns ON, the magnetizing current will continue to be charged to a higher peak, which results in both higher conduction loss and switching loss.

A bidirectional buck-boost converter was proposed by Kyritsis [13] to realize the power decoupling. Although in [13] no specific number regarding the overall inverter efficiency is mentioned, the power losses associated with the decoupling circuit will reduce the overall efficiency. Moreover, using a smaller decoupling capacitor leads to higher stresses for the power devices, which may result in more losses and lower efficiency. Tan *et al.* [14] combined the boost and flyback topologies to propose a new topology to implement the power decoupling, which can be viewed as a two-stage power conversion with first stage processing the dc power from PV and the second stage dealing with the power decoupling. Shinjo *et al.* [15] proposed an active power decoupling method for a push-pull converter.

The aforementioned techniques have the drawbacks of either complicating topologies or reducing efficiency. To reduce the cost of the decoupling circuit, a three-port converter, featuring fewer component count, and more compact structure, may be one of the best choices for power decoupling in a single-stage inverter. One port implements maximum power point tracking (MPPT) and the second port is dedicated to power decoupling. Krein and Balog proposed a power decoupling concept by adding a third-port via a high-frequency ac link [16]. Many three-port converters have been proposed in recent years, where they can be tailored for single-phase inverters with one-port dedicating to power decoupling function [17]–[24]. Table I summarizes the aforementioned topologies in terms of efficiency and switch counts.

TABLE I
COMPARISONS OF THREE-PORT TOPOLOGIES FOR AC MODULE

Topologies	efficiency	Switch components
Ref.[10]	70%	4(MOSFETs)+3 Diodes
Ref.[11]	86.7%(Calculated)	6(MOSFETS)+4 Diodes
Ref.[12]	73%	4(MOSFETS)+4 Diodes
Ref.[13]	-	6(MOSFETS)
Ref.[14]	85%	4(MOSFETS)+4 Diodes
Ref.[15]	-	9(MOSFETS)+4 Diodes
Ref.[16]	-	6(MOSFETS)+4 TRIACs
Ref.[17]	-	10(MOSFETS)+1 Diodes

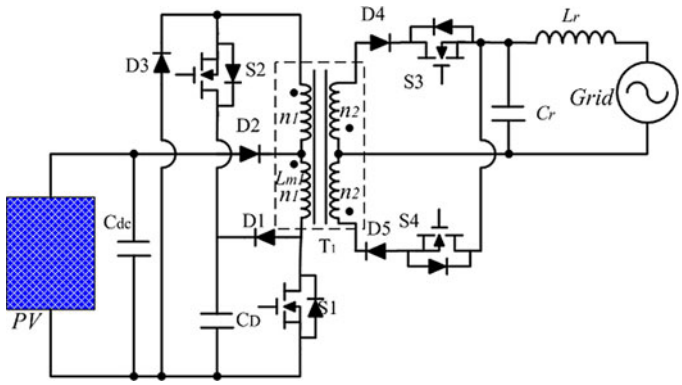

Fig. 2. Proposed topology.

In this paper, a novel integrated three-port flyback topology is proposed that realizes both single-stage dc–ac conversion and power decoupling. This results in a low component count, compact power stage, low cost, and a decent efficiency. This paper is organized as follows: The proposed topology is presented in Section II. The detailed operation principle is explained in Section III with the key design considerations discussed in Section VI. Simulation results are given in Section V. Experimental results are shown in Section VI followed by the conclusions drawn in Section VII.

II. PROPOSED TOPOLOGY

Fig. 2 shows the circuit configuration of the proposed single-stage microinverter. This topology is basically derived from a conventional flyback by adding additional switch S_2, and another transformer winding at primary side to implement power decoupling function. The power decoupling capacitor C_D is configured to function as both an energy storage element and a snubber capacitor to recycle the transformer's leakage energy. A diode D_2 is added to prevent the reverse current from power decoupling capacitor C_D to PV source. The diode D_3 offers a leakage energy discharge path, which consists of D_3, T_1, D_1, and C_D in the loop. Two secondary windings are designed to pump an ac current into the grid. The purposes of the D_4 and S_3 (D_5 S_4) in series connection are 1) to block power output of either secondary winding in the half-grid cycle period and 2) to

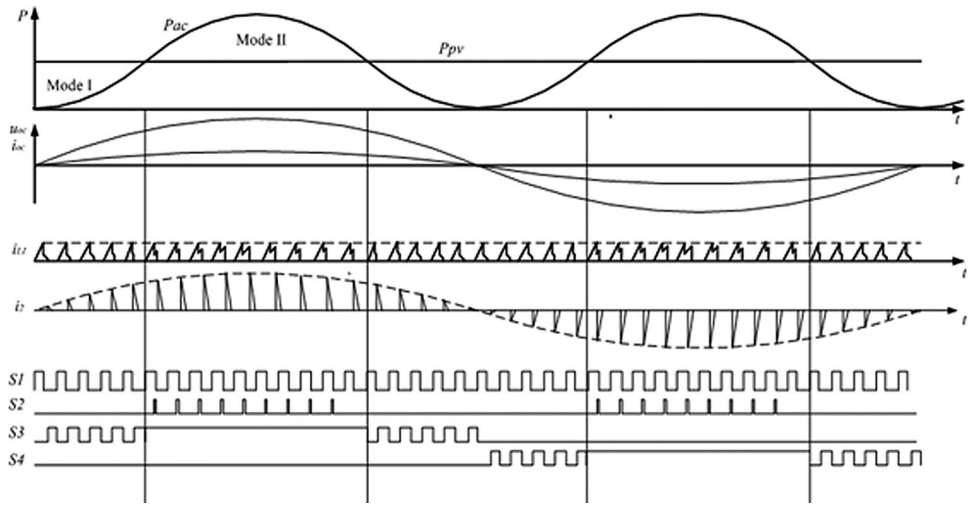

Fig. 3. Basic waveforms of the proposed converter.

shape the average sinusoidal current waveform to interface the grid.

III. Operation Principle

Fig. 3 shows the basic waveforms of the proposed topology, where $P_{\rm ac}$ is the output ac power, $P_{\rm pv}$ is the PV power, $u_{\rm ac}$ and $i_{\rm ac}$ are the output voltage and current, i_{L1} is the magnetizing current, i_2 is the current at secondary side, and S1–S4 are drive signals. Based on whether the PV power $P_{\rm pv}$ is greater than the output power $P_{\rm ac}$ or not, the circuit operation modes can be divided into two operation modes as illustrated in Fig. 3: mode I and mode II. In mode I, where the PV power $P_{\rm pv}$ is greater than the output power $P_{\rm ac}$, the surplus power is charged to the decoupling capacitor C_D through D_1, D_3 and transformer T_1. In mode II, the decoupling capacitor C_D supplies the power deficit. In this manner, the power drawn from the PV panel can maintain constant. As seen from Fig. 3, since the currents both in primary side and secondary side are operating in discontinuous conduction mode (DCM), the current across the switch increases from zero when switch S1 turns ON, thus achieving zero-current-switching, and the reverse recovery losses of diodes D_4 and D_5 are avoided as well, which will greatly improve the overall efficiency. The calculated peak efficiency is around 92.3%.

Fig. 4 shows magnetizing current $i_L(t)$, secondary current $i_2(t)$, waveforms, and switch driving signals in both mode I and mode II.

Based on the presented operation principle, the operation of the proposed topology is divided into four different circuit stages in each switching cycle. Each stage shown in Fig. 5 will be explained in details as follows.

A. Mode I ($P_{\rm PV} > P_{\rm ac}$)

Fig. 4(a) shows the operation waveforms in one switching interval for mode I. This mode occurs whenever the generated PV power is greater than the output ac power. The switching period T_s is divided into four intervals.

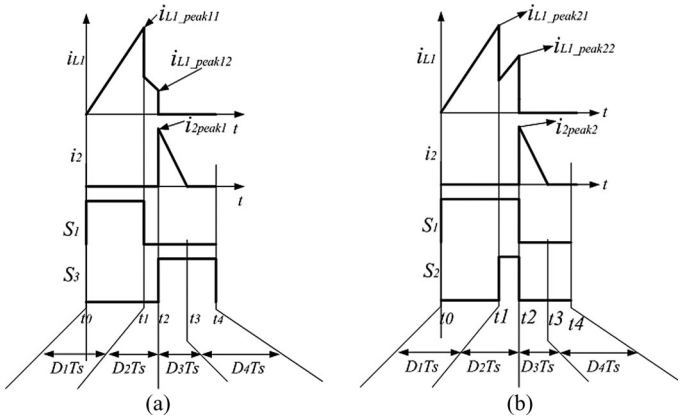

Fig. 4. Current and driver waveforms in both modes: (a) mode I and (b) mode II.

Stage1[t_0–t_1]: During this stage, as seen in Fig. 5(a), switch S_1 is turned ON. Then, the magnetizing current in transformer ramps up from zero to $i_{L1\text{-peak11}}$.The peak current $i_{L1\text{-peak11}}$ is calculated as follows:

$$i_{L1\text{-peak11}} = \frac{U_{\rm dc}}{L_{m1}} D_1 T_S \tag{1}$$

where L_{m1} and $U_{\rm dc}$ are magnetizing inductance of the primary winding n_1 and dc input voltage, respectively.

Stage2[t_1–t_2]: This stage starts when the main switch S_1 is turned OFF, while the switches in the secondary side are still OFF, as shown in Fig. 5(b). At this instant, the magnetizing current starts charging the decoupling capacitor C_D through D_1 and D_3. Assuming the voltage U_{cd} across the decoupling capacitor C_D is constant during one switching period, the magnetizing current i_{L1} can be expressed as follows:

$$i_{L1}(t) = \frac{-U_{cd}}{4L_{m1}}(t - t_1) + \frac{i_{L1\text{-peak11}}}{2} \tag{2}$$

Equation (2) indicates that the magnetizing current $i_{L1}(t)$ is decreasing linearly during this stage. This stage ends when $i_{L1}(t)$ reaches the required value, $i_{L1\text{-peak12}}$ where the energy in the

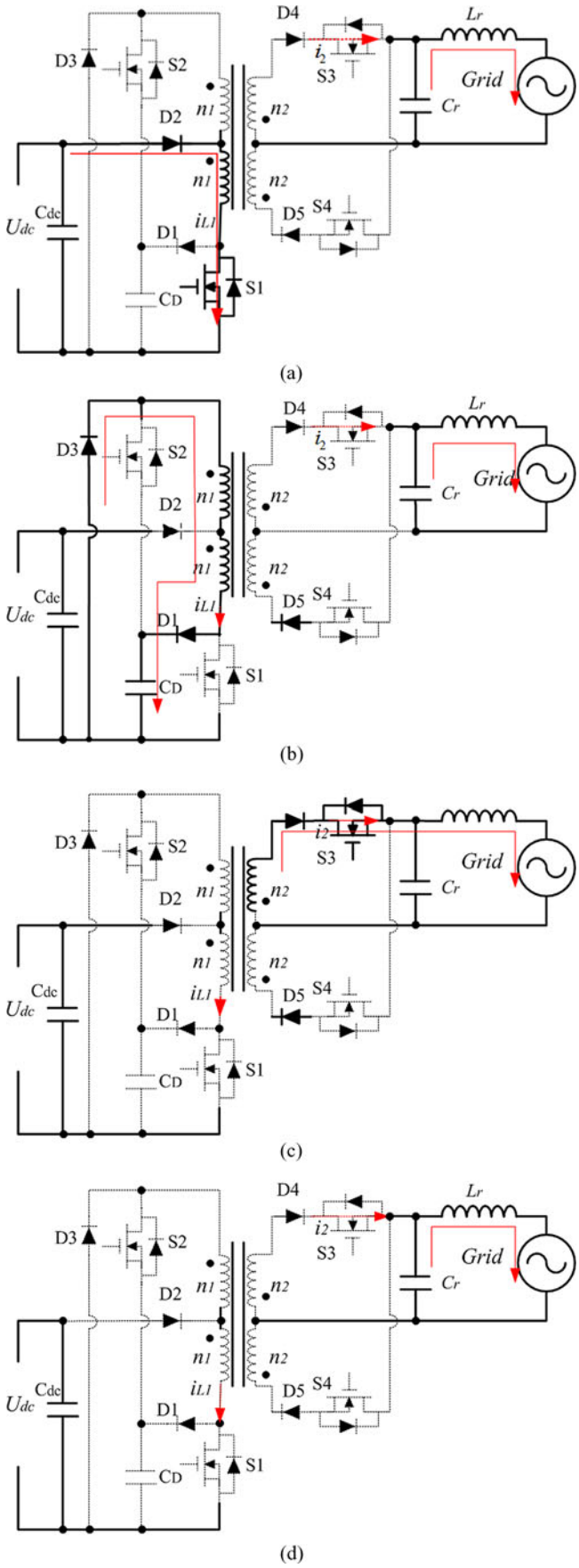

Fig. 5. Detailed circuit operation stages during mode-I. (a) Stage 1[t_0–t_1], (b) Stage 2[t_1–t_2], (c) Stage 3[t_2–t_3], and (d) Stage 4[t_3–t_4].

magnetizing inductance is exactly equal to the required energy to be pumped into the grid. At this instant, S_3 is turned ON to release the energy into the grid. As the power factor of single-stage inverter is assumed to be unity, the required value $i_{L1-\text{peak12}}$ can be calculated according to energy conservation law:

$$\frac{1}{2}(4L_{m1})i_{L1\text{-peak12}}^2 = T_S U I \sin^2\omega T_0 = 2T_S P_{\text{PV}} \sin^2\omega T_0 \tag{3}$$

where U and I are amplitudes of the grid voltage and the current injected into the grid, respectively, ω is the angle frequency of the grid voltage, and T_0 is the time instance. As seen from (3), the current $i_{L1\text{-peak12}}$ is varying with phase angle ωT_0, which can be expressed as follows:

$$i_{L1\text{-peak12}} = \sqrt{\frac{P_{\text{PV}}T_S}{L_{m1}}}\,|\sin\omega T_0|\,. \tag{4}$$

The peak current $i_{L1-\text{peak11}}$ is determined as given in (5) to maintain the PV power P_{PV} constant

$$i_{L1\text{-peak11}} = \sqrt{\frac{2P_{\text{PV}}T_S}{L_{m1}}}. \tag{5}$$

Now, the currents, $i_{L1\text{-peak11}}$ and $i_{L1\text{-peak12}}$, are determined. Then, the time duration for stages 1 and 2 can be easily calculated as follows:

$$\begin{aligned} D_1T_S &= L_{m1}\frac{i_{L1\text{-peak11}}}{U_{\text{dc}}} \\ D_2T_S &= 4L_{m1}\frac{i_{L1\text{-peak11}}/2 - i_{L1\text{-peak12}}}{U_C} \end{aligned} \tag{6}$$

Stage3[t_2–t_3]: During this stage, the current i_2 is released through one of the secondary windings and the corresponding ac switch, either S_3 or S_4, as shown in Fig. 5(c). The grid voltage during one switching period u_{ac} can be assumed to be constant; therefore, the current i_2 is expressed as follows:

$$i_2(t) = \frac{i_{Lm1\text{-peak12}}}{n_2/2n_1} - \left|\frac{u_{\text{ac}}}{L_{m2}}\right|(t-t_3) \tag{7}$$

where L_{m2} is the magnetizing inductance of the secondary side. As the current I reaches to zero at time t_3, the time duration D_3T_S can be calculated as follows:

$$D_3T_S = \frac{L_{m2}(2n_1 i_{L1\text{-peak12}}/n_2)}{|u_{\text{ac}}|}. \tag{8}$$

Substituting (4) and $u_{\text{ac}} = U_o\sin\omega t$ in (8). Then, the final D_3T_S expression is given in (9)

$$D_3T_S = \frac{L_3}{U_o}\sqrt{\frac{4P_{\text{PV}}T_S}{L_{m1}}}. \tag{9}$$

It is worth to mention that D_3T_S depends only on the PV power. Therefore, for a certain input power level, the duty ratio D_3 is constant for every switching period.

Stage4 [t_3–t_4]: As the current i_2 decreases to zero, this stage starts where all the switches are turned OFF, as shown in Fig. 5(d).The capacitor C_r and inductor L_r keep pumping energy to the grid, while the flux in the flyback transformer is reset. The duration time for this stage can be expressed as follows:

$$D_4T_S = (1 - D_1 - D_2 - D_3)T_S. \tag{10}$$

B. Mode II ($P_{\rm PV} < P_{\rm ac}$)

As the ac output power increases and becomes greater than the PV power, the topology enters the second operation mode (mode II). Fig. 4(b) shows the current waveforms and driving signals during this mode. Similar to mode I, mode II is also divided into four stages in one switching period. It is worth to mention that for this mode, the corresponding secondary side switch, either S_3 or S_4, is always ON (whether S_3 or S_4 is on depends on the polarity of grid ac voltage). Fig. 6 shows all the four circuit operation stages.

Stage1 [t_0–t_1]: This stage is quite similar to stage 1 in mode I. S_1 is turned ON, and the magnetizing inductance stores energy from PV panel through D_1, T_1, and S_1, as shown in Fig. 6(a). The magnetizing current ramps up linearly until it reaches $i_{L\text{-peak21}}$, as given in (11)

$$i_{L\text{-peak21}} = \frac{U_{\rm dc}}{L_{m1}} D_1 T_S. \tag{11}$$

To maintain constant power from PV panel, the peak current in this stage should be fixed as the input voltage from PV panel is assumed to be constant in the steady state. For a given input power $P_{\rm pv}$, the peak current $i_{L\text{-peak21}}$ is given in (5). Combining (11) and (5), the duration time $D_1 T_S$ is given as follows:

$$D_1 T_S = \frac{\sqrt{2P_{\rm PV} T_S / L_{m1}}}{U_{\rm dc}}. \tag{12}$$

Stage2 [t_1–t_2]: This mode starts when the magnetizing current reaches $i_{L\text{-peak21}}$. At that instant S_2 is turned ON, and all the diodes at the primary side are reversed biased, as it is shown in Fig. 6(b). As the magnetizing current in one primary winding is coupled into another primary winding during this stage, the magnetizing current $i_{L\text{-peak21}}$ will be halved. The energy stored in the decoupling capacitor C_D continues charging the new inductor with two windings in series as shown in Fig. 6(b), whose inductance is $4L_{m1}$. The new magnetizing current ramps up linearly until it reaches $i_{L\text{-peak22}}$, where the energy stored in the magnetizing inductance equals the required energy to be pumped into the ac side on the average basis of one switching period. Therefore, the peak current $i_{L\text{-peak22}}$ is given as follows:

$$i_{L\text{-peak22}} = 2\sqrt{\frac{P_{\rm PV} T_S}{L_{m1}}} \sin \omega t. \tag{13}$$

The ON-time for S_2 can be expressed as follows:

$$D_2 T_S = \frac{4L_{m1}\left(i_{L\text{-peak22}} - i_{L\text{-peak21}}/2\right)}{U_{cd}}. \tag{14}$$

Stage 3[t_2–t_3]: Once S_1 and S_2 are turned OFF simultaneously at t_3, the current at secondary side $i_2(t)$ is released through one of the secondary side, as shown in Fig. 6(c). Since the voltage ripple across the capacitor C_r during one switching period is negligible. Hence, its voltage can be assumed to be equal to the grid voltage $u_{\rm ac}$, and the current $i_2(t)$ is expressed as follows:

$$i_2(t) = \frac{2n_1 i_{L\text{-peak22}}}{n_2} - \frac{|u_{\rm ac}|}{L_{m2}}(t - t_2). \tag{15}$$

The duration time of this stage is similar to that of stage 3 in mode I given in (9).

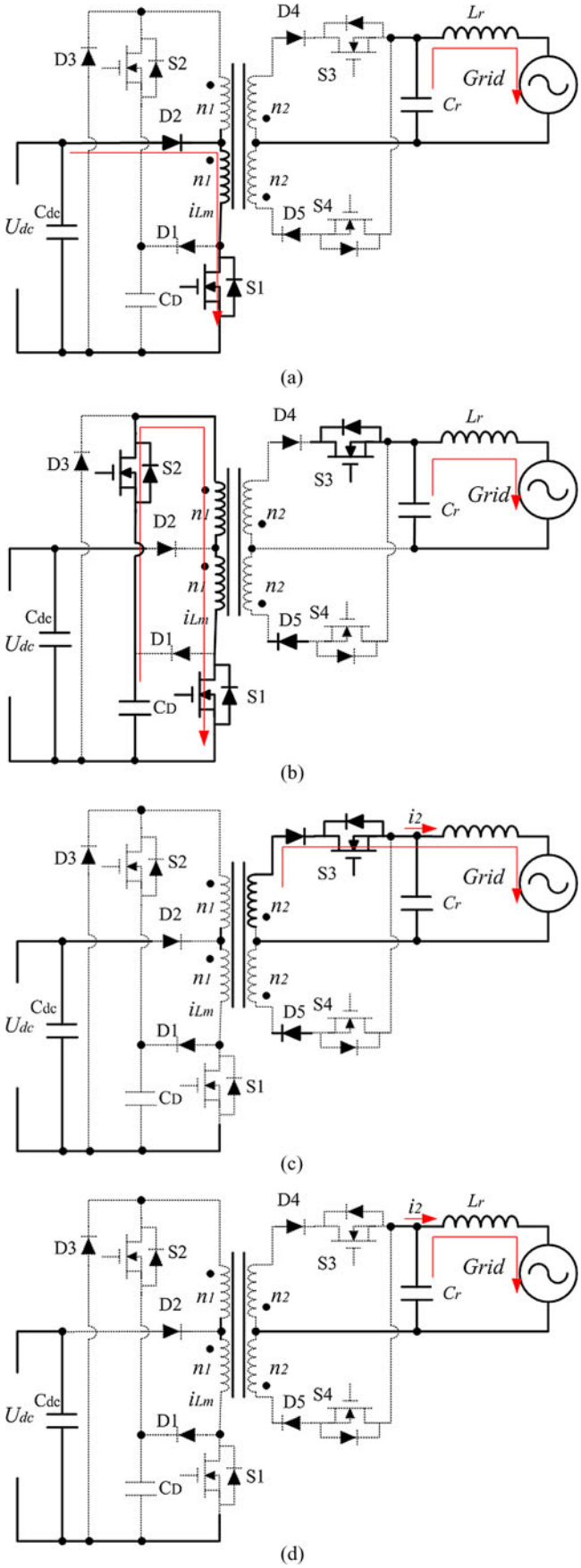

Fig. 6. Detailed circuit operation stages during mode II. (a)Stage 1[t_0–t_1], (b) Stage 2[t_1–t_2], (c) Stage 3[t_2–t_3], and (d) Stage 4[t_3–t_4].

Stage 4[t_3–t_4]: This stage is the same as stage 4 in mode I. No current flows through transformer windings, and the transformer is in magnetizing reset state. The output current is maintained by C_r and grid-tied inductor L_r, as shown in Fig. 6(d).

IV. Design Considerations

This section is dedicated to providing designing guidelines. Several nonidealities are taken in consideration, which make the design procedure to some extent a challenging.

A. Device Voltage Stress

As it was explained in Section III, the voltage across the decoupling capacitor C_D fluctuates at double line frequency, with a peak value of U_{peak_cd}. As a result, the voltage stress on S_1, S_2, D_1, and D_3 is U_{peak_cd}. When S_2 turns ON in mode II, D_2 is reversed biased. Hence, the blocking voltage is given as follows:

$$U_{D2\_\text{reverse}} = \frac{1}{2}U_{\text{peak-}cd} - U_{cd}. \tag{16}$$

The peak voltage stress on the D_4 or D_5 occurs when the output ac voltage is at its peak value U_{ac_peak} and S_2 is turned ON. The voltage stress is given as follows:

$$U_{D4\_\text{reverse}} = \frac{n_2 U_{\text{peak-cd}}}{2n_1} + U_{\text{ac\_peak}}. \tag{17}$$

S_3 and S_4 work alternatively at a half-line cycle basis. Suppose the converter operates in stage 3 (S_3 is ON and S_4 is OFF), the voltage across the secondary transformer's winding n_2 is clamped to grid voltage u_{ac}. This implies that the induced voltage across the secondary transformer winding, which is connected to S_4 is u_{ac} as well. Therefore, the voltage stress on S_4 is double grid voltage and the peak voltage stress is given as follows:

$$U_{S4} = 2U_{\text{ac\_peak}}. \tag{18}$$

B. Decoupling Capacitance Selection

As seen from Fig. 3, the energy being stored in or discharged from the decoupling capacitor during a half-line cycle can be calculated by integrating the area of mode I or mode II as follows:

$$\begin{aligned} E_{CD} &= 2\left(\int_0^{1/8f_{\text{grid}}} (P_{\text{PV}} - P_{\text{ac}}(t))dt\right) \\ &= \frac{1}{2}C_D(U_{cd\_\max}^2 - U_{cd\_\min}^2) \end{aligned} \tag{19}$$

where f_{grid} is the grid line frequency. The instantaneous ac output power p_{ac}, which includes the power pulsation with double line frequency, can be defined as follows:

$$P_{\text{ac}}(t) = u_{\text{ac}} i_{\text{ac}} = \frac{1}{2}U_o I_o(1 - \cos 2\omega t) \tag{20}$$

where $u_{\text{ac}} = U_o \sin\omega t$, and $i_{\text{ac}} = I_o \sin\omega t$.

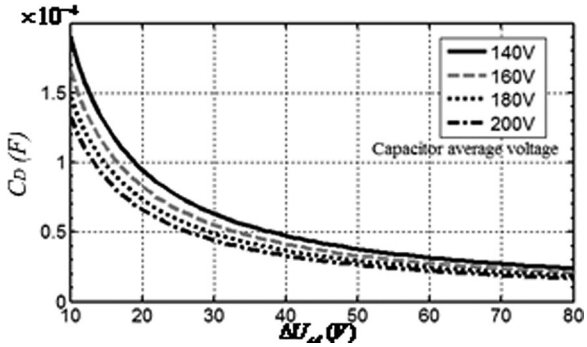

Fig. 7. Minimum decoupling capacitor (CD) versus the allowable ripple at different dc voltage level.

From (19) and (20), the required decoupling capacitance is found to be as follows:

$$C_D = \frac{P_{\text{PV}}}{\omega U_{cd\_\text{avg}} \Delta U_{cd}} \tag{21}$$

where

$U_{cd_\text{avg}} = \frac{1}{2}(U_{cd_\max} + U_{cd_\min})$an average dc voltage across C_D;

$\Delta U_{cd} = U_{cd_\max} - U_{cd_\min}$the voltage ripple across C_D.

From expression in (21), the decoupling capacitance is inversely proportional to the dc voltage, U_{cd_avg}, and voltage ripple ΔU_{cd}. Since other parameters in (21) (P_{PV} and ω) are fixed, the only way to change the decoupling capacitance value is by manipulating the former two parameters. A small capacitance can be achieved by increasing U_{cd_avg} or (and)ΔU_{cd}, so as to allow the long lifetime capacitors, such as film capacitor, to be used. Based on the aforementioned voltage stress analysis, it is worth to mention that a tradeoff decision has to be made between the voltage across the decoupling capacitor and the voltage stresses on the power devices. However, the minimal voltage across the decoupling capacitor must be greater than the voltage stress across S_1, which given as follows:

$$U_{s1\text{-stress}} = U_{\text{dc}} + \frac{n_1}{n_2}U_o \left|\sin(\omega_o t)\right|. \tag{22}$$

Otherwise, the energy stored in the primary side would damp into the decoupling capacitor.

Fig. 7 shows the relationship between the minimum required decoupling capacitor and the voltage ripple across its terminals at different dc voltage levels for a 100-W PV system.

C. Magnetizing Inductance Selection

The magnetizing inductance should be designed to be less than certain value so as a DCM operation is guaranteed. To maintain the DCM operation, the total duration time of all stages during mode I and mode II must satisfy the following constraint:

$$D1 + D2 + D3 < 1 \,\text{inModel} \tag{23}$$

Combining (6) and (9) and using the magnetizing inductance relationship between primary side and secondary side, $L_{m2} =$

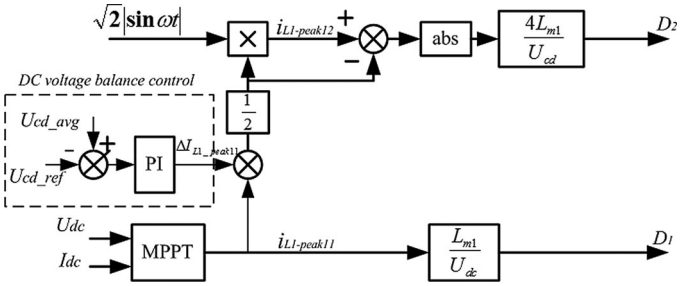

Fig. 8. Control diagram (mode I condition: $I_{\mathrm{ac\_ref}} <= I_{\mathrm{dc\_ref}}$; mode II: $I_{\mathrm{ac\_ref}} > I_{\mathrm{dc\_ref}}$).

$(n_2^2/n_1^2)L_{m1}$, then, the inductance L_{m1}, is given as follows:

$$L_{m1} < \frac{\sqrt{T_S/P_{\mathrm{PV}}}}{((\sqrt{2}/U_{\mathrm{dc}}) + (\sqrt{2} - |\sin\omega t|/U_{cd}) + (2n_2^2/U_o n_1^2))}. \tag{24}$$

D. Predictive Control Strategy

Fig. 8 shows the block diagram of the prediction diagram. According to the expressions (6), (12), and (14), the duty cycles D1 and D2 can be easily calculated out if the PV input voltage U_{dc}, decoupling capacitor's voltage U_{cd}, and the currents $i_{L1\text{-peak11}}$ and $i_{L1\text{-peak12}}$ are known. As for U_{dc} and U_{cd}, they can be easily obtained through voltage sensing, while $i_{L1\text{-peak11}}$ is achieved by the MPPT system through sensing U_{dc} and PV input current I_{dc}, and ac current reference $i_{L1\text{-peak12}}$ can be calculated using the dc current $i_{L1\text{-peak11}}$ based on the power balance law as follows:

$$I_{L1\text{-peak12}} = \frac{\sqrt{2}}{2}|\sin\omega t|\, I_{L1\text{-peak11}}. \tag{25}$$

However, due to the power losses and the existence of nonideal factors such as leakage inductance in the power conversion stage, expression (25) will not be valid in a real power conversion. To make power balanced among these three ports, a dc voltage balance control block is introduced as shown in dashed block in Fig. 8. The detailed explanation of this block will be presented in following Section IV-F.

The duration time D_1 is controlled in order to convert the pure dc power from PV source; while the duration time D_2 is controlled to generate the ac current at the output side. One thing should be mentioned that the control scheme is derived based on the assumption that the grid voltage is pure sinusoidal. When the grid voltage has some distortion, it will affect the total harmonic distortion (THD) of the injected ac current if the $i_{L1\text{-peak12}}$ is still calculated using expression (25). To mitigate the affect of the distorted grid voltage, the grid voltage is introduced based on the expression (3) to generate the current $i_{L1\text{-peak12}}$ as follows:

$$i_{L1\text{-peak12}} = \sqrt{\frac{T_S u_{\mathrm{ac}} I \sin\omega T_0}{2L_{m1}}} \tag{26}$$

where u_{ac} is the grid voltage and I is the amplitude of the current injected to the grid.

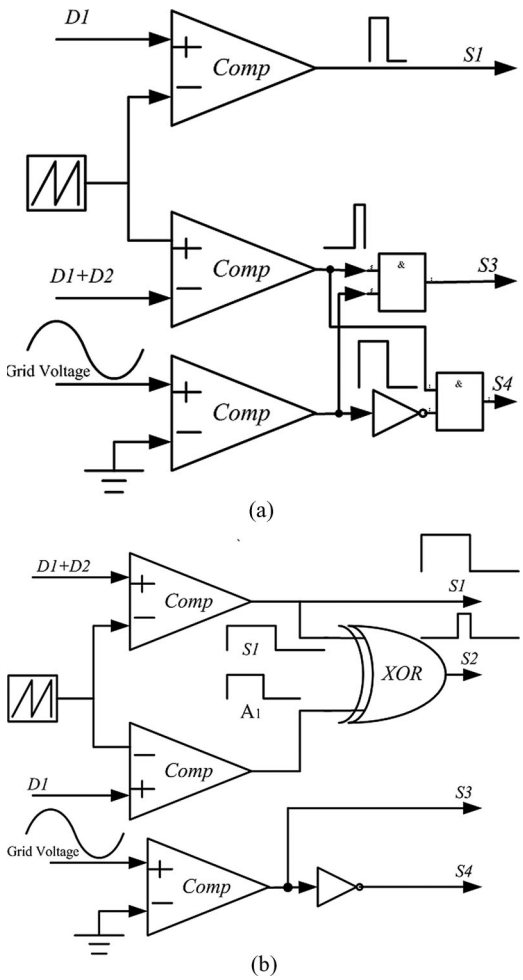

Fig. 9. PWM signal generation logic. (a) PWM signals for mode I and (b) PWM signals for mode II.

E. Generating Pulsewidth Modulation Signals

As described in Section D, the duration times can be estimated using predictive control. Fig. 9 shows the pulsewidth modulation (PWM) signal generation process for all switches. The choice of *S*3 or *S*4 depends on the polarity of the grid voltage; when the grid voltage is positive, the *S*4 is OFF, and the *S*3 is always ON in mode II and is switching in mode I. While the grid voltage is negative, the functions of *S*3 and *S*4 are completely exchanged.

F. Power Balance Control

Assuming a lossless system, the input power will be equal to the ac output power. In this ideal case, the average voltage across the decoupling capacitor will be balanced automatically, and thus, no control is required to stabilize the decoupling capacitor voltage. However, there are different kinds of losses associated with the power conversion. These losses, such as conduction losses, switching losses, and leakage energy within the transformer, are introduced. These losses should be taken in consideration during the design procedure in order to guarantee all specifications and standards. To study the effect of the leakage energy on the decoupling capacitor's voltage, the power

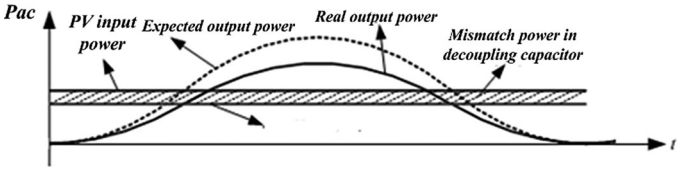

Fig. 10. Input power and output power mismatch with considering of leakage inductance.

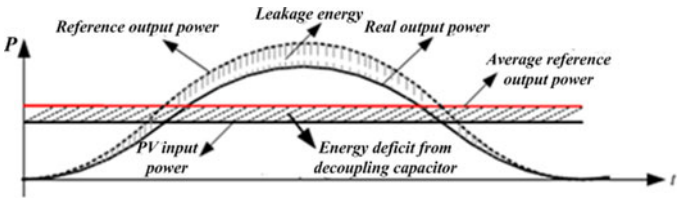

Fig. 11. Input power and output power balance control considering the leakage energy.

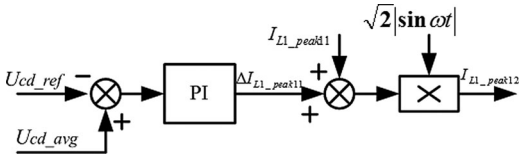

Fig. 12. Balanced decoupling capacitor's voltage control strategy.

conversion losses (conduction and switching losses) is ignored. Fig. 10 shows that with the existence of the leakage energy, the output power is less than the expected one. This amount of mismatch, shown in Fig. 10, will be stored in the decoupling capacitor. This leads to the continuous increase of the decoupling capacitor's voltage, thus resulting in a failure mode.

To prevent this failure mode, an additional control loop is required to keep the decoupling capacitor's voltage stable. This control loop aims to transfer the leakage energy into ac side, and prevent it from being accumulated in the decoupling capacitor. One simple way is to increase the reference output power, namely, the ac current, $I_{\mathrm{ac\_ref}}$, as shown in Fig. 11. If the reference output power is increased and the input power from PV source remains the same, this introduces an energy deficit between input power and reference output power, which has to be supplied from the decoupling capacitor. If this energy deficit equals to the leakage energy, the input power and output power will be balanced, and thus, the voltage across the decoupling capacitor will be stable as well. Based on this principle, the control strategy for balancing decoupling capacitor's voltage can be given as shown in Fig. 12.

G. Loss Calculation

The following are the components and mechanism contributing to the main power losses during normal operation:

1) conduction losses;
2) gate driving losses;
3) switching losses;
4) reverse recovery losses; and
5) core losses.

TABLE II
KEY CIRCUIT'S PARAMETERS

Circuit parameters	Values
Input voltage	60V
Grid voltage	110V ac
Nominal power	100W
Switching frequency	50kHz
Decoupling capacitor C_D	46uF
L_r	3mH
C_r	1uF
Transformer turn ratio	1:1:2.5:2.5
Magnetizing inductance L_m	20uH
Leakage inductance	0.5uH:0.5uH:3uH:3uH(1:1:2.5:2.5)

In this paper, a mathematical model for power loss calculation using the data-sheet parameters is used. As for the conduction losses, the current for each component can be easily obtained based the equations in the Section III, and thus, the conduction losses can be calculated out simply. The gate driving losses consist of two parts: one is the quiescent power supplies for the MOSFET gate driver, which can be easily achieved through direct measurement. The other is caused by charging or discharging the MOSFET input capacitance (Ciss). This part of the gate driver losses can be calculated using gate charge. As for the switching losses, for simplicity we assume the switching process is linear. In this way, the switching losses can be calculated through the current and voltage across the switches during ON and OFF-transients. Since the converter operates in discontinuous current mode, there are no reverse recovery losses in diodes *D*3 and *D*4. With regard to diodes at primary side, due to low voltage stress, Schottky diodes are chosen so that the reverse recovery losses at primary side are negligible. Core loss can be estimated using loss figures offered by the core manufacturer.

Besides the aforementioned losses, the losses caused by the parasitic capacitors of MOSFETs should be taken into account. During stage 2 of mode I as shown in Fig. 5(b), when *S*1 turns OFF and *S*3 or *S*4 is still OFF to block the current releasing to the secondary side. However, due to the existence of the parasitic capacitors C_{oss} of the MOSFET *S*3 and *S*4, at the time when *S*1 turns OFF, the magnetizing current will be released to the secondary side to charge the parasitic capacitor of *S*3 or *S*4, which may incur current spikes in this stage. The energy charged to the parasitic capacitor will be damped in *S*3 or *S*4 when it turns ON, whose losses can be simply calculated using$(1/2)C_{oss}V^2$ According our calculation, the calculated efficiency is almost 1.5% higher than that obtained in the experiment.

V. SIMULATION

The PSIM software is used to simulate the proposed topology and control strategy. The key circuit's parameters are listed in Table II.

Fig. 13 shows the simulation waveforms of the proposed converter. As seen from Fig. 13, the peak current from the PV source remains constant, which means the input power is constant. The envelope of the current i_2 in the secondary side is sinusoidal, resulting in pure ac current injected into the grid with unity power factor. The voltage ripple on the decoupling capacitor fluctuates

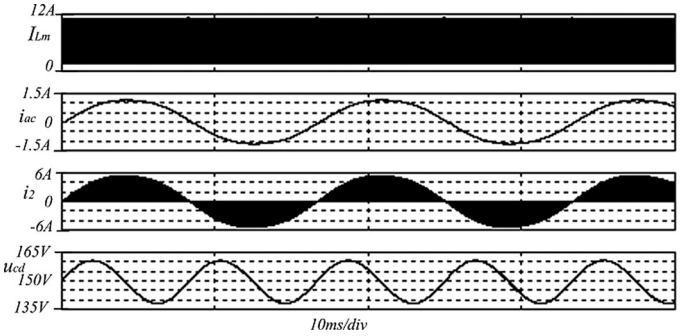

Fig. 13. Key waveforms.

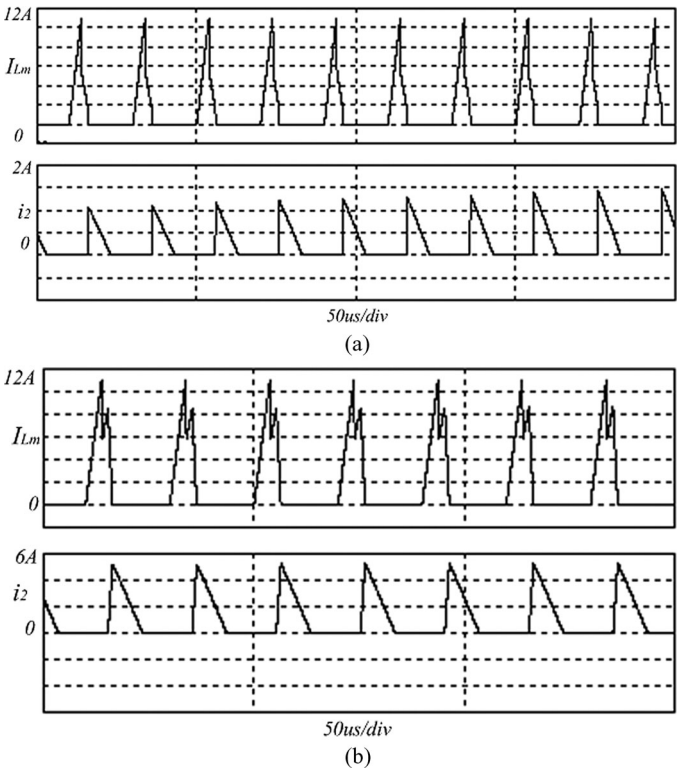

Fig. 14. Current waveforms in both modes: (a) mode I and (b) mode II.

at double line frequency, and its average voltage stays constant because of the power balance control strategy.

Fig. 14 shows the detailed current waveforms both at primary side and secondary side in mode I and II. In mode I, when S_1 is turned ON, the primary current increases linearly. As the current reaches peak value $i_{l1\text{-peak11}}$, S_1 is turned OFF. The primary current will be reduced to half by coupling it to another primary winding, then, it will decrease linearly by releasing the current to the decoupling capacitor through D_1 and D_3. As the primary current i_{Lm} decreases to the ac reference current $i_{\mathrm{ac\_ref}}$, S_3 or S_4 will be turned ON, transferring the current from the primary side to the secondary side. The only difference between mode I and mode II is in the second stage, where in mode II the primary current increases by turning ON S_2, and continuously charges the primary magnetizing inductor.

TABLE III
CIRCUIT'S PARAMETERS

Symbols	Values
S_1&S_2	STB50N25M5
D_1	STPS20170CFP
D_2	STTH3R06S
D_3	CSD0460
D_4&D_5	STTH3R06S
S_3&S_4	STF25NM50N
Transformer	RM14(3C95)
L_{m1}	20.3uH
C_D	2x23uF

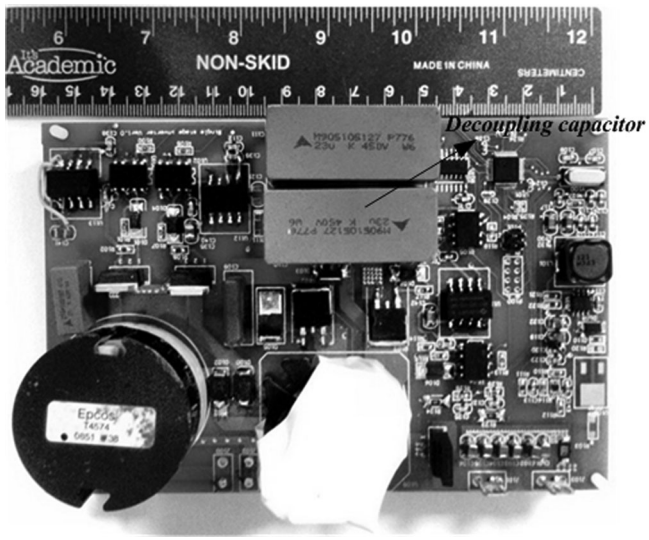

Fig. 15. 100-W prototype

VI. EXPERIMENTAL RESULTS

A 100-W, 110-V ac output prototype was built to verify the validity of the proposed topology. The prototype is shown in Fig. 15. All the control is implemented in a microprocessor (STM32F103). The circuit's parameters for the prototype are listed in Table III.

Before the converter pumps energy to the grid, the voltage across the decoupling capacitor has to be established first. By turning OFF *S*2, *S*3, and *S*4 and switching *S*1 at 10% duty cycle, the decoupling capacitor is charged. When the voltage across the decoupling capacitor is charged to 150 V, the converter ends its precharging stage and is switched to normal operation pumping energy to the grid.

Fig. 16 shows the driver signals and current waveforms in both primary side and secondary side for both modes. In mode I, when the switch *S*1 turns OFF, the energy stored in magnetizing inductor is released to the decoupling capacitor. Magnetizing current decreases until switch *S*3 turns ON, at which time the energy in the magnetizing inductor will be released to the transformer's secondary side. In mode II, the magnetizing current is further charged by turning ON switch S2 and the energy will be released to the secondary side by turning OFF switches *S*1 and *S*2. The voltage ripple across the decoupling capacitor,

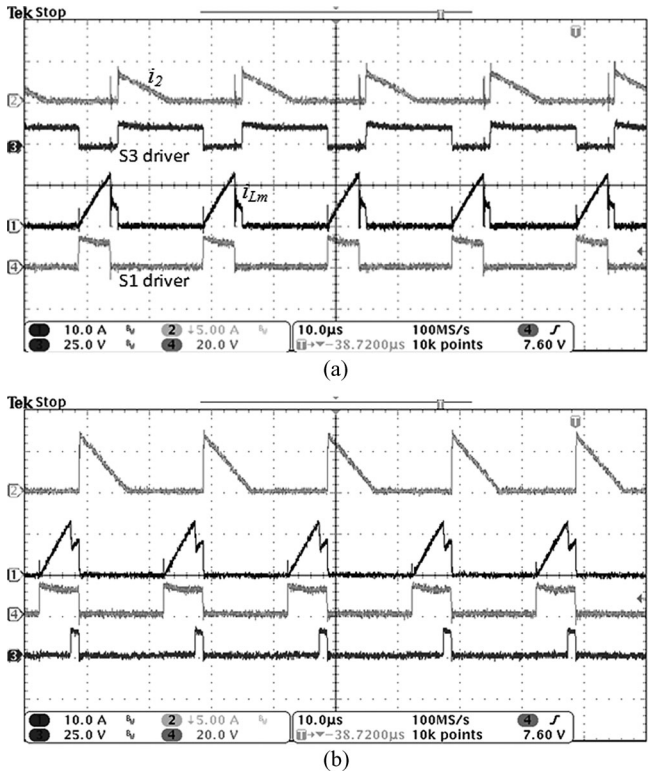

Fig. 16. Driver signals and current waveforms: (a) mode I and (b) mode II.

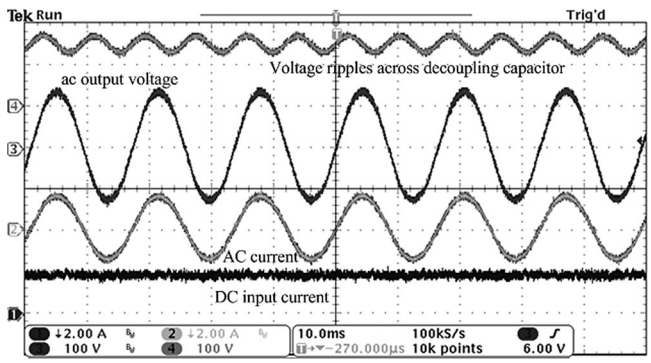

Fig. 17. Current and voltage waveforms

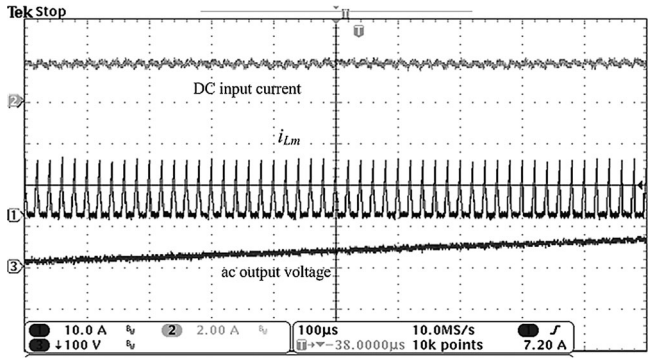

Fig. 18. DC input current and magnetizing current at primary side

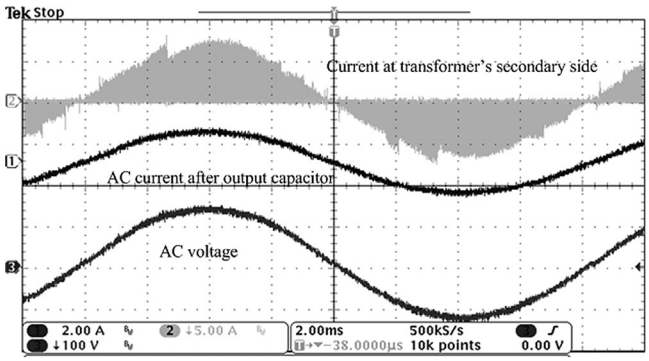

Fig. 19. Currents and voltage at secondary side.

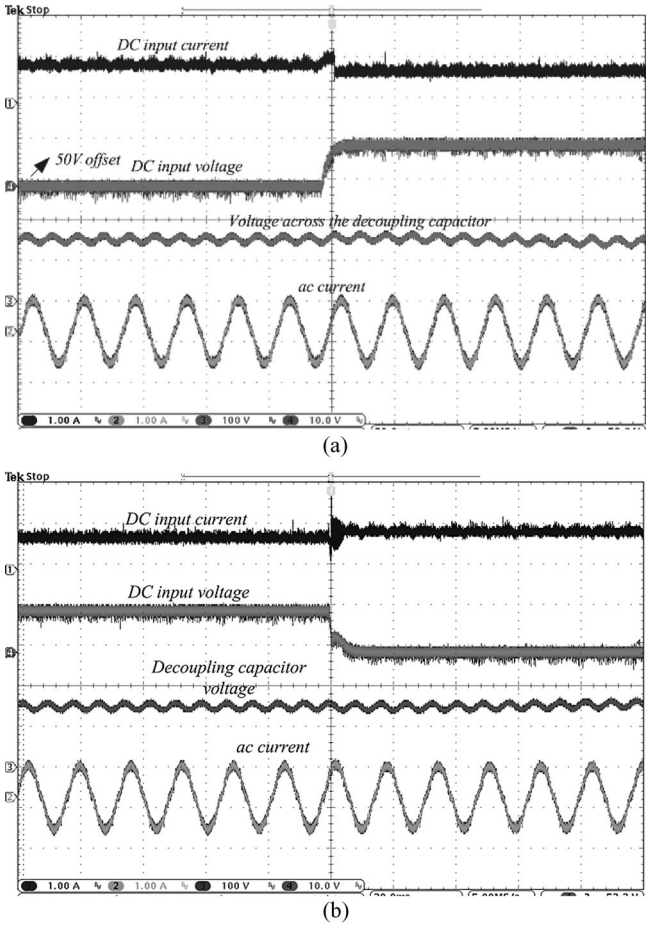

Fig. 20. Dynamic performance as the input voltage changes. (a) Input voltage changes from 50 to 60 V and (b) input voltage changes from 60 to 50 V.

output ac voltage, ac current, and the input current from PV panel are shown in Fig. 17. The voltage ripple, having double line frequency, fluctuates according to charging and discharging process. According to expression (21), the voltage ripple should be 42 V (peak to peak, 110 W), which matches the experimental result (41 V). As seen in Fig. 17, the dc voltage across the

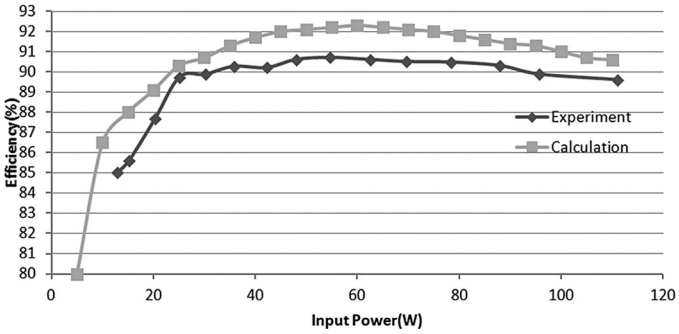

Fig. 21. Measured and calculated efficiency curves at 60-V input voltage.

decoupling capacitor is well regulated to 150 V, which verify the proposed power balance control strategy. The input current is almost constant, only having high-frequency ripples caused by switching frequency, which verifies the proposed power decoupling technique. Fig. 18 shows the peak magnetizing current and dc input current, which indicates that the input power is constant. Fig. 19 shows the peak current at transformer's secondary side, whose envelop is sinusoidal and the current after output capacitor filter is a sinusoidal waveform with THD less than 1.7%. The experimental waveforms match the simulation results pretty well. Fig. 20 shows that when the input voltage suddenly changes from 50 to 60 V the input current decreases and the output ac current keeps same to maintain both the input and the output power constant, which verifies the effectiveness of the predictive control strategy. Both the calculated and the measured efficiency curves under 60-V input voltage are plotted in Fig. 21. As shown in Fig. 21, the calculated efficiency curve, whose peak efficiency reaches 92.3%, is slightly higher than the experimental one 90.6%, which includes the control and driving power. All the efficiency data were measured by a power analyzer PZ4000.

VII. Conclusion

A new microinverter topology is proposed. It primarily aims for the ac-module PV systems. The proposed topology employs a new power decoupling technique where a small film capacitor can be used instead of an electrolytic capacitor. Hence, it will have a long lifespan comparable to the PV panel. The transformer leakage energy is handled by the decoupling circuit itself so there is no need for additional dissipative circuits, which leads to reduced power losses and improved efficiency. The experimental results show that the proposed topology achieves good efficiency, while realizing the power decoupling.

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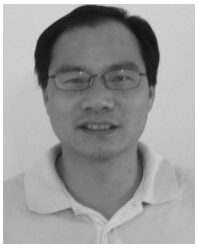

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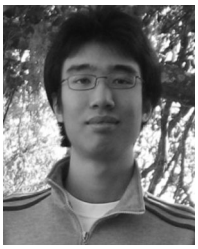

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