A Universal Adaptive Driving Scheme for Synchronous Rectification in LLC Resonant Converters

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***Abstract*—In this paper, a universal adaptive driving scheme for synchronous rectification (SR) is proposed. The drain to source voltage of the synchronous rectifier is sensed so that the paralleled body diode conduction is detected. Using the proposed SR driving scheme, the SR turn-OFF time is tuned to eliminate the body diode conduction. The SR gate driving signal can be tuned within all operating frequency regions. Moreover, a simple digital implementation is introduced. Compared with analog ones, it enables more intelligent and precise SR control, improving converter efficiency. For rapid prototyping purposes, the digital SR tuning system is realized in Cyclone III field-programmable gate array (FPGA).**

***Index Terms*—Digital control, LLC resonant converter, synchronous rectification (SR).**

I. Introduction

THE LLC resonant converter is becoming more and more popular for its high efficiency, because of both zero-voltage switching for the primary-side main switches and zero-current switching (ZCS) for the secondary-side rectifiers [1]. To further improve the efficiency, the synchronous rectifiers (SR) are employed, since the conduction loss is much lower than that of the diode rectifiers. However, the efficiency optimization depends on the well adjustment of SR gate driving signals. Today, with the explosive increase in consumer electronics and IT equipment, the demand for high-power-density converters is growing. Thus, the LLC resonant converter is required to operate at high frequencies. As a result, the SR driving scheme for the LLC resonant converter becomes tough.

Fig. 1 shows the LLC resonant converter with SR on the secondary side. Presently, there have been proposed several SR driving schemes [2]–[8].

One solution [2] is sensing secondary side current $i_{\rm SEC}$ to generate SR gate driving signal. This method is precise, but due to the large current on the secondary side, it requires a large size current transformer and it presents a lower efficiency due to the extra resistance of the transformer windings.

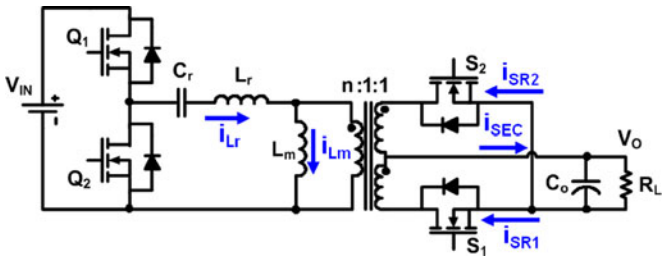

Fig. 1. LLC resonant converter with the synchronous rectification.

An alternative solution [3] is sensing current through the transformer's primary side winding. Provided that the resonant inductor L_r and the magnetizing inductor L_m are external to the main transformer, the current though primary side winding is a precise replica of the secondary side current. Although a smaller loss could be achieved when compared to the secondary side current sensing, three magnetic components are needed, losing the integration of leakage, magnetizing inductors, and transformer into one single element.

In [4], the authors proposed a primary side resonant current i_{Lr} sensing method to determine the SR gate driving signals. However, it needs to decouple the magnetizing current i_{Lm}, and thus complicated auxiliary circuit is added.

A promising driving method is based on sensing the SR drain to source voltage $V_{ds\rm SR}$. The sensed $V_{ds\rm SR}$ is processed by the control circuits as follows [5]:

1) before the SR is turned ON, the paralleled body diode conducts shortly and there is a large forward voltage drop, which is compared with a threshold voltage $V_{\rm th\_on}$ to turn ON the SR;
2) when the SR current is decreasing toward zero, $V_{ds\rm SR}$ also becomes small, which is then compared with another threshold voltage $V_{\rm th\_off}$ to turn OFF the SR.

However, the accuracy of this driving scheme is highly affected by the SR package [6], [7]. Due to the inevitable package inductance, the sensed terminal drain to source voltage of the SR is actually the sum of the MOSFET's ON-status resistive voltage drop and the package inductive voltage drop, which deviates greatly from the purely resistive voltage drop of the MOSFET as the switching frequency increases. Therefore, the actual SR drive signal $V_{gs\rm SR}$ is significantly shorter than the expected value.

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To compensate for the inductive characteristic of the sensed V_{dsSR}, a carefully designed capacitive network can be connected to the sensed terminals [7]. However, the package inductance L_{SR} and the pure resistor R_{ds_on} need to be determined in advance to calculate the parameters of the components: C_{CS} and R_{CS} in the capacitive network. Although the inductive phase lead influence is diminished, the design and the parameter tuning process are time consuming.

Different from the aforementioned V_{dsSR} sensing, in [8], the SR body diode forward voltage drop is detected to tune the gate driving signal. If the body diode conducts, the large forward voltage drop is sensed by the valley detection circuit; then V_{gsSR} pulse width increases accordingly. Finally, the SR is tuned until the circuit cannot detect the body diode conduction. However, the maximum pulse width of the SR driving signal cannot be larger than that of the main switch, and thus, the SR cannot be tuned within all operating frequency regions. Moreover, the design procedure of the analog compensator to generate V_{gsSR} is complicated.

Recently, the digital control has begun to be widely used, since it enables more intelligent power management. This is also happening with the SR. The authors in [9]–[13] have demonstrated that the digital implementation can tune the SR gate driving signals more precisely in synchronous buck converters.

This paper proposes a universal adaptive solution for the SR driving scheme based on measuring V_{dsSR} of the synchronous rectifier, extending the digital solution proposed in [13] for synchronous buck converters and analog solution [8] for LLC resonant converters. This approach can tune the SR gate driving signal V_{gsSR} well within all switching frequency regions. The digital implementation is rather simple, requiring short tuning time and low-complexity digital logics. The transient behavior due to the switching frequency variations is also analyzed and experimentally verified.

The paper is organized as follows. Section II describes the universal adaptive SR solution; Section III analyzes the SR transient performance; and finally, Section IV reports the implementation and the experimental performance obtainable with the proposed solution.

II. Universal Adaptive SR Driving Scheme

The desired SR gate driving signals for the LLC resonant converter are shown in Fig. 2. In different switching frequency regions, when the primary main switches Q_1 and Q_2 are turned ON, the secondary side current i_{SEC} starts to go through the SRs, thus the SRs should be turned ON synchronously with the main switches. However, the turn-OFF times of the SRs and the main switches are not exactly in phase. When operating below the resonant frequency ($f_s < f_0$), the SR should be turned OFF earlier than the main switch. Otherwise, the SR would conduct circulating energy, namely a reverse current from the load to the source, thus producing a greater increase in the RMS currents and turn-OFF current, and causing efficiency to deteriorate dramatically. When operating above the resonant frequency ($f_s > f_0$), the SR should be turned OFF a bit later than the main switch. Otherwise, the sharply decreased current would

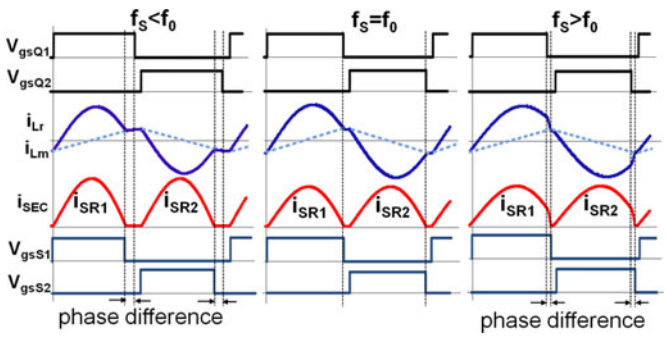

Fig. 2. Desired SR gate driving signals in different switching frequency regions.

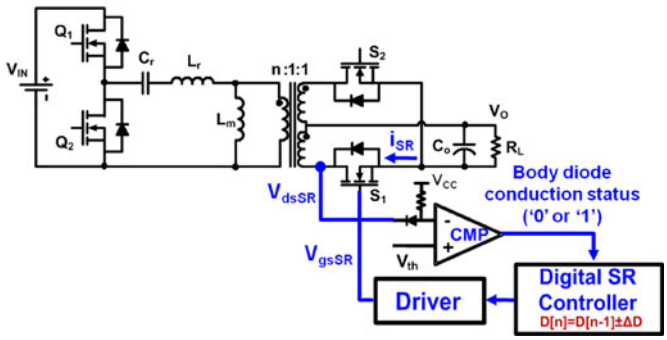

Fig. 3. Control blocks of proposed universal adaptive SR driving scheme.

go through the paralleled body diode, resulting in a serious reverse recovery.

To well tune the SR gate driving signal within all switching frequency regions, the universal adaptive driving scheme is proposed as shown in Fig. 3. The turn-ON time of the SR is the same with the primary main switch, but the turn-OFF time is digitally tuned based on the sensed SR drain to source voltage V_{dsSR}. When the SR is turned OFF, the body diode conduction is detected by a comparator (CMP), since its forward voltage drop is much larger when compared with the MOSFET's ON-status resistive voltage drop. If the body diode conducts, the SR pulse width is increased in the next switch cycle; if not, the SR pulse width is decreased. Thus, the SR gate driving signal is digitally tuned to eliminate the body diode conduction.

The main waveforms are also reported in Fig. 4. The sensed V_{dsSR} is compared with the threshold voltage V_{th} at every turn-OFF moment, and then the compared result is sent to the digital logics. If body diode conducts, the comparator (CMP) output is high (1). As a consequence, the SR pulse width is increased in order to reduce the body diode conduction time. When the comparator output is low (0), there is no body diode conduction and the SR is considered to be tuned. Since it is not possible to detect when the SR pulse width is larger than needed, when the comparator output is low, the SR duty is decreased by ΔD. Finally, the tuning algorithm alternates between the conditions reported in Fig. 4(c) and (d).

When $f_s > f_0$, if the SR is turned OFF earlier, the sharply decreased current will go through the body diode, producing a serious reverse recovery. However, with the proposed method,

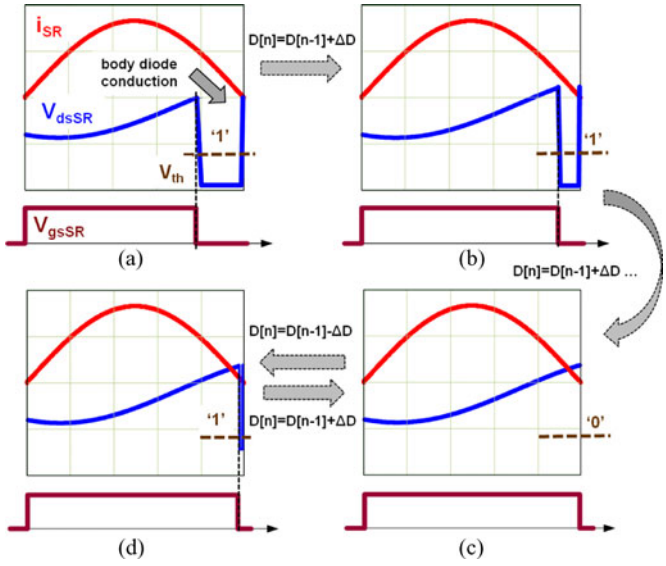

Fig. 4. SR turn-OFF tuning process to eliminate the body diode conduction.

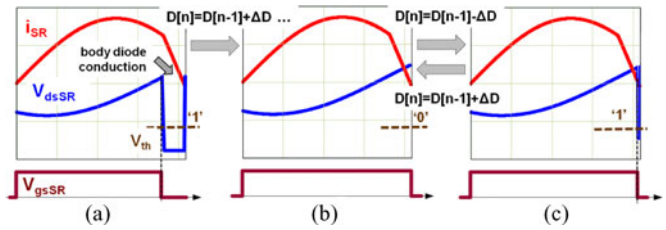

Fig. 5. SR turn-OFF tuning process when $f_s > f_0$.

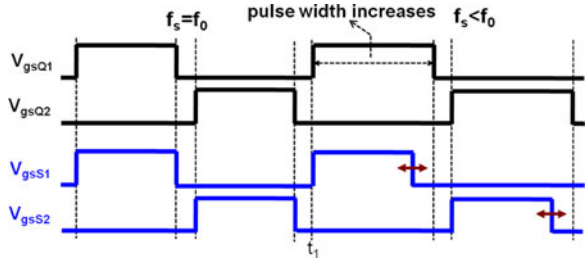

Fig. 6. Transient process as f_s decreases.

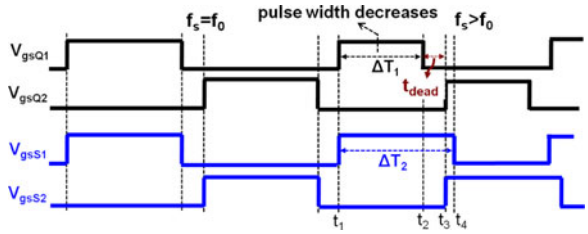

Fig. 7. Transient process as f_s increases.

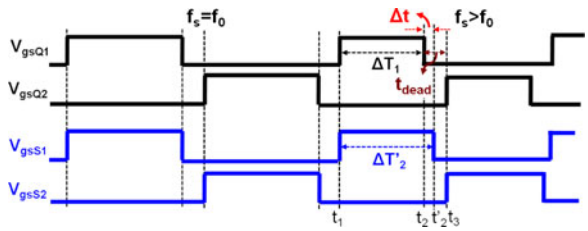

Fig. 8. SR pulse width limitation to avoid shoot-through when f_s increases.

if a high time resolution is employed to sense the CMP output, the body diode conduction status could also be detected as well. Therefore, Fig. 5 shows that with the same process described earlier, the SR could be tuned well; to even $f_s > f_0$ region.

As a summary, with the proposed universal adaptive SR driving scheme by minimizing the paralleled body diode conduction, the SR gate driving signal could be tuned within all operating frequency regions for the LLC resonant converter.

III. SR Transient Performance Investigation

In the LLC resonant converter, the regulation of the output voltage is obtained by switching frequency variations. When the input voltage and load change slightly, the corresponding switching frequency f_s changes in the vicinity of resonant point f_0, assuming that this is the designed point at the nominal condition. During the holdup time, the input voltage decreases rapidly; accordingly, f_s decreases with a similar speed to obtain a high gain. During over current protection or the constant current limitation process, f_s increases quickly from a normal operating point to above the resonant frequency region. Therefore, it is important to verify that during all these transient conditions there is no shoot-through. For such purposes, the transients associated with switching frequency variations are hereafter described.

Let us start with an f_s decrease at time t_1 as shown in Fig. 6, that is, the pulse widths of main switch signals V_{gsQ1} and V_{gsQ2} increase. For $f_s < f_0$, the SR current goes to zero earlier than the turn-OFF time of V_{gsQ1} and V_{gsQ2} shown in Fig. 2. If the SR gate driving signal is tuned fast, the SR is turned OFF earlier than the main switch. Even if the SR tuning process is slower, the SR is still turned OFF earlier, since the pulse widths of V_{gsQ1} and V_{gsQ2} have increased. In both cases, there is no shoot-through.

Fig. 7 shows the case when f_s increases at time t_1, that is, the pulse widths of the main switch gate driving signals V_{gsQ1} and V_{gsQ2} decrease. If the SR tuning process is slow, as shown in Fig. 7, this means that the SR does not response to the increased switching frequency. If

$$\Delta T_2 > \Delta T_1 + t_{\text{dead}} \tag{1}$$

from t_3 to t_4, main switch Q_2 starts to conduct, but synchronous rectifier S_1 is still ON. As a result, there will be a shoot-through between the main switch and the SR. Therefore, some protections should be designed to avoid shoot-through when f_s increases but SR does not respond quickly enough to follow the frequency variation.

The provision that has been adopted is to limit the pulse width of the SR driving signal as shown in Fig. 8: if (1) is satisfied, the actual SR pulse width is limited to $\Delta T'_2$

$$\Delta T'_2 = \Delta T_1 + \Delta t. \tag{2}$$

As shown in Fig. 2, since it is above the resonant frequency region ($f_s > f_0$), the SR should be turned OFF slightly later

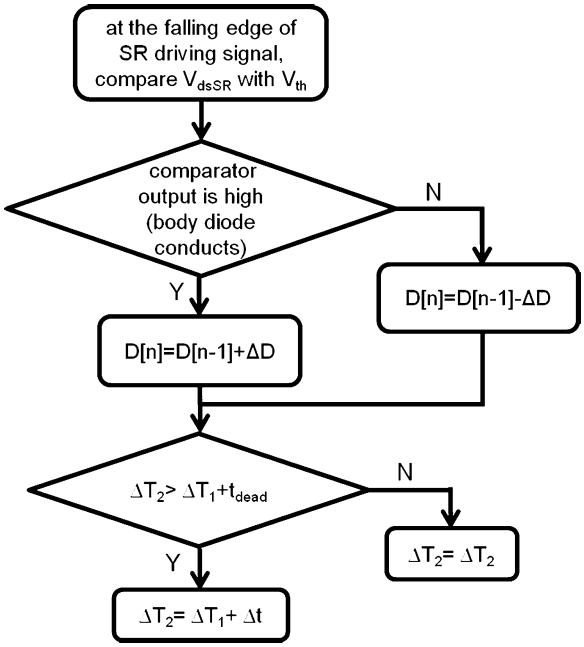

Fig. 9. Control flowchart of the proposed SR tuning process.

than the primary main switch, thus Δt is added as the delayed turn-OFF time. In order to avoid shoot-through, Δt should be designed smaller than the dead time $t_{\rm dead}$.

Sum up, Fig. 9 shows the flowchart of the proposed algorithm implemented in the digital logics. ΔD represents the time resolution of digital pulse width modulator [14], [15], which should be as small as possible to precisely tune the SR turn-OFF moment.

IV. Implementation and Experimental Results

The experiment is carried out on a 300-W half bridge LLC resonant converter prototype, whose input voltage is 400 V, output voltage is 12 V. The main converter parameters are shown in Table I. Fig. 10 shows the field-programmable gate array (FPGA) development kit, the LLC power stage, and the comparator board. The comparator board is plugged on the secondary side of the half bridge LLC resonant converter, comparing SR drain to source voltage $V_{ds\rm SR}$ with the threshold voltage $V_{\rm th}$ to determine the body diode conduction. Being a closed-loop system, the delay time produced by the comparator, FPGA, and driver are compensated by the tuning algorithm.

Even if the application is targeted to IC integration, for rapid prototyping purposes the SR controller is built in ALTERA Cyclone III FPGA [16] using the Verilog HDL. The maximum clock frequency insider the FPGA is set to be 250 MHz, thus the time resolution ΔD is 4 ns. After the estimation, there are about 700 logic gates built in the FPGA.

The SR turn-ON moment is the same with the primary main switch, but the turn-OFF time is tuned by the proposed universal adaptive driving scheme.

Fig. 11 shows that during SR ON status, the voltage drop is much smaller than the body diode forward voltage drop, since the ON-status resistor $R_{ds\_\rm on}$ is very small. At time t_1, SR is

TABLE I
Parameters of LLC Resonant Converter

Designed parameters	Parameters Value
Input voltage	400V
Output voltage	12V
Resonant capacitor	10nF
Resonant inductor	5.6μH
Transformer leakage inductor	2.1μH
Transformer magnetizing inductor	100μH
Transformer turns ratio	17:1:1
Primary side main switch	2×STB11NM60ND
Secondary side SR	2×BSC017N04NS
Output capacitor	440μF

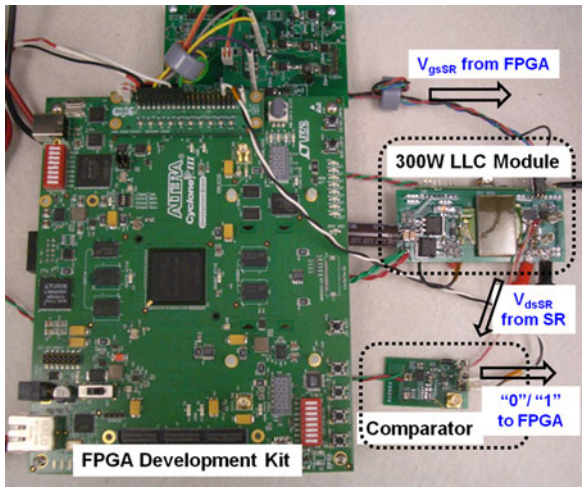

Fig. 10. Hardware implementation photograph.

turned OFF, and $V_{ds\rm SR}$ drops due to the body diode conduction, which is then compared with a threshold voltage $V_{\rm th}$. Thus, the comparator (CMP) output $V_{\rm CMP}$ is high when body diode conducts.

Fig. 12 shows that after the tuning process, the SR paralleled body diode conducts for a very short time. The comparator output is "0," "1," ... alternately, which demonstrates that the SR gate driving signal is always in the tuning process.

Within different operating frequency regions, the SR gate driving signals are not in phase with the main switches. When the switching frequency is below the resonant frequency ($f_s < f_0$), as shown in Fig. 13, the SR is turned OFF earlier than the primary main switch. The time difference between two gate driving signals is Δt_1. When the switching frequency becomes even lower, the time difference becomes much larger ($\Delta t_2 > \Delta t_1$) shown in Fig. 14. This verifies the reason why the commercial SR controllers for the synchronous buck converters cannot be used in the LLC resonant converter. Since there is large time mismatch between SR and main switch gate driving signals.

Fig. 15 shows that when $f_s = f_0$, the SR is tuned to be turned OFF at the same time as the main switch. Since only at the resonant frequency point, there is almost no phase difference between the SR and primary main switch gate driving signals.

When $f_s > f_0$, the SR turn-OFF time is tuned to be slightly delayed with respect to the main switch ($\Delta t \approx 40$ ns), in order

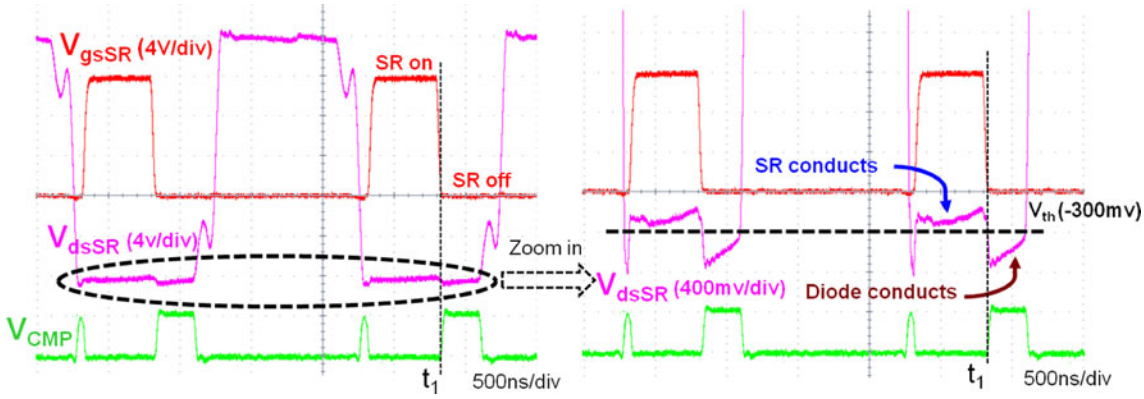

Fig. 11. Waveforms before SR tuning.

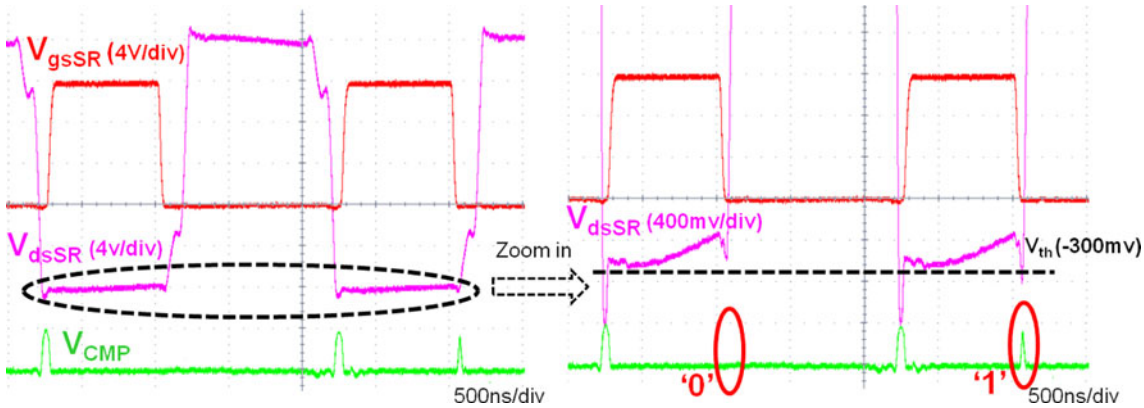

Fig. 12. Waveforms after SR tuning.

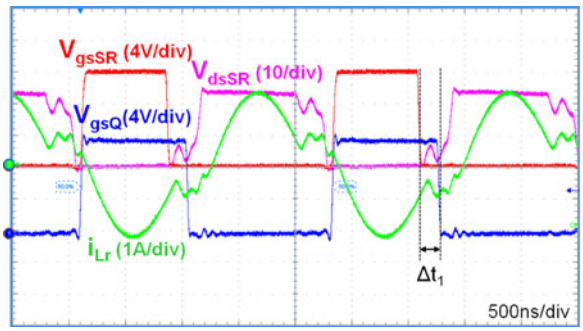

Fig. 13. SR after tuning below the resonant frequency ($f_s = 450$ kHz).

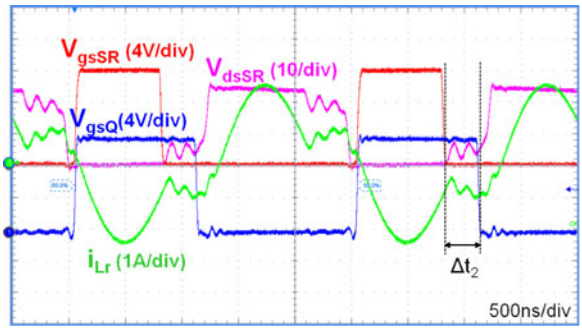

Fig. 14. SR after tuning below the resonant frequency ($f_s = 400$ kHz).

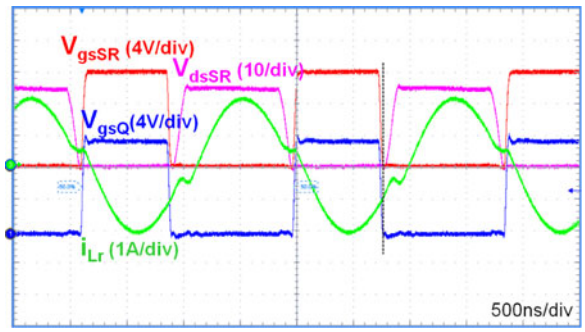

Fig. 15. SR after tuning at the resonant frequency ($f_s = 540$ kHz).

to let the sharply decreased current pass through, as shown in Fig. 16.

As shown earlier, within all switching frequency regions, the SR gate driving signal could be tuned using the proposed universal adaptive driving scheme.

Fig. 17 shows the SR gate drive waveforms using a commercial SR controller [5] designed for the LLC resonant converter. As analyzed in Section I, due to the inductive characteristic of the sensed SR drain to source voltage, the SR is turned OFF earlier than desired. When $f_s = 500$ kHz, the SR duty cycle loss is nearly 170 ns. Compared with this commercial SR controller,

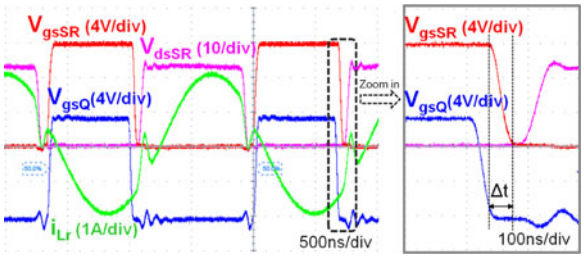

Fig. 16. SR after tuning above the resonant frequency (f_s = 600 kHz).

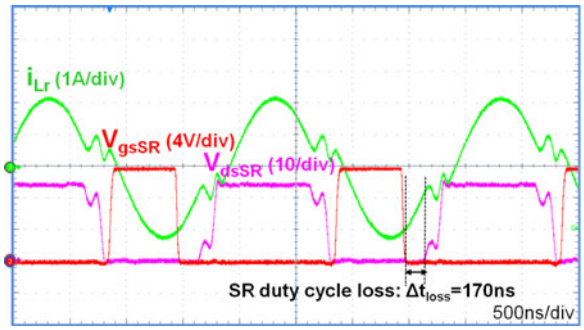

Fig. 17. SR duty cycle loss when using the commercial SR driving controllers.

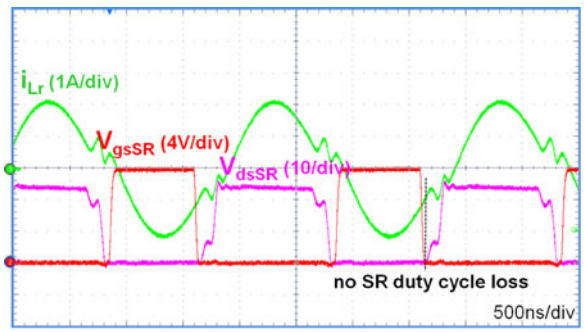

Fig. 18. Improved performance when using the proposed SR driving scheme.

when using the proposed digital driving scheme, there is almost no SR duty cycle loss as shown in Fig. 18.

Fig. 19 shows the efficiency comparison between the commercial SR controller and proposed digital SR driving scheme. The LLC resonant converter efficiency is improved by 0.46% at the full load when f_s = 500 kHz. To increase the power density, the switching frequency f_s will be pushed to even higher in future; as a result, the influence of the parasitic inductance becomes more serious. Thus, there will be more duty cycle loss when using the commercial SR controllers. With the proposed solution, the efficiency improvement will become much more significant.

As analyzed in Section III, when f_s decreases, there is no shoot-through concern. Thus, the f_s increase transient is tested in Fig. 20. When f_s increases, the limitation (2) to the pulse width of the SR gate driving signal is active to prevent the shoot-through. Fig. 20 shows the waveforms when f_s increases from 500 to 700 kHz in several switching cycles. After SR has been fully turned OFF, the drain to source voltage V_{dsSR} starts to

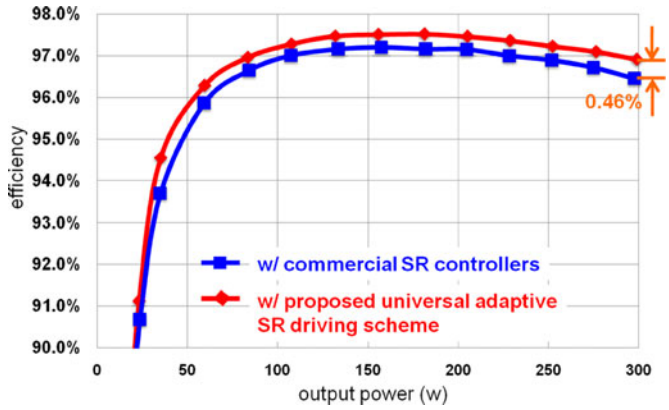

Fig. 19. Efficiency comparison with the commercial SR controllers.

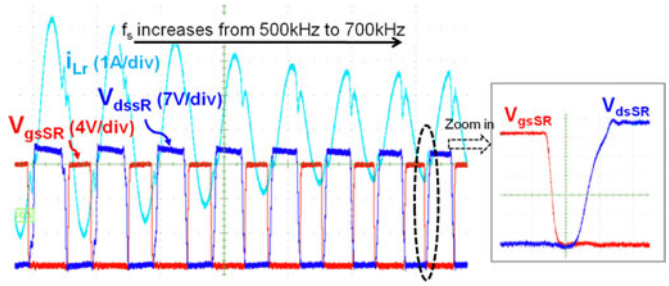

Fig. 20. Protection to avoid shoot-through when f_s increases quickly.

build up slowly. ZCS is kept and no shoot-through is guaranteed even if f_s increases up to 700 kHz.

V. Conclusion

The universal adaptive SR driving scheme for LLC resonant converters is proposed and its digital implementation is experimentally verified in this paper. By sensing the SR drain to source voltage V_{dsSR} and comparing with the threshold V_{th}, the body diode conduction status is detected. The digital logic tunes the SR duty cycle to eliminate the body diode conduction in order to achieve the highest efficiency in all operating frequency regions of the LLC resonant converter. Finally, the protection is investigated to avoid shoot-through during the transient process.

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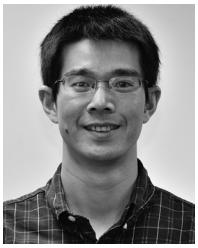

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