# A ZVS Grid-Connected Three-Phase Inverter

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***Abstract*—A six-switch three-phase inverter is widely used in a high-power grid-connected system. However, the antiparallel diodes in the topology operate in the hard-switching state under the traditional control method causing severe switch loss and high electromagnetic interference problems. In order to solve the problem, this paper proposes a topology of the traditional six-switch three-phase inverter but with an additional switch and gave a new space vector modulation (SVM) scheme. In this way, the inverter can realize zero-voltage switching (ZVS) operation in all switching devices and suppress the reverse recovery current in all antiparallel diodes very well. And all the switches can operate at a fixed frequency with the new SVM scheme and have the same voltage stress as the dc-link voltage. In grid-connected application, the inverter can achieve ZVS in all the switches under the load with unity power factor or less. The aforementioned theory is verified in a 30-kW inverter prototype.**

***Index Terms*—Grid connected, soft switching, space vector modulation (SVM), three-phase inverter, zero-voltage switching (ZVS).**

## I. Introduction

In A high-power grid-connected inverter application, the six-switch three-phase inverter is a preferred topology with several advantages such as lower current stress and higher efficiency. To improve the line current quality, the switching frequency of the grid-connected inverter is expected to increase. Higher switching frequency is also helpful for decreasing the size and the cost of the filter. However, higher switching frequency leads to higher switching loss [1]. The soft-switching technique is a choice for a high-power converter to work under higher switching frequency with lower switching loss and lower EMI noise.

In the past few years, there have been many studies on soft-switching techniques for a three-phase converter. And they can generally be divided into two configurations according to the position where the soft-switching function is realized [2]: dc-side and ac-side soft-switching circuits. The topologies are shown in Fig. 1. In the left topology of Fig. 1, an auxiliary circuit is installed between the dc input source and the bus of the three-phase bridge switches. This auxiliary circuit is used to create the zero-voltage duration of the dc bus at the desired switching instant. And then the corresponding devices in three-phase legs can be switched under the zero-voltage condition. In the right topology of Fig. 1, the inverter can achieve zero-voltage switching (ZVS) or zero-current switching (ZCS) in any switching devices without changing the dc-bus voltage. However, the auxiliary circuit needs to be connected to each ac output node of the phase leg. The main advantage of the ac-side soft-switching inverter is that the auxiliary circuit is in shunt with the main bridge. Therefore, the auxiliary circuit does not need to carry the load current throughout the inverter operation reducing the conduction loss. In dc-side soft-switching topologies, the resonant dc-link (RDCL) converter is really simplified, but the RDCL imposes substantial voltage stress (>2.5 times as high as the dc-bus voltage) across the devices. The active-clamped RDCL (ACRDCL) converter [3]–[5] has lower voltage stress (1.3–1.4 times as high as the dc-bus voltage).

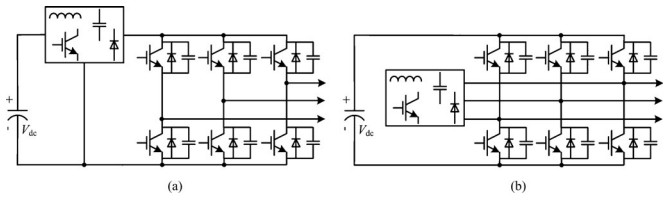


Fig. 1. Soft-switching three-phase inverter topology: (a) dc-side topology and (b) ac-side topology.

Both RDCL and ACRDCL converters have to use discrete pulse modulation (DPM). DPM requires the dc-link resonating frequency to be several times higher than the switching frequency of the pulsewidth modulation (PWM) converter for similar current spectral performance [6], which normally causes undesirable subharmonics. In [7], the PWM scheme is used to control the RDCL inverters, but the switching loss is increased, and the PWM range is also limited. The maximum voltage stress of the quasi-resonant dc-link PWM inverter (QRDCL) is only 1.01–1.1 times as high as the dc-bus voltage [8], [9]; however, the auxiliary device of QRDCL is normally in series with the dc bus causing higher conduction loss and switching loss, especially in high-power application. The PWM scheme can be used to control the QRDCL inverters, while normal PWM schemes still need to be modified in order to synchronize the turn-on events of main switches, which can increase the current ripple. The active-clamping ZVS-PWM half-bridge inverter

Manuscript received May 12, 2011; revised July 24, 2011, September 14, 2011, and November 30, 2011; accepted December 31, 2011. Date of current version April 20, 2012. This work was supported in part by the National Natural Science Foundation of China under Grant 50877072, in part by the China Postdoctoral Science Foundation under Grant 2011M500773, and in part by the National High Technology Research and Development of China 863 Program (2007AA05Z243). Part of this paper was presented at the Applied Power Electronics Conference, Washington, DC, February 15 to February 19, 2009. Recommended for publication by Associate Editor C. A. Canesin.

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Digital Object Identifier 10.1109/TPEL.2012.2184559

[10] also has lower voltage stress (1.01–1.1 times as high as the dc-bus voltage). According to [10], in this active-clamping ZVS-PWM half-bridge inverter, to achieve better soft-switching performance, the slow reverse recovery switch antiparallel diode is the primary choice because the diode reverse recovery energy is used to obtain the soft commutation condition. In the ZVS dc-link single-phase full-bridge inverter [11], the switch voltage is clamped to the dc-link voltage. The PWM modulation scheme is modified to achieve ZVS under different power factor loads. Besides the dc-side soft-switching technique, there are also some ac-side soft-switching techniques suitable for higher power application. The auxiliary resonant commutated pole (ARCP) converter achieves zero-voltage turn-on for main switches and zero-current turn-off for an auxiliary switch [12]. The ARCP converter has excellent performance, but two low-frequency capacitors are necessary in the resonant cell and it is difficult to control the capacitors' midpoint voltage without an additional control circuit. A new ZVS-PWM single-phase full-bridge inverter using a simple ZVS-PWM commutation cell is proposed in [13]. No auxiliary voltage source or low-frequency center-tap capacitor is needed in the cell. The main switches operate at ZVS and the auxiliary switches operate at ZCS. The inductor-coupled ZVT inverter achieves the zero-voltage turn-on condition for main switches and the near-zero current turn-off condition for auxiliary switches [14]–[16]. This topology offers several advantages over the ARCP. The problems associated with the split dc capacitor bank are avoided, and the ZVT operation requires no modification compared to normal space vector modulation (SVM) schemes. The peak current stress of the auxiliary switches is half of that of the main switches. The major problem of this topology is to use coupled inductors, which are normally bulky in high-power applications. An improved ZVS inverter used two coupled magnetic components in one resonant pole [17] to ensure the main switches operating under the ZVS condition and the auxiliary switches operating under the ZCS condition when the load varies from zero to full. Since an independent coupled magnetic component structure avoids the unwanted magnetizing current antiparallel loop, the size of the coupled inductors can be minimized with lower magnetizing inductance, and its saturation can be eliminated. The ZVS timing requirement is also satisfied over the full load range by using the variable timing control with simple and reliable ZV detection [18], [19].

The zero-current transition (ZCT) inverter [20]–[22] achieves ZCS in all of the main and auxiliary switches and their antiparallel diodes. This topology needs six auxiliary switches and three *LC* resonant tanks. The simplified three-switch ZCT inverter [23] needs only three auxiliary switches to achieve zero-current turn-off in all of the main switches and auxiliary switches. Compared with the six-switch ZCT inverter, the resonant tank current stress of the three-switch ZCT inverter is higher.

The structure of the ZVS-SVM controlled three-phase PWM rectifier [24] is similar to the ACRDCL converter. With the special SVM scheme proposed by the authors, both the main switches and the auxiliary switch have the same and fixed switching frequency. The reverse recovery current of the switch

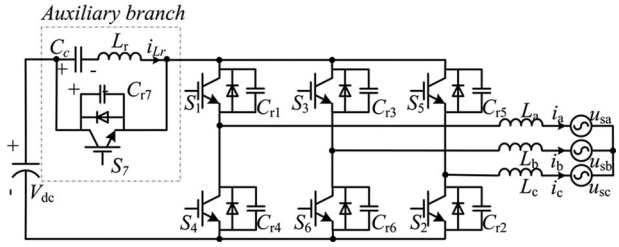


Fig. 2. ZVS three-phase inverter.

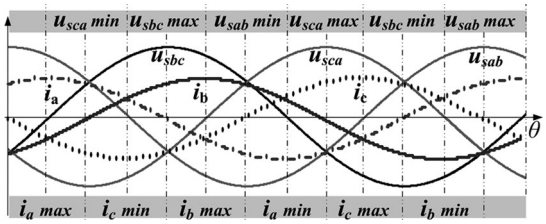


Fig. 3. Grid line voltage and inverter output current waveform.

antiparallel diodes is suppressed well and all the switches can be turned ON under the zero-voltage condition. Moreover, the voltage stress in both main switches and the auxiliary switch is only 1.01–1.1 times of the dc-bus voltage. In this paper, a ZVS three-phase grid-connected inverter is proposed. The topology of the inverter is shown in Fig. 2, which is similar to the rectifier topology proposed in [24]. All the soft-switching advantages under the rectifier condition can be achieved in a grid-connected inverter application, and the voltage stress in both main switches and the auxiliary switch is the same as the dc-bus voltage. The operation principle of this SVM scheme is described in detail. The experimental results of a 30-kW hardware prototype are presented to verify the theory.

## II. Inverter Topology and Modulation Scheme

The topology in Fig. 2 is composed of a standard PWM inverter and a clamping branch. The clamping branch consists of active switch $S_7$, resonant inductor $L_r$, and clamping capacitor $C_c$. During most time of operation, the active switch $S_7$ is in conduction, and energy circulates in the clamping branch. When the auxiliary switch $S_7$ is turned OFF, the current in the resonant inductor $i_{Lr}$ will discharge the parallel capacitors of the main switch and then the main switch can be turned ON under the zero-voltage condition. When the main switch is turned ON, $L_r$ suppresses the reverse recovery current of an antiparallel diode of the other main switch on the same bridge.

Since there are three legs in the main bridge, normally the auxiliary switch must be activated three times per PWM cycle if the switch in the three legs is modulated asynchronously. To make the auxiliary switch having the same switching frequency as the main switch, a special SVM scheme is proposed to control the inverter. Suppose that the grid-connected inverter works with unity power factor; the grid line voltage and the inverter output current waveform are shown in Fig. 3; the corresponding voltage sector definition is shown in Fig. 4.

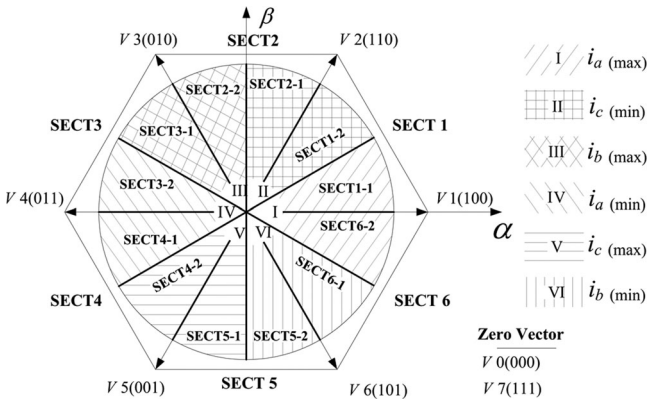


Fig. 4. Grid voltage and inverter current space vector diagram.

In voltage SVM, the whole utility cycle can be divided into six voltage sectors, and every grid voltage sector can still be divided into two different smaller sectors according to the maximum value of the phase current in the inverter. For example, the grid voltage sector SECT1 can be divided into SECT1-1 and SECT1-2. In SECT1-1, the absolute value of the phase-A current obtains the maximum value, and in SECT1-2, the absolute value of the phase-C current does the same.

Since the operation of the converter is symmetrical in every 30°, assume that the inverter is operating in SECT1-1. If the grid-connected inverter works with unity power factor, $i_a > 0$ and $i_c < i_b < 0$ in SECT1-1. The phase voltage and phase current in phase A obtains the maximum value; there exist four switching states as shown in Fig. 4: 111, 100, 110, and 000. The equivalent circuits of these four switching states are shown in Fig. 5.

If the switching sequence in SECT1-1 is 111-100-110-111, as shown in Fig. 6, then the zero vector will always be 111 and switch $S_1$ will always be in conduction. When the switching state changes from 111 to 100, switches $S_6$ and $S_2$ will be turned ON simultaneously. The auxiliary branch needs to act in this transition process to suppress the reverse recovery currents of antiparallel diodes of $S_3$ and $S_5$ and create the ZVS condition for $S_6$ and $S_2$. During the state from 100 to 110, the current in $S_6$ at first will flow into the antiparallel diode of $S_3$. During the state from 110 to 111, the current in $S_2$ will flow into the antiparallel diode of $S_5$. These two transitions are normal soft switching. Thus, the auxiliary branch only needs to act once in one switching cycle to resonant the dc bus to zero, creating the ZVS condition for the switches and suppressing the diode recoveries in two phases. The auxiliary switch can work at the same frequency as the main switch. And the main switch can be turned ON or OFF at the exact time decided by the SVM control. The resonant process equivalent circuits in the state change from 111 to 100 as shown in Fig. 7. The key waveform of the inverter equivalent circuit in SECT1-1 is shown in Fig. 8.

Take SECT1-1 as an example for analysis, the steady-stage circuit and key waveforms of the inverter are shown in Figs. 9 and 10, respectively. During circuit topological changes, the complete circuit operation in SECT1-1 can be divided into nine stages.

The following assumptions are made to simplify the analysis of the ZVS inverter:

1) switches $S_1$–$S_7$ are considered as an ideal switch with its antiparallel diode;
2) capacitances $C_{r1}$–$C_{r7}$ paralleled with switches $S_1$–$S_7$, respectively, include parasitic capacitance and external capacitance;
3) in one switching cycle, the inductor current ripple is small and can be considered as a constant current source;
4) the capacitance of the clamping capacitor $C_c$ is large enough, so the voltage ripple across it is small, and thus can be regarded as a voltage source;
5) the resonant frequency of $C_c$ and $L_r$ is much lower than the operation frequency of the converter.

*Stage 1 ($t_0$–$t_1$):* Main switches $S_1$, $S_3$, and $S_5$ and auxiliary switch $S_7$ are ON. The circuit is in the state 111. In the auxiliary resonant cell, the voltage of $L_r$ is clamped by clamping capacitor $C_c$, and its current $i_{Lr}$ increases at the rate of

$$\frac{di_{Lr}}{dt} = -\frac{V_{Cc}}{L_r}. \tag{1}$$

*Stage 2 ($t_1$–$t_2$):* In $t_1$, $S_7$ is turned OFF; the resonant inductor $L_r$ discharges the parallel capacitors $C_{r4}$, $C_{r6}$, and $C_{r2}$ and charges parallel capacitor $C_{r7}$ of the auxiliary switch $S_7$. $S_7$ is turned OFF under the ZVS condition because of the snubber capacitor $C_{r7}$.

*Stage 3 ($t_2$–$t_3$):* In $t_2$, the voltage across $S_7$ reaches $V_{\rm dc}$, $S_7$ is OFF, the voltages across $C_{r4}$, $C_{r6}$, and $C_{r2}$ drop to zero, and the antiparallel diodes of these main switches start to conduct. The resonant between $L_r$ and these paralleled capacitors stops. $S_2$ and $S_6$ can be turned ON under the ZVS condition.

*Stage 4 ($t_3$–$t_4$):* In $t_3$, $S_2$ and $S_6$ are turned ON under the ZVS condition. In this stage, the currents in phase B and phase C convert from the antiparallel diodes of $S_3$ and $S_5$ to $S_2$ and $S_6$, respectively. When the main switch transition process completes, the antiparallel diodes of $S_3$ and $S_5$ experience diode reverse recovery. Due to the existence of the resonant inductor $L_r$, the diode reverse recovery is suppressed and the current in $L_r$ $i_{Lr}$ changes at the rate of

$$\frac{di_{Lr}}{dt} = \frac{V_{\rm dc} - V_{Cc}}{L_r}. \tag{2}$$

*Stage 5 ($t_4$–$t_5$):* Main switches $S_3$, $S_4$, and $S_5$ are OFF at $t_4$; the circuit reaches the state 100. $L_r$, $C_{r3}$, $C_{r4}$, $C_{r5}$, and $C_{r7}$ start to be in resonance. The voltages across $S_3$, $S_4$, and $S_5$ start to increase and the voltage across $S_7$ starts to decrease. At $t_5$, the voltages across $S_2$, $S_4$, and $S_6$ reach to $V_{\rm dc}$, the voltage across $S_7$ decreases to zero, and the antiparallel diode of $S_7$ starts to conduct. $S_7$ can be turned ON under the ZVS condition. $L_r$, $C_{r3}$, $C_{r4}$, $C_{r5}$, and $C_{r7}$ stop to be in resonance. The time between $t_2$ and $t_5$ is the duty cycle loss of $S_2$ and $S_6$. As stages 3–5 are very short compared with the whole switching cycle, the impact of this duty cycle loss on the circuit operation during the whole switching cycle can be ignored.

*Stage 6 ($t_5$–$t_6$):* At $t_5$, the circuit reaches the state 100. The main switches $S_1$, $S_2$, and $S_6$ and the auxiliary switch $S_7$ are

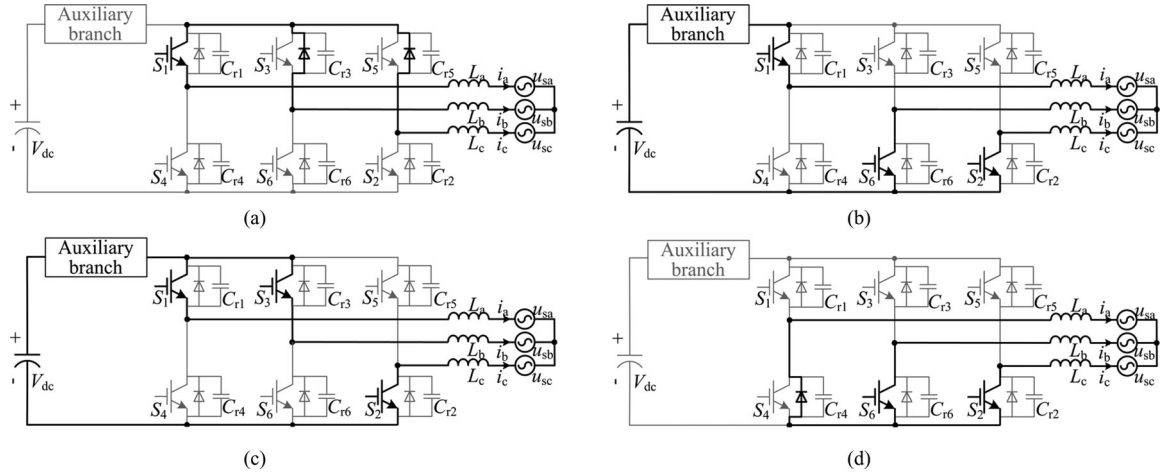


Fig. 5. Four switching states in the SECT1-1: (a) state 111, (b) state 100, (c) state 110, and (d) state 000.

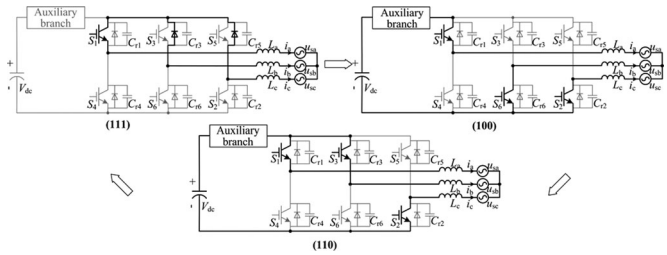


Fig. 6. Switching sequence in SECT1-1: 111-100-110-111.

ON. The resonant inductor is charging the clamping capacitor $C_c$.

*Stage 7 ($t_6$–$t_7$):* At $t_6$, $S_6$ is turned OFF. The inductor $L_b$ will charge $C_6$ and discharge $C_3$. Due to the existence of $C_3$ and $C_6$, $S_6$ is turned OFF under the ZVS condition.

*Stage 8 ($t_7$–$t_8$):* The circuit reaches the state 110. The main switch $S_1$, $S_3$, and $S_2$ and the auxiliary switch $S_7$ are ON. The resonant inductor is charging the clamping capacitor $C_c$.

*Stage 9 ($t_8$–$t_9$):* At $t_7$, $S_2$ is turned OFF. The inductor $L_c$ will charge $C_2$ and discharge $C_5$. Due to the existence of $C_5$ and $C_2$, $S_2$ is turned OFF under the ZVS condition. At $t_9$, the voltage on $S_5$ decreases to zero, and the antiparallel diode of $S_5$ starts to conduct. $S_6$ can be turned ON under the ZVS condition. The circuit reaches the state 100. After $t_9$, a new switching cycle starts again.

## III. Theoretical Analysis of the Soft-Switching Grid-Connected Inverter

When the circuit is working in the steady state, the mean voltage of the resonant inductor is zero

$$\int_0^{T_s} u_{L1}dt \approx \int_0^{t_1} u_{L1}dt + \int_{t_2}^{t_3} u_{L1}dt + \int_{t_4}^{t_8} u_{L1}dt = \int_0^{t_1} -V_{Cc}dt + \int_{t_2}^{t_3} (V_{\rm dc} - V_{Cc})\,dt + \int_{t_4}^{t_8} -V_{Cc}dt = V_{\rm dc}D_0T - V_{Cc}T \quad (3)$$

where the short-lived states ($t_1$–$t_2$) and ($t_3$–$t_4$) have been ignored and $D_0$ is the auxiliary switch turn-off duty cycle; then the clamping capacitor voltage is

$$V_{Cc} = V_{\rm dc}D_0. \quad (4)$$

Fig. 11 shows the equivalent circuit diagrams during resonant stage 4.

According to the aforementioned steady analysis, $i_{Lr} = i_a$ at $t_4$. In stage 5, the voltage of $L_r$ is still clamped by dc-bus voltage. At $t_5$

$$i_{Lr(t5)} = i_a + \frac{V_{\rm dc}}{L_r}(t5 - t4). \quad (5)$$

In stage 4, $L_r$, $C_{r3}$, $C_{r4}$, $C_{r5}$, and $C_{r7}$ start to be resonant. Fig. 11 shows the equivalent circuit diagrams during resonant stage 4. The circuit initialization is

$$\begin{cases} V_{C_3} = V_{C_4} = V_{C_5} = 0 \\ V_{C7} = V_{\rm dc} \\ i_{Lr} = i_a. \end{cases} \quad (6)$$

Suppose $C_{r3} = C_{r4} = C_{r5} = C_r$

$$\begin{cases} L_r \dfrac{di_{Lr}}{dt} = v_{\rm dc} - v_{Cc} - v_{Cr3}(t) \\ (3C_r + C_{r7})\dfrac{dv_{Cr3}}{dt} = i_{Lr} - i_a. \end{cases} \quad (7)$$

Solving the aforementioned equation

$$i_{Lr}(t_4) = i_a + (V_{\rm dc} - V_{Cc})\sqrt{\frac{3C_r + C_{r7}}{L_r}} \cdot \sqrt{1 - \frac{V_{Cc}^2}{(V_{\rm dc} - V_{Cc})^2}} \quad (8)$$

$$v_{C7}(t_4) = V_{Cc} - (V_{\rm dc} - V_{Cc})\cos[\omega_r(t_4 - t_3)] \quad (9)$$

$$Z_r = \sqrt{\frac{L_r}{(3C_r + C_{r7})}}. \quad (10)$$

In $t_4$, $S_7$ can be turned ON under the ZVS condition if the voltage across $S_7$ can decrease to zero. Because $V_{Cc}$ is much

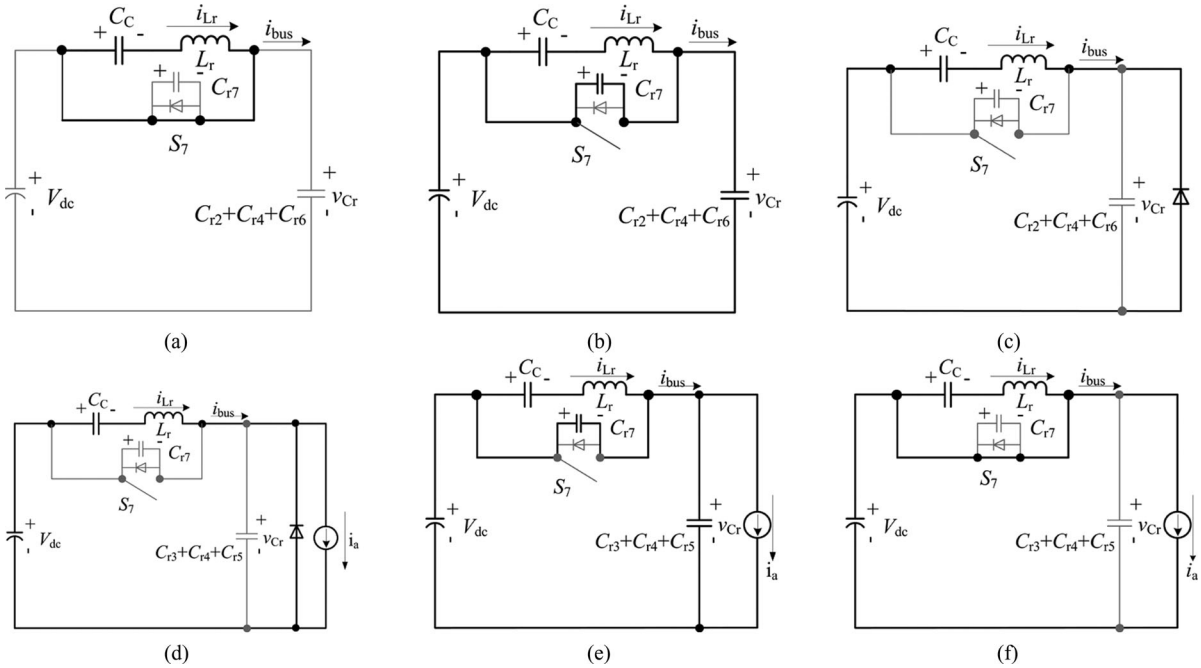


Fig. 7. Operation stages of a soft-switching grid-connected inverter equivalent circuit: (a) stage 1($t_0$–$t_1$), (b) stage 2 ($t_1$–$t_2$), (c) stage 3 ($t_2$–$t_3$), (d) stage 4 ($t_3$–$t_4$), (e) stage 5 ($t_4$–$t_5$), and (f) stage 6 ($t_5$–$t_6$).

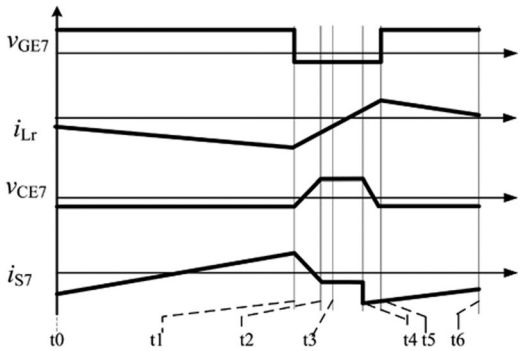


Fig. 8. Key waveform of the inverter equivalent circuit.

smaller than $V_{\rm dc}$, it is easy for the voltage on $S_7$ to decrease to zero; then the auxiliary switch is always under the zero-voltage turn-on condition. From $t_4$ to $t_1$, the auxiliary switch $S_7$ is in conduction, the resonant inductor $L_r$ is clamped by the clamp capacitor voltage, and then

$$i_{Lr(t1)} = i_a + (V_{\rm dc} - V_{Cc})\frac{1}{Z_r}\cdot\sqrt{1-\frac{V_{Cc}^2}{(V_{\rm dc}-V_{Cc})^2}} - \frac{V_{Cc}}{L_r}(1-D_0)T. \tag{11}$$

In stage 2, $L_r$ discharges $C_{r4}$, $C_{r6}$, and $C_{r2}$ and charges $C_{r7}$. Fig. 12 shows the equivalent circuit diagrams during resonant stage 2.

The circuit initialization is

$$\begin{cases} V_{C2} = V_{C4} = V_{C6} = V_{\rm dc} \\ V_{C7} = 0 \\ i_{Lr} = i_{Lr(t1)}. \end{cases} \tag{12}$$

Suppose that $C_{r3} = C_{r4} = C_{r5} = C_r$,

$$\begin{cases} L_r\dfrac{di_{Lr}}{dt} = v_{\rm dc} - v_{Cc} - v_{Cr2}(t) \\ (3C_r + C_{r7})\dfrac{dv_{Cr2}}{dt} = i_{Lr}. \end{cases} \tag{13}$$

Solving the aforementioned equation

$$v_{Cr2}(t) = V_{\rm dc} - V_{Cc} - \sqrt{V_{Cc}^2 + i_{Lr(t1)}^2 Z_r^2} \times \sin\left(\omega_r t - \arctan\frac{V_{Cc}}{\left|i_{Lr(t1)}Z_r\right|}\right) \tag{14}$$

$$i_{Lr} = -\frac{\sqrt{V_{Cc}^2 + i_{Lr(t1)}^2 Z_r^2}}{Z_r} \times \cos\left(\omega_r t - \arctan\frac{V_{Cc}}{\left|i_{Lr(t1)}Z_r\right|}\right). \tag{15}$$

In $t_2$, $S_6$ and $S_2$ can be turned ON under conditions of ZVS if the voltage on the main switch bridge decreases to zero. According to (14), the ZVS condition for the main switch is

$$\sqrt{V_{Cc}^2 + i_{Lr(t1)}^2 Z_r^2} > V_{\rm dc} - V_{Cc}. \tag{16}$$

When the circuit is working in the steady state, the mean current of the clamping capacitor is zero, and the auxiliary switch's turn-off duty cycle should be

$$D_0 \approx \frac{(i_a + V_{\rm dc}/Z_r)\,2L_r}{TV_{\rm dc} + 2L_r V_{\rm dc}/Z_r}. \tag{17}$$

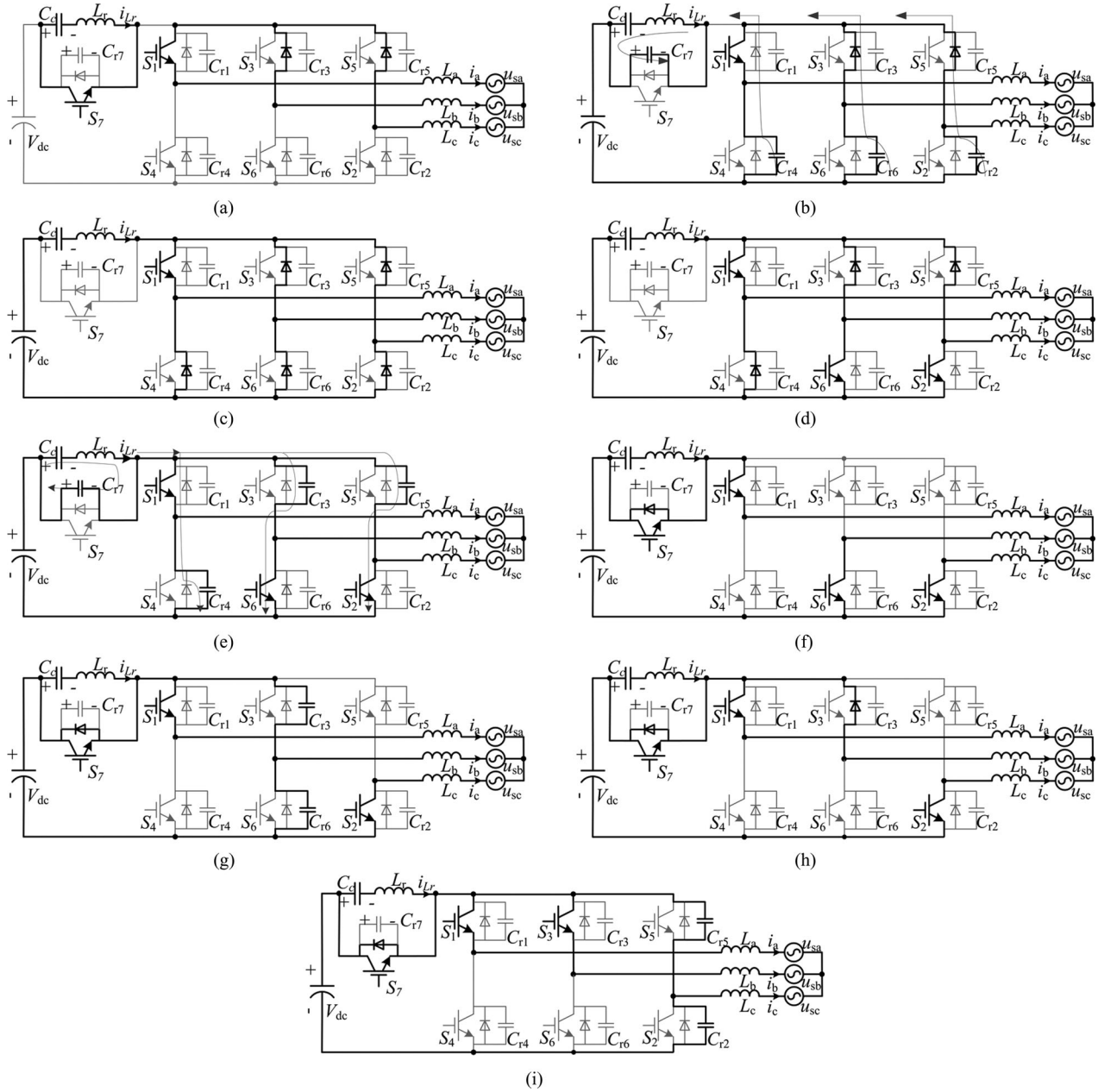


Fig. 9. Operation stages of a soft-switching grid-connected inverter: (a) stage 1($t_0$–$t_1$), (b) stage 2 ($t_1$–$t_2$), (c) stage 3 ($t_2$–$t_3$), (d) stage 4 ($t_3$–$t_4$), (e) stage 5 ($t_4$–$t_5$), (f) stage 6 ($t_5$–$t_6$), (g) stage 7 ($t_6$–$t_7$), (h) stage 8 ($t_7$–$t_8$), and (i) stage 9 ($t_8$–$t_9$).

Combining (9) and (17)

$$i_{Lr}(t_1) = -i_a + (V_{Cc} - V_{\rm dc})\sqrt{\frac{3C_r + C_{r7}}{L_r}} \cdot \sqrt{1 - \frac{V_{Cc}^2}{(V_{\rm dc} - V_{Cc})^2}}. \quad (18)$$

Combining (16) and (18), the ZVS condition for the main switch is

$$V_{Cc}^2 + i_a^2 Z_r^2 + 2 i_a Z_r (V_{\rm dc} - V_{Cc}) > 0. \quad (19)$$

In SECT1-1, $i_a$ is always positive. Then, according to (19) with the proposed modulation scheme, the ZVS condition for the main switch can always be satisfied.

## IV. Modulation Scheme Under Different Current Power Factors

The aforementioned analysis is based on the assumption that the grid-connected inverter works with unity power factor. Actually, the ZVS inverter can still work when $\varphi_u \neq \varphi_i$; the corresponding voltage sector definition is shown in Fig. 4. The grid

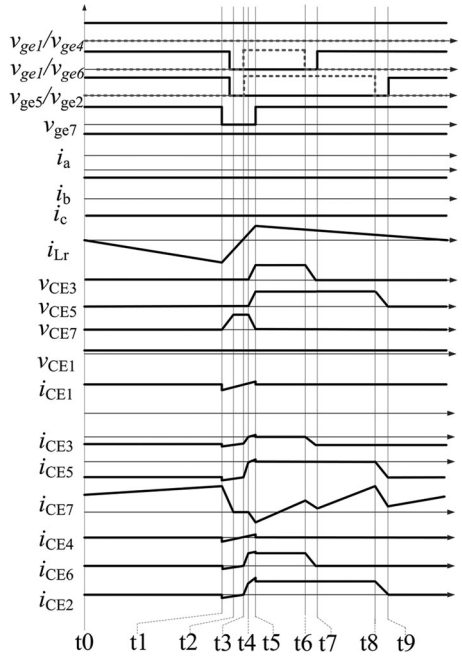


Fig. 10. Voltage space vectors and the time diagram in SECT1-1.

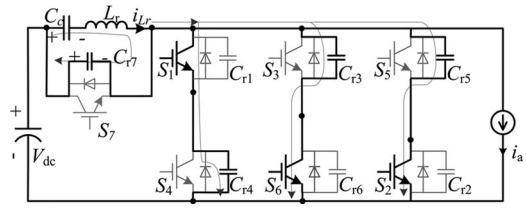


Fig. 11. Equivalent circuit during the resonant period (stage 4).

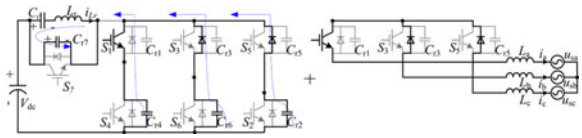

Fig. 12. Equivalent circuit during the resonant period (stage 2).

voltage and inverter current are expressed, respectively, as

$$\begin{cases} u_{sa} = U_S \cos(\omega t + \varphi_u) \\ u_{sb} = U_S \cos\left(\omega t - \dfrac{2\pi}{3} + \varphi_u\right) \\ u_{sc} = U_S \cos\left(\omega t + \dfrac{2\pi}{3} + \varphi_u\right) \end{cases} \tag{20}$$

$$\begin{cases} i_a = I_S \cos(\omega t + \varphi_i) \\ i_b = I_S \cos\left(\omega t - \dfrac{2\pi}{3} + \varphi_i\right) \\ i_c = I_S \cos\left(\omega t + \dfrac{2\pi}{3} + \varphi_i\right). \end{cases} \tag{21}$$

Take $|\varphi_u - \varphi_i| \le \pi/6$ for example; the auxiliary switch $S_7$ only needs to act once in one switching cycle to resonant the dc bus to zero, creating the ZVS condition for switches and suppressing the diode recoveries in two phases. The auxiliary switch can work at the same frequency as the main switch. And the main switch can be turned ON or OFF at the exact time decided by the SVM control. The modulation scheme of the main switch with $|\varphi_u - \varphi_i| \le \pi/6$ is shown in Table I.

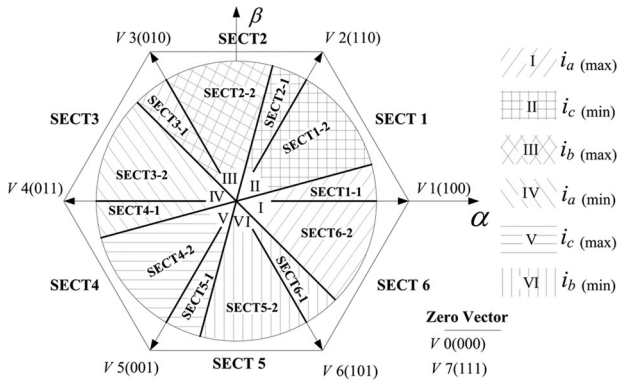


Fig. 13. Grid voltage and inverter current space vector diagram (PF $\neq$ 1).

## V. Experimental Results

A 30-kVA prototype of the three-phase soft-switching grid-connected inverter controlled by DSP (TMS320F2407A), as shown in Fig. 1, is built to verify the theory. The parameters of the circuit are $V_{\rm dc} = 680$ V, grid phase voltage 220 $V_{\rm rms}$, the output filter inductor $L = 0.3$ mH, the resonant capacitance $C_r = 3.3$ nF, the resonant inductance $L_r = 30$ $\mu$H, and the operation frequency $f = 16$ kHz. The switches $S_1$–$S_7$ are CM200DU-24NFH (1200 V/200 A).

Fig. 14 shows the grid voltage and the phase current of the ZVS grid-connected inverter under different power factors. The phase THDi of the ZVS grid-connected inverter under 30-kW output power is 3.3%, which is similar to that of the hard-switching inverter. It means that there is a slight influence of the auxiliary resonance branch to the inverter output voltage and current quality.

The waveforms of the collector–emitter (CE) voltage and the conduction current of the main switch $S_6$ in SECT1-1 are shown in Fig. 15. The positive reference direction of the insulated gate bipolar transistor (IGBT) conduction current is from the collector to the emitter. It can be seen from Fig. 15 that the CE voltage of the main switch is clamped to zero before the main switch is turned ON, and then the ZVS turn-on of the main switch is realized.

The waveforms of the CE voltage and the conduction current of the antiparallel diode of the main switch $S_6$ in SECT1-1 are shown in Fig. 16. It can be seen from Fig. 16 that the reverse recovery current of the antiparallel diode has been suppressed well.

The waveforms of the auxiliary switch current and voltage are shown in Fig. 17. It can be seen from Fig. 17 that in most time of a switching cycle, the auxiliary switch $S_7$ is ON; then the duty cycle loss of main switches is small compared with the whole switching cycle. The resonant branch current and auxiliary switch voltage are shown in Fig. 18. It can be seen from

TABLE I
SWITCHING SEQUENCE OF THE ZVS INVERTER

| sector | Voltage vector angle | Zero vector | First vector | Second vector | Zero vector |
|---|---|---|---|---|---|
| SECT6-2 | $11\pi/6+\varphi_i-\varphi_u\sim2\pi$ | 1 1 1 | 1 0 0 | 1 0 1 | 1 1 1 |
| SECT1-1 | $0\sim\pi/6+\varphi_i-\varphi_u$ | 1 1 1 | 1 0 0 | 1 1 0 | 1 1 1 |
| SECT1-2 | $\pi/6+\varphi_i-\varphi_u\sim\pi/3$ | 0 0 0 | 1 1 0 | 1 0 0 | 0 0 0 |
| SECT2-1 | $\pi/3\sim\pi/2+\varphi_i-\varphi_u$ | 0 0 0 | 1 1 0 | 0 1 0 | 0 0 0 |
| SECT2-2 | $\pi/2+\varphi_i-\varphi_u\sim2\pi/3$ | 1 1 1 | 0 1 0 | 1 1 0 | 1 1 1 |
| SECT3-1 | $2\pi/3\sim5\pi/6+\varphi_i-\varphi_u$ | 1 1 1 | 0 1 0 | 0 1 1 | 1 1 1 |
| SECT3-2 | $5\pi/6+\varphi_i-\varphi_u\sim\pi$ | 0 0 0 | 0 1 1 | 0 1 0 | 0 0 0 |
| SECT4-1 | $\pi\sim7\pi/6+\varphi_i-\varphi_u$ | 0 0 0 | 0 1 1 | 0 0 1 | 0 0 0 |
| SECT4-2 | $7\pi/6+\varphi_i-\varphi_u\sim4\pi/3$ | 1 1 1 | 0 0 1 | 0 1 1 | 1 1 1 |
| SECT5-1 | $4\pi/3\sim3\pi/2+\varphi_i-\varphi_u$ | 1 1 1 | 0 0 1 | 1 0 1 | 1 1 1 |
| SECT5-2 | $3\pi/2+\varphi_i-\varphi_u\sim5\pi/3$ | 0 0 0 | 1 0 1 | 0 0 1 | 0 0 0 |
| SECT6-1 | $5\pi/3\sim11\pi/6+\varphi_i-\varphi_u$ | 0 0 0 | 1 0 1 | 1 0 0 | 0 0 0 |

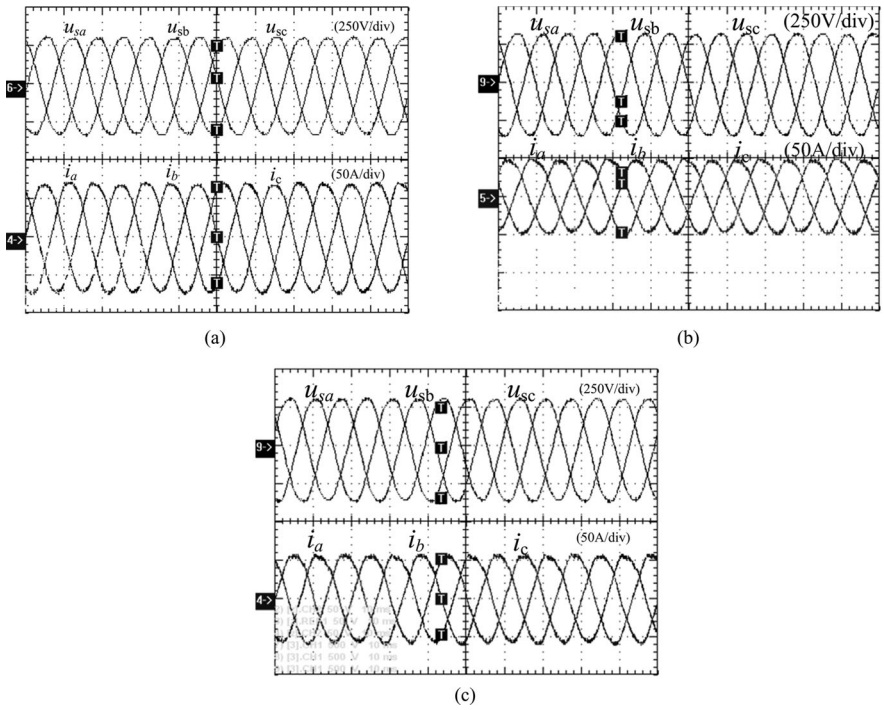


Fig. 14. Inverter output current and grid voltage (10 ms/div): (a) $\varphi_u = \varphi_i$, (b), $\varphi_u - \varphi_i = -\pi/6$, (c) $\varphi_u - \varphi_i = \pi/6$.

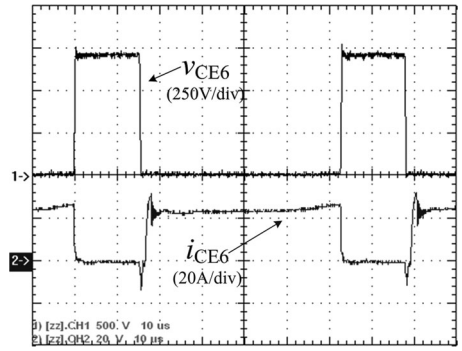


Fig. 15. CE voltage and current of $S_6$ (IGBT on) (5 $\mu$s/div).

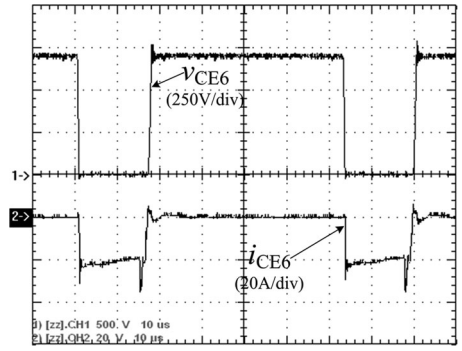


Fig. 16. CE voltage and current of $S_6$ (diode on) (2.5 $\mu$s/div).

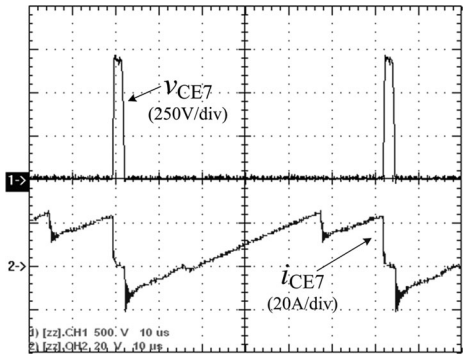


Fig. 17. CE voltage and current of $S_7$ (25 $\mu$s/div).

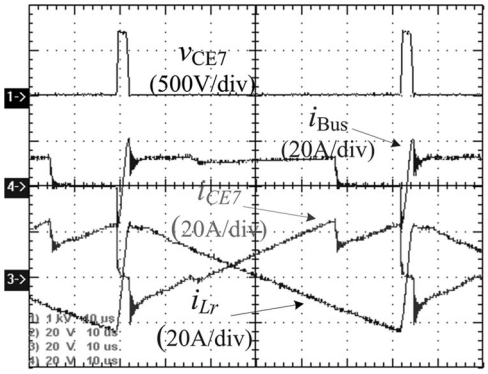


Fig. 18. CE voltage and current of $S_7$, $i_{\rm bus}$, and $i_{Lr}$ (10 $\mu$s/div).

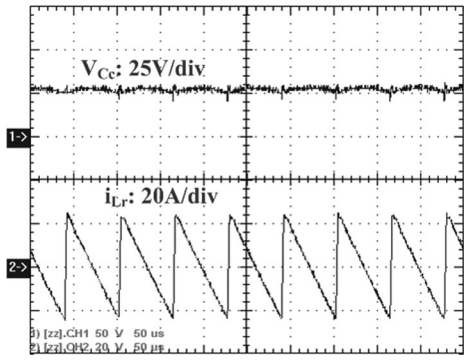


Fig. 19. $V_{Cc}$ and $i_{Lr}$ (50 $\mu$s/div).

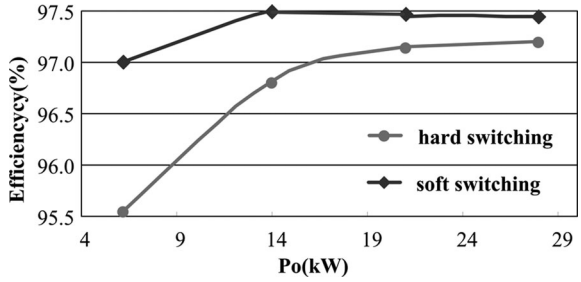


Fig. 20. Efficiency curve.

Fig. 18 that the current of the resonant inductor is symmetrical high-frequency current. The mean value of the current in $S_7$ is equal to the mean value of $i_{\rm bus}$. It means that the larger the inverter's output power, the more the conduction losses of auxiliary switch $S_7$.

The clamping capacitor voltage and the resonant inductor current are shown in Fig. 19, the voltage on the clamping capacitor $C_c$ is less than 30 V, and then the clamping capacitor is easy to be chosen. The efficiency curve of the ZVS inverter and hard-switching counterpart is shown in Fig. 20. All the efficiency is measured through the YOKOGAWA WT1600 power analyzer.

## VI. Conclusion

The analysis and experimentation presented verify that the SVM-controlled three-phase soft-switching grid-connected inverter can realize ZVS operation for all switching devices, and the reverse recovery current in the antiparallel diodes of all switching devices is suppressed well. SVM can be realized at the fixed switching frequency. And the switching voltage stress across all the power switch devices is the same as the dc-link voltage. The ZVS can be achieved in the grid-connected ZVS inverters under the load with unity power factor or less. The reduced switching loss increases its efficiency and makes it suitable for practical applications.

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