A ZVS Interleaved Boost AC/DC Converter Used in Plug-in Electric Vehicles

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***Abstract*—This paper presents a novel, yet simple zero-voltage switching (ZVS) interleaved boost power factor correction (PFC) ac/dc converter used to charge the traction battery of an electric vehicle from the utility mains. The proposed opology consists of a passive auxiliary circuit, placed between two phases of the interleaved front-end boost PFC converter, which provides enough current to charge and discharge the MOSFETs' output capacitors during turn-ON times. Therefore, the MOSFETs are turned ON at zero voltage. The proposed converter maintains ZVS for the universal input voltage (85 to 265 V_{rms}), which includes a very wide range of duty ratios (0.07–1). In addition, the control system optimizes the amount of reactive current required to guarantee ZVS during the line cycle for different load conditions. This optimization is crucial in this application since the converter may work at very light loads for a long period of time. Experimental results from a 3 kW ac/dc converter are presented in the paper to evaluate the performance of the proposed converter. The results show a considerable increase in efficiency and superior performance of the proposed converter compared to the conventional hard-switched interleaved boost PFC converter.**

***Index Terms*—AC/DC converter, continuous current mode (CCM), dc/dc converter, interleaved boost converter, power factor correction (PFC), zero-current switching (ZCS), zero-voltage switching (ZVS).**

NOMENCLATURE

Δi_{LA}	Inductor current ripple of boost A (A).
ω_l	Line frequency (rad/s).
ψ	Phase-shift between leading leg and lagging leg pulses.
C_{So}	Output capacitance of the boost MOSFET (F).
D	PFC duty ratio.
f_s	Switching frequency (Hz).
$i_{\mathrm{Aux},p}$	Peak value of the auxiliary circuit current (A).
i_{in}	Input current of power factor correction (PFC) (A).
i_{LA}	Inductor current of boost A (A).
i_{LB}	Inductor current of boost B (A).
i_{SA1}	Switch S_{A1} current (A).
I_{BAT}	Battery current (A).
I_o	DC output current (A).
I_P	Peak current of the boost inductor (A).
I_{ref}	Peak value of the auxiliary circuit reference current (A).
I_V	Valley current of the boost inductor (A).
k_1	Controller coefficient.
p_{in}	Instantaneous input power (W).
p_{ref}	Instantaneous input power reference value (W).
$P_{\mathrm{in,pk}}$	Peak input power (W).
P_{ref}	Power reference value (W).
r_o	Load incremental resistance (Ω).
P_{sw}	Switching losses (W).
R_e	Converter effective load resistance (Ω).
R_L	PFC inductor series resistance (Ω).
t	Time (s).
t_d	Dead time (s).
u	Control input.
v_{AUX}	Voltage across auxiliary circuit (V).
v_{in}	Instantaneous input voltage of PFC (V).
V_{BAT}	Battery voltage (V).
V_d	Output diode forward voltage drop (V).
V_o	DC output voltage (V).
x	State variables.
ESR	Equivalent series resistance (Ω).
SiC	Silicon carbide.
Si	Silicon.

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I. INTRODUCTION

ELECTRIC vehicle (EV) power conditioning systems usually utilize a high-energy battery pack to store energy for the electric traction system [1]. A typical block diagram of the power conditioning system in an EV is shown in Fig. 1. The high-energy battery pack is typically charged from a utility ac outlet [2]. This energy conversion during the battery charging is performed by an ac/dc converter. Such ac/dc converters, which are used to charge the high-energy battery, usually consist of two stages: front-end boost converter, which performs input PFC and ac/dc conversion, and full-bridge dc/dc converter for battery charging and galvanic isolation [3]. PFC is essential to improve the quality of the input current, which is drawn from the utility so as to comply with the regulatory standards like IEC 61000-3-2.

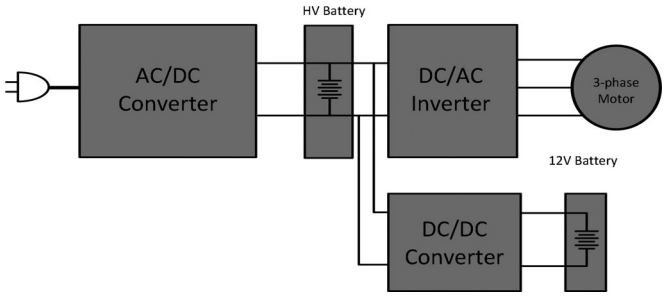


Fig. 1. Block diagram of EV power conditioning system.

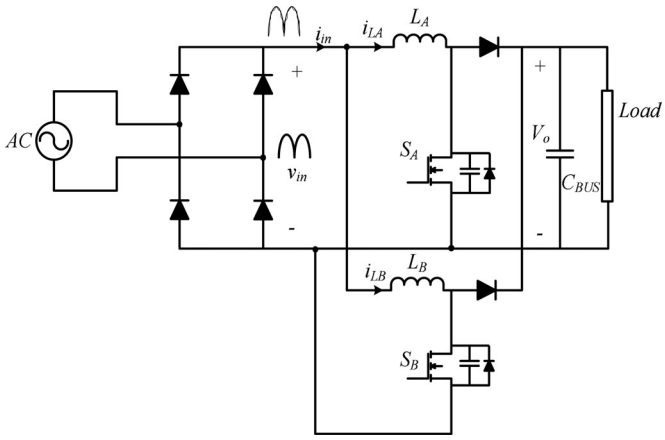


Fig. 2. Interleaved boost PFC schematic.

Boost converters are generally used to realize input PFC and ac/dc conversion [4]–[9] in the front end of an ac/dc converter. In high power applications, interleaving continuous current mode (CCM) PFC boost stages, as shown in Fig. 2, is a very common approach to effectively decrease the inductor footprint and volume as well as the output capacitor current ripple [7]–[14]. A typical boost PFC utilizes a switch and a diode. In the range of a few kilowatt, power MOSFETs are usually used to realize the boost converter.

The main sources of switching losses in boost PFC converters are hard turn-ON of the MOSFET and the reverse recovery of the boost diode during its turn-OFF. In order to eliminate the switching losses in a MOSFET-based boost PFC converter, different auxiliary circuits have been proposed [15]–[25]. The typical placement of a zero-voltage switching (ZVS) auxiliary circuit is shown in Fig. 3. Commonly, these auxiliary circuits consist of a combination of passive components such as small inductors and capacitors and additional active components such as MOSFETs and diodes.

Auxiliary circuits in ZVS- puslewidth modulation (PWM) single-switch converters are generally one of two types, nonresonant [15] and resonant [16]–[23], depending on whether there is an *LC* resonant network placed in series with the switch. Typical nonresonant and resonant ZVS auxiliary circuits are shown in Fig. 4(a) and (b)–(d), respectively. There is a third type, dual auxiliary circuits [23], that is a combination of both resonant and nonresonant circuits. These circuits, which were first categorized in [23], are shown in Fig. 4(e).

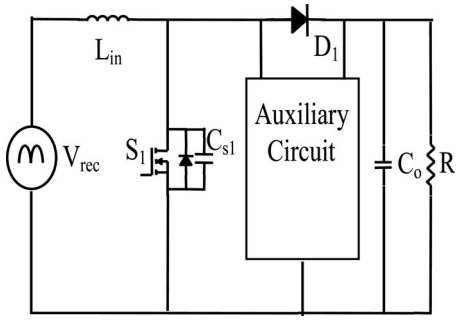


Fig. 3. Placement of ZVS auxiliary circuit in boost PFC converter.

For each converter in Fig. 4, the auxiliary switch is turned ON just before the main converter switch is to be turned ON. The auxiliary switch is used to discharge the capacitor across the main switch so that it can turn ON with ZVS. Some capacitance, either internal to the device and/or external, is needed to slow down the rise in voltage across the main switch so that it can turn OFF with ZVS. The auxiliary switch is turned OFF shortly after the main switch is turned ON, and all the energy in the auxiliary circuit is eventually transferred to the output. After this is done, the auxiliary circuit is fully deactivated and the converter operates like a conventional PWM converter. The components in the auxiliary circuit have lower ratings than those in the main power circuit because the circuit is active for a fraction of the switching cycle. This allows a device that can turn ON with fewer switching losses than the main switch to be used as the auxiliary switch.

The addition of an active auxiliary circuit to a PWM converter can also eliminate the reverse-recovery current of the main power boost diode if a Si device is used. It can be seen from Fig. 4 that all the auxiliary circuits have an inductor located in series with the auxiliary switch. This allows current to be gradually transferred away from the boost diode to the auxiliary switch when it is turned ON so that the charge in the diode is slowly removed during turn-OFF; with such a gradual transition from conduction state to OFF-state of the diode, its reverse-recovery current can be greatly reduced, thus, eliminating reverse recovery losses.

The key limitations of the previously proposed auxiliary circuits for single-switch boost PFC converters are the use of extra semiconductor devices such as diodes and MOSFETs [15]–[23] as well as passive components and the extra losses associated with the auxiliary circuit. In resonant-type auxiliary circuits, the main switch can suffer from addition current stress [20], while in nonresonant-type auxiliary circuits [15], the auxiliary switch may undergo hard switching; these key problems in ZVS auxiliary circuit tend to somewhat offset the gain in efficiency achieved by soft switching of the main boost switches. In addition, the gating pulse of the auxiliary switch needs to be precisely synchronized to that of the main switch, which adds to the complexity of the boost PFC control system.

Auxiliary circuits with active semiconductor devices have also been used to achieve ZVS in interleaved boost PFC converters [24]–[26]. The key issue related to such auxiliary circuits is

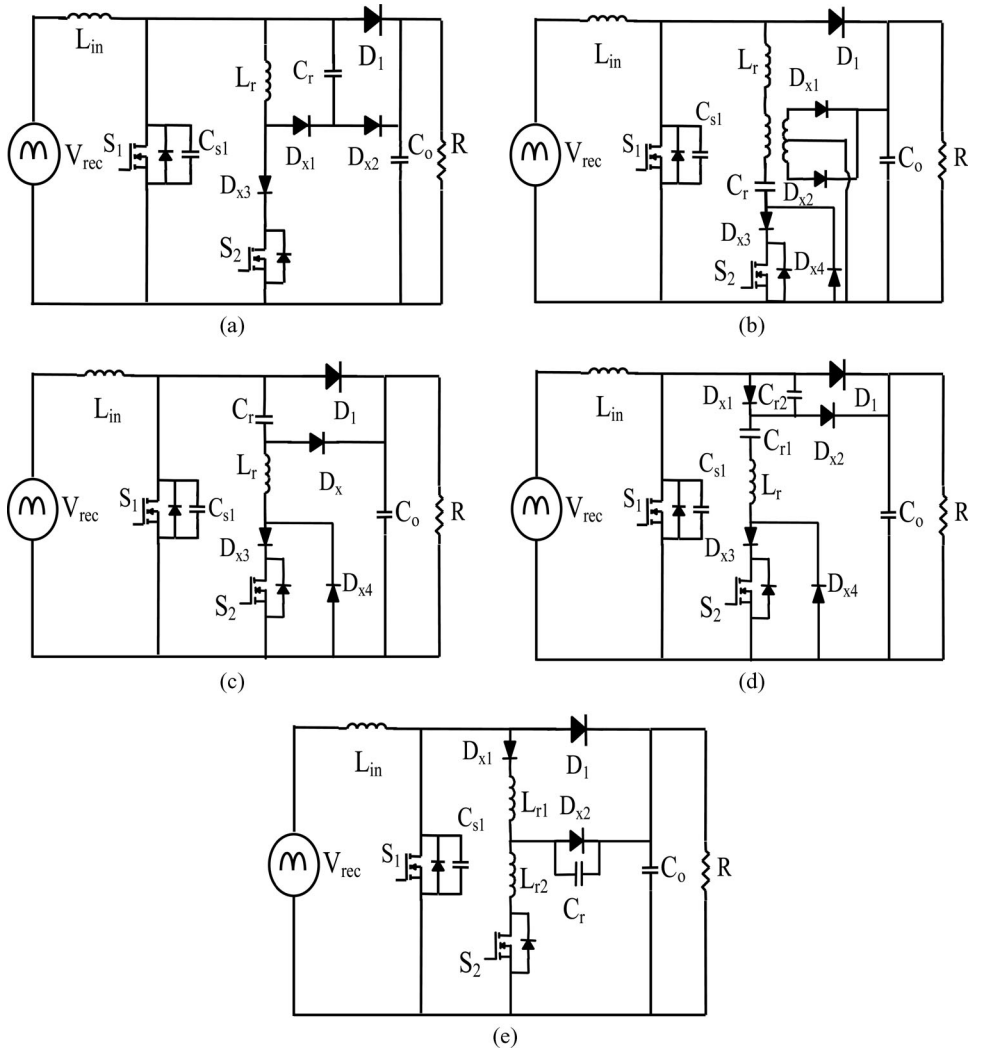


Fig. 4. ZVS-PWM ac–dc boost converters with active auxiliary circuits.

that basically two auxiliary circuits are implemented to achieve ZVS in both phases. This leads to use of multiple semiconductor switching devices to implement the auxiliary circuits [24]–[26], which increases the cost and complexity of the overall converter.

ZVS in interleaved boost converter can be easily achieved if the current in the boost inductors is always in critical conduction mode [27], but the main problem related to such critical conduction mode boost converters is the limitation of the maximum power handling capacity of the overall converter, typically such converters are applicable for operation around 1 kW and their inherent line current distortion. Magnetically coupled boost inductors in interleaved boost PFC converter can help achieving ZVS of the main switches [28], but design and mass replication of such coupled boost inductor cannot be done easily.

In [29], a simple passive auxiliary circuit was proposed to achieve ZVS in interleaved boost converter for dc–dc voltage conversion applications. The main drawback of this circuit is that the duty ratio of the boost switches has to remain strictly above 0.5, which cannot be guaranteed in PFC ac/dc applications especially for universal ac inputs that vary from 85 to 265 V_{rms}. In addition, the amount of reactive current flowing through this auxiliary circuit should be adjusted for the maximum load, so as to guarantee ZVS for all conditions. This causes excessive circulating current for light-load conditions and decreases the efficiency of the converter at light loads. In battery charger applications, since the converter has to operate at light loads for a long period of time, this constant circulating current significantly deteriorates the performance of the converter.

In this context, it should also be noted that in EV power conditioning systems, high efficiency of the power stages is imperative. The front-end ac/dc boost PFC converter plays a key role in transferring power from external utility mains to the EV battery packs, and the boost diodes in this converter are key source of losses. Presently, SiC diodes are gaining popularity in ac/dc boost converters [30] since they have near-zero reverse recovery losses but normally SiC diodes have greater forward voltage drops, typically 2.4 V and more as compared to 1.2 V in Si diodes for a 600 V device, which is required in this application. For instance, a 600-V 10-A SiC diode C3D10060A, from CREE, Inc., Durham, NC, has a forward voltage drop of 2.4 V compared to a 600-V 10-A fast recovery diode 10ETF06PBF, from Vishay, Shelton, CT, which has less than 1.2 V forward

voltage drop. In addition, the thermal coefficient of SiC diodes on the forward voltage drop is positive, implying that the voltage drop increases with temperature, while the one for Si diode is negative. Thus, the use of Si diodes in very high power (3 kW or more) ac/dc boost PFC converter contributes to high reverse-recovery losses, while the use of SiC diodes contributes to very high conduction losses in such converters.

In this paper, a novel interleaved boost PFC converter is proposed to achieve soft switching in the main switches of the converter. The proposed converter implements soft switching through a simple passive auxiliary circuit placed in between the two phases of the interleaved boost converter. This auxiliary circuit is able to provide reactive current to charge and discharge the output capacitors of the boost MOSFETs and guarantee ZVS. Since there are no extra semiconductors used in the auxiliary circuit, high efficiency and reliability are the main advantages of the proposed system. In addition, the proposed converter is able to optimize the amount of reactive current required to implement soft switching based on the load condition and the input voltage. Thus, the conduction losses caused by the auxiliary circuit are minimized based on the operating condition.

This paper is organized as follows. In Section II, the steady-state analysis of the proposed interleaved boost PFC converter is explained. A qualitative study of the proposed converter is given in Section III. Section IV presents the proposed control system for the interleaved boost converter. A summary of the design procedure for the auxiliary circuit inductor is provided in Section V. Experimental results obtained from a 3 kW prototype are presented in Section VI and finally Section VII is the conclusion.

II. Steady-State Analysis of the ZVS Interleaved Boost PFC Converter

Fig. 5 shows the power circuit of the ZVS interleaved boost PFC converter. In this converter, two boost converters operate with 180° phase shift in order to reduce the input current ripple of the converter. This 180° phase shift can be used to provide reactive current for realizing ZVS for power MOSFETs. This auxiliary circuit consists of a HF inductor and a dc-blocking capacitor. Since there may be a slight difference between the duty ratios of the two phases, this dc-blocking capacitor is necessary to eliminate any dc current arising from the mismatch of the duty ratios of the main switches in the practical circuit.

Fig. 6 shows the key waveforms of the converter for $D > 0.5$. According to this figure, there are eight operating modes in one switching cycle of the converter. The operating modes are explained as follows.

Mode I ($t_0 < t < t_1$): This mode starts when the gate pulse is applied to S_{A1}. Once the voltage is applied to the gate, S_{A1} is turned ON under zero voltage. Since S_{A1} and S_{B1} are ON during this interval, the voltage across the auxiliary inductor is zero. Thus, the current through the auxiliary circuit remains constant at $I_{\mathrm{Aux},p}$. During this interval, the switch S_{A1} current, i_{SA1}, is given by:

$$i_{SA1}(t) = I_V - I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{L_A}(t - t_0). \quad (1)$$

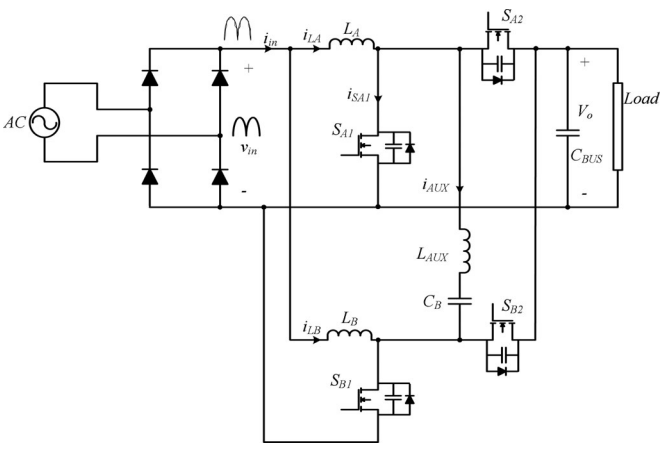


Fig. 5. Proposed ZVS interleaved boost PFC schematic.

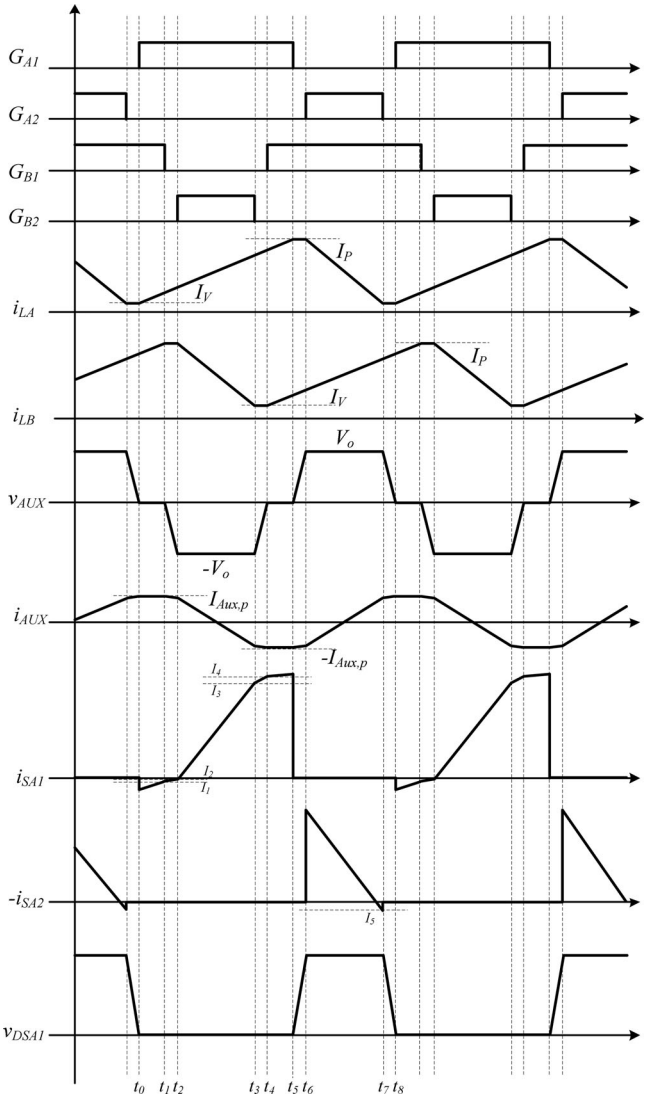


Fig. 6. Key waveforms of the converter for $D > 0.5$.

Since the two phases have 180° phase shift, the value of t_1 is given by:

$$t_1 - t_0 = (D - 0.5)\, T_s. \tag{2}$$

Therefore, the duty ratio is given by

$$D = (t_1 - t_0)\, f_s + \frac{1}{2}. \tag{3}$$

Inserting (2) into (1), the value of the switch current is calculated at t_1

$$I_1 = I_V - I_{\mathrm{Aux},p}(t) - \frac{v_{\mathrm{in}}}{2L_A f_s} - \frac{v_{\mathrm{in}}^2}{L_A f_s V_o}. \tag{4}$$

This mode ends once the gate voltage has been removed from S_{B1}.

Mode II ($t_1 < t < t_2$): This mode is the dead time between the phase B MOSFETs. During this interval, the auxiliary circuit current charges the output capacitance of S_{B1} and discharges the output capacitance of S_{B2}. In this mode, the average voltage across the boost inductance L_B is zero. Therefore, the current through L_B remains constant at its peak value. The voltage across the auxiliary inductor is given by:

$$v_{\mathrm{AUX}}(t) = -\frac{V_o}{(t_2 - t_1)}(t - t_1). \tag{5}$$

Thus, the current through auxiliary circuit is given by:

$$i_{\mathrm{AUX}}\,(t) = I_{\mathrm{Aux},p} - \frac{V_o}{2\,(t_2 - t_1)\, L_{\mathrm{AUX}}}\,(t - t_1)^2 \tag{6}$$

$t_2 - t_1 = t_d$ is the dead time between S_{B1} and S_{B2}. During this period, the output capacitors of the MOSFETs should fully charge and discharge in order to guarantee ZVS for S_{B1} and S_{B2}. Thus, the dead time is calculated as follows:

$$I_P + I_{\mathrm{Aux},p} - \frac{V_o}{2L_{\mathrm{AUX}}}t_d = 2C_{So}\frac{V_o}{t_d} \tag{7}$$

$$t_d = \frac{(I_P + I_{\mathrm{Aux},p})L_{\mathrm{AUX}}}{V_o} + \sqrt{\frac{(I_P + I_{\mathrm{Aux},p})^2 L_{\mathrm{AUX}}^2}{V_o^2} - 4C_{So}L_{\mathrm{AUX}}} \tag{8}$$

the current through switch S_{A1} is calculated as follows:

$$i_{SA1}\,(t) = I_V - I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{L_A}\,(t - t_0) + \frac{V_o}{2t_d L_{\mathrm{AUX}}}\,(t - t_1)^2\,. \tag{9}$$

This mode ends when the output capacitors completely charged and discharged. The switch current i_{SA1} at this point is given by:

$$I_2 = I_V - I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{L_A}\,(t_d + t_1 - t_0) + \frac{V_o}{2L_{\mathrm{AUX}}}t_d. \tag{10}$$

Mode III ($t_2 < t < t_3$): Once the output capacitors of S_{B1} and S_{B2} have been charged and discharged completely, the gate signal of S_{B2} is applied and S_{B2} is turned ON under ZVS. During this interval, the voltage across the auxiliary circuit is $-V_o$. The current through the auxiliary inductor, inductor L_A and switch S_{A1}, is given by:

$$i_{\mathrm{AUX}} = I_{\mathrm{Aux},p} - \frac{V_o}{2L_{\mathrm{AUX}}}t_d - \frac{V_o}{L_{\mathrm{AUX}}}\,(t - t_2) \tag{11}$$

$$i_{LA}(t) = I_V + \frac{v_{\mathrm{in}}}{L_A}\,(t - t_0)\,. \tag{12}$$

$$i_{SA1}\,(t) = I_V - I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{L_A}\,(t - t_0) + \frac{V_o}{2L_{\mathrm{AUX}}}t_d + \frac{V_o}{L_{\mathrm{AUX}}}\,(t - t_2)\,. \tag{13}$$

This mode ends once the gate signal of S_{B2} has become zero ($t_3 = t_0 + 0.5\,T_s - t_d$). The value of i_{SA1} at this point is given by:

$$I_3\,(t) = I_V - I_{\mathrm{Aux},p} + \frac{v_{\mathrm{in}}}{2f_s L_A} - \frac{v_{\mathrm{in}}t_d}{L_A} + \frac{V_o}{2L_{\mathrm{AUX}}}t_d + \frac{V_o}{f_s L_{\mathrm{AUX}}}\,(1 - D) - \frac{2V_o}{L_{\mathrm{AUX}}}t_d. \tag{14}$$

Mode IV ($t_3 < t < t_4$): During this mode, the output capacitor of S_{B2} is charging from zero to V_o and the output capacitor of S_{B1} is discharging from V_o to zero. This period is actually the dead time between S_{B2} and S_{B1} ($t_4 - t_3 = t_d$). The auxiliary inductor current, the boost inductor current, and the switch current, during this mode, is given by:

$$i_{\mathrm{AUX}}\,(t) = I_{\mathrm{Aux},p} + \frac{3V_o}{2L_{\mathrm{AUX}}}t_d - \frac{V_o}{f_s L_{\mathrm{AUX}}}\,(1 - D) - \frac{V_o}{2t_d L_{\mathrm{AUX}}}\,(t - t_3)^2 \tag{15}$$

$$i_{LA}(t) = I_V + \frac{v_{\mathrm{in}}}{L_A}\,(t - t_0) \tag{16}$$

$$i_{SA1}\,(t) = I_V - I_{\mathrm{Aux},p} - \frac{v_{in}}{L_A}\,(t - t_0) + \frac{V_o}{2L_{\mathrm{AUX}}}t_d + \frac{V_o}{L_{\mathrm{AUX}}}\,(t - t_2)\,. \tag{17}$$

This mode ends once the gate signal is applied to S_{B1}. The value of i_{SA1} at this instant is given by:

$$I_4\,(t) = I_V - I_{\mathrm{Aux},p} + \frac{v_{\mathrm{in}}}{2f_s L_A} + \frac{V_o}{L_{\mathrm{AUX}}}t_d + \frac{V_o}{f_s L_{\mathrm{AUX}}}\,(1 - D). \tag{18}$$

Mode V ($t_4 < t < t_5$): This mode starts when the gate signal is applied to S_{B1}. Once the gate has been applied, S_{B1} is turned ON under ZVS. Since S_{A1} and S_{B1} are ON during this period, the voltage across the auxiliary inductor is zero; hence, the auxiliary inductor current remains constant at its peak value, $I_{\mathrm{Aux},p}$. The boost inductor current and the switch current, during this mode, are given by:

$$i_{LA}(t) = I_V + \frac{v_{\mathrm{in}}}{L_A}\,(t - t_0) \tag{19}$$

$$i_{SA1}\,(t) = I_V + I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{L_A}\,(t - t_0)\,. \tag{20}$$

This mode ends once the gate signal is removed from S_{A1}. The value of i_{SA1} at this time is given by:

$$i_{SA1}(t) = I_V + I_{\mathrm{Aux},p} - \frac{v_{\mathrm{in}}}{f_s L_A} D. \tag{21}$$

Mode VI ($t_5 < t < t_6$): During this mode, the output capacitor of S_{A1} is charging from zero to V_o and the output capacitor of S_{A2} is discharging from V_o to zero. This period is actually the dead time between S_{A1} and S_{A2} ($t_6 - t_5 = t_d$). In this period, the current through the boost inductor L_A remains constant at its peak value. The auxiliary inductor current i_{AUX} is given by:

$$i_{\mathrm{AUX}}(t) = -I_{\mathrm{Aux},p} + \frac{V_o}{2t_d L_{\mathrm{AUX}}} (t - t_5)^2. \tag{22}$$

This mode ends once the output capacitors have completely been charged and discharged.

Mode VII ($t_6 < t < t_7$): During this mode, the voltage across the auxiliary circuit is V_o; hence, the current through the auxiliary circuit is given by:

$$i_{\mathrm{AUX}}(t) = -I_{\mathrm{Aux},p} + \frac{V_o}{2L_{\mathrm{AUX}}} t_d + \frac{V_o}{L_{\mathrm{AUX}}} (t - t_6). \tag{23}$$

During this mode, the MOSFET channel S_{A2} is conducting the current to the output. The current through this switch is given by:

$$i_{SA2}(t) = I_{\mathrm{Aux},p} - \frac{V_o}{2L_{\mathrm{AUX}}} t_d + \frac{V_o}{L_{\mathrm{AUX}}} (t - t_6) + I_P - \frac{v_{\mathrm{in}} - V_o}{L_A} (t - t_6). \tag{24}$$

The peak value of this current is given by:

$$I_5(t) = -I_{\mathrm{Aux},p} + \frac{V_o}{2L_{\mathrm{AUX}}} t_d + I_P. \tag{25}$$

This mode ends when i_{SA2} reaches zero. Thus t_7 is given by:

$$t_7 = t_6 + \frac{I_{\mathrm{Aux},p} - (V_o/2L_{\mathrm{AUX}}) t_d}{(V_o/L_{\mathrm{AUX}}) + (v_{\mathrm{in}} - V_o/L_A)}. \tag{26}$$

Mode VIII ($t_7 < t < t_8$): During this mode, the output capacitor of S_{A1} is discharging from V_o to zero and the output capacitor of S_{A2} is charging from zero to V_o. In this mode, the current through L_A is at its minimum value I_V and the excess current from the auxiliary circuit charges and discharges the output capacitors. The auxiliary inductor current is given by:

$$i_{\mathrm{AUX}}(t) = -I_{\mathrm{Aux},p} + \frac{V_o}{2L_{\mathrm{AUX}}} t_d + \frac{V_o}{L_{\mathrm{AUX}}} \frac{I_{\mathrm{Aux},p} - (V_o/2L_{\mathrm{AUX}}) t_d}{(V_o/L_{\mathrm{AUX}}) + ((v_{\mathrm{in}} - V_o)/L_A)} + \frac{V_o}{2L_{\mathrm{AUX}}} (t - t_7)^2. \tag{27}$$

Since this mode is the dead time between S_{A1} and S_{A2}, $t_8 = t_7 + t_d$. This mode ends once the output capacitors have been charged and discharged completely. Fig. 7 shows the key waveforms of the circuit for $D < 0.5$. According to this figure, the modes of operation are the same for the proposed circuit.

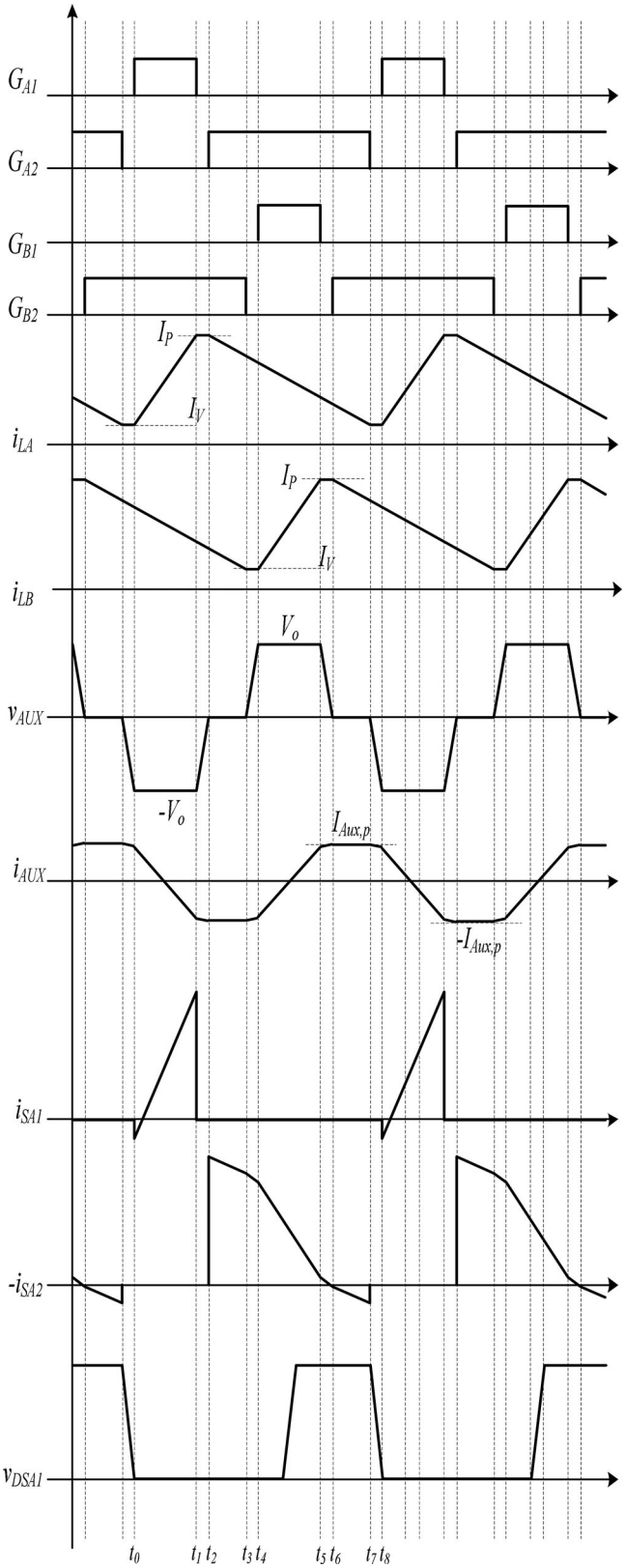


Fig. 7. Key waveforms of the converter for $D < 0.5$.

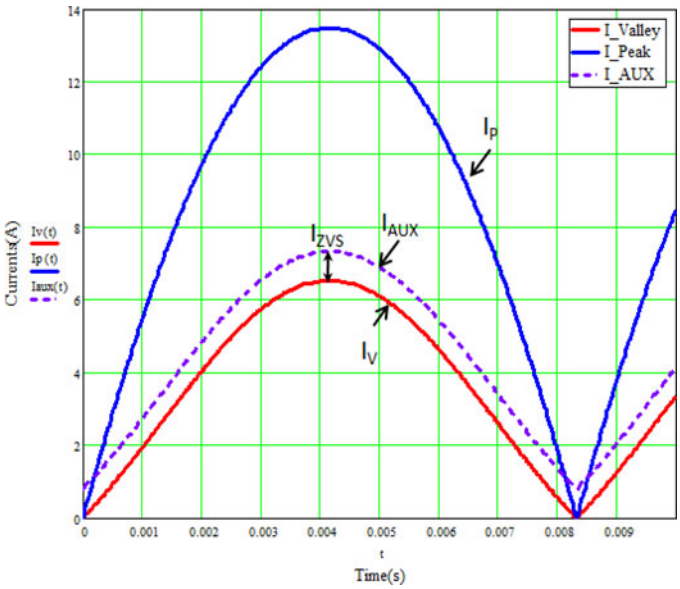


Fig. 8. Boost inductor valley current, peak current, and auxiliary inductor current.

III. Qualitative Study

In this section, some salient features of the proposed converter are discussed. According to the waveforms of the converter in Figs. 6 and 7, all MOSFETs of the interleaved boost converter are turned ON under zero voltage and the output MOSFETs are turned OFF at nearly zero current. This implies that the MOSFETs enjoy having near-zero switching losses. In order to guarantee ZVS for the MOSFETs, the inductive current of the auxiliary circuit should be enough to neutralize the input current and discharge and charge the output capacitors of the MOSFETs during turn-ON times of S_{A1} and S_{B1}. Also, the dead time between the gate pulses should be enough to allow complete charging and discharging of the output capacitors of the switches. Therefore, first the auxiliary inductor should be designed so as to provide enough inductive current to charge and discharge the capacitors, then the dead time should be properly adjusted to have enough time to complete the charge and discharge. Since the input current helps to charge and discharge the output capacitors of S_{A2} and S_{B2}, ZVS is automatically guaranteed for S_{A2} and S_{B2}.

Fig. 8 shows the boost inductor valley current, peak current, and the auxiliary inductor current. In order to guarantee ZVS, the auxiliary inductor current not only should neutralize the valley current I_V, but also should provide enough current to charge and discharge the output capacitors. The valley current I_V and the peak current I_P are given by:

$$I_V(t) = \frac{P_{\text{in}}}{V_{\text{in}}}|\sin(\omega_l t)| - \frac{V_{\text{in}} \cdot |\sin(\omega_l t)|1 - (V_{\text{in}}|\sin(\omega_l t)|)/V_o}{2L_A f_s} \quad (28)$$

$$I_P(t) = \frac{P_{\text{in}}}{V_{\text{in}}}|\sin(\omega_l t)| + \frac{V_{\text{in}}|\sin(\omega_l t)|(1 - (V_{\text{in}}|\sin(\omega_l t)|)/V_o)}{2L_A f_s}. \quad (29)$$

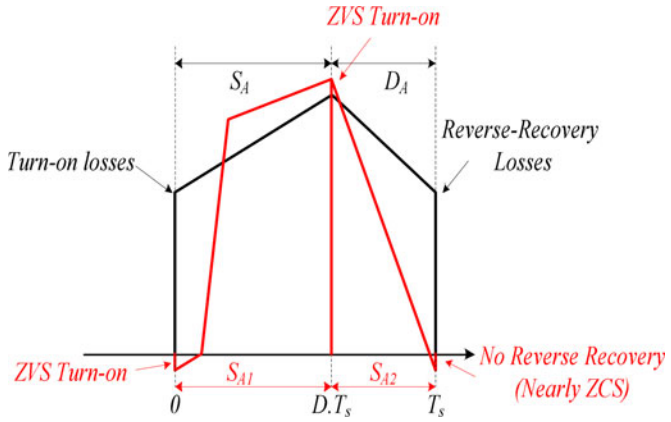


Fig. 9. Semiconductors' current waveforms for the conventional boost PFC and the proposed interleaved boost PFC.

The peak value of the auxiliary inductor current $I_{\text{Aux},p}$ is given by:

$$I_{\text{Aux},p}(t) = \frac{P_{\text{in}}}{V_{\text{in}}}|\sin(\omega_l t)| - \frac{V_{\text{in}}|\sin(\omega_l t)|1 - (V_{\text{in}}|\sin(\omega_l t)|)/V_o}{2L_A f_s} + \frac{2C_{So}V_o}{t_d}. \quad (30)$$

Fig. 9 compares the current waveforms of the MOSFET and boost diode in the conventional boost PFC converter and those of the MOSFETs in the interleaved boost PFC with the auxiliary circuit. According to this figure, there are two main sources of switching losses in the conventional boost PFC converter. The first source of switching losses is the turn-ON losses of the boost MOSFET and the second source is the reverse recovery of the output diode. The former one not only deteriorates the efficiency of the converter, but also introduces a lot of switching noise through the drain–gate capacitance of the MOSFET to the control circuit. This leads to an unreliable operation of the converter, while the later one creates a lot of losses in the converter. Recently, SiC diodes are used to mitigate the reverse-recovery losses of the output diodes. However, the SiC diodes usually have a large forward voltage drop for this application (typically the forward voltage drop in SiC diodes is 2.4 V as compared to around 1.2 V in Si diodes), which creates extra conduction losses in the converter during their conduction intervals and effectively decreases the advantage such diodes have due to zero reverse recovery, especially at very high output power and low ac inputs.

According to Fig. 9, the proposed auxiliary circuit can effectively cancel out the positive current imposed by the input inductor during the MOSFET turn-ON times and completely eliminate the turn-ON losses of the boost MOSFET. In addition, the auxiliary inductor current brings down the current prior to the output MOSFET turn-OFF times; hence, the output MOSFET undergoes near zero-current switching (ZCS) turn-OFF. Therefore, the switching losses are almost zero in the proposed converter.

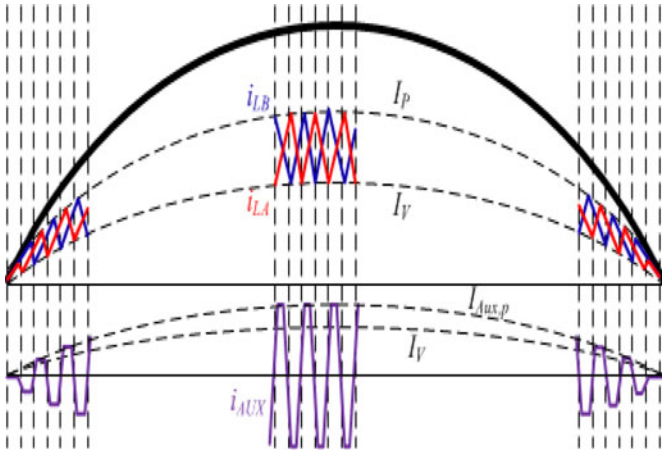


Fig. 10. Boost inductor currents and auxiliary circuit current.

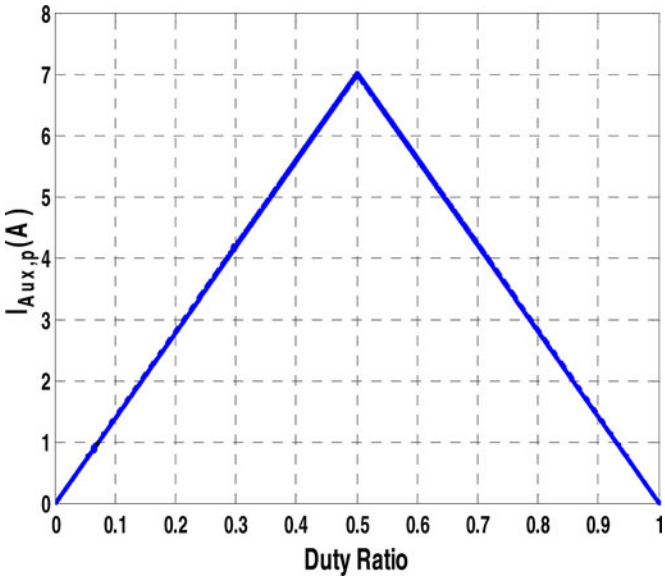
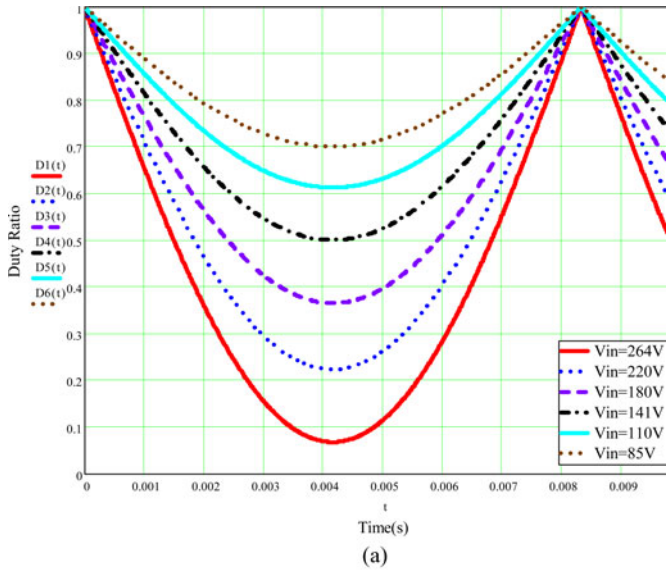
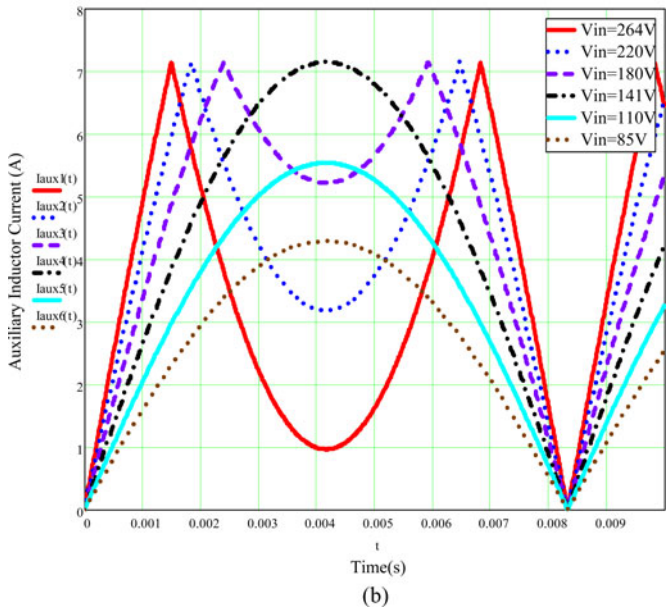


Fig. 11. Auxiliary circuit maximum current versus duty ratio.



(a)



(b)

Fig. 12 (a) Duty ratios for different input voltage. (b) Auxiliary circuit maximum current for different input voltage.

IV. Proposed Control System

Fig. 10 shows the current through the boost inductors and the auxiliary circuit current in half line cycle. According to this figure, the envelope of the auxiliary circuit current should be slightly higher than the valley current of each boost inductors. This implies that in order to optimally control the amount of reactive current through the auxiliary circuit, the peak value of the auxiliary inductor current should follow the envelope given by (30), which implies that the envelope of the auxiliary circuit current should be at its maximum when the boost inductor current is at its maximum. Fig. 11 shows the peak value of the auxiliary inductor current versus the boost duty ratio. According to this figure, for duty ratios higher than 0.5, the maximum value of the auxiliary circuit current decreases as duty ratio increases. This implies that if the input voltage is low enough to have duty ratios higher than 0.5 for the whole line cycle, the envelope of the auxiliary current follows the shape of the inductor current. In other words, the peak value of the auxiliary inductor current is maximum at the peak value of the input voltage, and as the input voltage decreases to zero, the peak value of the auxiliary inductor decreases to zero too. Fig. 12(a) and (b) illustrates this phenomenon. These figures show the variation of the duty ratio and the envelope of the auxiliary circuit current for different input voltages, respectively. According to this figure, the auxiliary circuit operates optimally if the duty ratios are higher than 0.5 during the half line cycle. This condition is satisfied for input voltages less than 141 and 400 V_{dc} output. However, for universal input voltage range (85 to 265 V_{rms}),

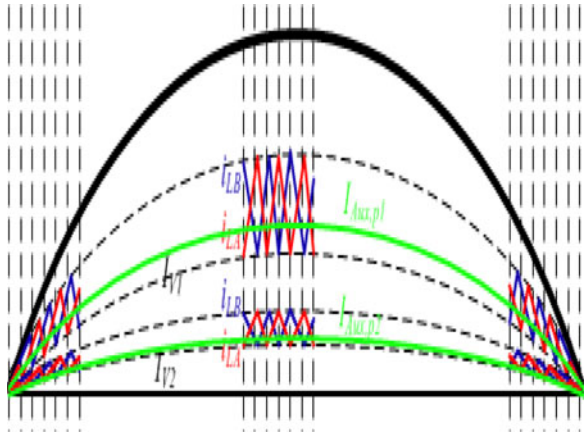


Fig. 13. Auxiliary circuit maximum current for different loads.

this condition is not satisfied and duty ratio becomes very small for higher voltages.

In addition, the peak value of the auxiliary circuit current should be adjusted based on the load condition in order to optimize the circulating current between the two phases of the interleaved boost converter. Fig. 13 depicts the optimal envelopes of the auxiliary circuit current for different loads. Therefore, in order to optimize the circulating current, the envelope should be just enough to overcome the valley current of the boost inductor in the half cycle.

Considering the aforementioned discussion, there are two main difficulties related to the optimization of the circulating current in the proposed converter. The first problem is the operation with duty ratios lesser than 0.5 and the second issue is optimizing the circulating current for different load conditions. Fig. 14 shows the block diagram of the proposed control system. The proposed control system includes an external voltage loop, internal current loop, and a switching frequency control loop. Therefore, a frequency loop is added to the control system to optimize the circulating current of the auxiliary circuit based on the load and duty ratio of the converter. Such load-adaptive switching frequency variation has been proved to increase efficiency in ZVS converters [36].

Fig. 15 shows the typical switching frequency variation at heavier and lighter loads. At heavy loads, the frequency is lower to provide more reactive current in the auxiliary circuit to overcome higher values of I_V and charge and discharge the output capacitors. Whereas at light loads, the frequency is higher to reduce the auxiliary circuit current in order to avoid any extra circulating current between the two phases. The required auxiliary circuit current for different loads is determined by:

$$I_{\mathrm{Aux},p} = I_{\mathrm{ref}} - \frac{\Delta i_{LA}}{2} + \frac{2C_{So}V_o}{t_d}. \tag{31}$$

The auxiliary circuit current is given by:

$$I_{\mathrm{Aux},p} = \frac{v_{\mathrm{in}}}{2L_{\mathrm{AUX}}f_s}. \tag{32}$$

The boost inductor ripple is given by:

$$\Delta i_{LA} = \frac{v_{\mathrm{in}}(1-(v_{\mathrm{in}}/V_o))}{L_A f_s}. \tag{33}$$

Inserting (32) and (33) into (31) determines the desired switching frequency of the converter

$$f_{s1} = \frac{v_{\mathrm{in}}L_A + v_{\mathrm{in}}(1-(v_{\mathrm{in}}/V_o))L_{\mathrm{AUX}}}{I_{\mathrm{ref}} + (2C_{So}V_o/t_d)}. \tag{34}$$

Fig. 16 shows the variation of the frequency with respect to the converter output power. Owing to the change of frequency, the circulating current is optimized for a very wide range of operation. Since the converter is used to charge the traction battery, there is actually a need for very wide range of operating conditions and the converter has to work at very light loads for a long period of time also. Thus, this optimization is imperative in this particular application.

The other issue regarding the auxiliary circuit was the operation with less than 0.5 duty ratio for input voltage higher than 141 V_{rms}. In order to accommodate this issue, another block is added to the control circuit to modify the frequency for duty ratios less than 0.5. Fig. 17 illustrates the operation of the auxiliary circuit for high input voltage. The auxiliary circuit follows the sinusoidal waveform from $D = 1$ to $D = 0.5$. However, afterward, the auxiliary circuit current decreases, which hinders the auxiliary circuit to provide ZVS condition for the power MOSFETs. In the proposed control system, the frequency is modified once the duty ratio has reached 0.5. The frequency profile and the modified auxiliary circuit current are depicted in Fig. 17. The peak value of the auxiliary circuit current is given by:

$$I_{\mathrm{Aux},p} = \begin{cases} \dfrac{V_o D}{2L_{\mathrm{AUX}}f_s} & \text{for } D < 0.5 \\ \dfrac{V_o(1-D)}{2L_{\mathrm{AUX}}f_s} & \text{for } D \geq 0.5 \end{cases}. \tag{35}$$

Therefore, the frequency can be modified so as to follow the sinusoidal reference for the auxiliary circuit current. Frequency profile as a function of duty ratio is shown in Fig. 18. According to this figure, the frequency is constant from $D = 1$ to $D = 0.5$, and after this point, the frequency is modified to have the auxiliary current follow the sinusoidal waveform, as shown in Fig. 18. Therefore, for $D < 0.5$ (or $v_{\mathrm{in}} > 200$ V), the frequency is given by:

$$f_s = \frac{(1-(v_{\mathrm{in}}/V_o))}{v_{\mathrm{in}}/V_o} f_{s1}. \tag{36}$$

There are two main points related to the proposed control system. First, the frequency loop is completely decoupled from the duty cycle loop. Fig. 19 illustrates the fact that by changing the frequency of the saw-tooth counter, the duty cycle does not change (i.e., $D_1 = D_2$). Second, the frequency change does not tamper the operating modes of the converter in terms of operating under CCM of the input inductors. Since the frequency is higher for light loads, the control system helps the converter to work in CCM for wider range of loads. In addition, for higher

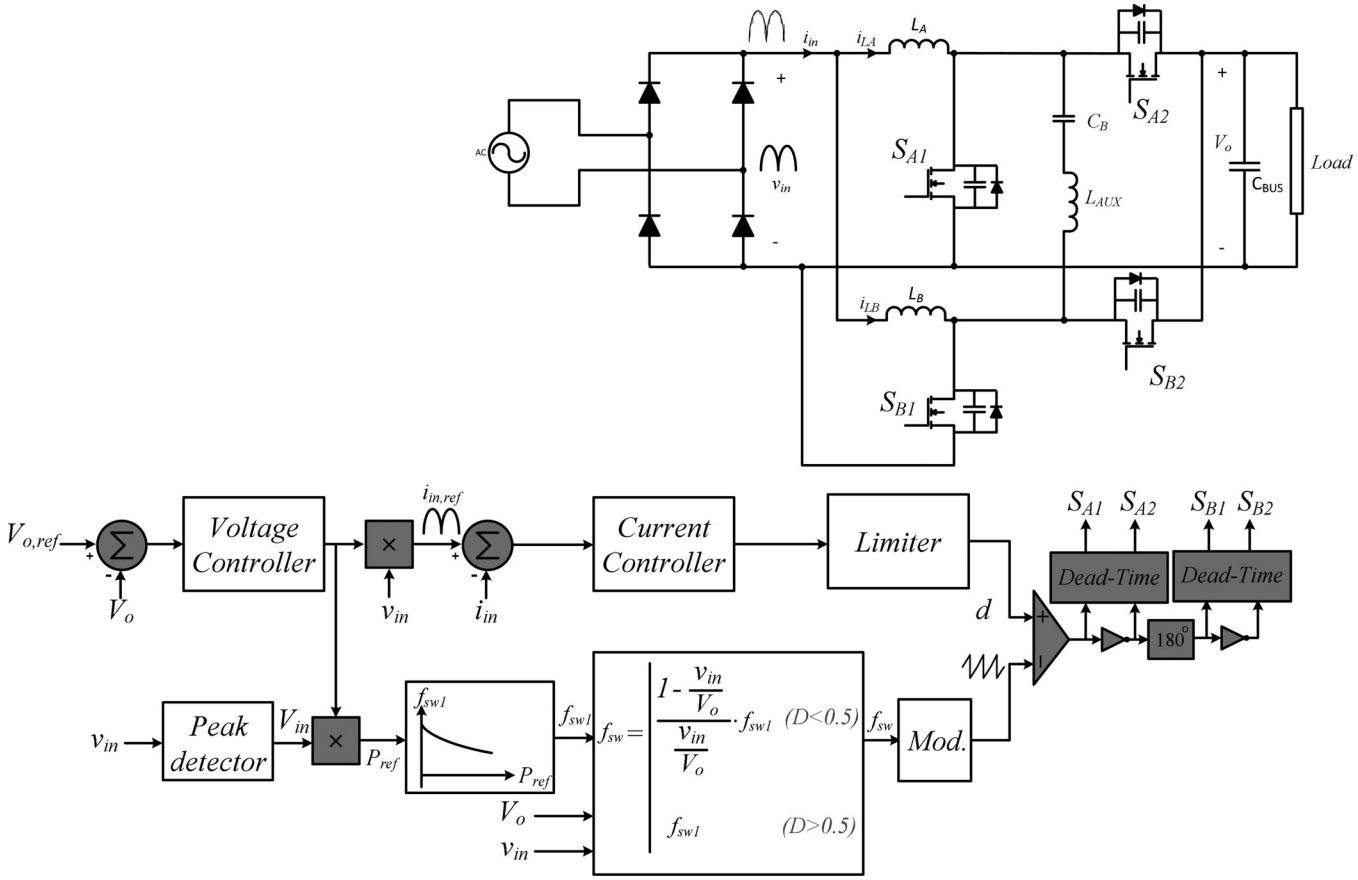


Fig. 14. Control system block diagram.

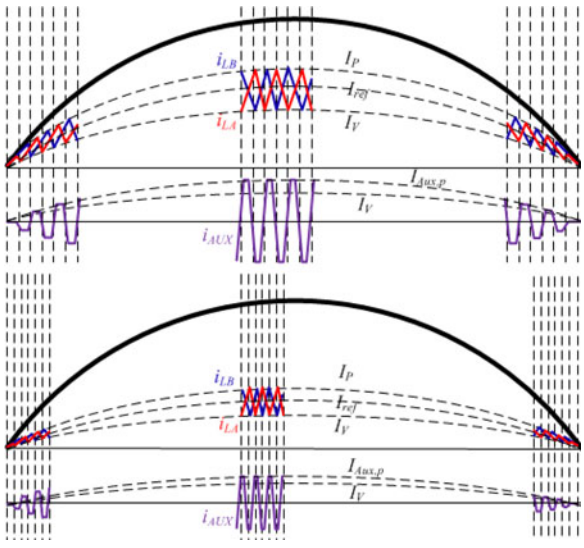


Fig. 15. Frequency change for different loads.

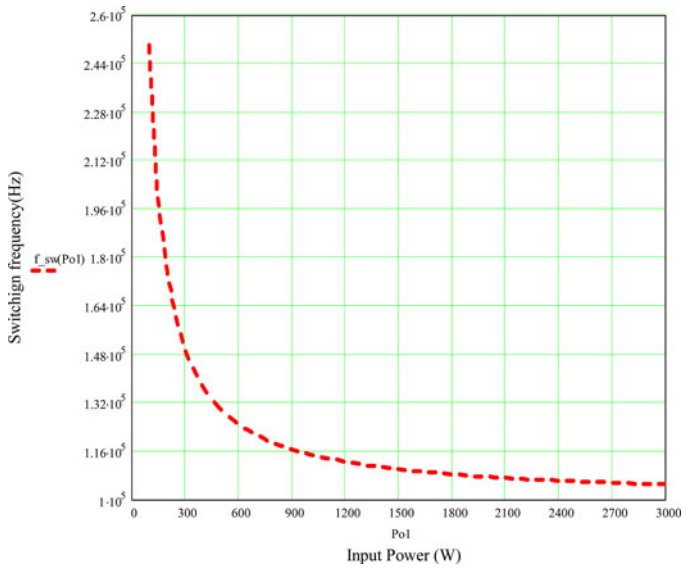


Fig. 16. Switching frequency variation versus load.

input voltage, frequency decreases at the peak value of the input current. Therefore, reducing the frequency does not bring the converter into discontinuous conduction mode.

V. Auxiliary Inductor Design

In this section, the design of the auxiliary inductor is explained in detail. The auxiliary inductor should be designed so as to

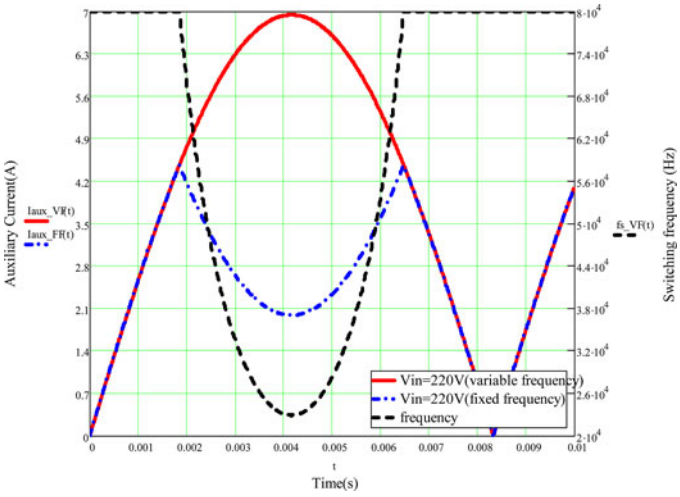


Fig. 17. Typical switching frequency variation for half an input ac line cycle above 141 V_{rms}.

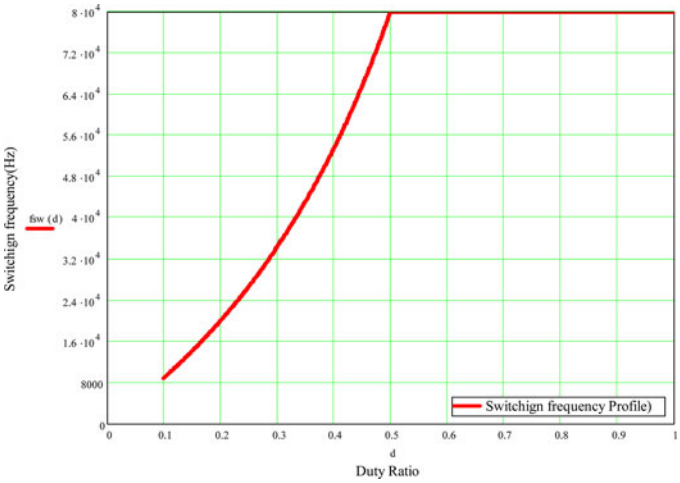


Fig. 18. Switching frequency variation versus duty ratio.

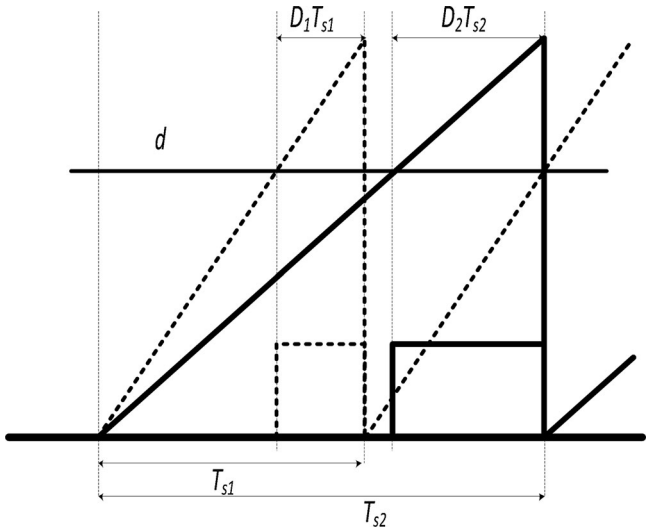


Fig. 19. PWM pulses for different frequencies.

provide enough energy to neutralize the energy in the boost inductor as well as charge and discharge the output capacitors of the MOSFETs. Thus, the key design criteria which needs are as follows.

1) Design the auxiliary inductor to have enough energy to be able to neutralize the valley current of the boost inductor and charge and discharge the output capacitors of the MOSFETs.
2) Design enough dead time to provide enough time for the output capacitors to charge and discharge.

The energy required to neutralize the boost inductor and charge and discharge the output capacitors of the MOSFETs is given by:

$$W = \frac{1}{2}L_A\left(\frac{P_{\rm in}}{V_{\rm in}} - \frac{V_{\rm in}\left(1-(V_{\rm in}/V_o)\right)}{2L_A f_s}\right)^2 + C_{So}V_o^2. \quad (37)$$

The energy of the auxiliary inductor should be greater or equal to the energy derived in (37). Therefore, we have:

$$\frac{1}{2}L_{\rm AUX}I_{{\rm Aux},p}^2 \geq \frac{1}{2}L_A \times \left(\frac{P_{\rm in}}{V_{\rm in}} - \frac{V_{\rm in}\left(1-(V_{\rm in}/V_o)\right)}{2L_A.f_s}\right)^2 + C_{So}V_o^2. \quad (38)$$

The peak value of the auxiliary circuit is given by:

$$I_{{\rm Aux},p} = \frac{V_o\left(1-(V_{\rm in}/V_o)\right)}{2L_{\rm AUX}f_s}. \quad (39)$$

Inserting (39) into (38) results in the following:

$$L_{\rm AUX} \leq \frac{\left(V_{\rm in}^2\left(1-(V_{\rm in}/V_o)\right)^2/4f_s^2\right)}{L_A\left(\left(P_{\rm in}/V_{\rm in}\right)-\left(V_{\rm in}\left(1-(V_{\rm in}/V_o)\right)/2L_A f_s\right)\right)^2 + 2C_{So}V_o^2}. \quad (40)$$

The dead time should be designed based on (8), which is rewritten again:

$$t_d = \frac{(I_P + I_{{\rm Aux},p})L_{\rm AUX}}{V_o} + \sqrt{\frac{(I_P + I_{{\rm Aux},p})^2 L_{\rm Aux}^2}{V_o^2} - 4C_{So}L_{\rm AUX}}. \quad (41)$$

Therefore, the design procedure is summarized in the following steps.

1) Select the minimum switching frequency, which corresponds to the peak value of the input current.
2) Calculate the value of the auxiliary inductance using (40).
3) Choose dead time so as to have enough time to completely charge and discharge the output capacitors of the MOSFETs using (41).

TABLE I
CONVERTER SPECIFICATIONS

Symbol	Parameter	Value
Po	Output Power	3KW
Vac	Input Voltage	170-267VAC
Vo	Output Voltage	235-431VDC
f_{sb}	Interleaved boost switching frequency	80KHz
f_{sf}	Full-Bridge Switching Frequency	220 KHz
$I_{in(max)}$	Maximum input current	16A
I_{inrush}	Maximum inrush current	32A
$P.F.$	Power Factor	> 98%

TABLE II
CONVERTER PARAMETERS

Symbol	Parameter	Value
L_A,L_B	Boost Inductor	270uH
C_{BUS}	Output Capacitor	1.4mF
C_B	Dc Blocking Capacitor	1uF
L_{AUX}	Auxiliary Inductor	120uH
S_{A1},S_{A2},S_{B1} ,S_{B2}	Power MOSFETs	STx25NM50N

VI. EXPERIMENTAL RESULTS

A 3 kW prototype is implemented to verify the performance of the proposed converter. The converter specifications are shown in Table I and the designed parameters are shown in Table II. Fig. 20 illustrates the system block diagram. At the input stage, there is an inrush current protection, which limits the inrush current of the converter. Since there is usually a big capacitor at the output of the PFC, the inrush current to charge the capacitor is very high and a circuit is required to limit this current. The next block is the electromagnetic interference (EMI) filter, which is designed to comply with the EMI standard (CISPR25/12) for EVs [31], [32]. The following block is the input diode rectifier. It rectifies the input voltage for the two-phase interleaved boost converter. The interleaved boost converter converts the rectified input voltage to the intermediate dc-bus voltage. The output capacitor of the interleaved boost converter is large (1.4 mF) in order to decrease the 2nd harmonic voltage ripple caused by the power ripple of the input boost PFC converter. In addition, there is a differential-mode (DM) filter at the output of the PFC in order to filter out the DM noise. At the output of this filter, a clean dc-bus voltage is provided to the full-bridge converter. Note that another EMI filter is required at the output of the full-bridge converter in order to provide filtering for the EMI noise injected by the inverter. Since the inverter is connected to the high-energy battery, it injects switching noise to the battery charger.

In order to implement the proposed controller, TMX320F28335 eZdSP board is employed. This DSP board has a floating-point DSP, which offers a very flexible environment for advanced mathematical calculations. This DSP has a 12-bit ADC with a sequencer that is able to convert multiple analog signals sequentially [33]. It also has six enhanced PWM (EPWM) modules, which can produce the desired PWM signals with a very high degree of flexibility [34]. The EPWM channels can be practically used up to 100 KHz. However, for the higher frequency range, high-resolution EPWM should be used to achieve a high-resolution PWM signal and to avoid limit cycle and instability. The high-resolution module is embedded in the DSP [35]. Since switching frequency is in the range of 50–240 KHz for the PFC and 220 KHz for the full-bridge converter, the high-resolution module should be utilized to produce the PWM pulses. In order to verify the performance of the proposed converter, two converters are implemented. The first one is the conventional interleaved boost PFC and the second one is the proposed converter.

Fig. 21(a) and (b) shows the prototype of the converter. Fig. 21(a) shows the control, communication, and protection circuits, and Fig. 21(b) illustrates the power circuit of the ac/dc converter.

Fig. 22 illustrates the waveforms of the conventional interleaved boost PFC converter. In Fig. 22, the gate pulse and the drain–source voltage of the boost MOSFET are depicted. According to this figure, the boost MOSFET is hard switched during the turn-ON and there are a lot of switching losses plus switching noise generated by the hard switching.

Fig. 23 shows the waveforms of the proposed converter. According to this figure, the boost MOSFET is turned-ON under zero voltage. This is due to the negative current provided by the auxiliary circuit. Basically, this figure shows that the output capacitor of the boost MOSFET is completely discharged prior to applying the gate signal and once the voltage across the MOSFET has become zero, the gate signal is applied to the MOSFET.

Fig. 24 shows the waveforms of the two phases of the proposed interleaved boost PFC converter as well as the auxiliary circuit current. This figure explains how the auxiliary circuit provides the reactive current for the both phases at the same time. The waveforms of the proposed converter for large duty ratios are shown in Fig. 25. Fig. 26 illustrates that the auxiliary circuit current changes during a line cycle based on the input current. The auxiliary circuit current is at its minimum at the zero crossing points of the input current and it is at its maximum at the peak of the input current. This implies that the auxiliary circuit current adaptively changes based on the shape of the input current and is optimized over the line cycle.

Fig. 27 illustrates the auxiliary circuit current around the input current zero crossing point and Fig. 28 shows the proposed converter waveforms around the peak point of the input current. Fig. 29 shows the input voltage and the input current of the proposed converter for 30% load and Fig. 30 illustrates the ones for full load. It can be seen that the input current and input ac voltage are absolutely in phase, thus, maintaining near unity (0.999) power factor.

Fig. 31 shows the phase A boost inductor current and the boost MOSFET drain–source voltage. The input current and phase A boost inductor currents are shown in Fig. 32. Figs. 33 and 34

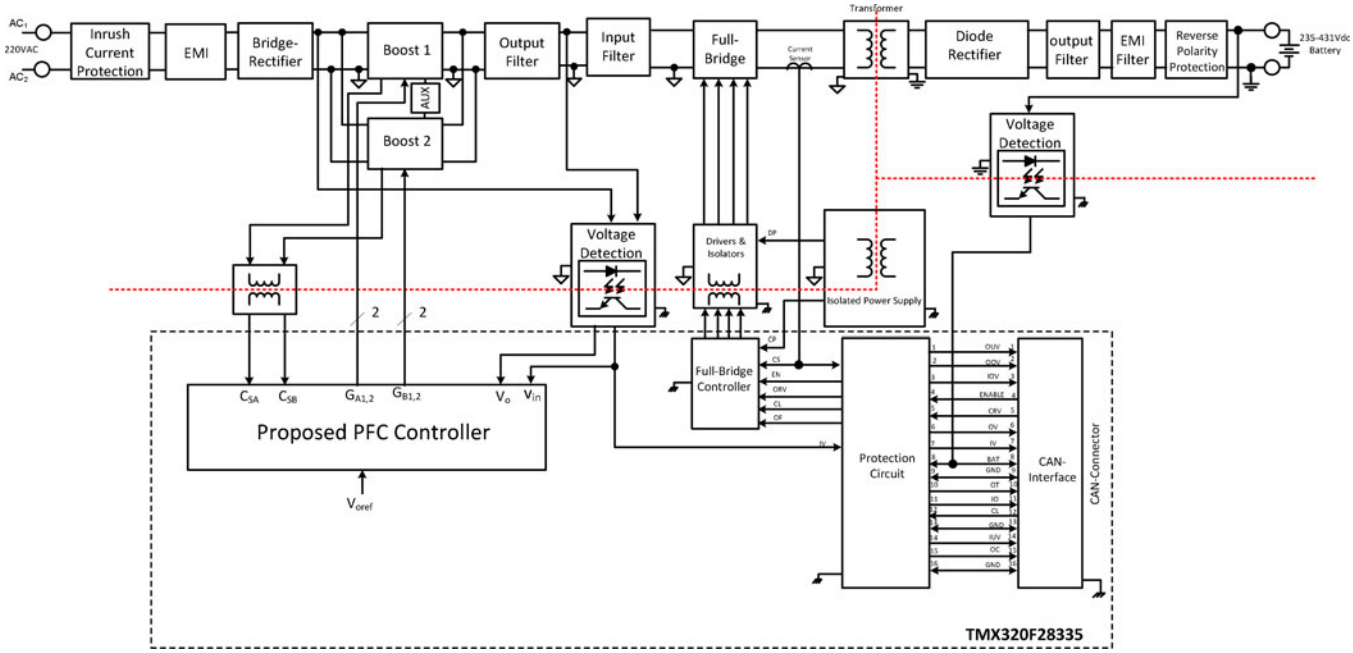


Fig. 20. AC/DC converter block diagram.

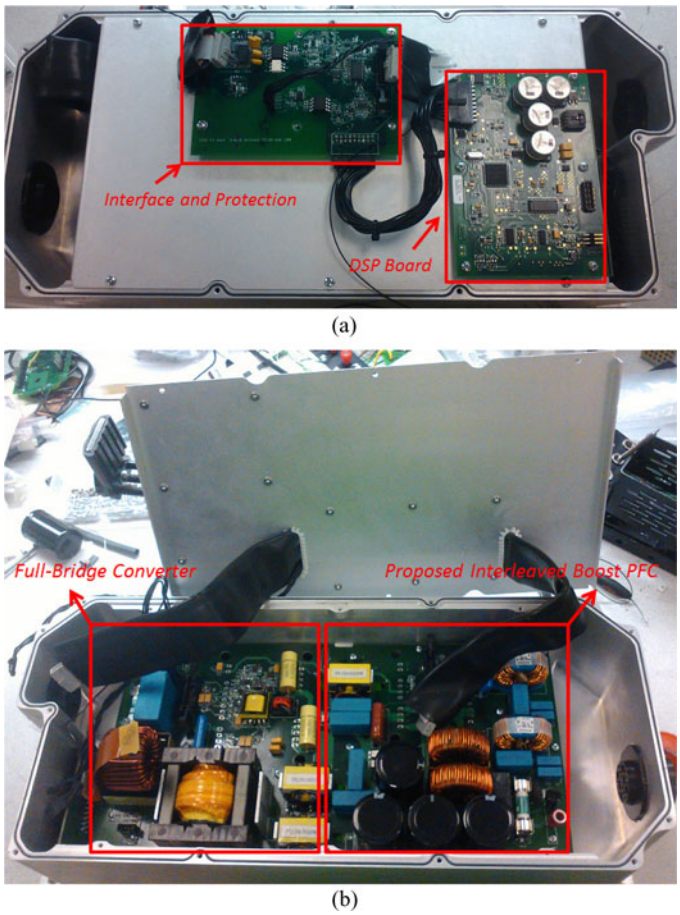


Fig. 21 (a). AC/DC converter prototype (control, communication, and protection). (b). AC/DC converter prototype (power circuit).

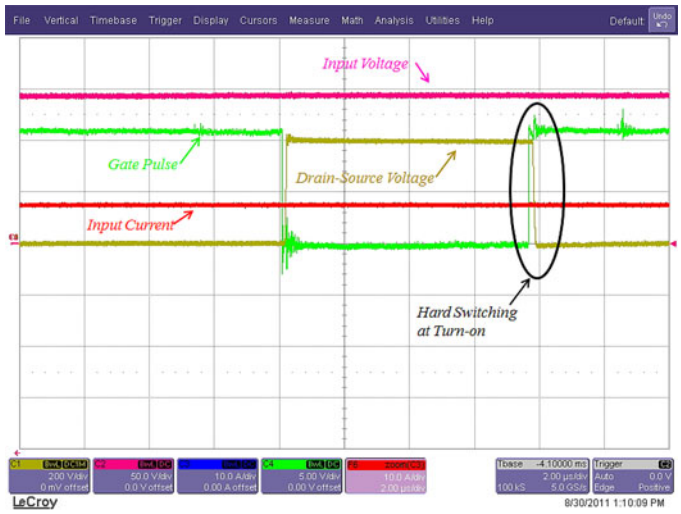


Fig. 22. Conventional interleaved boost PFC waveforms.

depict the transient response of the converter against a 50% positive step load and a 50% negative step load, respectively.

Fig. 35 shows the efficiency curves of the conventional interleaved boost PFC converter as well as the proposed interleaved boost PFC converter. According to this figure, the proposed converter shows better efficiency for the whole load range compared to the conventional one. The improvement in the efficiency can be attributed to the fact that the proposed converter eliminates two main sources of losses, which are the turn-ON losses of the boost MOSFETs and the reverse-recovery losses of the output diodes.

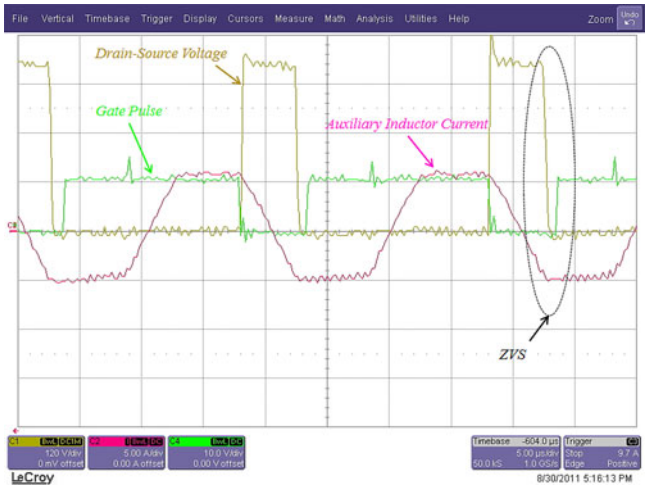


Fig. 23. Proposed interleaved boost PFC waveforms.

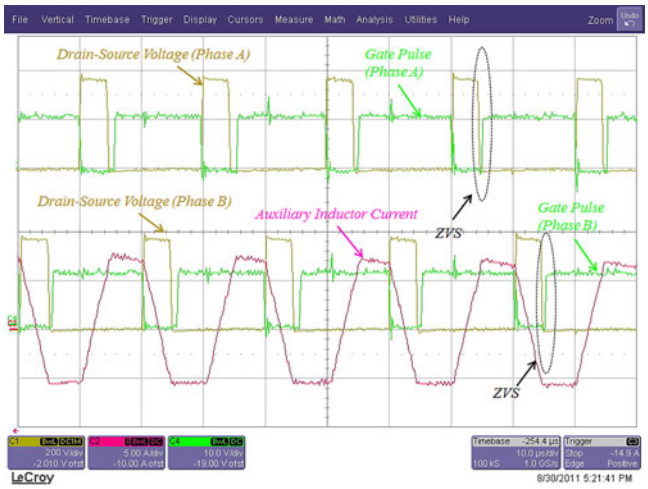


Fig. 24 Waveforms of two phases of the proposed interleaved boost converter plus auxiliary circuit current.

Fig. 25. Waveforms of the proposed interleaved boost converter for large duty ratios.

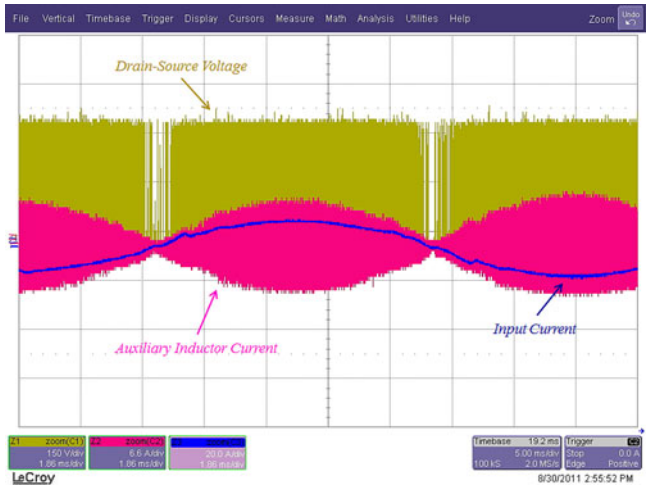


Fig. 26. Drain–source voltage of the boost MOSFET, auxiliary current, and input current.

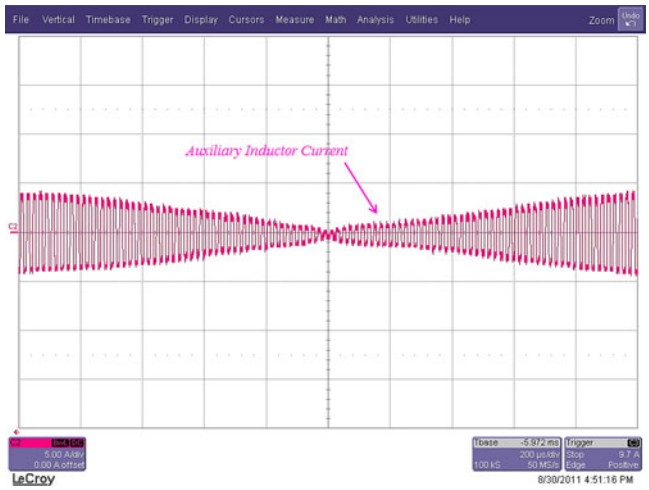


Fig. 27. Auxiliary current around the current zero crossing point.

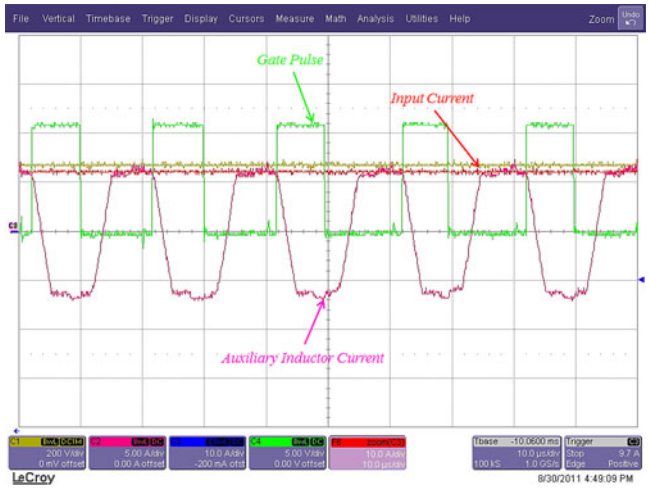


Fig. 28. Proposed converter waveforms around the peak point of the line cycle.

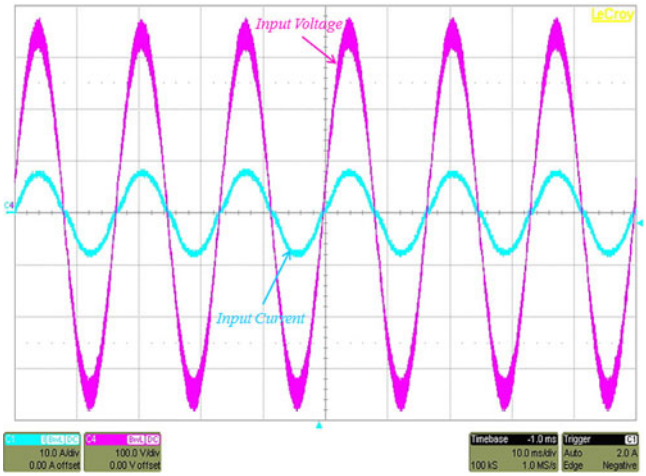


Fig. 29. Proposed converter input voltage and input current for 30% load.

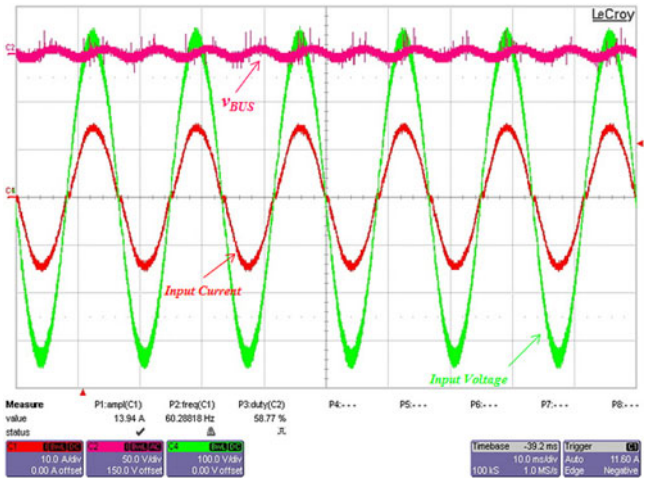


Fig. 30. Proposed converter input voltage and input current for full load.

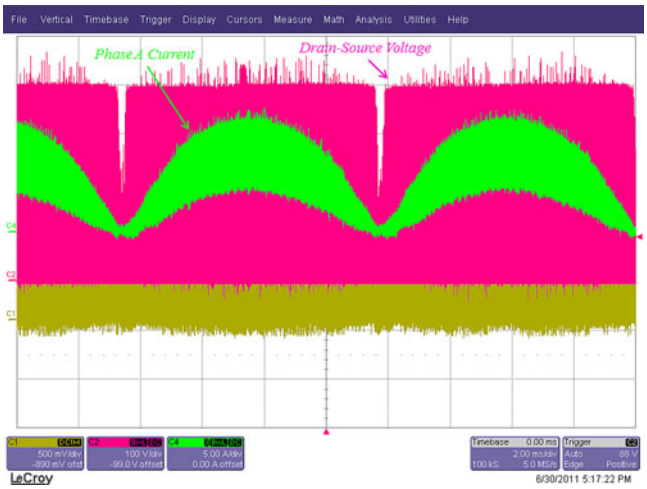


Fig. 31. Phase A boost inductor current and boost MOSFET drain–source voltage.

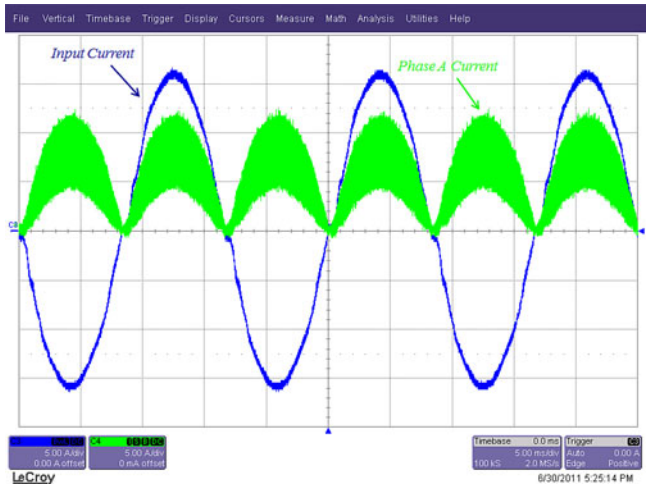


Fig. 32. Phase A boost inductor current and input current.

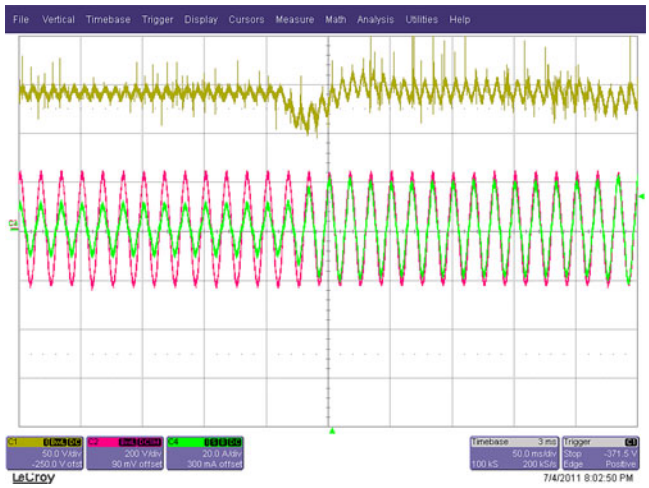


Fig. 33. Transient response of the converter to a 50% positive step load.

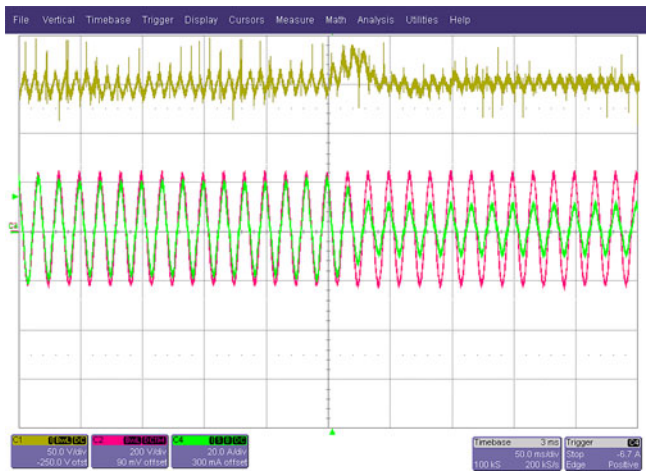


Fig. 34. Transient response of the converter to a 50% negative step load.

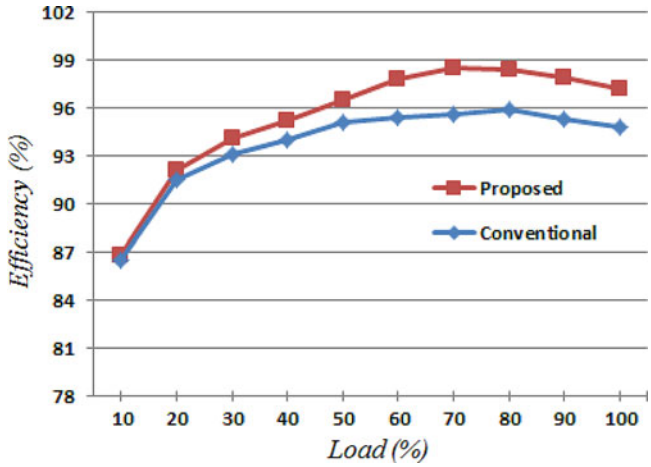


Fig. 35. Efficiency curves of the proposed and conventional converters ($v_{\rm in} = 220\ {\rm V_{ac}}$).

VII. Conclusion

In this paper, a new interleaved boost PFC converter is proposed, which provides soft switching for the power MOSFETs, through an auxiliary circuit. This auxiliary circuit provides reactive current during the transition times of the MOSFETs to charge and discharge the output capacitors of the MOSFETs. In addition, the control system effectively optimizes the amount of reactive current required to achieve ZVS for the power MOSFETs. The frequency loop, which is introduced in the control system, determines the frequency of the modulator based on the load condition and the duty cycle of the converter. The experimental results and efficiency curves show the superior performance of the proposed converter compared to the conventional one.

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