Analysis and Design of a Three-Level LLC Series Resonant Converter for High- and Wide-Input-Voltage Applications

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***Abstract*—In this paper, the analysis and design of a three-level LLC series resonant converter (TL LLC SRC) for high- and wide-input-voltage applications is presented. The TL LLC SRC discussed in this paper consists of two half-bridge LLC SRCs in series, sharing a resonant inductor and a transformer. Its main advantages are that the voltage across each switch is clamped at half of the input voltage and that voltage balance is achieved. Thus, it is suitable for high-input-voltage applications. Moreover, due to its simple driving signals, the additional circulating current of the conventional TL LLC SRCs does not appear in the converter, and a simpler driving circuitry is allowed to be designed. With this converter, the operation principles, the gain of the LLC resonant tank, and the zero-voltage-switching condition under wide input voltage variation are analyzed. Both the current and voltage stresses over different design factors of the resonant tank are discussed as well. Based on the results of these analyses, a design example is provided and its validity is confirmed by an experiment involving a prototype converter with an input of 400–600 V and an output of 48 V/20 A. In addition, a family of TL LLC SRCs with double-resonant tanks for high-input-voltage applications is introduced. While this paper deals with a TL LLC SRC, the analysis results can be applied to other TL LLC SRCs for wide-input-voltage applications.**

***Index Terms*—High and wide input voltage, LLC series resonant converter (SRC), three-level (TL).**

I. Introduction

In high-input-voltage applications such as three-phase systems, fuel cell systems, photovoltaic systems, and ship electric power distribution systems, the three-level converter (TLC) is advantageous because the voltage across each main switch is half of the input voltage [1]–[4]. However, the TLC is associated with high levels of switching loss due to its high input voltage, a condition that results in low efficiency. For this reason, it is necessary to apply a soft-switching technique when using a TLC.

A number of TLCs capable of soft-switching performance have been presented thus far. Those that use a high-frequency MOSFET as a main switch can be classified into two types: the three-level zero-voltage-switching pulsewidth modulation (PWM) converter (TL ZVS PWMC) and the three-level LLC series resonant converter (TL LLC SRC). The main advantages of these converters are that the voltage across each switch is half of the input voltage and that all main switches can be turned ON under ZVS. However, in TL ZVS PWMCs, ZVS cannot be achieved in all load conditions. The efficiency degrades due to the increase in the circulating current as the input voltage increases. In addition, all rectifier diodes suffer from a serious reverse-recovery problem. To overcome these drawbacks, many studies of TL ZVS PWMCs have been conducted, but these have required auxiliary circuits, resulting in high costs and a complex structure [5]–[11].

TL LLC SRCs can mitigate the aforementioned drawbacks of TL ZVS PWMCs. All main switches and rectifier diodes in the converters are softly switched without additional circuits under all load conditions. Regulation of the output voltage during line-voltage variation can be achieved with narrow variation in the switching frequency. This results in a reduction of the circulating current. Therefore, the converters are highly efficient over a wide input voltage range [12]–[18]. However, there has been little research on the topic of TL LLC SRCs. The full-bridge-based TL LLC SRC introduced in [2] has the following drawbacks. Its four leading-leg switches have voltage stress of half of the input voltage, but its two lagging-leg switches have a stress level equal to that of the input voltage. The output voltage is regulated by a fixed frequency scheme, unlike general LLC SRCs. In [20] and [21], it is reported that the efficiency of a fixed-frequency LLC SRC is lower than that of a variable-frequency LLC SRC over wide line variation. In [19], another TL LLC SRC is introduced. In the converter, the voltage of each switch is clamped at half of the input voltage. Output voltage regulation is achieved by frequency modulation. Thus, the converter in [19] is more suitable for high- and wide-input-voltage applications compared to that in [2]. However, in order to ensure that the voltage across each switch is clamped at half of the input voltage, additional dead-time zones are required in their driving signals. This makes the effective duty cycle smaller and can lead to the generation of an additional circulating current. Due to this, it is difficult to optimize the efficiency. In addition, additional circuits are required to make the complex driving signals, and four gate-driving ICs or transformers are necessary for the main switches. Moreover, in [19], only the no-load and short-circuit operations were analyzed; the operations, gain of the resonant tank, stress on the resonant tank, and ZVS condition under a broad range of line-voltage variation were not discussed.

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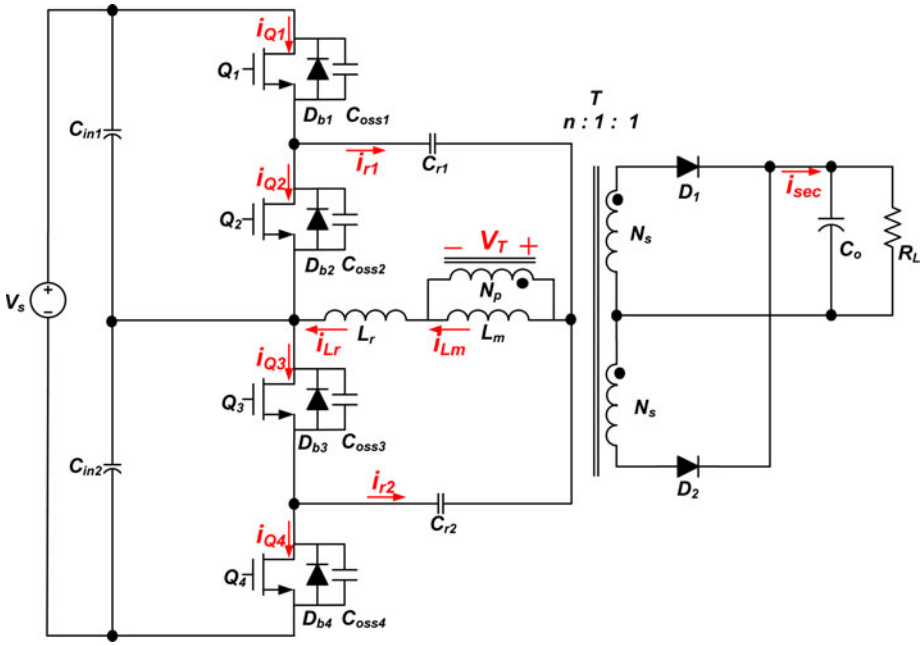

Fig. 1. Analysis and experimental circuit of the TL LLC SRC.

In this paper, a new TL LLC SRC for high- and wide-input-voltage applications is introduced, and its analysis results and design under wide input voltage variation are presented. The analysis results presented in this paper can be applied to other TL LLC SRCs for wide-input-voltage applications. The TL LLC SRC discussed in this paper consists of two half-bridge (HB) LLC SRCs in series that share a resonant inductor and a transformer. The upper switches of each HB LLC SRC are driven with a constant duty ratio ($D = 0.5$) simultaneously. On the other hand, the lower switches of each HB LLC SRC are driven complementarily to the upper switches. These operations allow the voltage across each switch to be clamped at half of the input voltage and that voltage balance to be achieved. The converter also has several advantages as follows. First, its driving signals are simple. Thus, it can be readily implemented using only a general-purpose controller without additional circuits. Only two gate-driving ICs or gate-driving transformers are required. Because no additional dead time between the driving signals is required, the efficiency can be easily optimized. Moreover, clamping diodes are not required. All main switches and rectifier diodes are softly switched under all line and load conditions. High efficiency can be achieved over a wide-input-voltage range. The offset voltages of resonant capacitors are a quarter of the input voltage, allowing the use of a low-voltage rating capacitor. The switching frequency changes in accordance with the given input and output conditions. Due to these advantages, it can be said that the converter is suitable for high- and wide-input-voltage applications.

The circuit operations of a new TL LLC SRC are briefly described in Section II. The analysis, design considerations, and design examples under a wide range of input voltage variation are presented in Sections III and IV, respectively. The validity of this study is confirmed by the experimental results of a prototype converter with an input of 400–600 V and an output of 48 V/20 A, as described in Section V. A family of TL LLC SRCs with double-resonant tanks for high-input-voltage applications is introduced in Section VI, and the conclusion is made in Section VII.

II. Circuit Operations

Fig. 1 shows the circuit configuration of the TL LLC SRC discussed in this paper. It consists of two HB LLC SRCs in series, sharing a resonant inductor and a transformer. Fig. 2 shows the key operating waveforms of the converter in a steady state. Referring to the figure, the switches Q_1 and Q_3 are driven with a constant duty ratio ($D = 0.5$) simultaneously. On the other hand, the switches Q_2 and Q_4 are driven complementarily to switches Q_1 and Q_3. Each switching period is divided into six modes, whose operating circuits are shown in Fig. 3. In order to illustrate the operation of the converter, several assumptions are made as follows.

1) The output capacitor C_O is large enough to be considered as a voltage source.
2) Two input capacitors in the series $C_{\rm in1}$ and $C_{\rm in2}$ are large enough to be considered as two voltage sources of $V_S/2$.
3) The main switches are all MOSFETs with parasitic diodes of D_{b1}, D_{b2}, D_{b3}, and D_{b4}.
4) The output capacitances of all MOSFETs have the same capacitance of $C_{\rm oss}$.
5) The two resonant capacitors C_{r1} and C_{r2} have the same capacitance of C_r.
6) The main transformer T has a turn ratio of $n = N_P/N_S$.

A. Steady-State Operation Under a High Input Voltage

Mode 1 [t_0–t_1]: Mode 1 begins when the switches of Q_1 and Q_3 are turned ON with ZVS at t_0. The current of L_r $i_{Lr}(t)$ increases with a sinusoidal shape by the resonance of C_{r1}, C_{r2},

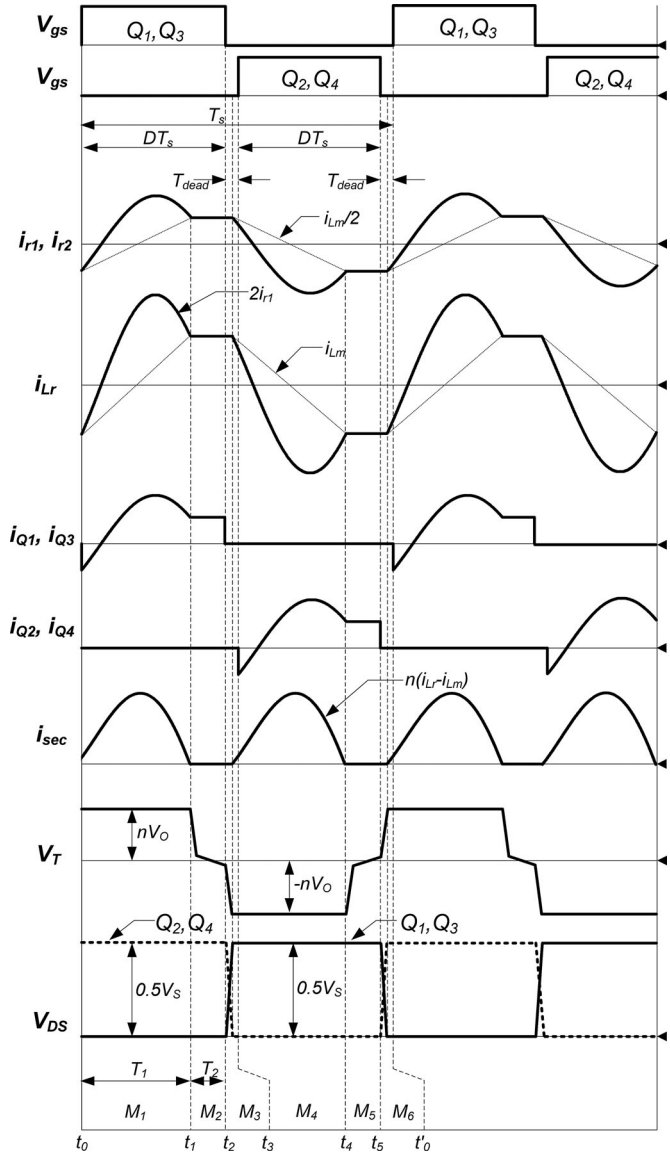

Fig. 2. Key operating waveforms of the converter in a steady state.

and L_r and is divided into $i_{r1}(t)$ and $i_{r2}(t)$. The rectifier diode D_1 is also conducting. The primary voltage of transformer $V_T(t)$ clamps at nV_O, where n is the turn ratio and V_O is the output. The magnetizing current $i_{Lm}(t)$ is linearly increased from a negative to a positive value by the reflected voltage nV_O. During this mode, the difference between $i_{Lr}(t)$ and $i_{Lm}(t)$ is transferred to the output stage. Fig. 4(a) shows the equivalent circuit describing mode 1. The voltages and currents during this mode can be expressed as follows:

$$V_{Cr1}(t) = \frac{V_S}{2 - nV_O - V_{k1}\cos\left[\omega_O(t-t_0)+\varphi_{k1}\right]} \quad (1)$$

$$V_{Cr2}(t) = \frac{V_S}{2 - V_{Cr1}(t)} \quad (2)$$

$$i_{r1}(t) = i_{r2}(t) = \frac{V_{k1}}{2z_O}\sin\left[\omega_O(t-t_0)+\varphi_{k1}\right] \quad (3)$$

$$i_{Lr}(t) = 2i_{r1}(t) = \frac{V_{k1}}{z_O}\sin\left[\omega_O(t-t_0)+\varphi_{k1}\right] \quad (4)$$

$$i_{Lm}(t) = i_{Lr}(t_O) + \frac{nV_O}{L_m}(t-t_0) \quad (5)$$

$$i_{Q_1}(t) = i_{Q_3}(t) = \frac{i_{Lr}(t)}{2} \quad (6)$$

$$V_{DS\_Q_2}(t) = V_{DS\_Q_4}(t) = \frac{V_S}{2} \quad (7)$$

$$i_{\sec}(t) = n(i_{Lr}(t) - i_{Lm}(t)) \quad (8)$$

where $V_{k1} = \sqrt{(z_O i_{Lr}(t_0))^2 + (V_S/2 - V_{Cr1}(t_0) - nV_O)^2}$, $\varphi_{k1} = \tan^{-1}(z_O i_{Lr}(t_0)/V_S/2 - V_{Cr1}(t_0) - nV_O)$, $\omega_O = 2\pi f_O = (1/\sqrt{2L_rC_r})$, and $z_O = \sqrt{L_r/2C_r}$.

Mode 2 [t_1–t_2]: Mode 2 begins when $i_{Lr}(t)$ goes back to the same level as $i_{Lm}(t)$. At this moment, D_1 is turned OFF with zero current switching (ZCS) and the secondary side of the transformer is separated from the primary side. Then, the magnetizing inductance L_m participates in the resonance. During this mode, the power to the load is only supplied by the output capacitor C_O. The equivalent circuit describing this mode can be obtained by removing nV_O from the circuit model related to mode 1. The voltages and currents during this mode can be expressed as follows:

$$V_{Cr1}(t) = V_S/2 - V_{k2}\cos\left[\omega'_O(t-t_1)+\varphi_{k2}\right] \cong V_{Cr1}(t_1) - \frac{i_{Lm}(t_0)}{2c_r}(t-t_1) \quad (9)$$

$$V_{Cr2}(t) = \frac{V_S}{2 - V_{Cr1}(t)} \quad (10)$$

$$i_{r1}(t) = i_{r2}(t) = \frac{V_{k2}}{2z'_O}\sin\left[\omega'_O(t-t_1)+\varphi_{k2}\right] \cong \frac{i_{Lm}(t_1)}{2} \cong \frac{-i_{Lm}(t_0)}{2} \quad (11)$$

$$i_{Lr}(t) = \frac{V_{k2}}{z'_O}\sin\left[\omega'_O(t-t_1)+\varphi_{k2}\right] \cong i_{Lm}(t_1) \cong -i_{Lm}(t_0) \quad (12)$$

$$i_{Lm}(t) = i_{Lr}(t) \quad (13)$$

$$V_{DS\_Q_2}(t) = V_{DS\_Q_4}(t) = \frac{V_S}{2} \quad (14)$$

where $V_{k2} = \sqrt{(z'_O i_{Lr}(t_1))^2 + (V_{Cr2}(t_1))^2} \cong \sqrt{(z'_O i_{Lr}(t_0))^2 + (V_{Cr2}(t_1))^2}$, $\varphi_{k2} = \tan^{-1}(z'_O i_{Lr}(t_1)/V_{Cr2}(t_1)) \cong -\tan^{-1}(z'_O i_{Lr}(t_0)/V_{Cr2}(t_1))$, $V_{Cr2}(t_1) = V_S/2 - V_{Cr1}(t_1)$, $\omega'_O = 2\pi f'_O = (1/\sqrt{2(L_r+L_m)C_r})$, and $z'_O = \sqrt{(L_r+L_m)/2C_r}$.

Mode 3 [t_2–t_3]: Mode 3 begins when the switches of Q_1 and Q_3 are turned OFF. Then, the voltages across Q_1 and Q_3 are linearly increased from zero and the voltages across Q_2 and Q_4 are linearly decreased from half of the input voltage by $i_{Lm}(t_2)$. In addition, $V_T(t)$ is decreased to $-nV_O$. If the voltages across Q_1 and Q_3 become half of the input voltage, $V_T(t)$ becomes $-nV_O$ and D_2 begins conducting. At the same time, the parasitic diodes of Q_2 and Q_4, namely D_{b2} and D_{b4}, are forward biased

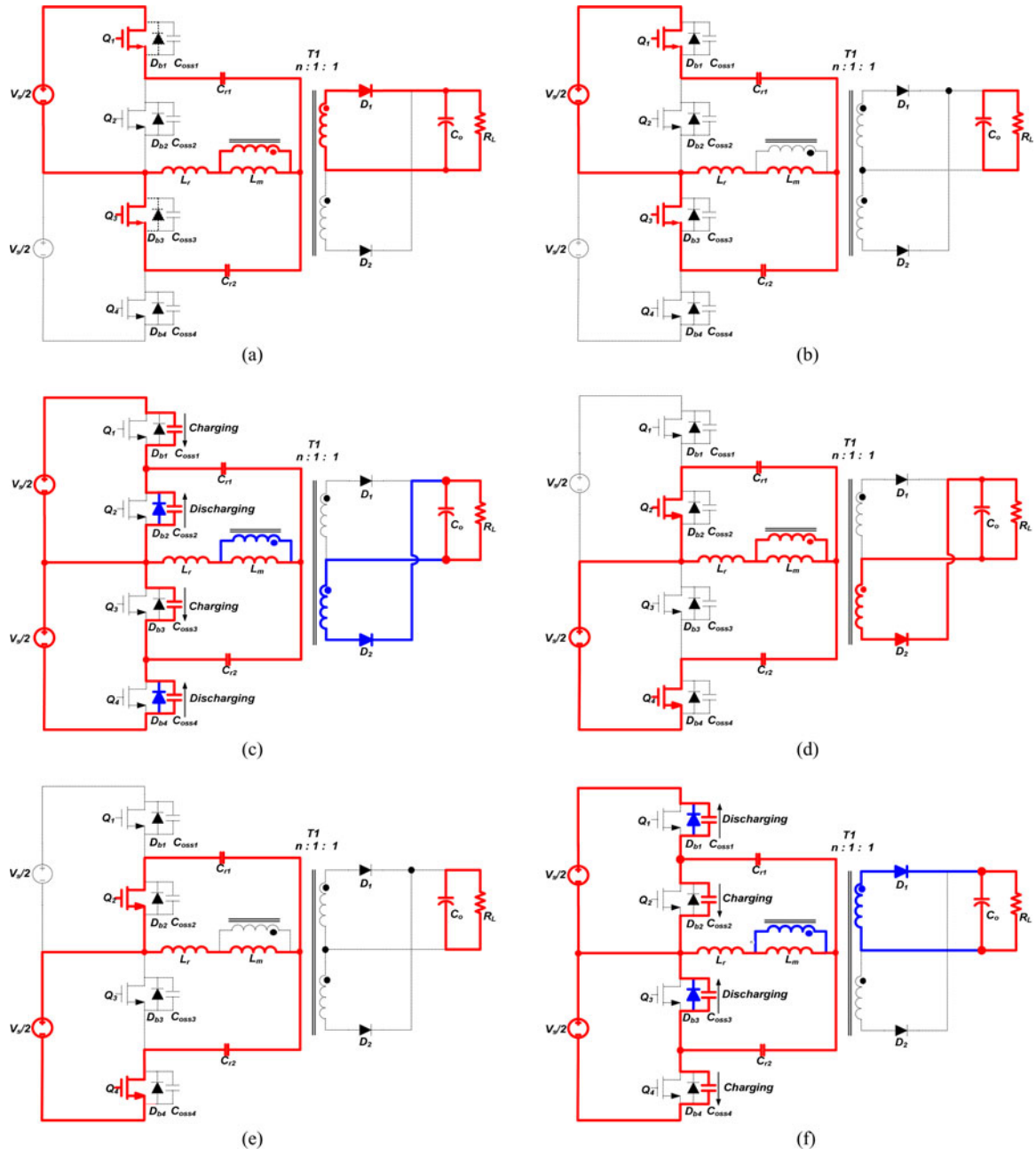

Fig. 3. Operating circuits during one switching period. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

and the resonance of C_{r1}, C_{r2}, and L_r occurs in again. At the end of this mode, the switches of Q_2 and Q_4 are turned ON with ZVS. The voltages and currents can be expressed as follows:

$$V_{Cr1}(t) \cong V_{Cr1}(t_2) + \frac{i_{Lm}(t_2)}{2c_r}(t - t_2)$$
$$\cong V_{Cr1}(t_2) - \frac{i_{Lm}(t_0)}{2c_r}(t - t_2) \quad (15)$$

$$V_{Cr2}(t) = \frac{V_S}{2 - V_{Cr1}(t)} \quad (16)$$

$$i_{r1}(t) = i_{r2}(t) = \frac{i_{Lm}(t_2)}{2} \cong \frac{-i_{Lm}(t_0)}{2} \quad (17)$$

$$V_{DS\_Q_1}(t) = V_{DS\_Q_3}(t) \cong \frac{i_{Lm}(t_2)}{4C_{oss}}(t - t_2)$$
$$\cong -\frac{i_{Lm}(t_O)}{4C_{oss}}(t - t_2) \quad (18)$$

$$V_{DS\_Q_2}(t) = V_{DS\_Q_4}(t) \cong \frac{V_S}{2} - \frac{i_{Lm}(t_2)}{4C_{oss}}(t - t_2)$$
$$\cong \frac{V_S}{2} + \frac{i_{Lm}(t_O)}{4C_{oss}}(t - t_2). \quad (19)$$

The operation principles for modes 4–6, whose operating circuits and equivalent circuit during the powering interval are

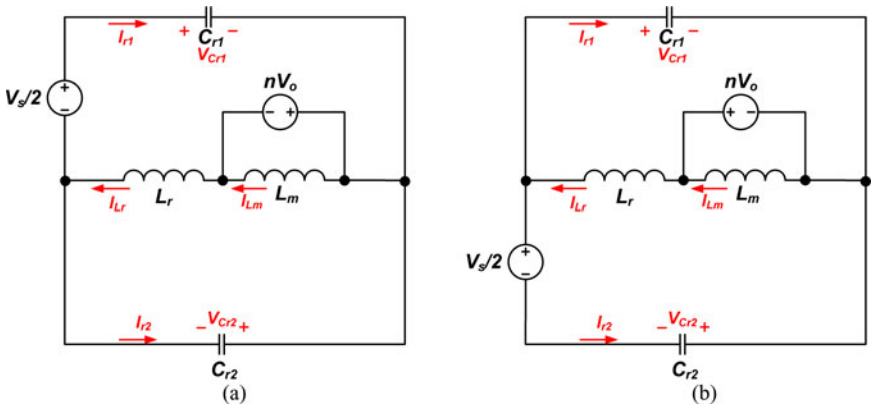

Fig. 4. (a) Equivalent circuit describing mode 1. (b) Equivalent circuit describing mode 4.

also shown in Figs. 3 and 4(b), respectively, are similar to modes 1–3. Therefore, they are not described here.

The operation of the converter during a switching period has been explained as having six modes. However, the converter can work in four modes when the maximum input voltage is applied. In such a case, the switching frequency equals to the resonant frequency f_O, and modes 2 and 5 are omitted from the six modes.

B. Worst Case Operation

If the converter operates over a wide-input-voltage range, it can enter into the worst case operation when the input voltage is at its minimum level. In consideration of this situation in the design, an analysis of the worst case operation is required.

As the input voltage decreases, the converter requires a higher gain to regulate the output voltage. The maximum gain that it can have is obtained at the boundary between the capacitive load region and the inductive load region of the resonant tank. Fig. 5 shows the key waveforms of the converter at the maximum gain point (MGP), where the maximum gain can be obtained. The operation principles are as follows.

Mode 1 [t_0–t_1]: Mode 1 begins when the switches of Q_1 and Q_3 are turned ON with hard switching at t_0. At this moment, D_1 also begins conducting. Then, $i_{Lr}(t)$ begins to increase in terms of its sinusoidal shape due to the resonance of C_{r1}, C_{r2}, and L_r and $i_{Lm}(t)$ increases linearly from zero to a positive value due to nV_O. The voltages and currents during this mode can be expressed as follows:

$$V_{Cr1}(t) = \frac{V_S}{2 - nV_O - V_{k3}\cos\left[\omega_O(t - t_0)\right]} \tag{20}$$

$$V_{Cr2}(t) = \frac{V_S}{2 - V_{Cr1}(t)} \tag{21}$$

$$i_{r1}(t) = i_{r2}(t) = \frac{V_{k3}}{2z_O}\sin\left[\omega_O(t - t_0)\right] \tag{22}$$

$$i_{Lr}(t) = \frac{V_{k3}}{z_O}\sin\left[\omega_O(t - t_0)\right] \tag{23}$$

$$i_{Lm}(t) = \frac{nV_O}{L_m}(t - t_0) \tag{24}$$

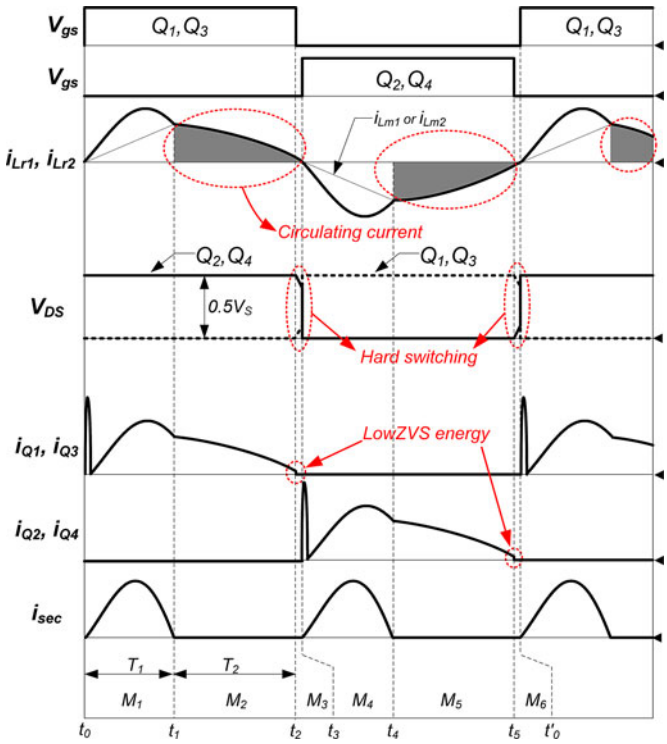

Fig. 5. Worst case operation.

where $V_{k3} = V_{Cr2}(t_0) - nV_O = V_S/2 - V_{Cr1}(t_0) - nV_O$.

Mode 2 [t_1–t_2]: Mode 2 begins when $i_{Lr}(t)$ goes back to the same level as $i_{Lm}(t)$. Then, the magnetizing inductance L_m participates in the resonance. The voltages and currents during mode 2 can be expressed as follows:

$$V_{Cr1}(t) = V_S/2 - V_{k4}\cos\left[\omega'_O(t - t_1) + \varphi_{k4}\right] \tag{25}$$

$$V_{Cr2}(t) = \frac{V_S}{2 - V_{Cr1}(t)} \tag{26}$$

$$i_{r1}(t) = i_{r2}(t) = \frac{V_{k4}}{2z'_O}\sin\left[\omega'_O(t - t_1) + \varphi_{k4}\right] \tag{27}$$

$$i_{Lr}(t) = i_{Lm}(t) = \frac{V_{k4}}{z'_O}\sin\left[\omega'_O(t - t_1) + \varphi_{k4}\right] \tag{28}$$

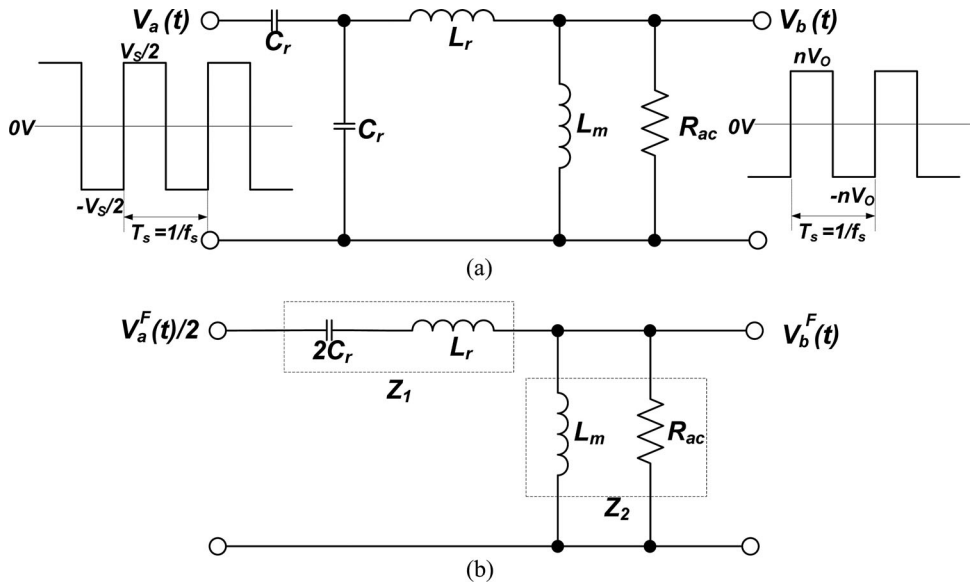

Fig. 6. (a) AC equivalent circuit for the discussed converter. (b) Equivalent circuit in Fig. 6(a).

where $V_{k4} = \sqrt{(z'_O i_{Lr}(t_1))^2 + (V_{Cr2}(t_1))^2}$ and $\varphi_{k4} = \tan^{-1}(z'_O i_{Lr}(t_1)/V_{Cr2}(t_1))$.

Mode 3 [t_2–t_3]: This is the resonant mode of C_{oss1}, C_{oss2}, C_{oss3}, C_{oss4}, C_{r1}, C_{r2}, L_r, and L_m. The duration of this mode is practically very narrow and C_{oss} has a very small value. Hence, to simplify the analysis, it can be assumed that this mode is extended from mode 2. The voltages and currents during this mode are then identical to those in mode 2.

The converter works in six modes, comparable to the normal operating condition at the MGP. However, all switches are turned ON with hard switching due to the low ZVS energy. Thus, the current through the switches experiences an abrupt spike at the beginning, as shown in Fig. 5. In addition, all of the parasitic diodes of the switches can experience reverse-recover transients. This makes the spike of the current through the switches much higher, resulting in low efficiency and low reliability. For these reasons, the converter should be designed to prevent the worst case operation scenario given wide variation in the input voltage. This can be achieved by making the maximum gain larger than the gain required for the regulation of the output voltage at the minimum input voltage under a full load condition.

III. Analysis and Design Considerations

A. DC Conversion Ratio

The power is transferred from the input to the output by the resonance of C_{r1}, C_{r2}, and L_r in the converter. Hence, all the currents in the resonant tank have a nearly sinusoidal shape, as shown in Fig. 2. This allows the use of fundamental harmonic approximation (FHA) to obtain the dc characteristic of the converter, which assumes that only the fundamental component of the square wave contributes to the power transfer to the output. Based on FHA, the ac equivalent circuit for the converter is derived as shown in Fig. 6. The ac equivalent load resistance $R_{\rm ac}$ and the fundamental components of the input and output voltages of the resonant tank can be obtained as follows:

$$R_{\rm ac} = \frac{8n^2 R_L}{\pi^2} \tag{29}$$

$$V_a^F(t) = \frac{2V_S}{\pi}\sin(2\pi f_S t) \tag{30}$$

$$V_b^F(t) = \frac{4nV_O}{\pi}\sin(2\pi f_S t). \tag{31}$$

The dc conversion ratio of resonant tank M can then be expressed as follows:

$$M = \frac{V_b^F(t)}{V_a^F(t)/2} = \frac{nV_O}{V_S/4} = \frac{Z_2}{Z_1+Z_2} = \frac{k}{\sqrt{(1+k-(1/f_n^2))^2 + Q^2k^2\,(f_n-(1/f_n))^2}} \tag{32}$$

where $Q = (1/R_{\rm ac})\sqrt{L_r/2C_r}$, $k = L_m/L_r$, $f_O = (1/2\pi\sqrt{2L_rC_r})$, $f_n = f_S/f_O$.

Fig. 7 shows the curves of M plotted over the normalized frequency f_n. The converter will be operated on the negative slope region (or the inductive load region) of the curves to ensure ZVS operation [22]. Thus, Fig. 7 shows that the maximum gain, which is determined by k or Q, affects the operating range of the switching frequency regulating the output voltage under line variation. That is, a larger maximum gain makes $f_{S\_\rm MGP}$, which is the switching frequency at the MGP, higher and the negative slope of M sharper. The curve of M having a larger $f_{S\_\rm MGP}$ and a sharper negative slope narrows the operating range of the switching frequency under the same line condition, as shown in Fig. 7. For this reason, it can be said that a larger maximum gain narrows the operating range of the switching frequency.

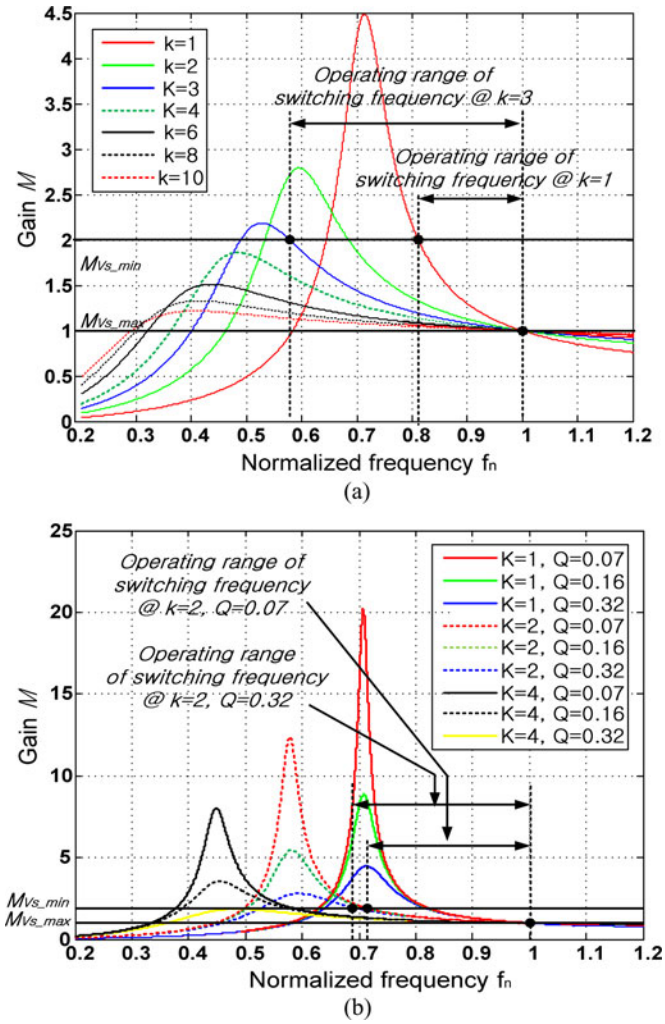

Fig. 7. DC conversion ratio M. (a) At different k values with $Q = 0.32$. (b) At different Q values with $k = 1$, 2, and 4, respectively.

B. Maximum Gain

Because the operating range of the converter is affected by the maximum gain $M_{\max}$ of the resonant tank, a detailed analysis is required.

Operation at the MGP was described in the previous section. The resonant currents are not sinusoidal at this point. This is why FHA cannot be used to obtain $M_{\max}$. In order to obtain $M_{\max}$, the resonant-current-analysis (RCA) method is used.

The output voltage can be obtained from $i_{Lr}(t_1) = i_{Lm}(t_1)$ in Fig. 5, as

$$V_O = \frac{V_S/2 - V_{Cr1}(t_0)}{n\left((z_O/L_m)(T_1/\sin\omega_O T_1) + 1\right)} \tag{33}$$

where $T_1 = t_1 - t_0$.

From the fact that the difference between $i_{Lr}(t)$ and $i_{Lm}(t)$ is transferred to the output stage during mode 1, the load equation can be expressed as follows:

$$n\left(\frac{\int_{t_0}^{t_1}(i_{Lr}(t) - i_{Lm}(t))dt}{T_S/2}\right) = \frac{V_O}{R_L}. \tag{34}$$

The output voltage can be represented by substituting (23) and (24) into (34)

$$V_O = \frac{2C_r(V_S/2 - V_{Cr1}(t_0))(1-\cos\omega_O T_1)}{(nT_1^2/2L_m) + (T_1 + T_2/nR_L) + 2nC_r(1-\cos\omega_O T_1)} \tag{35}$$

where $T_2 = t_2 - t_1$.

The following equations can be obtained by ignoring the dead time in Fig. 5:

$$i_{Lr}(t_2) = \frac{V_{k2}}{z'_O}\sin\left[\omega'_O T_2 + \varphi_{k2}\right] \cong 0 \tag{36}$$

$$V_{Cr1}(t_2) = \frac{V_S}{2} - V_{k2}\cos\left[\omega'_O T_2 + \varphi_{k2}\right] \cong \frac{V_S}{2} - V_{Cr1}(t_0). \tag{37}$$

Then, two equations for the output voltage can be obtained from (36) and (37), respectively, as

$$V_O = \frac{(A/z'_O)\cos\omega_O T_1 \sin\omega'_O T_2 + (A/z_O)\sin\omega_O T_1 \cos\omega'_O T_2}{n\left((\sin\omega_O T_1 \cos\omega'_O T_2/z_O) - ((1-\cos\omega_O T_1)/z'_O)\sin\omega'_O T_2\right)} \tag{38}$$

$$V_O = \frac{V_{Cr1}(t_0) - A\left(\cos\omega_O T_1 \cos\omega'_O T_2 - \sqrt{1+k}\sin\omega_O T_1 \sin\omega'_O T_2\right)}{n\left((1-\cos\omega_O T_1)\cos\omega'_O T_2 + \sqrt{1+k}\sin\omega_O T_1 \sin\omega'_O T_2\right)} \tag{39}$$

where $A = \frac{V_S}{2} - V_{Cr1}(t_0)$.

From (33) and (35), T_2 can be expressed as follows:

$$T_2 = \frac{\pi^2 z_O}{8QkL_r}\left(\frac{T_1(1-\cos\omega_O T_1)}{\omega_O \sin\omega_O T_1} - \frac{T_1^2}{2}\right) - T_1. \tag{40}$$

From (33) and (38), T_2 can be represented by

$$T_2 = \frac{1}{\omega'_O}\left(\tan^{-}\left(\frac{-T_1}{\sigma}\right) + \pi\right) \tag{41}$$

where $\sigma = (kL_r/z'_O) + (T_1/\sqrt{1+k}\tan\omega_O T_1)$.

From (40) and (41), the equation for only T_1 can be obtained as follows:

$$\frac{\pi^2 z_O}{8QkL_r}\left(\frac{T_1(1-\cos\omega_O T_1)}{\omega_O \sin\omega_O T_1} - \frac{T_1^2}{2}\right) - T_1 - \frac{1}{\omega'_O}\left(\tan^{-}\left(\frac{-T_1}{\sigma}\right) + \pi\right) = 0. \tag{42}$$

Hence, when the values of the circuit parameters of L_r, f_O, k, and Q are given, an unknown value of T_1 can be determined from (42) while T_2 can be obtained using (40) or (41). With these T_1 and T_2 values, the initial value of the resonant capacitor $V_{Cr1}(t_0)$ can be calculated by solving (38) and (39) at any input voltage. With this value of $V_{Cr1}(t_0)$, $M_{\max}$ can be obtained via (33). The switching frequency at the MGP f_{S_MGP} can be obtained using

$$f_{S\_\mathrm{MGP}} = \frac{1}{2(T_1 + T_2)}. \tag{43}$$

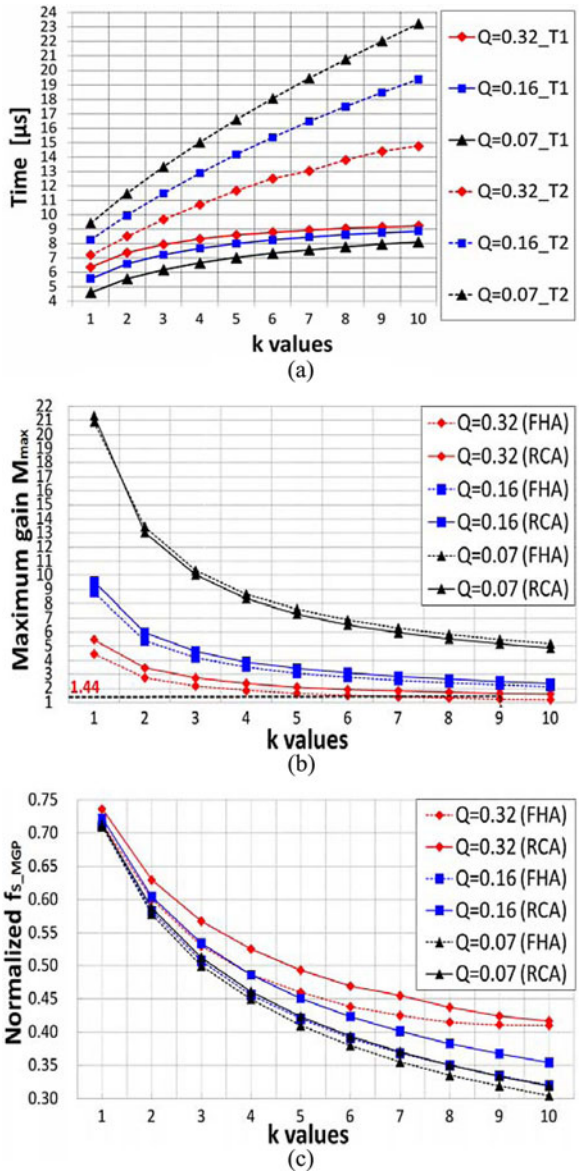

Fig. 8. (a) T_1 and T_2 at the MGP. (b) Maximum gain. (c) Switching frequency at the MGP.

For example, if $L_r = 20\ \mu$H and $f_O = 50$ kHz, T_1, T_2, $M_{\max}$, and f_{S_MGP} can be obtained, as shown in Fig. 8.

Fig. 8(a) shows that T_2 is always longer than T_1 at the MGP and that it gets longer as k increases. Therefore, it can be known that T_2 increases as the input voltage decreases and that its increase is affected by k.

In Fig. 8(b) and (c), the $M_{\max}$ and f_{S_MGP} values based on RCA are compared with those based on FHA. As shown in the figures, the $M_{\max}$ and f_{S_MGP} values based on RCA are larger compared to those based on FHA. This implies that the converter operates practically with less overall variation of the switching frequency than that obtained by FHA under line conditions. To predict more approximately and easily the operating range of the switching frequency, the curves of M in Fig. 7(a) can be offset using the $M_{\max}$ and f_{S_MGP} values obtained by RCA, as shown in Fig. 9. This counterbalancing method is done to find

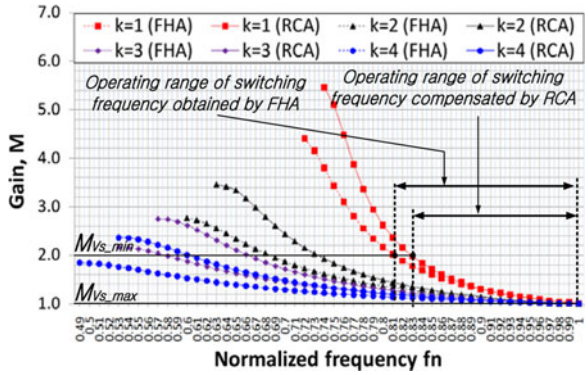

Fig. 9. Gain curves of M offset by RCA when $Q = 0.32$.

the curves of M based on FHA having the same as $M_{\max}$ and f_{S_MGP} values obtained by RCA after slightly adjusting the k values. This method finds the curves of M having the same as $M_{\max}$ and f_{S_MGP} values obtained by RCA, and these curves become the offset FHA curves. Although the offset curves cannot predict the dc gain values at other frequencies precisely, their use can reduce the large gap between the operating range of the switching frequency obtained by FHA and the practical operating range of the switching frequency and can, therefore, enhance the optimal design of the converter against broad line variation. This will be verified by the experimental results in Section VI.

C. ZVS Condition

To ensure ZVS operation, (18) should be larger than half of the input voltage during mode 3. In this case, the ZVS condition can be expressed as

$$i_{Lr}(t_2) = i_{Lm}(t_2) \geq \frac{0.5V_S}{T_{\mathrm{dead}}} \times 4C_{OSS} \tag{44}$$

where $t_2 = T_1 + T_2$.

If the switching frequency f_S equals the resonant frequency f_O, the maximum magnetizing inductance value for ZVS can be obtained from (44) via the equation

$$L_m \leq \frac{\pi\sqrt{L_r C_r}T_{\mathrm{dead}}}{8C_{OSS}}\left(\frac{nV_O}{V_S/2}\right) = \frac{T_O T_{\mathrm{dead}}}{32C_{OSS}} \tag{45}$$

where $T_O = 1/f_O$.

Fig. 10 shows $i_{Lr}(t)$ and $i_{\mathrm{sec}}(t)$ under line variation. Because T_2 increases as the input voltage decreases, $i_{Lr}(T_1+T_2)$ becomes lower, as shown in Fig. 10. Hence, (44) may not be satisfied at the minimum input voltage $V_{S\_\min}$. In addition, the circulating current increases. These results explain why the efficiency is severely degraded as the input voltage decreases. In order to overcome these circumstances, the variable range of T_2 (or the switching frequency) should be designed to be narrow. This can be achieved with the selection of a low value of k, as observed in Fig. 7(a).

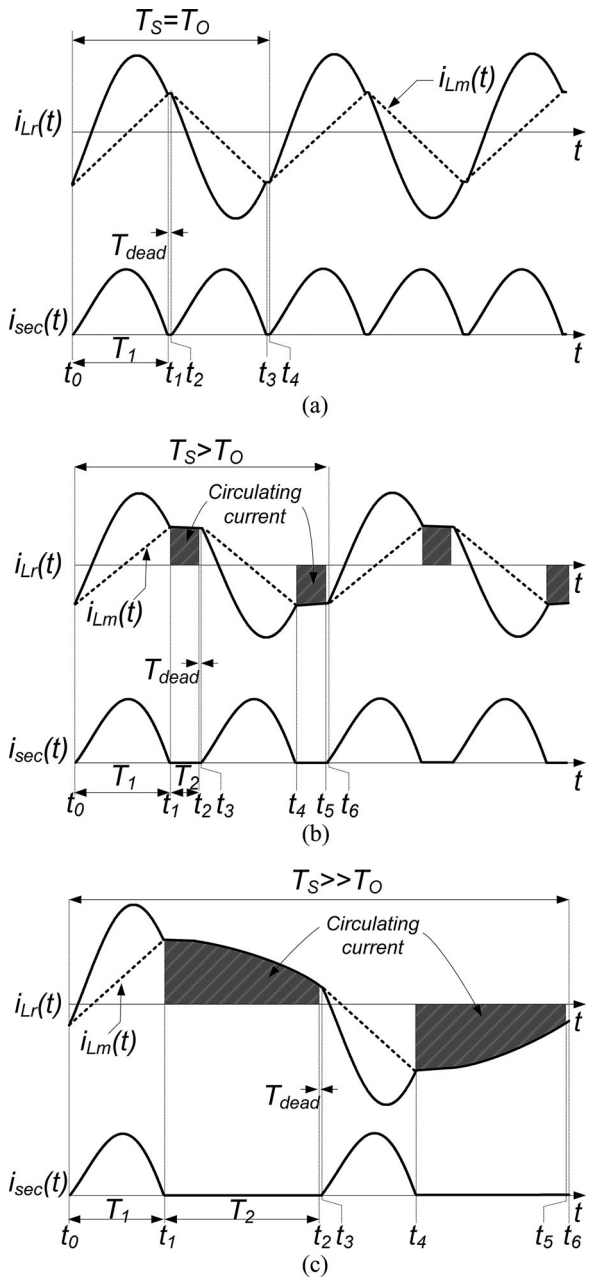

Fig. 10. Resonant inductor current and secondary current under line variation. (a) At $V_{S\_\max}$. (b) At V_{S_medium}. (c) At $V_{S\_\min}$.

D. Stress Analysis

For the visualization of state trajectories describing the operation of the converter, the normalized states in each operation mode can be introduced as follows:

$$V_{nCr1}=\frac{V_{Cr1}}{V_S/4},\quad V_{nCr2}=\frac{V_{Cr2}}{V_S/4},\quad i_{nLr}=\frac{z_O i_{Lr}}{V_S/4},$$

$$V_{nk}=\frac{V_{k1}}{V_S/4}\quad V_{nk2}=\frac{V_{k2}}{V_S/4},\quad M=\frac{nV_O}{V_S/4},\quad k=\frac{L_m}{L_r}.$$

In addition, it is known that modes 4 and 5 are symmetrical to modes 1 and 2. Therefore, (1) and (4), (2) and (4), (9) and (12), and (10) and (12) can be rewritten in normalized forms, respectively, as

$$(V_{nCr1}-2+M)^2+i_{nLr}^2=V_{nk1}^2 \text{ for mode 1} \quad (46)$$

$$(V_{nCr1}-M)^2+i_{nLr}^2=V_{nk1}^2 \text{ for mode 4} \quad (47)$$

$$(V_{nCr1}-2)^2+(\sqrt{1+k}i_{nLr})^2=V_{nk2}^2 \text{ for modes 2 and 3} \quad (48)$$

$$V_{nCr1}^2+(\sqrt{1+k}i_{nLr})^2=V_{nk2}^2 \text{ for modes 5 and 6.} \quad (49)$$

If the converter is operated in four modes, (47) and (49) cannot be considered because modes 2 and 5 are omitted. Moreover, modes 3 and 6 can both be neglected due to their narrow time duration.

For a state trajectory analysis, the parameters shown in the following are used and the converter is designed to be operated with f_O as the switching frequency at its maximum input voltage level.

1) Input voltage: $V_S = 400$–600 V.
2) Output voltage: $V_O = 48$ V.
3) Output current: $I_O = 20$ A.
4) Resonant inductor : $L_r = 20\ \mu$H.
5) Turn ratio of the transformer : $n = 3$.

Fig. 11 shows the state trajectories plotted with different values of k or Q using (46)–(49). From Fig. 11, it is shown that the offset voltage of the resonant capacitor is a quarter of the input voltage. This allows the use of a low-voltage rating capacitor.

From Fig. 11, all stresses of the resonant tank can be plotted over k or Q, as shown in Fig. 12(a) and (b). From Fig. 12(a) and (b), it is seen that all stresses of the resonant tank decrease initially and finally become constant with increasing k at $V_{S\_\max}$. This occurs because the energy stored in L_m decreases as k increases but shows nearly no change at larger k values. In addition, the lower value of Q increases the current stress of the

TABLE I
COMPONENTS LIST

Input capacitances (C_{in1},C_{in2})	330μF
Primary switches (Q_1, Q_2, Q_3, Q_4)	FQA30N40 (C_{OSS}=750pF)
Secondary diodes (D_1, D_2)	MBRP3010N
Resonant capacitances (C_{r1}, C_{r2})	260nF ±1%
Resonant inductance (L_r)	16μH
Leakage inductance (L_{lkg})	4μH
Magnetizing inductance (L_m)	80μH
Transformer turns ratio (N_P : N_{S1} : N_{S2})	21 : 7 : 7
Output capacitance (C_O)	2200μF
Controller	MC33067 (T_{dead}=400ns)

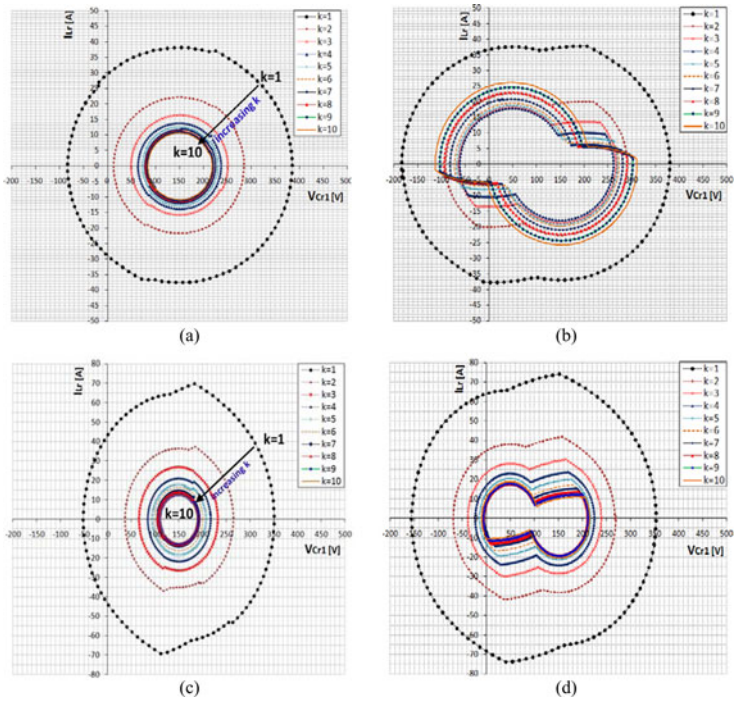

Fig. 11. State trajectories at $V_S = 400$–600 V. (a) $V_S = 600$ V and $Q = 0.32$ ($f_n = 1$). (b) $V_S = 400$ V and $Q = 0.32$ ($f_n < 1$). (c) $V_S = 600$ V and $Q = 0.16$ ($f_n = 1$). (d) $V_S = 400$ V and $Q = 0.16$ ($f_n < 1$).

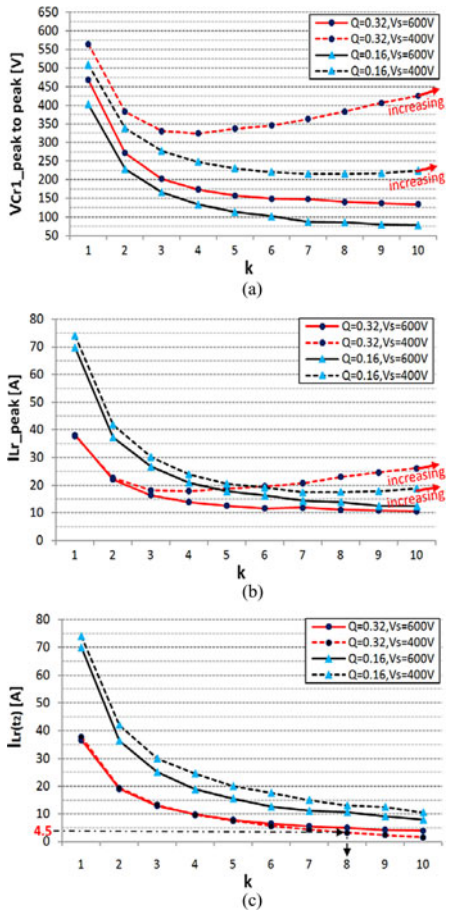

Fig. 12. Stress and ZVS energy. (a) Peak-to-peak voltage stress of the resonant capacitor. (b) Peak current stress of resonant inductor. (c) $i_{Lr}(t_2)$.

resonant inductor because the energy stored in L_m increases due to the lower resonant frequency. All stresses of the resonant tank increase as the input voltage decreases. This arises because the energy stored in L_m increases due to the lower switching frequency. For this reason, it is important to consider all stresses at $V_{S\_\min}$ in applications with a wide input voltage range. For stresses of the resonant tank at $V_{S\_\min}$, whereas they decrease initially, eventually increase as k increases. This occurs because the energy stored in L_m decreases at first while the energy stored in the resonant capacitor increases due to the increasing value of T_2 as k increases. Moreover, a higher Q value increases the voltage stress of the resonant capacitor but makes the current stress of the resonant inductor lower at relatively low k values.

IV. Design Example

The specifications for the design of an example converter are given as follows. The design is focused on ensuring output regulation and achieving nearly constant and high efficiency against the given input voltage variation. In addition, the stress of the resonant tank is considered in the design. To simplify the design, the possible Q values are limited to 0.32.

A. Design Specification

1) Input voltage $V_S = 400$–600 V.
2) Output voltage $V_O = 48$ V.
3) Output current $I_O = 20$ A.
4) Resonant frequency $f_O = 50$ kHz.

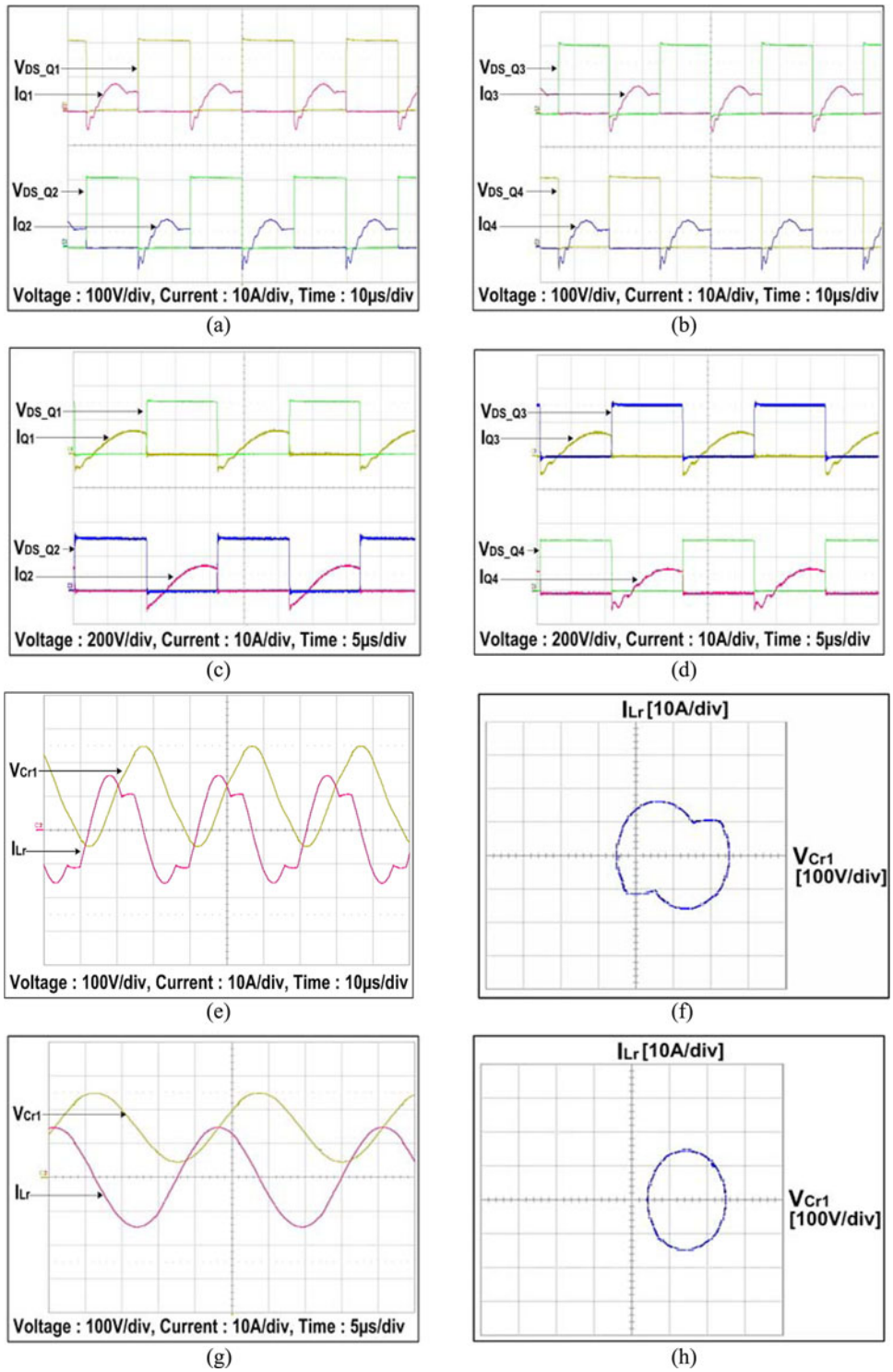

Fig. 13. Experimental waveforms. (a) Current and voltage of $Q1$ and $Q2$ when $V_s = 400$ V and $I_o = 20$ A. (b) Current and voltage of $Q3$ and $Q4$ when $V_s = 400$ V and $I_o = 20$ A. (c) Current and voltage of $Q1$ and $Q2$ when $V_s = 600$ V and $I_o = 20$ A. (d) Current and voltage of $Q3$ and $Q4$ when $V_s = 600$ V and $I_o = 20$ A. (e) Current and voltage of the resonant tank when $V_s = 400$ V and $I_o = 20$ A. (f) State trajectory with C_{r1} and L_r when $V_s = 400$ V and $I_o = 20$ A. (g) Current and voltage of the resonant tank when $V_s = 600$ V and $I_o = 20$ A. (h) State trajectory with C_{r1} and L_r when $V_s = 600$ V and $I_o = 20$ A.

B. Selection of the Turn Ratio of the Transformer

At $V_{S\_\max}$, the converter will operate with the resonant frequency as the switching frequency; hence, the dc gain of the resonant tank will be equal to unity. The turn ratio of the transformer can then be obtained using (32)

$$M_{f_s=f_o} = \frac{nV_O}{V_{S\_\max}/4} = 1. \tag{50}$$

Therefore, the turn ratio n is about three.

C. Selection of the Parameters of the Resonant Tank

To regulate the output at $V_{S\_\min}$ when $n = 3$, the required dc gain of the resonant tank is 1.44 according to (32). However, the maximum gain of the resonant tank should be larger than 1.44 because the converter should be prevented from entering into the worst case operation scenario at $V_{S\_\min}$ and the full load condition. The possible k values are then limited to 9 from the curves based on RCA in Fig. 8(b).

At $V_{S\_\min}$, in order to minimize the circulating current and the current stress of resonant inductor in Fig. 12(b), Q is determined by 0.32 and the available k values can be limited to 6 again by considering the design margin.

From state trajectories in Fig. 11, the curves of $i_{Lr}(t_2)$ can be obtained over k or Q, as shown in Fig. 12(c). In the example design, FQA30N40 and MC33067 are used as primary switches and a controller, respectively. Then, $i_{Lr}(t_2)$ should be larger than 4.5 A using (44) in order to ensure ZVS operation over the given input voltage range. When Q is 0.32 and the available k values are limited to 6, it is confirmed that $i_{Lr}(t_2)$ is larger than 4.5 A from Fig. 12(c).

To minimize the voltage stress of the resonant capacitor in Fig. 12(a), k is determined to be 4 among the available k values.

The resonant capacitance and the resonant inductance can be obtained from the definitions of Q and f_O and can be calculated using

$$C_r = \frac{1}{4\pi R_{\rm ac} Q f_O} \tag{51}$$

$$L_r = 2(R_{\rm ac}Q)^2 C_r. \tag{52}$$

Therefore, the resonant capacitance is approximately 260 nF and the resonant inductance is about 20 μH.

The magnetizing inductance of the transformer can be obtained with the definition of k. It is 80 μH. The maximum magnetizing inductance required for ZVS is about 160 μH according to (45); hence, the magnetizing inductance with 80 μH is a reasonable value over the given input voltage range.

V. Experimental Results

A prototype of the proposed TL LLC-SRC was built and tested to verify the operational principle, advantages, and analysis results against wide line variation, using the components, as shown in Table I.

A. Waveforms

Fig. 13 shows the main experimental waveforms. Fig. 13(a)–(d) shows both the drain-to-source voltage $V_{\rm DS}$ and the current I_D of each switch under a full load with an input of 600 or 400 V. From Fig. 13(a)–(d), it is seen that the voltages of all switches are clamped at half of the input voltage and that they maintain the balance. All of the switches are turned ON with ZVS under all line conditions. Fig. 13(e) and (g) shows the voltage and current of the resonant tank under a full load at an input of 400 or 600 V. As shown in Fig. 13(e) and (g), the converter works in six modes with an input of 400 V, but in four modes with an input of 600 V. Fig. 13(f) and (h) shows the state trajectories of the resonant tank with an input of 400 or 600 V. From Fig. 13(f) and (h), it is seen that all of the stresses of the resonant tank increase as the input voltage decreases.

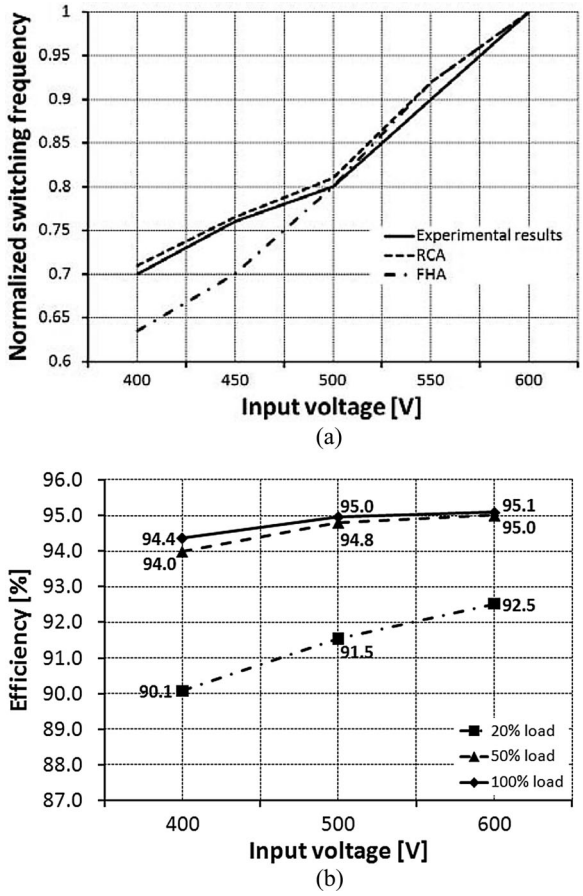

Fig. 14. (a) Normalized switching frequency at a full load under an input of 400–600 V. (b) Efficiencies under an input of 400–600 V.

B. Switching Frequency

Fig. 14(a) shows the switching frequencies with an input range of 400–600 V. From the experimental results, it is very clear that the dc gain of the resonant tank approximately follows the curve offset by RCA, rather than FHA against wide input voltage variation.

C. Efficiency

Fig. 14(b) shows the efficiency as measured by a power analyzer (PPA2520, KinetiQ) at different load conditions with an input of 400–600 V. The maximum efficiency is 95.1% under a full load with a 600-V input. Moreover, the efficiency decreases as the input voltage decreases due to the increase in the circulating current. However, the variation of the efficiency against the given input voltage range is narrow, as shown in Fig. 14(b).

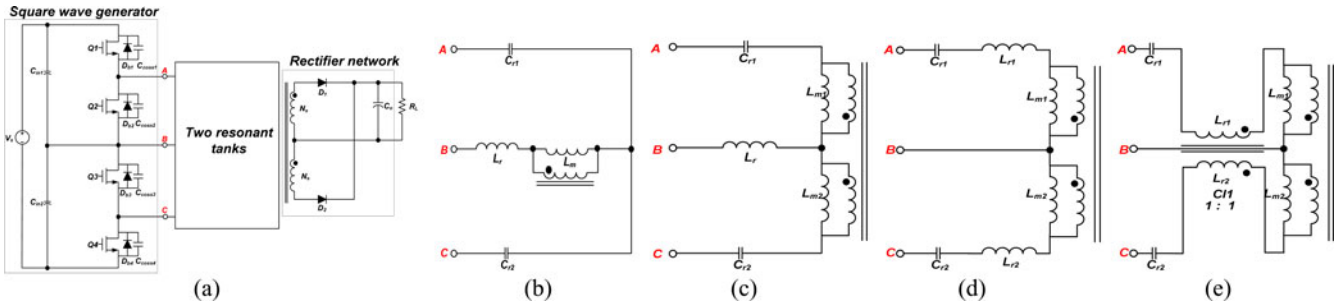

Fig. 15. Family of TL LLC SRCs with double-resonant tanks for high-input-voltage applications. (a) Schematic of TL LLC SRC with two resonant tanks. (b) Type 1 sharing the resonant inductor and the transformer with single primary winding. (c) Type 2 sharing the resonant inductor and the transformer with two primary windings. (d) Type 3 with two separated resonant inductors. (e) Type 4 with a coupled resonant inductor.

VI. Family of TL LLC SRCs for High-Input-Voltage Applications

A family of TL LLC SRCs with double-resonant tanks for high-input-voltage applications is presented in this section. The converters have three stages, as shown in Fig. 15(a): a square wave generator, two resonant tanks, and a rectifier network.

Double-resonant tanks are classified into four types. Fig. 15(b) was described earlier in this paper. Fig. 15(c) and (d) shows a transformer with two primary windings. By adopting this structure, the copper loss in the transformer can be reduced because the current through the resonant inductor is divided into two primary windings. However, if there is a large difference between the resonant capacitances, Fig. 15(b)–(d) can show a lack of balance in two resonant currents. This problem can be alleviated with a coupled resonant inductor, as shown in Fig. 15(e).

VII. Conclusion

Thus far, there has been little research on the topic of TL LLC SRCs. In this paper, a new TL LLC SRC for high- and wide-input-voltage applications is introduced, and the operations, analysis results, and design under a wide range of input voltage variation are presented. From the design based on the analysis results, it is confirmed in Section V that in the proposed converter, the voltage across each switch is half of the input voltage, while the efficiency is 95.1% under a full load (20 A) and a 600-V input. It also shows a narrow range of variation with an input range of 400–600 V. Moreover, it is verified that as the input voltage decreases, the stress of the resonant tank increases; the gain follows the curve as offset by RCA and not FHA. These analysis results can be applied to other TL LLC SRCs for wide-input-voltage applications.

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