Analysis and Design of a Zero-Voltage-Switching and Zero-Current-Switching Interleaved Boost Converter

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***Abstract*—A novel interleaved boost converter with zero-voltage switching (ZVS) and zero-current switching (ZCS) characteristics is proposed in this paper. By using the interleaved approach, this topology not only decreases the current stress of the main circuit device but also reduces the ripple of the input current and output voltage. Moreover, by establishing the common soft-switching module, the soft-switching interleaved converter can greatly reduce the size and cost. The main switches can achieve the characteristics of ZVS and ZCS simultaneously to reduce the switching loss and improve the efficiency with a wide range of load. This topology has two operational conditions depending on the situation of the duty cycle. A driving circuit is designed for the proposed topology to determine the two conditions automatically. The operational principle, theoretical analysis, and design method of the proposed converter are presented. Finally, simulations and experimental results are used to verify the feasibility and exactness of the proposed converter.**

***Index Terms*—Interleaved boost converter, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

AN INTERLEAVED boost converter usually combines more than two conventional topologies, and the current in the element of the interleaved boost converter is half of the conventional topology in the same power condition. Besides, the input current ripple and output voltage ripple of the interleaved boost converter are lower than those of the conventional topologies.

The single boost converter can use the zero-voltage switching (ZVS) and/or zero-current switching (ZCS) to reduce the switching loss of the high-frequency switching [1]–[4], [13]–[16], [18]. However, they are considered for the single topology. Many soft-switching techniques are then introduced to the interleaved boost converters. The interleaved boost converters with ZCS or ZVS are proposed in [5]–[8], [17]. These topologies have higher efficiency than the conventional boost converter because the proposed circuits have decreased the switching losses of the main switches with ZCS or ZVS. Nevertheless, these circuits can just achieve the junction of ZVS or ZCS singly or need more auxiliary circuits to reach the soft switching. In [9], the soft-switching circuit for the interleaved boost converter is proposed. However, its main switches are zero-current turn-ON and zero-voltage turn-OFF and the converter works in the discontinuous mode. The maximum duty cycle of the converter is also limited.

In [10], it does not reduce the switching losses of the interleaved boost converter by the soft-switching techniques, but it decreases the voltage stresses of the switches by the double-voltage technique with the help of the double-voltage capacitor. This topology has a characteristic that the operational analysis is not equivalent in $D > 50\%$ and $D < 50\%$. A soft-switching bridgeless power factor correction circuit is shown in [11]. It is not the aforementioned interleaved boost converter, but it is two conventional boost converters working in the ac input source. Its two main circuits use the common resonant circuit, so it has less resonant elements. This topology has lighter weight and costs less. And this circuit reduces the switching losses and improves the efficiency by ZVS technique, but it does not improve the turn-OFF switching losses by a ZCS technique.

This paper proposes a novel interleaved boost converter with both characteristics of zero-voltage turn-ON and zero-current turn-OFF for the main switches to improve the efficiency with a wide range of load. The voltage stresses of the main switches and auxiliary switch are equal to the output voltage and the duty cycle of the proposed topology can be increased to more than 50%. The proposed converter is the parallel of two boost converters and their driving signals stagger 180° and this makes the operation assumed symmetrical. Moreover, by establishing the common soft-switching module, the soft-switching interleaved converter can further reduce the size and cost.

II. Analysis of Operation

Fig. 1 shows the proposed circuit. It uses the interleaved boost topology and applies the common soft-switching circuit. The resonant circuit consists of the resonant inductor L_r, resonant capacitor C_r, parasitic capacitors C_{Sa} and C_{Sb}, and auxiliary switch S_r to become a resonant way to reach ZVS and ZCS functions. Fig. 2 shows the two operating modes of this circuit, depending on whether the duty cycle of the main switch is more than 50% or not.

A. Operational Analysis of $D < 50\%$ Mode

The operating principle of the proposed topology is described in this section. There are 24 operational modes in the complete cycle. Only the 12 modes related to the main switch S_a are analyzed, because the interleaved topology is symmetrical. Fig. 3 shows the related waveforms when the duty cycle of the main

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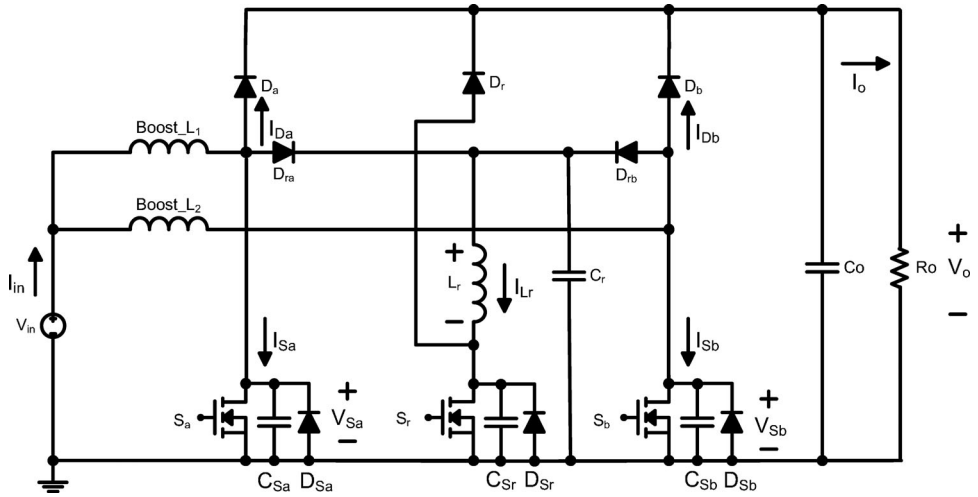

Fig. 1 A novel interleaved boost converter with characteristics of zero-voltage switching and zero-current switching.

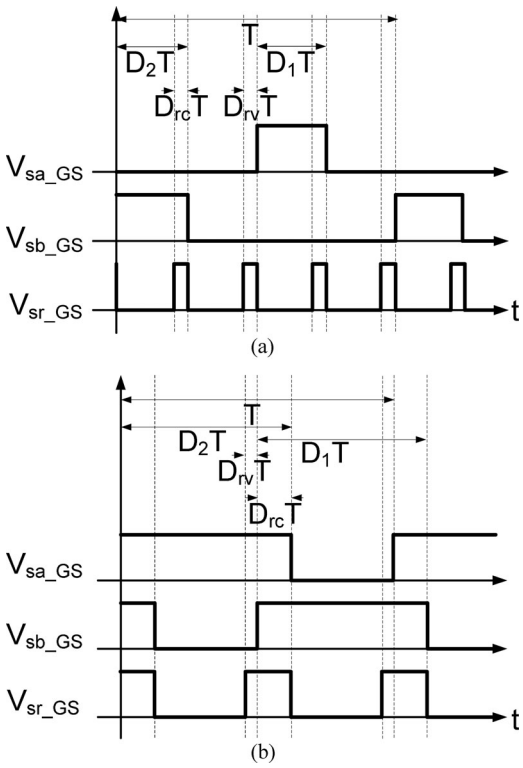

Fig. 2 Switching waveforms of the main switches S_a and S_b and auxiliary switch S_r. (a) $D < 50\%$ mode. (b) $D > 50\%$ mode.

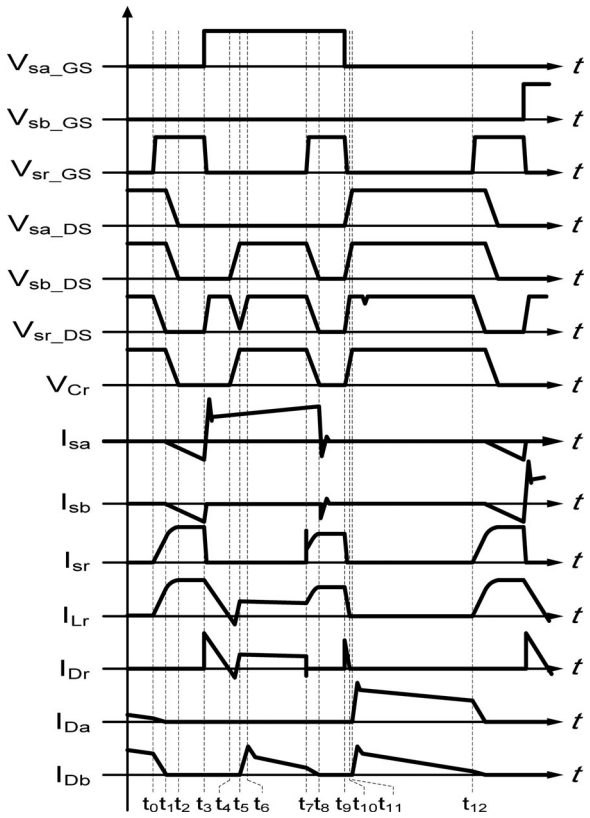

Fig. 3 Related waveforms ($D < 50\%$).

switch is less than 50%. There are some assumptions to simplify the circuit analysis.

1) All power switches and diodes are ideal.
2) The input inductor and output capacitor are ideal.
3) The two inductors are equal; Boost_L_1 = Boost_L_2.
4) The duty cycles of the main switches are equal; $D_1 = D_2$.

Mode 1 [t_0–t_1]: Fig. 4(a) shows the equivalent circuit. In this mode, the main switches S_a and S_b are turned OFF, the auxiliary switch S_r and the rectifier diodes D_a and D_b are turned ON, and the clamped diode D_r is turned OFF. The voltages across the parasitic capacitors C_{Sa} and C_{Sb} of the main switches and the resonant capacitor C_r are all equal to the output voltage; i.e., $V_{Sa} = V_{Sb} = V_{Sr} = V_o$ in the previous mode. The resonant inductor current I_{Lr} linearly ramps up until it reaches $I_{\rm in}$ at $t = t_1$. When the resonant inductor current I_{Lr} is equal to $I_{\rm in}$, the mode 1 will end. Then, the rectifier diodes are turned OFF.

The interval time t_{01} is

$$t_{01} = L_r \cdot \frac{I_{\rm in}}{V_o}. \tag{1}$$

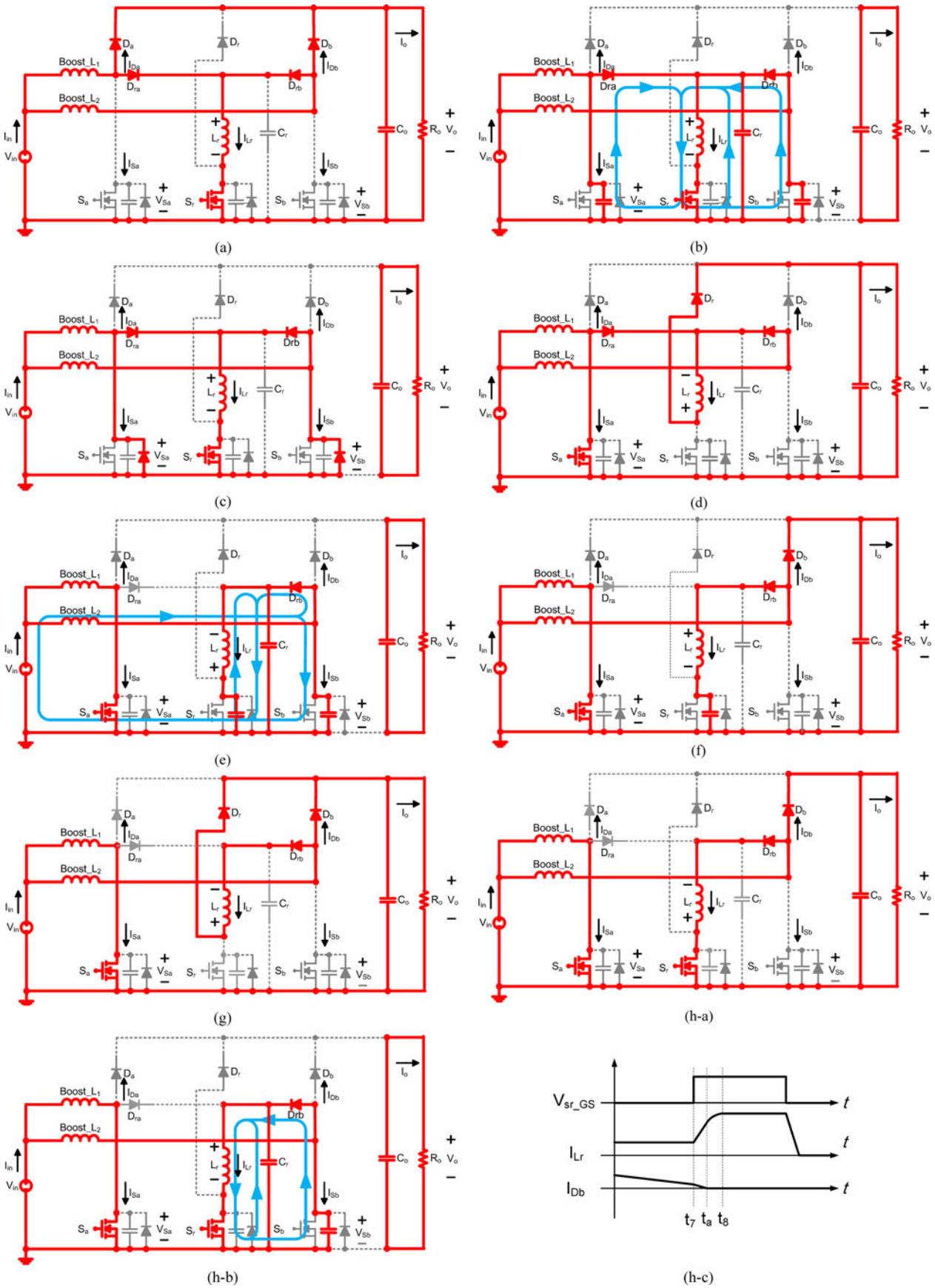

Fig. 4 Equivalent circuits of different modes ($D < 50\%$). (a) Mode 1 [t_0–t_1]. (b) Mode 2 [t_1–t_2]. (c) Mode 3 [t_2–t_3]. (d) Mode 4 [t_3–t_4]. (e) Mode 5 [t_4–t_5]. (f) Mode 6 [t_5–t_6] (g) Mode 7 [t_6–t_7]. (h-a) Mode 8 [t_7–t_a]. (h-b) Mode 8 [t_a–t_8]. (h-c) Detailed waveform of the Mode 8.

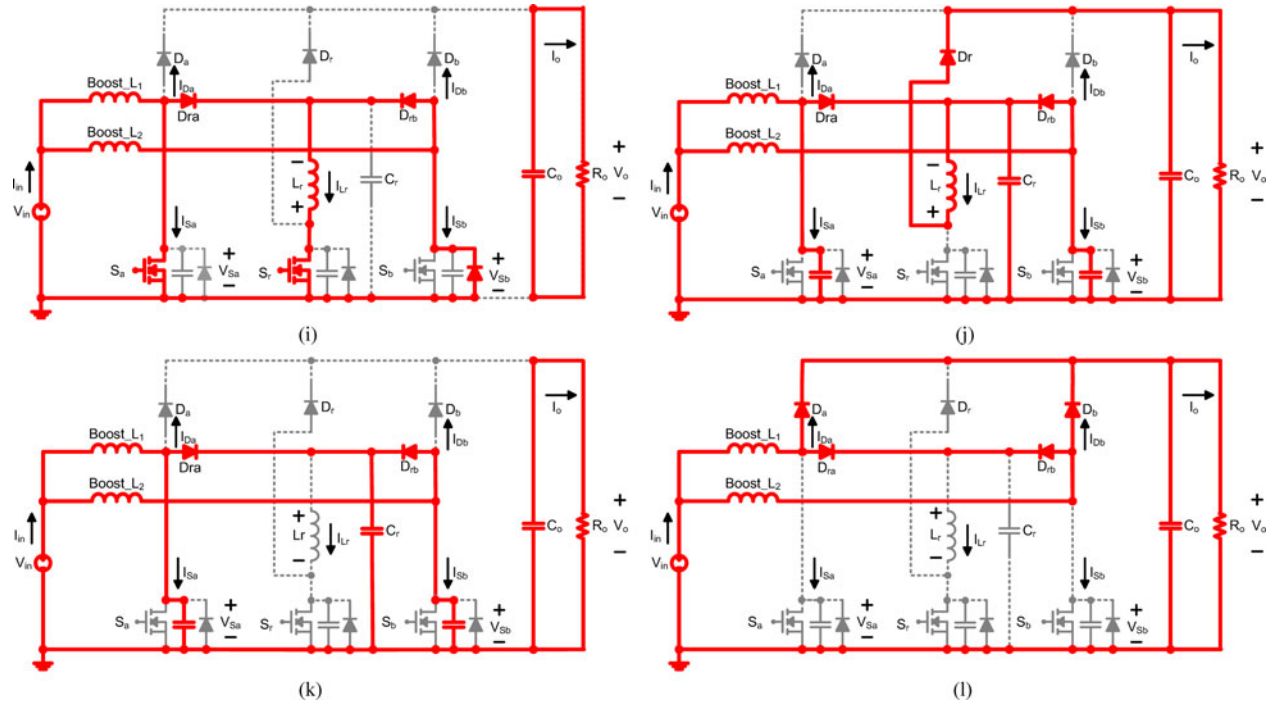

Fig. 4 (*Continued.*) Equivalent circuits of different modes ($D < 50\%$). (i) Mode 9 [t_8–t_9]. (j) Mode 10 [t_9–t_{10}]. (k) Mode 11 [t_{10}–t_{11}]. (l) Mode 12 [t_{11}–t_{12}].

Mode 2 [t_1–t_2]: In mode 2, the resonant inductor current continues to increase to the peak value, and the main switch voltages V_{Sa} and V_{Sb} decrease to zero, because the resonance occurs among C_{Sa}, C_{Sb}, C_r and L_r. Then, the body diodes D_{Sa} (S_a) and D_{Sb} (S_b) can be turned ON.

The resonant time t_{12} and resonant inductor current i_{Lr} (t_2) are

$$t_{12} = \frac{\pi}{2\omega_0} = \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sa} + C_{Sb} + C_r)} \tag{2}$$

$$i_{Lr}(t_2) = I_{\text{in}} + \frac{V_o}{Z_0} = I_{\text{in}} + \frac{V_o}{\sqrt{L_r/(C_{Sa} + C_{Sb} + C_r)}} \tag{3}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_r\,(C_{Sa} + C_{Sb} + C_r)}}$$

$$Z_0 = \sqrt{\frac{L_r}{(C_{Sa} + C_{Sb} + C_r)}}.$$

Mode 3 [t_2–t_3]: Fig. 4(c) shows the equivalent circuit of this mode. At the end of mode 2, the main switch voltage V_{Sa} decreases to zero, so the body diode D_{Sa} of S_a is turned ON at t_2. At this time, the main switch can achieve ZVS. The on-time t_{03} of the auxiliary switch S_r needs to be more than $t_{01} + t_{12}$ to achieve the function of ZVS.

The interval time t_{03} is

$$t_{03} \geq t_{01} + t_{12} = L_r \cdot \frac{I_{\text{in}}}{V_o} + \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sa} + C_{Sb} + C_r)}. \tag{4}$$

Mode 4 [t_3–t_4]: Fig. 4(d) shows the equivalent circuit of this mode. In this mode, the auxiliary switch S_r is turned OFF, and the clamped diode D_r is turned ON. During this interval, the energy stored in the resonant inductor L_r is transferred to the output load. The resonant inductor current I_{Lr} decreases to zero and the clamped diode D_r is turned OFF at t_4.

The energy discharge time of the resonant inductor is

$$t_{34} = \frac{L_r}{V_o}\left(I_{\text{in}} + \frac{V_o}{\sqrt{L_r/(C_{Sa} + C_{Sb} + C_r)}}\right). \tag{5}$$

Mode 5 [t_4–t_5]: In this mode, the clamped diode D_r is turned OFF. The energy of the boost_L$_2$ is transferred to C_r and C_{Sb} and the energy stored in the parasitic capacitor C_{Sr} of the auxiliary switch is transferred to the resonant inductor L_r and resonant capacitor C_r at this time. The rectifier diode D_b is turned ON when the voltage across the main switch S_b reaches V_o at $t = t_5$.

The resonant inductor current i_{Lr} (t) is

$$i_{Lr}(t) = -V_o\sqrt{\frac{CC_{Sr}}{L_r\,(C + C_{Sr})}}\sin\sqrt{\frac{C + C_{Sr}}{L_rCC_{Sr}}}t + \frac{I_{L2}C_{Sr}}{C + C_{Sr}} \times \left(1 - \cos\sqrt{\frac{C + C_{Sr}}{L_rCC_{Sr}}}t\right). \tag{6}$$

The resonant time t_{45} is

$$t_{45} = \pi\sqrt{\frac{L_rCC_{Sr}}{C + C_{Sr}}} \tag{7}$$

where $C = C_r + C_{Sb}$.

Mode 6 [t_5–t_6]: Fig. 4(f) shows the equivalent circuit. The parasitic capacitor C_{Sr} of the auxiliary switch is linearly charged by $I_{L2} - I_o$ to V_o. Then, the clamped diode D_r is turned ON at t_6.

The interval time t_{56} is

$$t_{56} = \frac{C_{Sr} \cdot V_o}{I_{L2} - I_o}. \tag{8}$$

Mode 7 [t_6–t_7]: Fig. 4(g) shows the equivalent circuit. In this mode, the clamped diode D_r is turned ON. The energy stored in the resonant inductor L_r is transferred to the output load by the clamped diode D_r. At t_7, the clamped diode D_r is turned OFF because the auxiliary switch *Sr* is turned ON.

The interval time t_{67} and the resonant inductor current are

$$t_{67} = D_1 T - (D_{rc} T + t_{36}) \tag{9}$$

$$i_{Lr}(t_7) \approx i_{Lr}(t_6) = I_{L2} - I_o. \tag{10}$$

Mode 8 [t_7–t_8]: In the interval [t_7–t_a], the resonant inductor current I_{Lr} increases linearly until it reaches I_{L2} and the rectifier diode current I_{Db} decreases to zero at $t = t_a$, so the rectifier diode D_b is turned OFF. Fig. 4(h-a) shows the equivalent circuit and the detailed waveform is shown in Fig. 4(h-c).

The interval time t_{7a} is

$$t_{7a} = L_r \cdot \frac{I_o}{V_o}. \tag{11}$$

As for the interval time [t_a–t_8], Fig. 4(h-b) shows the equivalent circuit. The resonant inductor current continues to increase to the peak value and the main switch voltage V_{Sb} decreases to zero because of the resonance among C_{Sb}, C_r, and L_r. At $t = t_8$, the body diode D_{Sb} of S_b is turned ON.

The interval time t_{a8} is

$$t_{a8} = \frac{\pi}{2\omega_1} = \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sb} + C_r)}. \tag{12}$$

Then, t_{78} is

$$t_{78} = t_{7a} + t_{a8} = L_r \cdot \frac{I_o}{V_o} + \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sb} + C_r)}. \tag{13}$$

Mode 9 [t_8–t_9]: In this mode, the resonant inductor current I_{Lr} is equivalent to a constant current source. In order to meet the demand that the main switch S_a is turned OFF under the ZCS condition, $i_{Lr}(t_8) \approx i_{Lr}(t_9)$ must be greater than I_{in}. Then the main switch currents I_{Sa} and I_{Sb} are less than or equal to zero, so the main switch S_a is turned OFF under the ZCS condition.

The interval time t_{89} is

$$t_{89} = D_1 T - t_{38}. \tag{14}$$

And, the zero-current switching conditions are

$$1) \quad i_{Lr}(t_8) \approx i_{Lr}(t_9) = i_{Lr}(t_a) + \frac{V_o}{\sqrt{L_r/(C_{Sb} + C_r)}} \geq I_{\text{in}} \tag{15}$$

2) the duty time of ZCS is longer than the interval time t_{78} ($D_{rc} T > t_{78}$).

Mode 10 [t_9–t_{10}]: When the main switch S_a and the auxiliary switch S_r are turned OFF, the energy stored in the resonant inductor L_r is transferred to the output load by the clamped diode D_r. When the resonant inductor current I_{Lr} decreases to zero at t_{10}, the clamped diode D_r is turned OFF. Then, the capacitors C_{Sa}, C_{Sb}, and C_r are charged by I_{in}.

The interval time $t_{9\text{–}10}$ and capacitor voltages of C_{Sa}, C_{Sb}, and C_r are

$$\begin{aligned} t_{9-10} &= \frac{L_r}{V_o}\left(i_{Lr}(t_a) + \frac{V_o}{Z_1}\right) \\ &= \frac{L_r}{V_o}\left(i_{Lr}(t_a) + \frac{V_o}{\sqrt{L_r/(C_r + C_{Sb})}}\right) \end{aligned} \tag{16}$$

$$\begin{aligned} V_{Cr}(t_{10}) &= V_{Sa}(t_{10}) = V_{Sb}(t_{10}) \\ &= \frac{1}{(C_{Sa} + C_{Sb} + C_r)} \int_{t9}^{t10} [I_{\text{in}} - i_{Lr}(t)]\, dt. \end{aligned} \tag{17}$$

Mode 11 [t_{10}–t_{11}]: The capacitors C_{Sa}, C_{Sb}, and C_r are linearly charged by I_{in} to V_o, and the rectifier diodes D_a and D_b are turned ON at t_{11}.

This charged time $t_{10\text{–}11}$ is

$$t_{10-11} = \frac{(C_{Sa} + C_{Sb} + C_r) \cdot (V_o - V_{Cr}(t_{10}))}{I_{\text{in}}}. \tag{18}$$

Mode 12 [t_{11}–t_{12}]: In this mode, the operation of the interleaved boost topology is identical to that of the conventional boost converter. Fig. 4(l) shows the equivalent circuit. The ending time t_{12} is equal to the starting time t_0 of another cycle, because the operation of the interleaved topology is symmetrical.

The interval time $t_{11\text{–}12}$ is

$$t_{11-12} = \frac{T}{2} - (D_1 T + t_{03} + t_{9-11}). \tag{19}$$

1) Voltage Ratio of $D < 50\%$ Mode: Fig. 5(a) shows the real waveforms of the proposed circuit and Fig. 5(b) shows the simplified waveforms. We can ignore some trivial stages. Table I shows the correspondence between the real stages and simplified ones. Fig. 6 shows the equivalent circuits about the operation for the boost inductor Boost_L_1. The inductor Boost_L_2 has the similar results.

So, when the switch is turned ON, the boost inductor current can be derived to be

$$\begin{aligned} \sum_{Sa=\text{on}} \Delta i_{L1} &= \frac{V_{\text{in}} \times (\Delta t_{bc} + \Delta t_{de} + \Delta t_{ef} + \Delta t_{fg} + \Delta t_{hi})}{L_1} \\ &= \frac{V_{\text{in}} \times (D_1 + D_{rc} + 2D_{rv})\, T}{L_1}. \end{aligned} \tag{20}$$

And when the switch is turned OFF, the boost inductor current is

$$\begin{aligned} \sum_{Sa=\text{off}} \Delta i_{L1} &= \frac{(V_{\text{in}} - V_o) \times (\Delta t_{ab} + \Delta t_{cd} + \Delta t_{gh})}{L_1} \\ &= \frac{(V_{\text{in}} - V_o) \times [1 - (D_1 + D_{rc} + 2D_{rv})]T}{L_1}. \end{aligned} \tag{21}$$

Then, the voltage conversion ratio can be derived to be

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1 - (D_1 + D_{rc} + 2D_{rv})}. \tag{22}$$

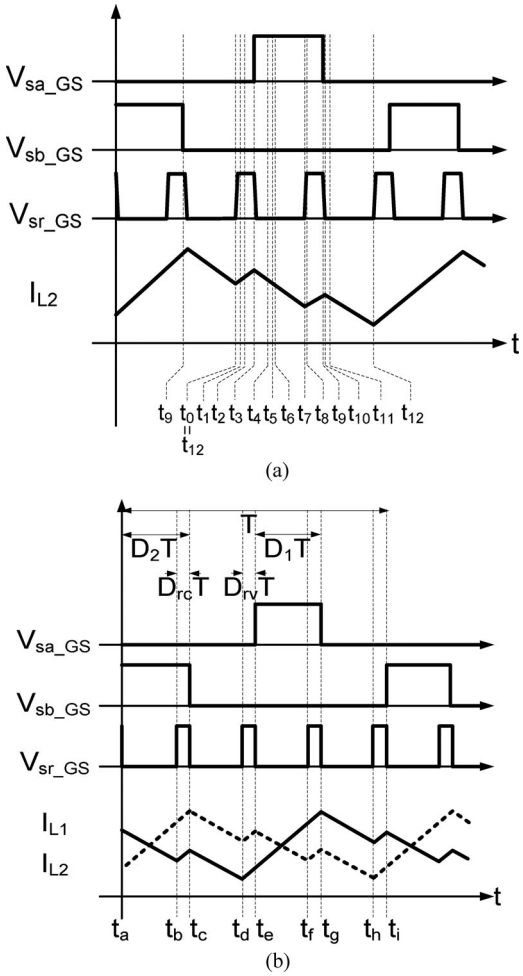

Fig. 5 Switching stages ($D < 50\%$). (a) Real switching stages. (b) Simplified switching stages.

TABLE I
CORRESPONDENCE BETWEEN THE REAL STAGES AND THE SIMPLIFIED ONES ($D < 50\%$)

Real operation stages	Simplified operation stages (Boost_L_1)	Simplified operation stages (Boost_L_2)
$[t_0$-$t_3]$	$[t_d$-$t_e]$	$[t_h$-$t_i]$
$[t_3$-$t_7]$	$[t_e$-$t_f]$	$[t_a$-$t_b]$
$[t_7$-$t_{10}]$	$[t_f$-$t_g]$	$[t_b$-$t_c]$
$[t_{10}$-$t_{12}]$	$[t_g$-$t_h]$	$[t_c$-$t_d]$

B. Operational Analysis of $D > 50\%$ Mode

The principle of the proposed topology operated in $D > 50\%$ mode is described in this section. There are 14 operational modes in the complete cycle. Only seven modes related to the main switch S_a are analyzed, because the interleaved topology is symmetrical. Fig. 7 shows the waveforms when the duty cycle of the main switch is more than 50%. Some assumptions simplifying the circuit analysis are like those in $D < 50\%$ mode.

Mode 1 [t_0–t_1]: Fig. 8(a) shows the equivalent circuit. In this mode, all switches S_a, S_b, and S_r are turned ON, and the rectifier diodes D_a and D_b and clamped diode D_r are turned OFF. The main switch currents I_{Sa} and I_{Sb} are less than or equal to zero when the previous mode ends. The main switch S_b can achieve the ZCS characteristic at $t = t_1$ if the condition in (24) can be met.

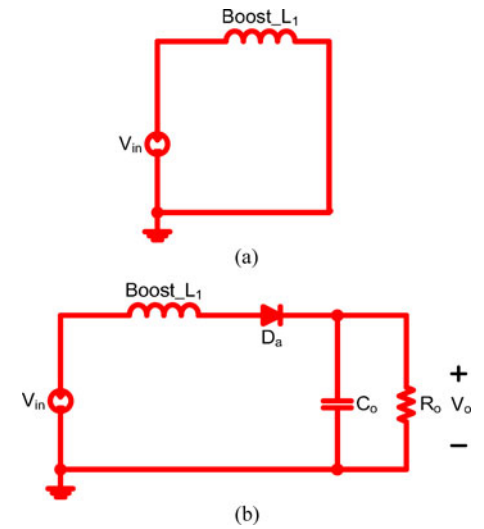

Fig. 6 Equivalent circuits for the boost inductor ($D < 50\%$). (a) Boost_L_1 in the stage $[t_b$–$t_c]$, stage $[t_d$–$t_e]$, stage $[t_e$–$t_f]$, stage $[t_f$–$t_g]$ and stage $[t_h$–$t_i]$. (b) Boost_L_1 in the stage $[t_a$–$t_b]$, stage $[t_c$–$t_d]$ and stage $[t_g$–$t_h]$.

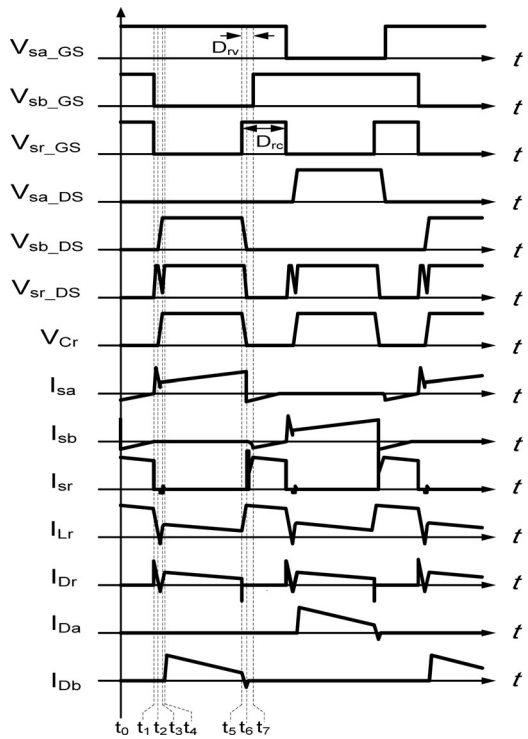

Fig. 7 Related waveforms ($D > 50\%$).

The interval time t_{01} and the resonant inductor current are

$$t_{01} = (D_1 - t_{07})\,T = (D_1 - 0.5)\,T \tag{23}$$

$$i_{Lr}(t_1) = i_{L2}(t_a) + \frac{V_o}{\sqrt{L_r/(C_{Sb} + C_r)}} \geq I_{\text{in}}. \tag{24}$$

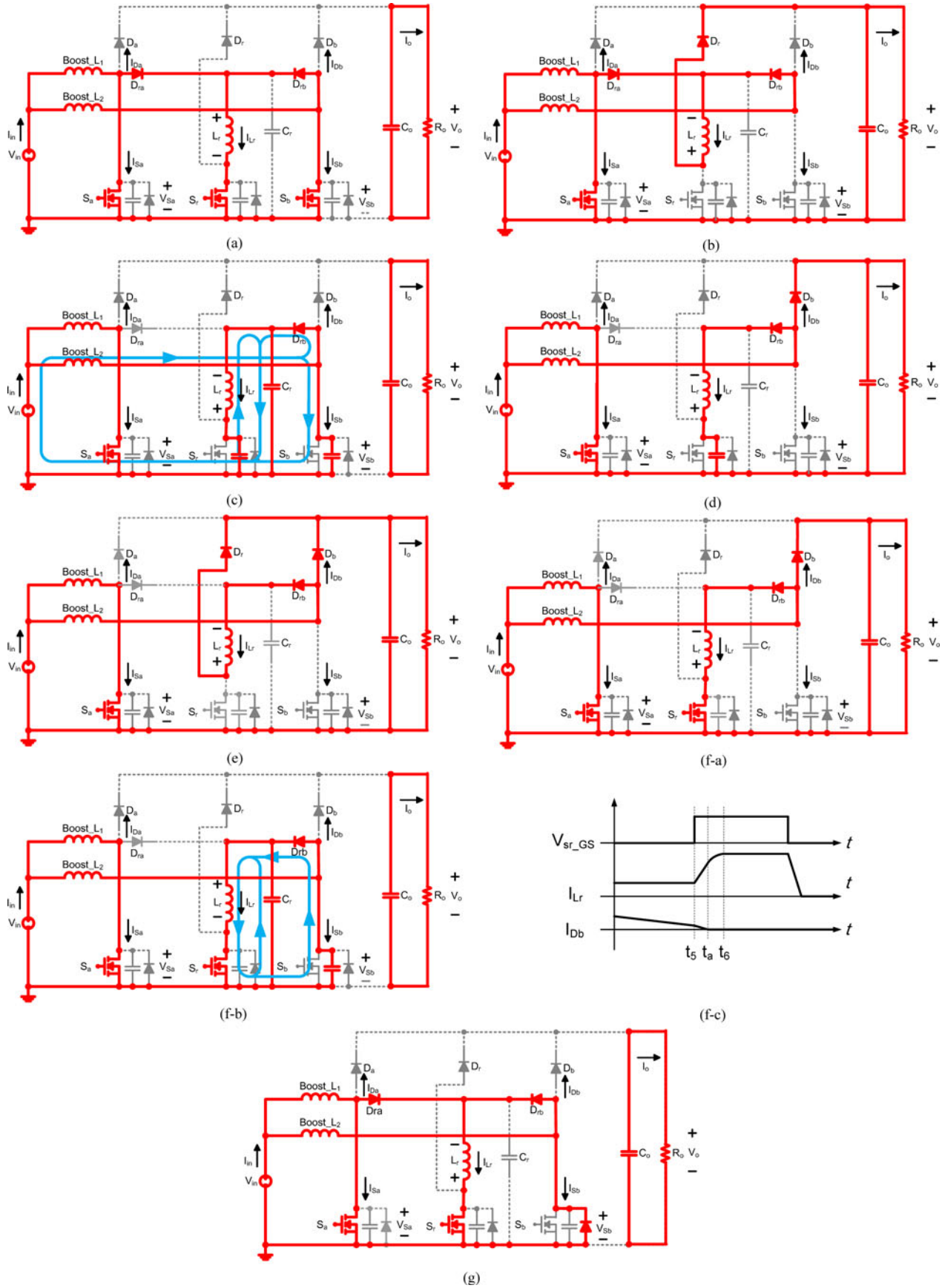

Fig. 8 Equivalent circuits of different modes ($D > 50\%$). (a) Mode 1 [t_0–t_1]. (b) Mode 2 [t_1–t_2]. (c) Mode 3 [t_2–t_3]. (d) Mode 4 [t_3–t_4]. (e) Mode 5 [t_4–t_5]. (f-a) Mode 6 [t_5–t_a]. (f-b) Mode 6 [t_a–t_6]. (f-c) Detailed waveform of the Mode 6. (g) Mode 7 [t_6–t_7].

Mode 2 [t_1–t_2]: The energy stored in the resonant inductor L_r is transferred to the output load by the clamped diode D_r, because the auxiliary switch S_r is turned OFF. When the resonant inductor current I_{Lr} decreases linearly until it reaches zero at $t = t_2$, the clamped diode D_r is turned OFF.

The interval time t_{12} is

$$t_{12} = \frac{L_r}{V_o} I_{\text{in}}. \tag{25}$$

Mode 3 [t_2–t_3]: In this mode, the clamped diode D_r is turned OFF. The energy stored in the boost_L_2 and the energy stored in the parasitic capacitor C_{Sr} of the auxiliary switch are transferred to the resonant inductor L_r, resonant capacitor C_r, and parasitic capacitor C_{Sb} of the main switch at this time. The rectifier diode D_b is turned ON when the main switch voltage V_{Sb} and resonant capacitor voltage V_{Cr} increase to V_o at $t = t_3$.

The resonant inductor current is

$$i_{Lr}(t) = -V_o \sqrt{\frac{CC_{Sr}}{L_r\,(C + C_{Sr})}} \sin \sqrt{\frac{C + C_{Sr}}{L_r C C_{Sr}}}\, t + \frac{I_{L2} C_{Sr}}{C + C_{Sr}} \times \left(1 - \cos \sqrt{\frac{C + C_{Sr}}{L_r C C_{Sr}}}\, t\right). \tag{26}$$

The resonant time t_{23} is

$$t_{23} = \pi \sqrt{\frac{L_r C C_{Sr}}{C + C_{Sr}}}. \tag{27}$$

Mode 4 [t_3–t_4]: After t_3, the parasitic capacitor C_{Sr} of the auxiliary switch is linearly charged by $I_{L2} - I_o$ to V_o. Then, the clamped diode D_r is turned ON at t_4.

The interval time t_{34} is

$$t_{34} \approx \frac{C_{Sr} \cdot V_o}{I_{L2} - I_o}. \tag{28}$$

Mode 5 [t_4–t_5]: Fig. 8(e) shows the equivalent circuit. At t_4, the clamped diode D_r is turned ON. The energy stored in the inductor L_r is transferred to the output load by the clamped diode D_r. The clamped diode D_r is turned OFF when the auxiliary switch S_r is turned ON at $t = t_5$.

The interval time t_{45} and the resonant inductor current are

$$t_{45} = 0.5T - t_{04} - D_{rv}T \tag{29}$$

$$i_{Lr}(t_5) = i_{Lr}(t_4). \tag{30}$$

Mode 6 [t_5–t_6]: Fig. 8(f-a) shows the equivalent circuit and the detailed waveform is shown in Fig. 8(f-c). In the interval [t_5–t_a], the resonant inductor current I_{Lr} increases linearly until it reaches I_{L2} and the rectifier diode current I_{Db} decreases to zero at $t = t_a$, then the rectifier diode D_b is turned OFF.

The interval time t_{5a} is

$$t_{5a} = L_r \cdot \frac{I_o}{V_o}. \tag{31}$$

As for the interval time [t_a–t_6], Fig. 8(f-b) shows the equivalent circuit. The resonant inductor current continues to increase to the peak value and the main switch voltage V_{Sb} decreases to zero because of the resonance among C_{Sb}, C_r, and L_r. At t_6, the body diode D_{Sb} of S_b is turned ON.

The interval time t_{6a} is

$$t_{a6} = \frac{\pi}{2\omega_1} = \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sb} + C_r)}. \tag{32}$$

And the interval time t_{56} is

$$t_{56} = t_{5a} + t_{a6} = L_r \cdot \frac{I_o}{V_o} + \frac{\pi}{2} \cdot \sqrt{L_r \cdot (C_{Sb} + C_r)}. \tag{33}$$

Mode 7 [t_6–t_7]: When the resonant capacitor voltage V_{Cr} and the main switch voltage V_{Sb} are equal to zero, the body diode D_{Sb} of S_b is turned ON. Then, Mode 7 will start. In this mode, the resonant inductor current I_{Lr} is equal to a constant current source. If the condition of $i_{Lr}(t_6) \approx i_{Lr}(t_7) \geq I_{\text{in}}$ can be satisfied, the main switch currents I_{Sa} and I_{Sb} can be less than or equal to zero. Then, the main switch S_a can be turned OFF under the ZCS condition. And the main switch S_b reaches ZVS because of the conduction of the body diode D_{Sb} in this mode. The interval time t_{67} is

$$t_{67} = 0.5T - t_{06}. \tag{34}$$

And the zero-current switching conditions are

$$1) \quad i_{Lr}(t) = i_{L2}(t_a) + \frac{V_o}{\sqrt{L_r/(C_{Sb} + C_r)}} \geq i_{\text{in}}(t) \tag{35}$$

2) the duty time of ZCS is longer than the interval time t_{56} ($D_{rc}T > t_{56}$).

1) Voltage ratio of $D > 50\%$ Mode: Fig. 9(a) shows the real waveforms and Fig. 9(b) shows the simplified waveforms in this mode. Some trivial stages are ignored. Table II shows the correspondence between the real stages and the simplified ones. Fig. 10 shows the equivalent circuits of the operation for the boost inductor Boost_L_1.

When the switch is turned ON, the boost inductor current is

$$\sum_{Sa=\text{on}} \Delta i_{L1} = \frac{V_{\text{in}} \times (\Delta t_{ab} + \Delta t_{bc} + \Delta t_{cd} + \Delta t_{de} + \Delta t_{fg})}{L_1} = \frac{V_{\text{in}} \times (D_1 + D_{rv})\,T}{L_1}. \tag{36}$$

And when the switch is turned OFF, the boost inductor current is

$$\sum_{Sa=\text{off}} \Delta i_{L1} = \frac{(V_{\text{in}} - V_o) \times (\Delta t_{ab} + \Delta t_{cd} + \Delta t_{gh})}{L_1} = \frac{(V_{\text{in}} - V_o) \times [1 - (D_1 + D_{rc} + 2D_{rv})]T}{L_1}. \tag{37}$$

Then, the voltage conversion ratio can be derived to be

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1 - (D_1 + D_{rv})}. \tag{38}$$

III. Design Considerations and Soft-Switching Conditions

The design results in this section are used in the experimental prototype circuit. It is the interleaved boost converter operating in the continuous conduction mode (CCM) with both ZVS and ZCS characteristics.

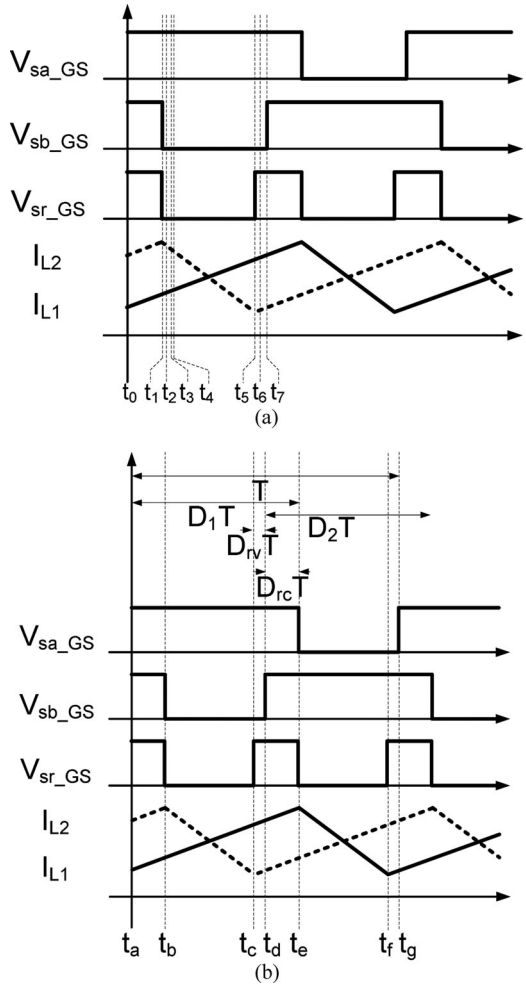

Fig. 9 Switching waveforms ($D > 50\%$). (a) Real waveforms. (b) Simplified waveforms.

TABLE II
CORRESPONDENCE BETWEEN THE REAL STAGES AND THE SIMPLIFIED ONES (D> 50%)

Real operation stages	Simplified operation stages (Boost_L_1)	Simplified operation stages (Boost_L_2)
$[t_0$-$t_1]$	$[t_a$-$t_b]$	$[t_e$-$t_f]$
$[t_1$-$t_5]$	$[t_b$-$t_c]$	$[t_f$-$t_g]$
$[t_5$-$t_7]$	$[t_c$-$t_d]$	$[t_g$-$t_h]$

A. Converter Specification

The switching frequency f_s is 50 kHz, the output voltage V_o is 400 V, and the range of the output power P_{out} is 200–600 W. The prototype circuit operates at 150–250 V_{dc}.

B. Selection of the Boost Inductors and Output Capacitor

The output capacitor is a high-voltage bulk capacitor (490 μF, 450 V). And the boost inductors (Boost_L_1 and Boost_L_2) are designed to operate in the CCM. Their design considerations can refer to [19]–[22].

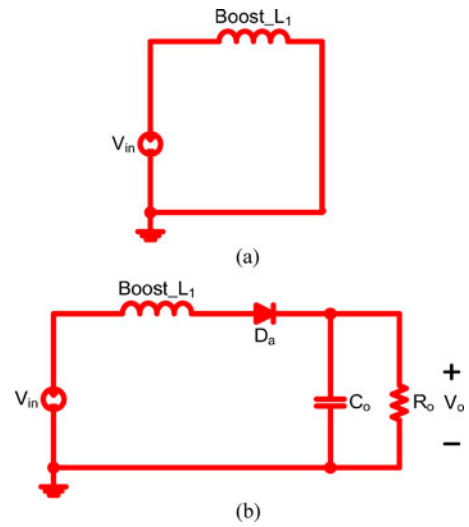

Fig. 10 Equivalent circuits for the boost inductor ($D > 50\%$). (a) Boost_L_1 in the stage $[t_a$–$t_b]$, stage $[t_b$–$t_c]$, stage $[t_c$–$t_d]$, stage $[t_d$–$t_e]$, and stage $[t_f$–$t_g]$. (b) Boost_L_1 in the stage $[t_e$–$t_f]$.

The minimum boost inductor when $D < 50\%$ is

$$L_{\min}|_{L=L_1 \text{ or } L_2} = \frac{(D_1 + 2D_{rv})\left[1 - (D_1 + 2D_{rv})\right]^2 R_{\max}}{f_S} = 2.36\,\text{mH}.$$

The minimum boost inductor when $D > 50\%$ is

$$L_{\min}|_{L=L_1 \text{ or } L_2} = \frac{(D_1 + D_{rv})\left[1 - (D_1 + D_{rv})\right]^2 R_{\max}}{f_S} = 1.43\,\text{mH}.$$

So, we select the boost inductors to be 2.4 mH.

C. Selection of the Main Switches, Auxiliary Switch, and Diodes

When the main switches and auxiliary switch are turned OFF, the voltage stress of these switches is equal to the output voltage (400 V). The current stress of the main switches is equal to the maximum boost inductor current:

$$I_{L\max}|_{L=L_1 \text{ or } L_2} = \frac{V_{\text{in}}}{2\left[1 - (D_1 + D_{rv})\right]^2 R} + \frac{V_{\text{in}}(D_1 + D_{rv})T}{2L_1} = 1.99\,\text{A}.$$

The current stress of the auxiliary switch is equal to the maximum resonant inductor current at $t = t_6$:

$$i_{Lr}(t_6) = \frac{V_{\text{in}}}{2\left[1 - (D_1 + D_{rv})\right]^2 R} - \frac{V_{\text{in}}(D_1 + D_{rv})T}{2L_2} + \frac{V_o}{\sqrt{L_r/(C_{Sb} + C_r)}} = 7.72\,\text{A}.$$

Therefore, two IRF840s are used as the main switches S_a and S_b and the auxiliary switch S_r is IRFP460. As for the rectifier diodes D_a and D_b, the voltage stress is equal to V_o and the current stress is equal to I_{Sa}. They are HFA08TB60s. The current stress of D_{ra} and D_{rb} is half of I_{Lr} and the current stress

of the clamped diode D_r is equal to I_{Lr}, and these diodes are HFA08TB60s.

D. Condition of Soft Switching

The resonant capacitors C_{Sa} and C_{Sb} are parasitic capacitors of the main switches S_a and S_b, respectively. However, the resonant capacitor C_r is an additional capacitor and the resonant inductor L_r is also an additional inductor.

1) Design of the Duty Time for the ZVS Conditions: To achieve the aim of the ZVS of the main switches, the voltages across S_a and S_b in Mode 2 for $D < 50\%$ and Mode 6 for $D > 50\%$ must be assured to decrease to zero. It must be considered that there is enough time to reach the zero-voltage switching.

Therefore, in Mode 2 ($D < 50\%$), the $D_{rv}T$ must be longer than

$$D_{rv}T > t_{12} = \frac{\pi\sqrt{L_r\left(C_{Sa}+C_{Sb}+C_r\right)}}{2} = \frac{3.14\times\sqrt{10\mu\times 2120p}}{2} = 225\,\text{ns}.$$

And $D_{rv}T$ in Mode 6 ($D > 50\%$) is

$$D_{rv}T > t_{56} = \frac{\pi\sqrt{L_r\left(C_{Sb}+C_r\right)}}{2} = \frac{3.14\times\sqrt{10\mu\times 1810p}}{2} = 211\ \text{ns}.$$

Therefore, the maximum $D_{rv}T$ is selected in the design.

2) Design of the Duty Time for the ZCS Conditions: If the conditions in Mode 9 for $D < 50\%$ and Mode 7 for $D > 50\%$ are met, then the main switches can achieve ZCS. In Mode 9, the resonant inductor current and $D_{rc}T$ are

$$i_{Lr}\left(t_9\right) = I_{L2}\left(t_a\right) + \frac{V_o}{Z_1} = I_{L2}\left(t_a\right) + \frac{V_o}{\sqrt{L_r/(C_{Sb}+C_r)}} = 7.05\text{A} > I_{\text{in}}$$

$$D_{rc}T > t_{78} = t_{7a} + t_{a8} = L_r\cdot\frac{I_o}{V_o} + \frac{\pi}{2}\cdot\sqrt{L_r\cdot\left(C_{Sb}+C_r\right)} = 249\,\text{ns}.$$

And the resonant inductor current and $D_{rc}T$ in Mode 7 are

$$i_{Lr}\left(t_6\right) = I_{L2}\left(t_a\right) + \frac{V_o}{Z_1} = i_{L2}(t_a) + \frac{V_o}{\sqrt{L_r/(C_{Sb}+C_r)}} = 7.72\text{A} > I_{\text{in}}$$

$$D_{rc}T > t_{56} = t_{5a} + t_{a6} = L_r\cdot\frac{I_o}{V_o} + \frac{\pi}{2}\cdot\sqrt{L_r\cdot\left(C_{Sb}+C_r\right)} = 249\,\text{ns}.$$

Therefore, we can select the maximum $D_{rc}T$ in the design and the soft-switching conditions can be satisfied.

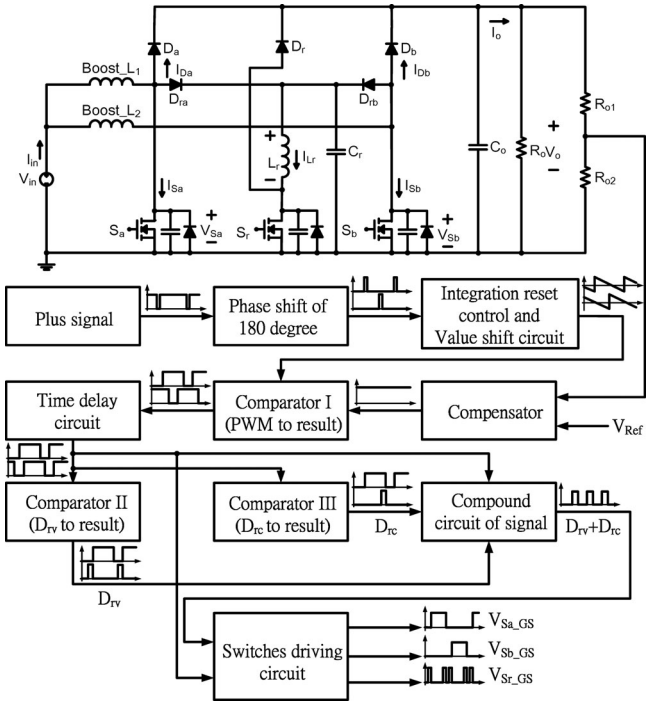

Fig. 11 Driving circuit.

TABLE III
PARAMETERS AND COMPONENTS OF THE CONVERTER

Specification			
Input voltage	V_{in}	150 V	250V
Duty cycle	D	D>50%	D<50%
Output voltage	V_O	400 V	
Output current	I_O	0.5A~1.5A	
Output power	P_O	200W~600W	
Switching frequency	f_S	50 kHz	
Boost_L_1,Boost_L_2		2.4 mH	
Output capacitor	C_O	470 μF	
Resonant inductor	L_r	10 μH	
Resonant capacitor	C_r	1.5 nF	
Main switches	S_a, S_b	IRF840	
Auxiliary switch	S_r	IRFP460	
Rectifiers	D_a, D_b	HFA08TB60	
Auxiliary diodes	D_t ,D_{ra}, D_{rb}	HFA08TB60	

E. Design of the Driving Circuit

Fig. 11 shows the driving circuit of the proposed topology. It uses the time delay circuit to delay PWM1 and PWM2 signals and then the circuit sends them to the comparators II and III to produce D_{rv} and D_{rc} signals.

The specialty of this circuit lies on the automatic judgment whether the duty cycle is more than 50% or not. Therefore, it does not need to be adjusted by human. The circuit can automatically produce the necessary driving signals of the main switches and the auxiliary switch no matter what condition the duty cycle is in. Furthermore, the users can also only apply the ZVS or ZCS function just by adjusting the driving circuit.

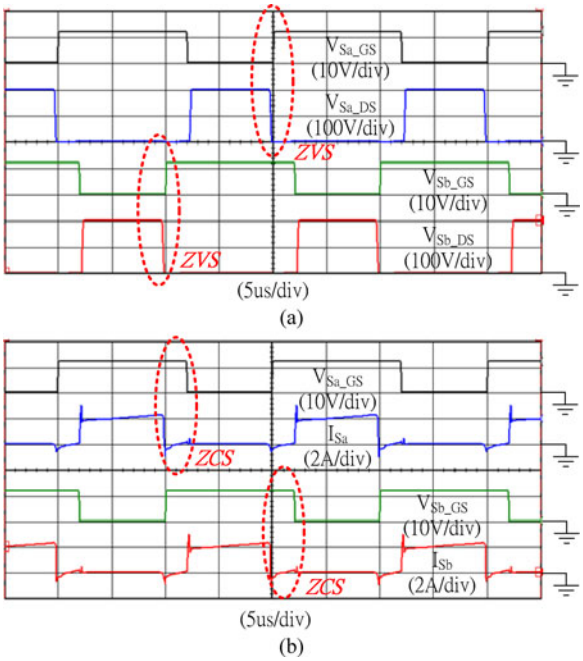

Fig. 12 Simulation waveforms of the main switches S_a and S_b ($D > 50\%$ and load current 1.5 A). (a) ZVS. (b) ZCS.

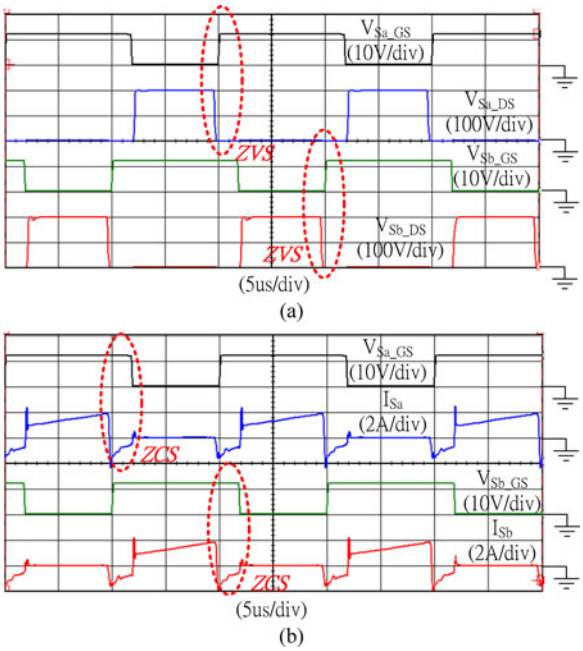

Fig. 13 Simulation waveforms of the main switches S_a and S_b ($D > 50\%$ and load current 0.5 A). (a) ZVS. (b) ZCS.

However, because this driving circuit is composed of the low-cost ICs, the driving signals of the proposed converter may be affected by each other. It can be improved by more precisely designed IC.

IV. Simulation and Experimental Results

Table III gives the parameters and components used in this paper. Figs. 12–14 show the simulation results. They verify the

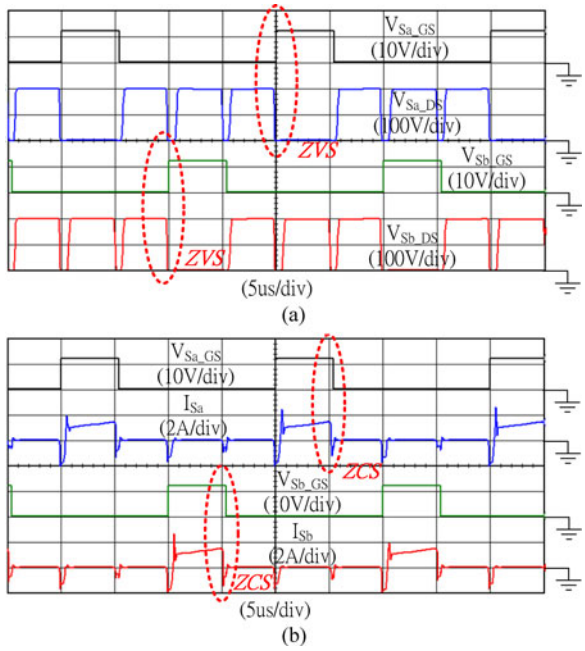

Fig. 14 Simulation waveforms of the main switches S_a and S_b ($D < 50\%$). (a) ZVS. (b) ZCS.

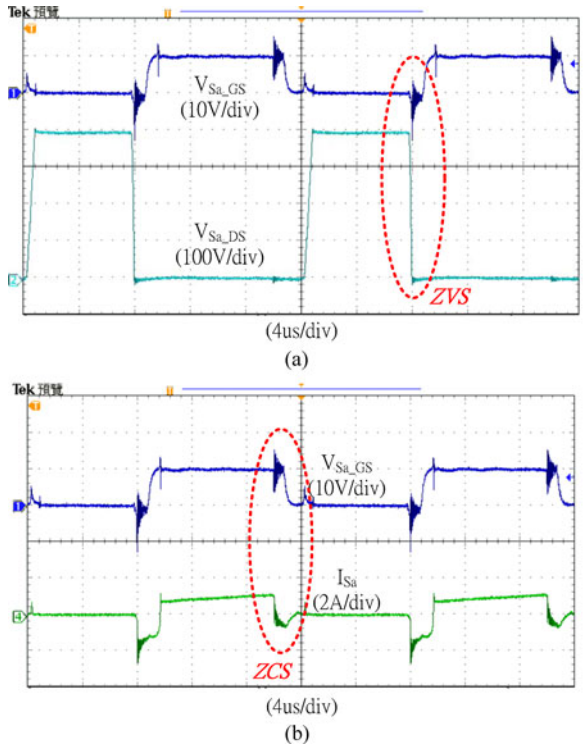

Fig. 15 Switching waveforms of the main switch S_a (load current 0.5 A). (a) ZVS. (b) ZCS.

operation of the proposed circuit. However, the experiments are conducted to further confirm them. Based on the design considerations in Section III, the proposed interleaved boost converter with both ZVS and ZCS characteristics was built.

Fig. 15 shows the experimental waveforms of the proposed circuit when the input voltage is 150 V and the load current is

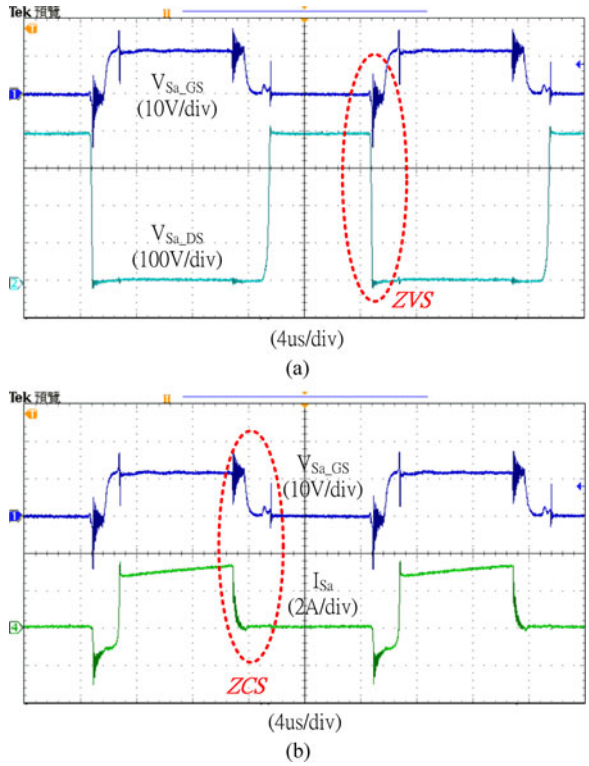

Fig. 16 Switching waveforms of the main switch S_a (load current 1.5 A). (a) ZVS. (b) ZCS.

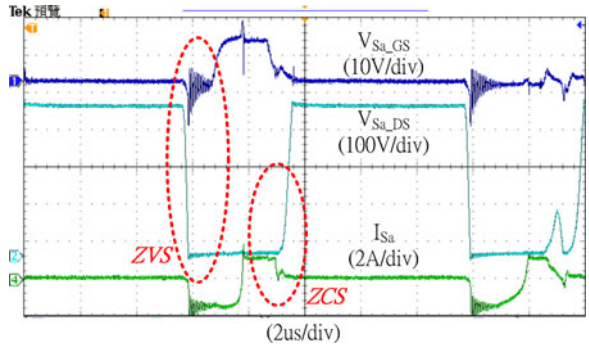

Fig. 17 Switching waveforms of the main switch S_a ($D < 50\%$).

0.5 A. In Fig. 15(a), the voltage V_{Sa_DS} reaches zero before the main switch S_a is turned ON, and the main switch current I_{Sa} is less than or equal to zero when the main switch S_a is turned OFF in Fig. 15(b).

Fig. 16 shows the waveforms of the proposed circuit at load current of 1.5 A. In Fig. 16(a), the voltage V_{Sa_DS} reaches zero before the switch is turned ON, and the switch current I_{Sa} is less than or equal to zero when the main switch S_a is turned OFF in Fig. 16(b). The experimental waveforms are shown in Fig. 17 when the proposed converter is operated in the situation of duty cycle less than 50%. The related voltage and current waveforms of the auxiliary switch are shown in Fig. 18. Fig. 19 shows the efficiency comparison of the proposed topology.

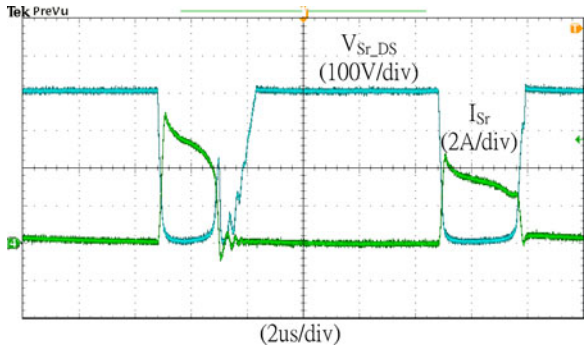

Fig. 18 Switching waveforms of the auxiliary switch S_r.

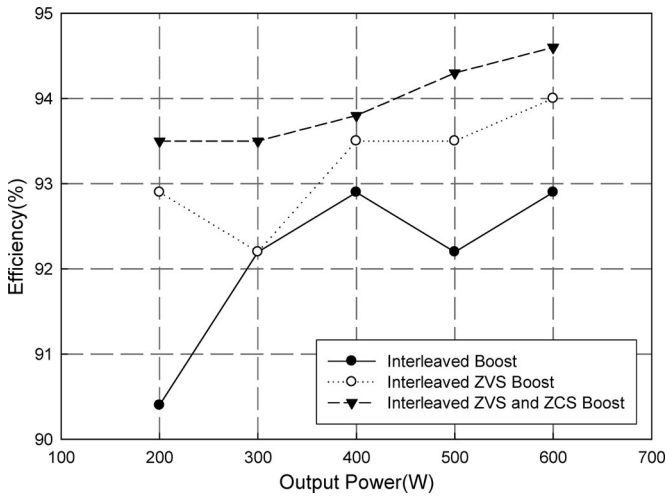

Fig. 19 Measurement of Efficiency.

V. Conclusion

A novel interleaved boost converter with both zero-voltage-switching and zero-current-switching functions is proposed in this paper. The duty cycle of this topology can be more or less than 50%. A prototype circuit of this converter has been implemented. Its input voltage is from 150 to 250 V and output voltage is 400 V. The load variation is from 200 to 600 W. It has many characteristics.

1) The main switches S_a and S_b can achieve both ZVS and ZCS.
2) The voltage stress of all switches is equal to the output voltage.
3) It has the smaller current stress of elements.
4) It uses the resonant inductor L_r, resonant capacitor C_r, parasitic capacitors C_{Sa} and C_{Sb}, and auxiliary switch S_r to become a common resonant way to reach ZVS and ZCS of the main switches S_a and S_b.
5) The driving circuit can automatically detect whether the driving signals of the main switches are more than 50% or not and get the driving signal of the auxiliary switch.
6) The users can only apply the ZVS or ZCS function just by the adjustment of the driving circuit.

7) The efficiency is 94.6% with output power of 600 W and input voltage of 150 V and it is 95.5% with output power of 400 W and input voltage of 250 V.

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