Analysis, Modeling, and Implementation of a Multidevice Interleaved DC/DC Converter for Fuel Cell Hybrid Electric Vehicles

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***Abstract*—Multiphase converter topologies for use in high-performance applications have received increasing interest in recent years. This paper proposes a novel multidevice interleaved boost converter (MDIBC) that interfaces the fuel cell with the powertrain of hybrid electric vehicles. In this research, a multidevice structure with interleaved control is proposed to reduce the input current ripples, the output voltage ripples, and the size of passive components with high efficiency compared with the other topologies. In addition, low EMI and low stress in the switches are expected. The proposed dc/dc converter is compared to other converter topologies such as conventional boost converter (BC), multidevice boost converter (MDBC), and two-phase interleaved boost converter (IBC) to verify its dynamic performance. Furthermore, a generalized small-signal model is derived for these dc/dc converters, which has not been previously discussed. A digital dual-loop control is designed to achieve the proper regulator for the converters with fast transient response. The dc/dc converter topologies and their controller are designed and investigated by using MATLAB/Simulink. Finally, the proposed converter (MDIBC) is experimentally validated with results obtained from a 30-kW prototype that has been built and tested in our laboratory based on TMS320F2808 DSP. The simulation and experimental results have demonstrated that the proposed converter is more efficient than other dc/dc converter topologies in achieving high performance and reliability for high-power dc/dc converters.**

***Index Terms*—Converter losses model, closed-loop control strategy, direct digital control (DDC), digital signal processor (DSP), dc/dc boost converters, fuel cell hybrid electric Vehicles (FCHEVs), generalized small-signal model.**

I. Introduction

FUEL CELL (FC) technologies are expected to become an attractive power source for automotive applications because of their cleanness, high efficiency, and high reliability. Although there are various FC technologies available for use in automotive systems, the polymer electrolyte membrane FC (PEMFC) has been found to be a prime candidate, since PEMFC has high power density with lower operating temperatures when compared to other types of FC systems [1]–[3]. Although FC systems exhibit good power capability during steady-state operation, the dynamic response of FCs during transient and instantaneous peak power demands is relatively slow. Therefore, the FC system can be hybridized with energy storage systems (ESS) (e.g., batteries or supercapacitors) to improve the performance of the FC system during transient and instantaneous peak power demands of a hybrid electric vehicle (HEV) and to recover energy through regenerative braking [1]–[6]. For these applications, a high-power dc/dc converter is a key element that interfaces the FC or ESS with the dc bus in the powertrain of the HEVs. Therefore, the dc system with multiple dc/dc converters may play an important role in the future powertrain system. The topology design of dc/dc converters has been documented in many pieces of literature [7]–[13]. In addition, the design of high-power dc/dc converters and their controller play an important role to control power regulation particularly for a common dc bus. The advantages and disadvantages of serveral topologies of dc/dc converters, based on their component count, are presented and compared in [11]–[14]. Furthermore, for high-power applications, multiphase interleaved converters have been proposed for use in electric vehicle applications [15]–[21].

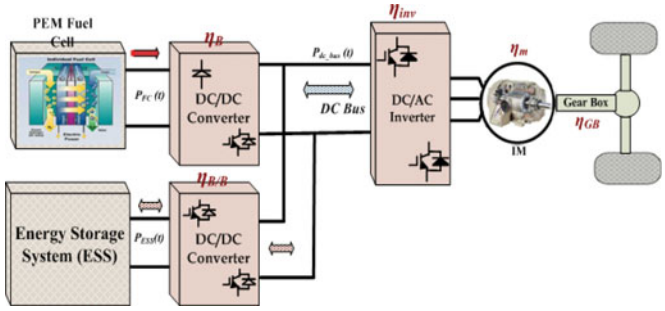

Fig. 1. Block diagram of the FCHEV.

The fuel cell hybrid electric vehicle (FCHEV), as shown in Fig. 1, utilizes an FC as the main power source and the ESS (e.g., batteries and supercapacitors) as the auxiliary power source to assist the propulsion of the vehicle during transients and to recuperate energy during regenerative braking. In this configuration, the FC is connected to the dc bus through a boost converter, whereas the ESS is connected to the dc bus via a bidirectional dc/dc converter. As was mentioned in much of the literature, the dc/dc converter is one of the most important components in a FC powered system. It allows a desired level of dc voltage to be obtained without having to increase the stack size. As a result, this research will focus on a nonisolated dc/dc converter that interfaces the FC with the powertrain of HEVs. In high-power boost

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converters, the major design aspect is the selection of the boost inductor and the output capacitor. The major concern is the size, cost, and weight of such a high-power inductor that is perhaps the single heaviest component in the entire dc/dc converter. To reduce the inductor size and weight, a small inductance value is preferred. In addition, the dc/dc converter performance directly influences the characteristics of the FC stack or the ESS (e.g., batteries).

Indeed, the ripple and harmonic content of the current is one of the various phenomena influencing FC lifespan as well as battery lifetime as reported in [6], [10], and [12]. It is clear that the main objective of this research is to minimize inductor size, capacitor, current/voltage ripples, and harmonic content. Another objective of this study is to present a DSP-based digital control implementation for a high-power interleaved converter to solve the synchronization problem of the interleaved scheme. The digital control can play an important role in improving the control efficiency in high-power interleaved converter applications. Additionally, the digital control features programmability, modularity, and better dynamic response. They have become more popular because of the decreasing cost of hardware, such as microprocessors, analog to digital converters, and digital to analog converters.

In this paper, a novel multidevice interleaved boost converter (MDIBC) has been studied and analyzed to reduce the size and weight of the passive components, such as the inductor, capacitor, and input/output electromagnetic interference (EMI) filter. Meanwhile, the input current ripple and output voltage ripple can be minimized with high efficiency and reliability. Furthermore, the proposed converter will be compared to other dc/dc converter topologies (e.g., BC, MDBC, and IBC) to investigate its dynamic response. Furthermore, the generalized small-signal model (SSM) and losses model are derived in order to design the appropriate closed-loop control and calculate the efficiency, respectively. These models consider the internal resistances of the inductor and capacitor. Moreover, a dual-loop control strategy based on TMS320F2808 DSP has been developed to implement the control strategy for the dc/dc converter. Simulation and experimental results are provided.

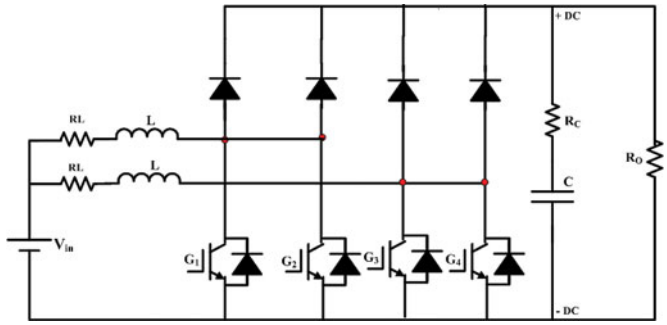

Fig. 2. Structure of the proposed dc/dc converter (MDIBC). ($m = 2$ and $n = 2$).

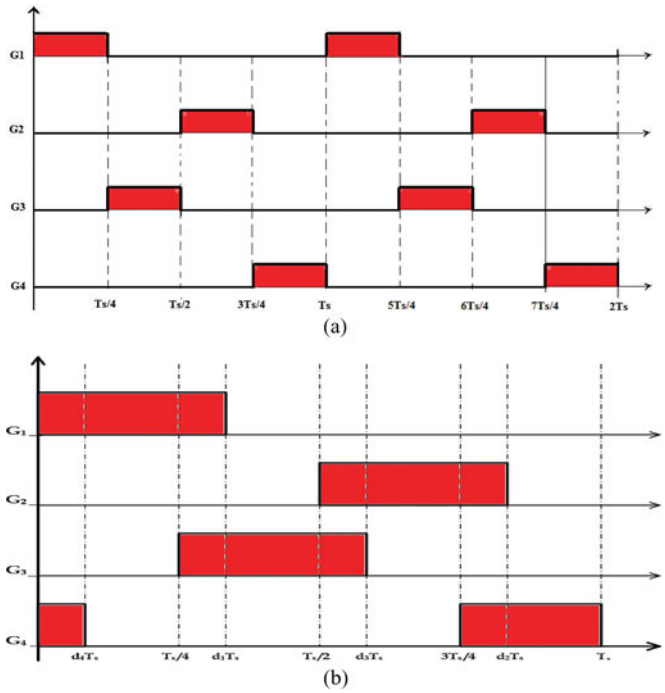

Fig. 3. Sequence of the driving gate signals for switches. (a) $d = T_s/4$. (b) $d \geq T_s/4$.

II. Proposed Converter Structure

The structure of the MDIBC is depicted in Fig. 2. This converter consists of two-phase interleaved with two switches and two diodes connected in parallel per phase. The easy way to reduce the size of the inductor, capacitor, and input/output EMI filter is by increasing the frequency of the inductor current ripple and the output voltage ripple. The phase-shift interleaved control is proposed to achieve the control strategy. This control strategy will provide a doubled ripple frequency in inductor current at the same switching frequency, which can contribute to a higher system bandwidth. This bandwidth achieves a fast dynamic response for the converter and reduces the size of the passive components.

In addition, the sequence of the driving signals is very important to providing a doubled ripple frequency in inductor current at the same switching frequency and to achieve the interleaved control between inductors as illustrated in Fig. 3. With the proposed control, the switching pattern is shifted by $360^\circ/(n \times m)$, where m is the number of parallel power switches per channel, while n is the number of channels or phases. The input current ripple is $(n \times m)$ times of the switching frequency. Similarly, the output voltage ripple is $(n \times m)$ times of the switching frequency. As a result, the size of the passive components will be reduced by m times compared with the n-phase interleaved dc/dc converters. In this proposed converter structure, m is selected to be 2, while n is chosen to be 2. Fig. 3 demonstrates the sequence of the driving signals at different duty cycles. Furthermore, the equivalent circuits of the proposed converter modes for $d > 0.25$ are presented in Fig. 4, where d is the duty cycle. It is also assumed that the proposed converter operates in the continuous conduction mode (CCM). The load current is assumed to be ripple free. All switches have identical duty cycles which means $d_1 = d_2 = d_3 = d_4 = d$.

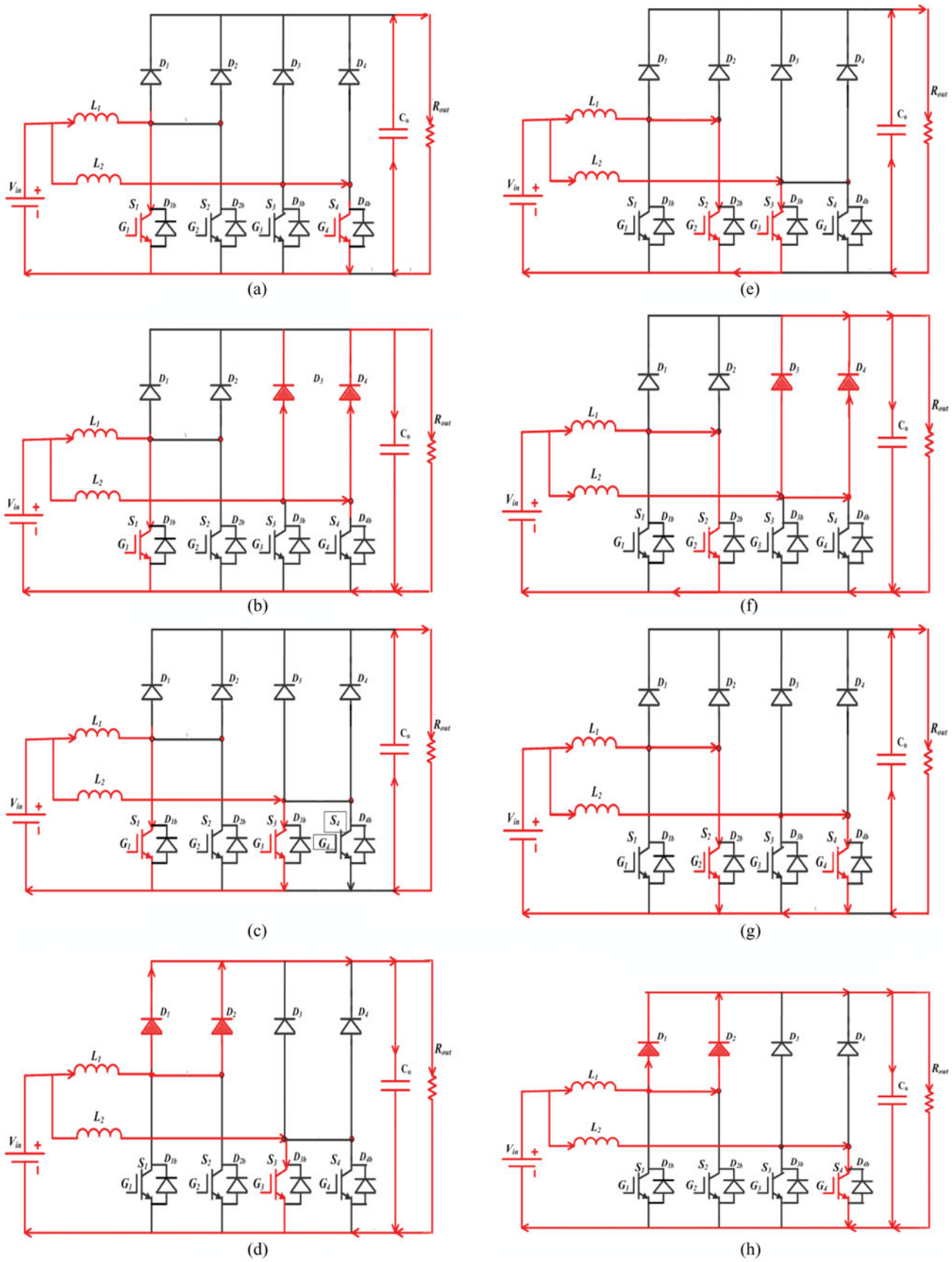

Fig. 4. Equivalent circuits of the proposed converter for $d > 0.5$. The intervals are mentioned in Fig. 3(b). (a) Mode 1: $0 \leq t \leq d_1\ T_s$. (b) Mode 2: $d_4\ T_s \leq t \leq T_s/4$. (c) Mode 3: $T_s/4 \leq t \leq d_1\ T_s$. (d) Mode 4: $d_1\ T_s \leq t \leq T_s/2$. (e) Mode 5: $T_s/2 \leq t \leq d_3\ T_s$. (f) Mode 6: $d_3\ T_s \leq t \leq 3\ T_s/4$. (g) Mode 7: $3\ T_s/4 \leq t \leq d_2\ T_s$. (h) Mode 8: $d_2\ T_s \leq t \leq T_s$.

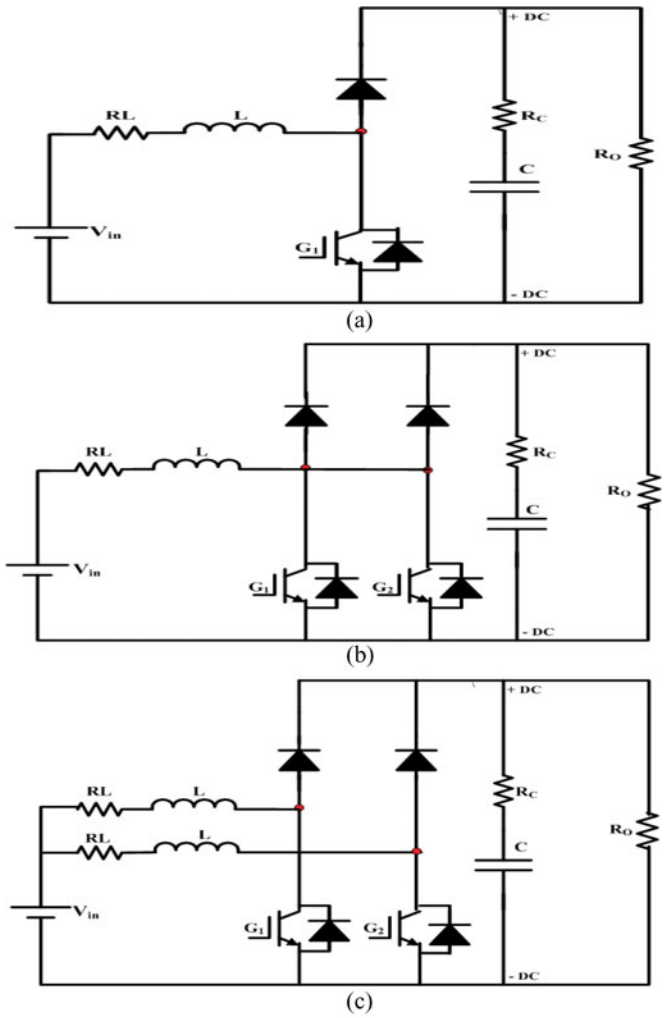

Fig. 5. DC/DC converter topologies. (a) BC. (b) MDBC. (c) Two-phase IBC.

In this research, the proposed converter is compared with three dc/dc converter topologies including conventional boost converter (BC), multidevice boost converter (MDBC), and two-phase interleaved boost converter (IBC) to investigate its performance. Fig. 5 presents the configurations of these dc/dc converters [6], [14]–[19].

III. Generalized Small-Signal Model

SSM is a well-known method used to analyze the performance of nonlinear systems such as pulse-width modulated (PWM) dc/dc converters. To obtain a certain performance objective, the SSM is crucial to the design of the closed-loop control for PWM dc/dc converters. The ac-equivalent circuit models have been studied in the literature [22]–[26]. In this paper, a generalized SSM is derived, which has not been discussed previously, to design the appropriate controller using bode diagram. In this paper, the small-signal transfer functions from the duty cycle to the inductor current and from the duty cycle to the output voltage in CCM are derived as follows:

$$G_{vd}(s) = \frac{\hat{\nu}_o(s)}{\hat{d}(s)} = G_{dv}\frac{(1+(s/\omega_{zv1}))(1-(s/\omega_{zv2}))}{\Delta(s)} \quad (1)$$

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = G_{di}\frac{(1+(s/\omega_{zi}))}{\Delta(s)} \quad (2)$$

where

$$G_{dv} = \frac{V_o}{(1-D)}\left[\frac{-mR_L + n\,(1-mD)^2\,R_o}{\delta\,R_L + n\,(1-mD)^2\,R_o}\right] = \frac{V_o}{1-D} \quad (3)$$

$$\omega_{zv1} = \frac{1}{C\,R_C} \quad (4)$$

$$\omega_{zv2} = \frac{n\,(1-mD)^2\,R_o - mR_L}{mL} \quad (5)$$

$$\Delta(s) = \frac{s^2}{\omega_0^2} + \frac{s}{Q\omega_0} + 1 \quad (6)$$

$$\omega_0 = \sqrt{\frac{\delta\,R_L + n\,(1-mD)^2\,R_o}{\delta\,LC\,(R_o + R_C)}} \quad (7)$$

$$\zeta = \frac{\delta\,L + C\left(\delta\,R_L\,(R_o+R_C) + n\,(1-mD)^2\,R_oR_C\right)}{2\sqrt{\delta\,LC\,(R_o+R_C)\left[\delta R_L + n\,(1-mD)^2\,R_o\right]}} \quad (8)$$

$$Q = \frac{1}{2\xi} \text{ and } \delta = \left(\frac{1-m\,D}{1-D}\right) \quad (9)$$

$$G_{\mathrm{di}} = \frac{V_o\,(m+\delta)}{\delta\,R_L + n\,(1-mD)^2\,R_o} \quad (10)$$

$$\omega_{zi} = \frac{1}{C\,(R_C + (\delta\,R_o/\,(m+\delta)))} \quad (11)$$

$$V_o = \frac{V_{\mathrm{in}}}{(1-m\,D)} \quad (12)$$

$$I_L = \frac{V_o}{n(1-m\,D)R_o} \quad (13)$$

where V_o is the output voltage, C is the capacitance, L is the inductance, and R_L is the internal resistance of the inductor. R_C is the internal resistance of the capacitor, n is the number of phases, m is the number of parallel switches per phase, V_{in} is the input voltage, D is the duty ratio, and R_o is the resistance of the load. The transfer function (1) is a second-order system, which has two LHP poles: one LHP zero given by (4) and one RHP zero given by (5). The angular corner frequency w_0 and right-half-plane zero $w_z v_2$ are the functions of the nominal duty cycle D. In the closed-loop voltage control, the system elements will change as the duty cycle changes, which means that the transfer function will change accordingly. The boost converter under feedback control is a nonlinear function of the duty cycle, which makes the controller design of the boost converter more challenging from the viewpoint of stability and bandwidth [22], [26].

IV. Closed-Loop Control Strategy

The closed-loop control strategy of the PWM boost converter should be designed to satisfy the current and voltage requirements. In this study, the proportional-integer (PI) controllers are

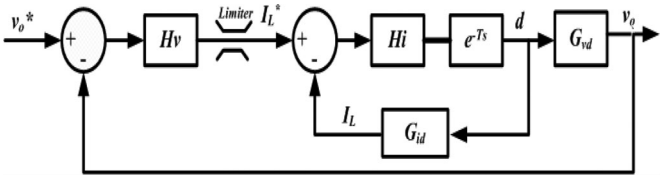

Fig. 6. Schematic diagram of the dual-loop control.

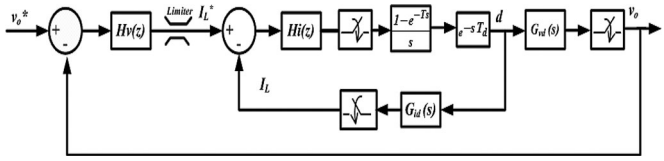

Fig. 7. Dual-loop digital control structure.

designed to keep a constant bus voltage of 400 V in converter output irrespective of the variations in load and input voltage. The dual-loop control strategy is more efficient than other techniques in achieving a high performance for the PWM boost converter. Fig. 6 shows the schematic diagram of the dual-loop control structure in the s-domain.

In general, there are two basic approaches to designing the digital controller for dc/dc PWM converters. The first approach is to design the controller in the s-domain using conventional methods and the resulting controller is transformed into the z-domain using appropriate z-transformations. This method is called the digital redesign approach (RDA). The RDA has some drawbacks such as sampling and quantization errors, computational time delay, and discretization effects. The second approach, called direct digital control (DDC), is to directly design the controller in the z-domain itself and thus there is no need for transformation from s- to z-domains. Since the DDC starts with the system discrete transfer functions, it is possible to include the effect of sampling, zero-order-hold (ZOH), and computational time delay effects in order to guarantee the stability of the design [25]–[29]. As a result, the final digital control is more realistic and meets the design specifications without any tuning. In this paper, a dual-loop control strategy is designed using DDC based on TMS320F2808 DSP, as will be explained in the following section.

A. Design of the Digital Controller

In the dual-loop control structure, the outer loop is the voltage loop, which generates the current reference for the inner current loop. The inner current loop can suffice the faster transient response of the dc/dc converter's requirement. This controller requires the sampling of two variables, namely output voltage V_o and inductor current I_L, which are obtained from conventional Hall effect transducers. A limiter on the inductor current reference is crucial in this controller. This is because during large signal transient like startup period, there is a big difference between the voltage reference and the dc output voltage. As a result, the output of the voltage compensator could give a command to the current loop higher than the maximum allowable inductor current, resulting in inductor saturation and damage to the device.

To design the proper dual-loop controller for a dc/dc PWM converter, the continuous-time transfer functions ($G_{\rm vd}(s)$ and $G_{\rm id}(s)$) of the boost converter are first discretized using one of the discretization methods, such as zero-order-hold (ZOH), matched pole-zero, backward difference, and bilinear transformation methods. The appropriate transformation method to be utilized here is the ZOH method. Once the discrete transfer functions of the system are available, the digital controller (*H(z)*) is directly designed in the z-domain using methods similar to the continuous-time frequency response methods. Fig. 7 presents the entire dual-loop system containing the voltage loop controller (*Hv*(*z*)), the current loop controller (*Hi*(*z*)), the ZOH and computational delay e^{-sTd}, and the control to output transfer functions ($G_{\rm vd}(s)$ and $G_{\rm id}(s)$) of the converter. The discrete-time transfer functions ($G_{\rm vd}(z)$ and $G_{\rm id}(z)$) of the converter that include the ZOH and computational delay e^{-sTd} are given as follows:

$$G_{vd}(z) = \mathrm{Z}\left\{\frac{1-e^{-sTs}}{s}.e^{-sTd}.G_{\rm vd}(s)\right\} \tag{14}$$

$$G_{\rm id}(z) = \mathrm{Z}\left\{\frac{1-e^{-sTs}}{s}.e^{-sTd}.G_{\rm id}(s)\right\}. \tag{15}$$

The loop gains for the inner current loop and the outer voltage loop can be expressed as follows:

$$T_i(z) = H_i(z).G_{id}(z) \tag{16}$$

$$T_v(z) = \frac{H_v(z).H_i(z).G_{vd}(z)}{1+T_i(z)}. \tag{17}$$

In this paper, the digital PI controllers are designed based on the required phase margin Φ_m and critical frequency ω_{cz} by using the bode diagram in the discrete-time domain; the transfer function of the digital PI controller in the z-domain is given by

$$H(z) = k_p + \frac{k_i\, T_s\, z}{z-1} \tag{18}$$

where

$$k_p = \frac{\cos\theta}{|G_p(z)|} \tag{19}$$

$$k_i = \frac{-\omega_{cz}\,\sin\theta}{|G_p(z)|} \tag{20}$$

$$\theta = 180 + \phi_m - \angle G_p(z). \tag{21}$$

Here, $G_p(z)$ is the discrete-time transfer function of the open-loop system (e.g., $G_{\rm vd}(z)$ or $G_{\rm id}$ (z)).

For example, Fig. 8 shows the bode plots for the current-loop gain and voltage-loop gain, which are designed for the MDIBC topology with converter parameters listed in Table I.

The plots demonstrate that the current-loop gain has a crossover frequency as high as 2 kHz, with a phase margin of 50.4°. To avoid the interaction between the subsystems and to accommodate the slow FC response, low control bandwidth is used for voltage loop. Outer voltage loop has a crossover frequency of 50 Hz and a phase margin of 74.6°.

TABLE I
DC/DC CONVERTER PARAMETERS

Topology	*L (μH)*	*R_L (mΩ)*	*C (μF)*	*R_C (mΩ)*	*[n m]*
*Boost Converter (**BC**)*	750	68	550	0.697	[1 1]
*Multi-Device Boost Converter (**MDBC**)*	375	34	275	1.394	[1 2]
*Interleaved Boost Converter (**IBC**)*	375	34	320	1.15	[2 1]
*Multi-Device Interleaved Boost Converter (**MDIBC**)*	187.5	17	160	2.3	[2 2]

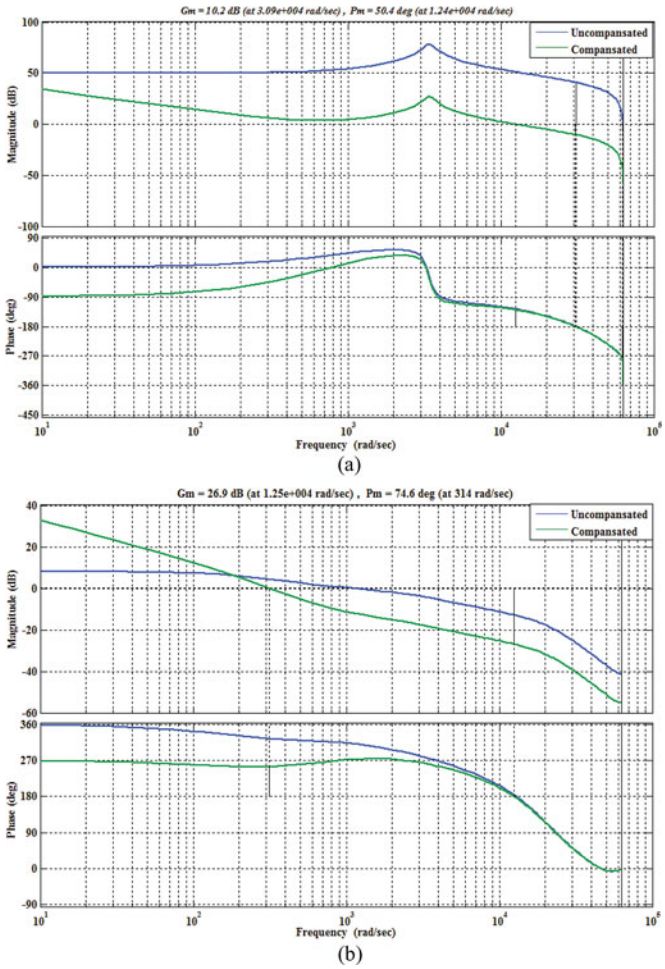

Fig. 8. Frequency response of the dual-loop control. (a) Current gain. (b) Voltage gain.

V. ANALYTICAL CALCULATION OF THE CONVERTER LOSSES

To estimate the semiconductor power losses of different circuit topologies, the switching and conduction losses are analytically calculated using the manufacturer's datasheets. Therefore, the power losses of the boost converter are calculated in order to estimate the converter efficiency. The converter efficiency can be calculated by

$$\text{Efficiency}(\eta) = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{losses}}} \tag{22}$$

$$P_{\text{losses}} = P_T + P_D + P_C. \tag{23}$$

The losses of the switch P_T are given by

$$P_T = \left[I^2_{S\text{rms}}\, r_{\text{CE}} + V_{\text{CE}}\, I_{S\text{av}} + \frac{V_o}{V_{\text{CC}}\, I_C} \left[\begin{array}{l} E_{\text{off}}\,(I_{S\text{av}} + (\Delta I/2)) \\ +E_{\text{on}}\,(I_{S\text{av}} - (\Delta I/2)) \end{array} \right] F_s \right]. \tag{24}$$

In this study, the insulated gate bipolar transistor (IGBT) represents the switch. The IGBT characteristics (e.g., r_{CE}, V_{CE}, V_{CC}, I_C, E_{off}, and E_{on}) are given in the IGBT datasheet. $I_{S\text{rms}}$, $I_{S\text{av}}$, and ΔI represent the rms current of the IGBT, the mean current of the IGBT, and the current ripple, respectively. The diode losses P_D are evaluated as follows:

$$P_D = I^2_{D\text{rms}}\, r_F + V_{F0}\, I_{D\text{av}} + \frac{V_o}{V_{\text{CC}}\, I_F} \left[E_{\text{rr}}\,(I_{D\text{av}})\right] F_s \tag{25}$$

where the diode characteristics (e.g., r_F, V_{F0}, V_{CC}, I_F, and E_{rr}) are given in the datasheet. $I_{D\text{rms}}$ and $I_{D\text{av}}$ represent the rms current and the mean current of the diode. The losses of the passive components P_C are approximately given by

$$P_C = I^2_{L\text{rms}} R_L + I^2_{C\text{rms}} R_C. \tag{26}$$

The inductor core losses are produced from the flux density ripple B_{ac}, which is proportional to the inductor current ripple ΔI. These losses are estimated based on the charts given by the manufacturer (METGLAS, Inc., CC core). Therefore, the core losses of the inductor $P_{\text{cond}-\text{ind}}$ can be estimated by [30]

$$P_{\text{core\_ind}} = W_t.\left[6.5.F^{1.51}_{\text{sw,kHz}}.B^{1.74}_{ac,T}\right] \tag{27}$$

$$B_{ac,T} = \frac{0.4\pi.N.\Delta I_L.10^{-4}}{L_{g\,,\text{cm}}} \tag{28}$$

where W_t is the weight of the core (kg), N is the number of turns per coil, ΔI_L is the current ripple, and L_g is the length of the air-gab (cm). The output power is calculated as follows:

$$P_{\text{out}} = V_o\, I_{O\text{av}} \tag{29}$$

where $I_{O\text{av}}$ is the average output current.

VI. SIMULATION RESULTS

In this section, the PWM dc/dc converter topologies are designed and realized by using MATLAB/Simulink in order to validate the performance of the proposed converter. These simulations are carried out on resistive load with 200 V input voltage, 400 V output voltage, and 20 kHz switching frequency F_s. A dual-loop control strategy is applied to achieve the closed-loop control for the dc/dc converters. The comparative study between the BC, MDBC, two-phase IBC, and the proposed converter (MDIBC) is performed under the following converter parameters as mentioned in Table I. Figs. 9 and 10 illustrate the performance of the BC and MDBC, respectively, during load change. Figs. 11 and 12, respectively, show the response of the IBC and the MDIBC during load step. In addition, Figs. 13

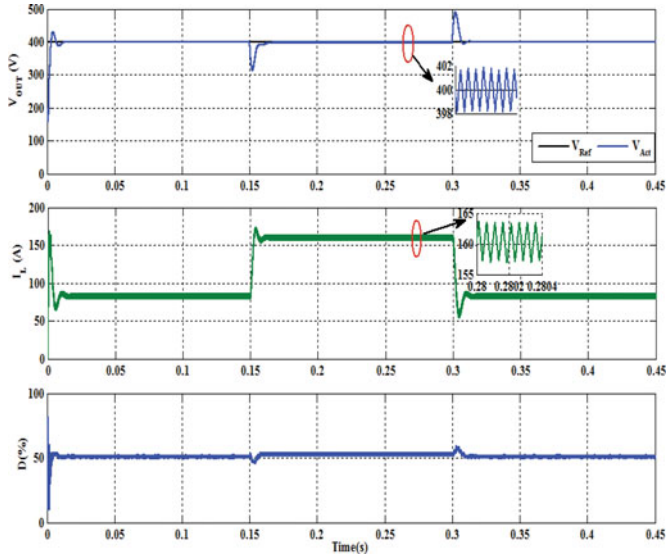

Fig. 9. Dynamic response of the BC during load change.

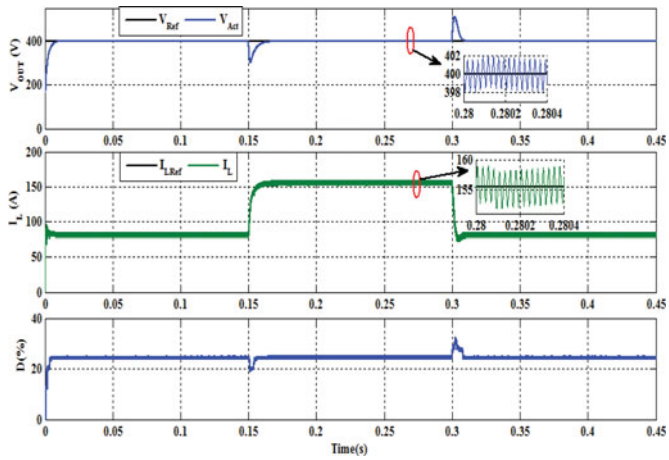

Fig. 10. Dynamic response of the MDBC during load change.

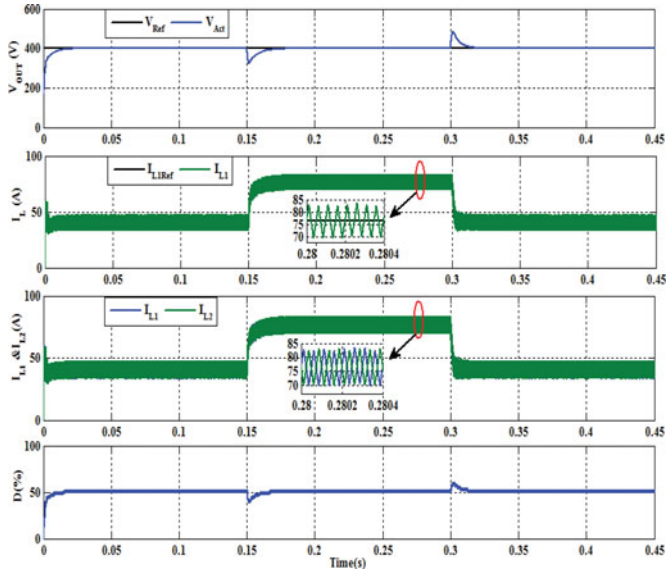

Fig. 11. Dynamic response of the IBC during load change.

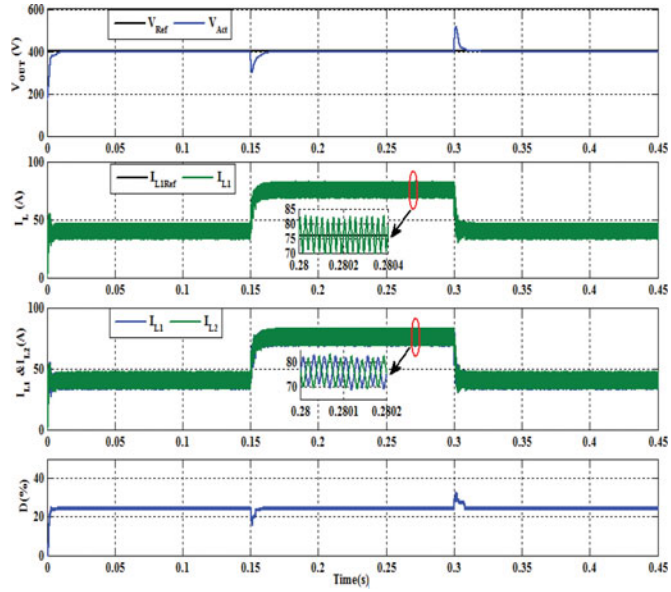

Fig. 12. Dynamic response of the MDIBC during load change.

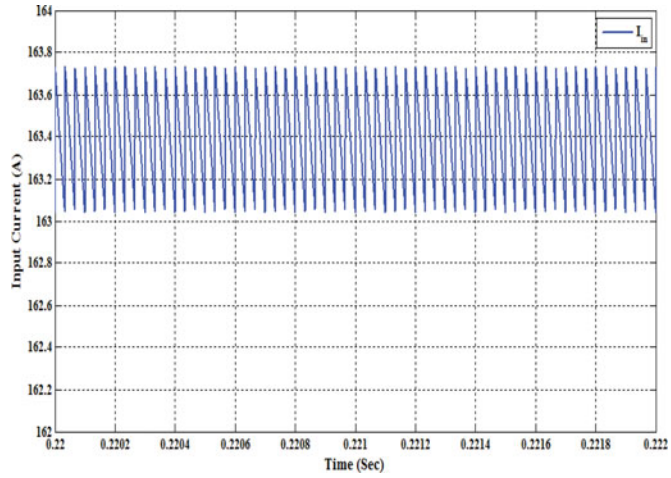

Fig. 13. Input current ripple of the IBC.

and 14 demonstrate the input current ripple of the IBC and the MDIBC, respectively.

Moreover, the comparative efficiency between dc/dc converter topologies during load change and input voltage change is shown in Figs. 15 and 16, respectively. To evaluate the distributed losses of the dc/dc converter, Fig. 17 presents the distributed power losses of the IBC and the proposed converter (MDIBC). As demonstrated in Fig. 17, the proposed converter has the ability to reduce the total losses and especially the conduction losses and core losses.

On the other hand, to verify a more realistic load current profile, a standard driving cycle, NEDC, is used in small scale, especially the last part. In our previous studies [31], [32], we analyzed different driving cycles (such as NEDC and FTP75) and different control strategies that can be used for FC/supercapacitor HEVs. In these studies, the load power profile is calculated based on the dynamic model of the vehicle and

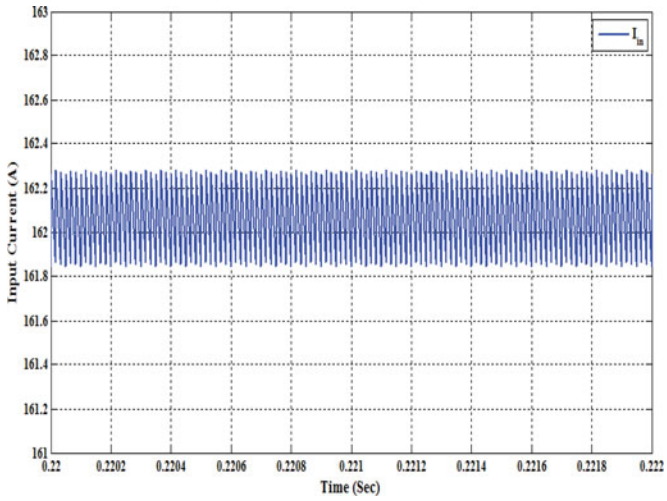

Fig. 14. Input current ripple of the MDIBC.

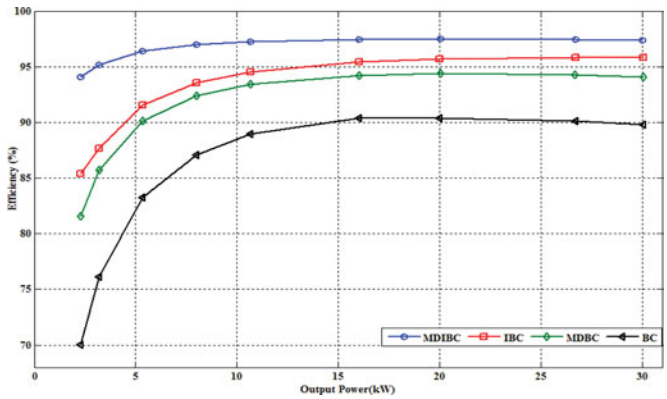

Fig. 15. Comparative efficiency between dc/dc converters at load change based on the loss model (at $V_{\rm in} = 200$ V, $V_{\rm out} = 400$ V, and $F_s = 20$ kHz).

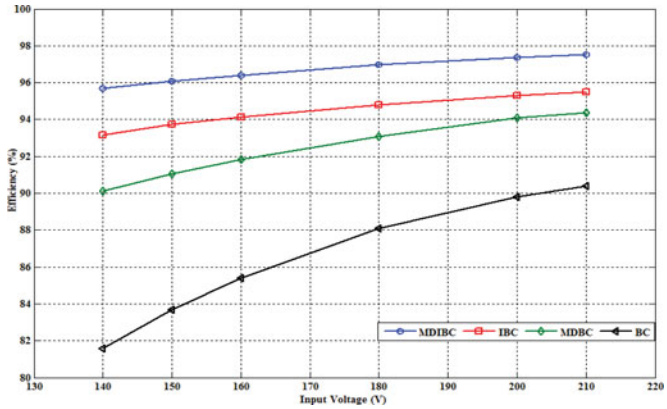

Fig. 16. Comparative efficiency between dc/dc converters at input voltage change based on the loss model (at $V_{\rm out} = 400$ V and $F_s = 20$ kHz).

the driving cycle. Therefore, in this research, the load current profile calculated based on the NEDC driving cycle is studied to verify the feasibility of the proposed converter topology (MDIBC) and its characteristic performance over transient load. The MDIBC and the load current profile are simulated by using MATLAB/Simulink as shown in Figs. 18 and 19, respectively.

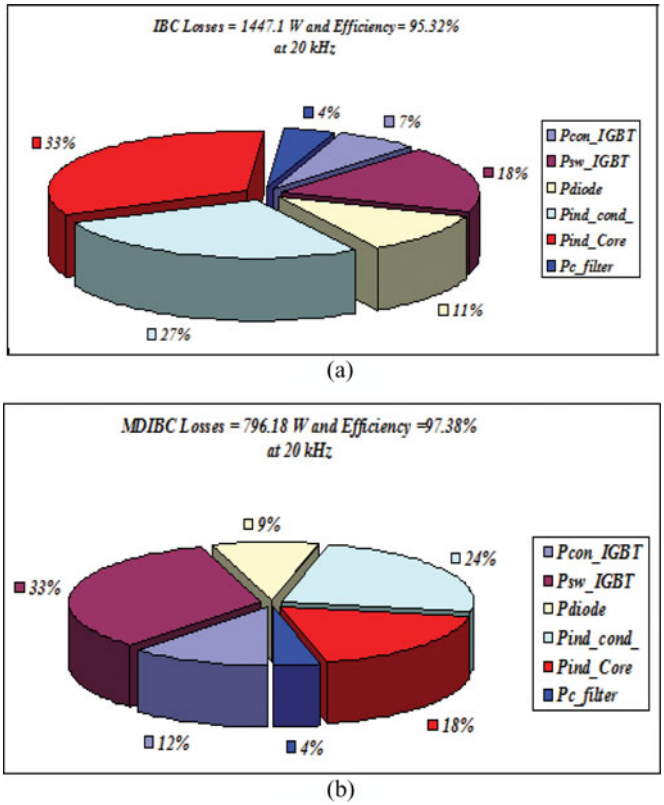

Fig. 17. Distributed power losses (at $V_{\rm in} = 200$ V, $V_{\rm out} = 400$ V, and $F_s = 20$ kHz). (a) IBC. (b) Proposed converter (MDIBC).

In this model, the load current profile is represented by a current source, while the input voltage $V_{\rm in}$ of an FC is represented by a voltage source with internal resistance as illustrated in Fig. 18. Fig. 20 shows the dynamic response of the proposed converter over the load current profile.

As shown in Figs. 13 and 14, the ripple frequency of the input current in MDIBC is doubled when using the proposed interleaved technique with multidevice. As a result, the inductor size and capacitor size are reduced by 50% compared with the conventional IBC topology. Furthermore, when comparing the proposed converter with other topologies, it is noticed that the proposed topology, MDIBC, can improve the efficiency (see Figs. 15 and 16), can reduce the passive component size (see Table II), and can improve the transient response (see Fig. 20).

VII. Experimental Results

To verify the obtained simulation results, an experimental setup of a 30-kW MDBIC has been designed and implemented in our laboratory. The eZdsp F2808 DSP is used for control strategy implementation and LEM current and voltage sensors are used for measuring feedback signals. The required measuring and interface circuits have been designed and built. The digital signal processors (DSPs) are finding wide application in many engineering fields especially in the field of power electronics and these are suitable in almost all high-frequency power conversion applications. This is because of their ability to perform complex mathematical computations within a minimum amount

TABLE II
PARAMETERS OF THE DC/DC CONVERTERS

Items	*DC/DC Converter Topologies*		
	IBC	***MDIBC***	***The Reduction***
Inductor *[L (μH)]*	375	187.5	**50 %**
Output Capacitor *[C (μF)]*	320	160	**50%**
Inductor Current Ripple per/phase	31.86 A	15.78 A	**50%**
Switching Frequency	20 kHz	20 kHz	-----
Inductor Current Ripple	20 kHz	40 kHz	-----

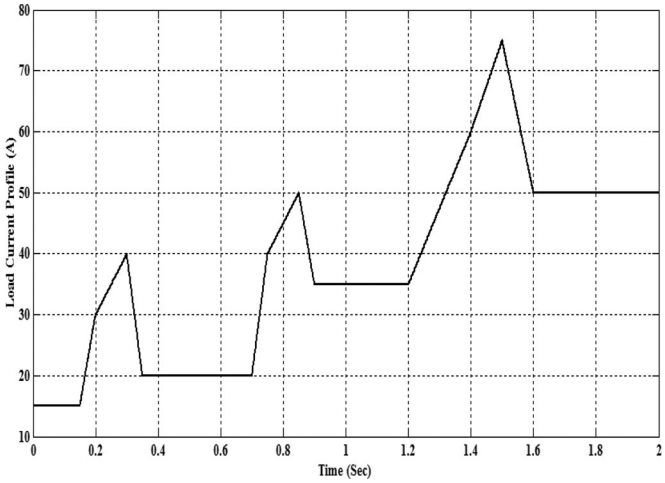

Fig. 19. Load current profile for the converter.

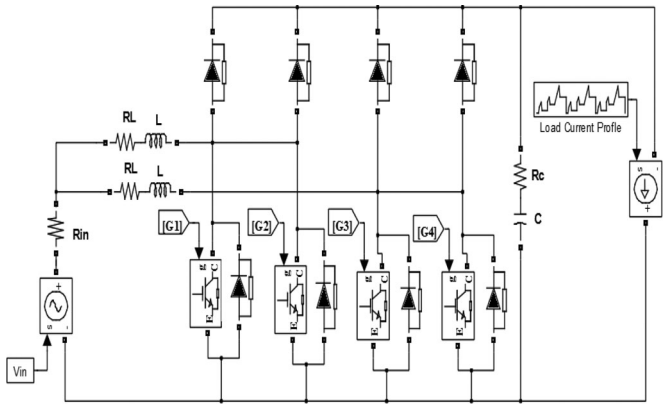

Fig. 18. Proposed converter (MDIBC) with current load profile.

of time and with less effort. Furthermore, the digital controller is flexible because the implementation involves only software instructions and is independent of the converter size. In this paper, a real-time digital control based on TMS320F2808 DSP is implemented with dual-loop current control in order to achieve a fast response during transient operation. The control strategies are implemented using the TI C2000 package in Simulink and eZdsp TMS320F2808. In this section, the DSP implementation and the experimental results of the IBC and the proposed converter (MDIBC) are provided. Fig. 21 shows the experimental setup of a 30-kW MDIBC. Fig. 22(a) illustrates the dual-loop controller implemented in a DSP for IBC. Fig. 22(b) shows the digital phase-shift scheme implemented in a DSP for ePWMs.

Fig. 23 shows the dynamic response of the dc/dc IBC under load step with the proposed control strategy, input voltage step, and reference voltage step. Fig. 24 illustrates the steady-state inductor currents of the IBC. To validate the proposed converter (MDIBC), Fig. 25(a) illustrates the dual-loop controller implemented in a DSP for the MDIBC. Fig. 25(b) shows the digital phase-shift scheme implemented in a DSP for ePWMs. Fig. 25(c) demonstrates the generated gate signals (ePWMs) for the MDIBC. Fig. 26 presents the dynamic response of the dc/dc MDIBC over load step with the proposed control strategy, input voltage step, and reference voltage step. Fig. 27 illustrates the steady-state inductor currents of the MDIBC. Fig. 28 shows the comparative study of the efficiency between the dc/dc converters based on laboratory measurements.

Table II demonstrates the comparative study between the dc/dc converters (IBC and MDIBC) based on the experimental results.

As shown in Fig. 23(a), the dynamic response of the two-phase IBC has high voltage ringing at load step, and this topology is sensitive to the duty cycle at load change. On the other hand, the dynamic response of the MDIBC is faster than the IBC and it has very small voltage ringing at load step [as illustrated in Fig. 26(a)], because the interleaved control between the power switches provides a higher system bandwidth. In addition, the proposed digital controller based on a DSP provides a good solution for the synchronization problem between phases. As a result, the size of the passive components (inductor, output capacitor, and EMI filter) is reduced by 50% compared with the multichannel interleaved converter at the same switching frequency. In addition, the proposed converter (MDIBC) and its digital control reduce the input current/the output voltage ripples and the inductor current ripple in each channel by 50% compared with a multichannel interleaved converter. It should be pointed out that the proposed converter could provide a significant contribution to the field of FCHEVs, particularly in FC high-power applications. The advantages of the proposed converter can be summarized as follows:

1) size and weight of passive components (inductor and capacitor) are reduced;
2) ripples of the input current and output voltage waveforms are reduced;
3) ripple frequencies of the input and output waveforms are increased;
4) reliability and efficiency of the system are improved;

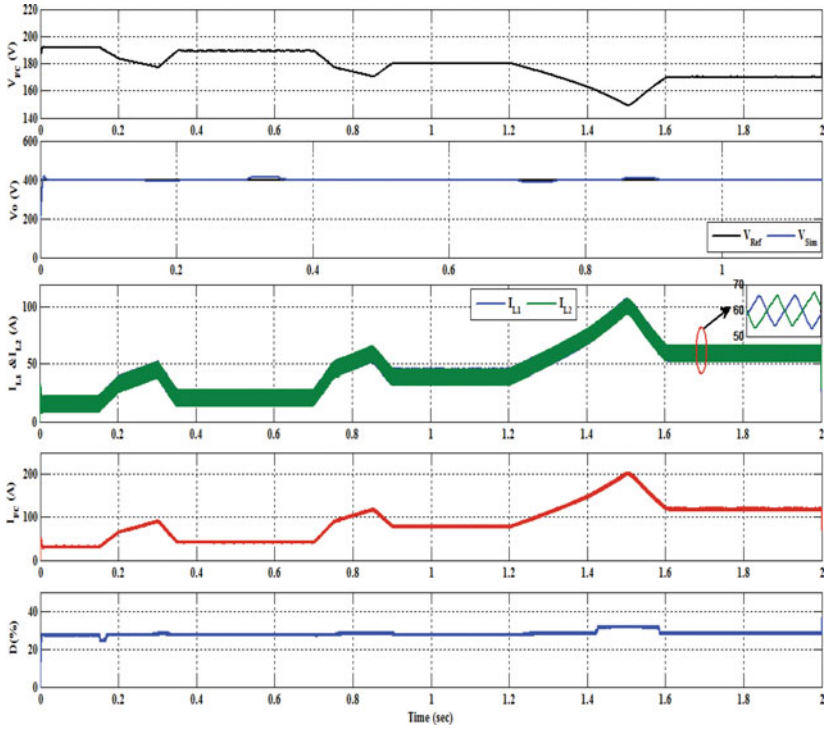

Fig. 20. Dynamic response of the MDIBC under load current profile.

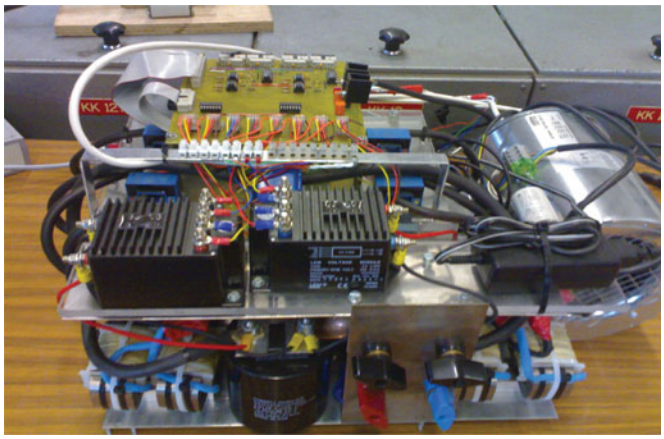

Fig. 21. Prototype of a 30-kW MDIBC.

5) current ratings of power electronic devices are reduced, because the current ratings are proportional to the continuous power rating of the circuit.

Moreover, in this paper, the concept of the multidevice interleaved dc/dc converter (MDIBC) has been proposed to interface the FC with the powertrain of the HEVs or to the distributed generation system in high power level. In addition, the proposed converter can be modified to achieve bidirectional operating modes (boost/buck modes) for ESS, such as batteries and supercapacitors in high-power vehicle applications. Therefore, in bidirectional operation, the proposed converter comprises two inductors, four switches (IGBTs), and four antiparallel diodes for boost mode as well as buck mode. As a result, the proposed converter not only reduces the cost and im-

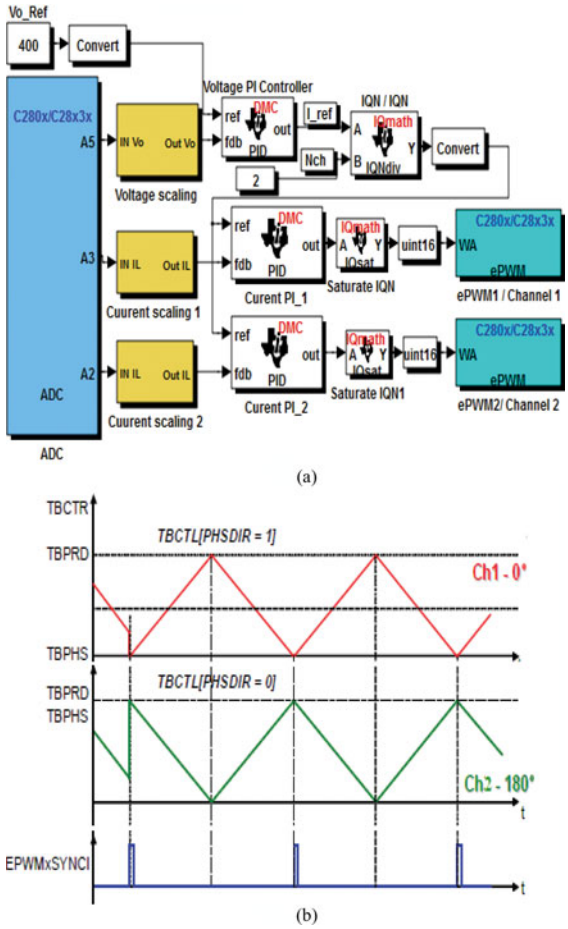

Fig. 22. DSP implementation for IBC. (a) Digital dual-loop control. (b) Phase-shift scheme with synchronization with ePWM1.

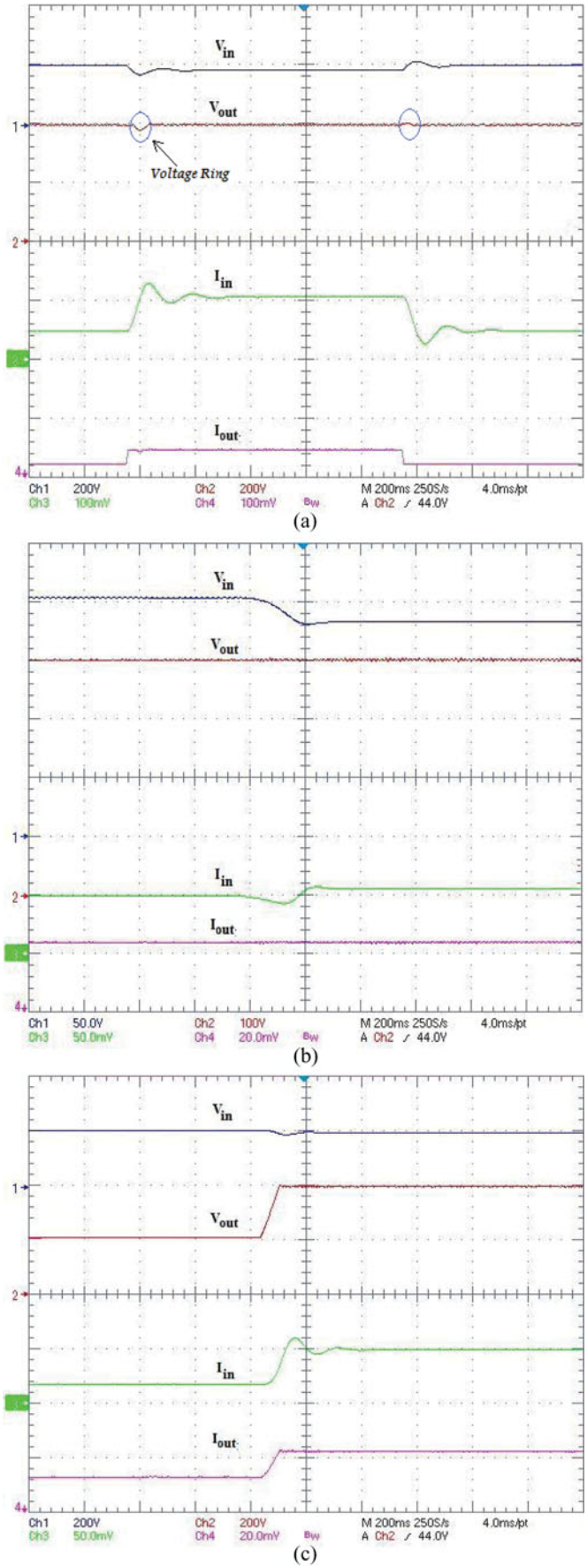

Fig. 23. Dynamic response of the IBC (1 mV/A). (a) Over load step. (b) Over input voltage step. (c) Over reference voltage step.

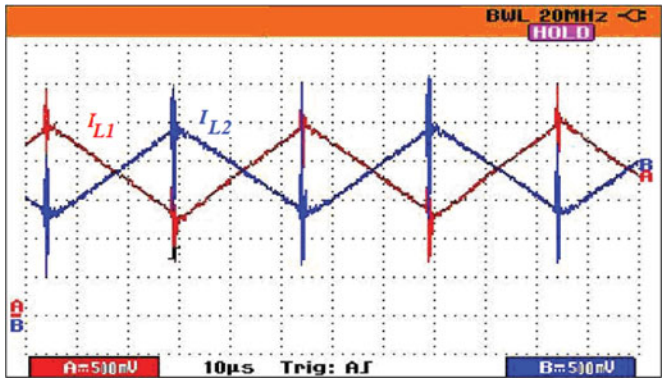

Fig. 24. Steady-state inductor currents of the IBC (40 mV/A).

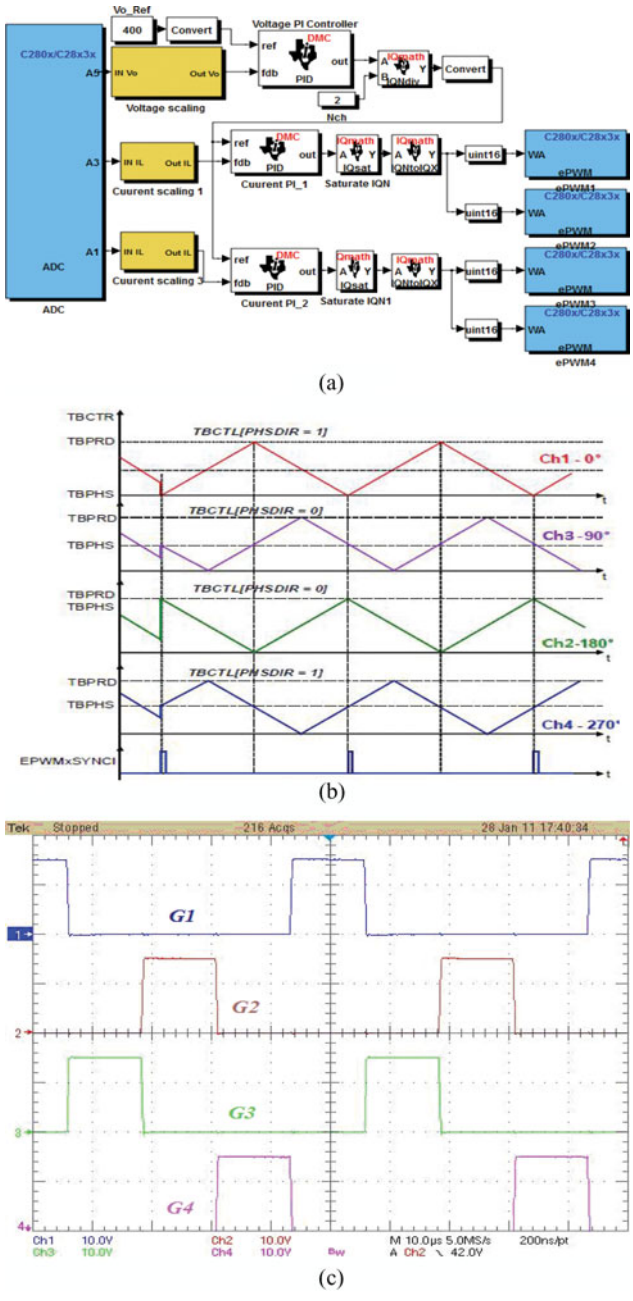

Fig. 25. DSP implementation for the MDIBC. (a) Digital dual-loop control. (b) Phase-shift scheme with synchronization with ePWM1. (c) Generated gate signals (ePWMs).

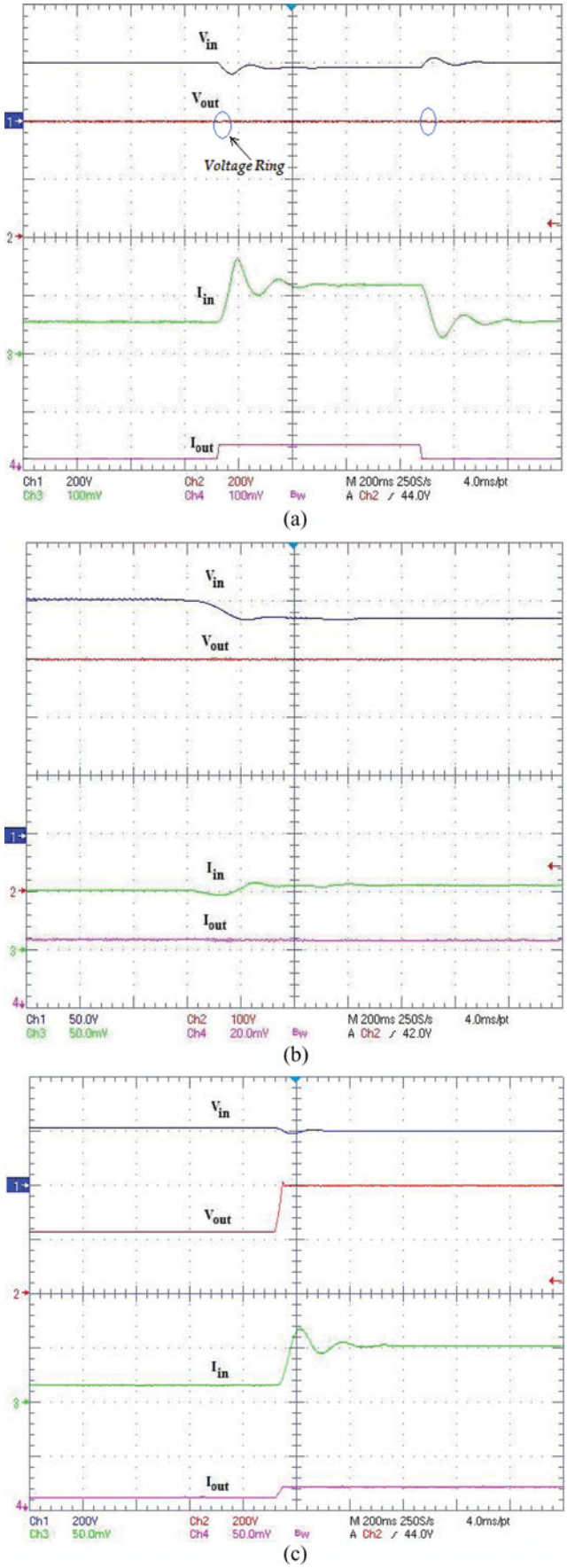

Fig. 26. Dynamic response of the MDIBC (1 mV/A). (a) Load step. (b) Input voltage step. (c) Reference voltage step.

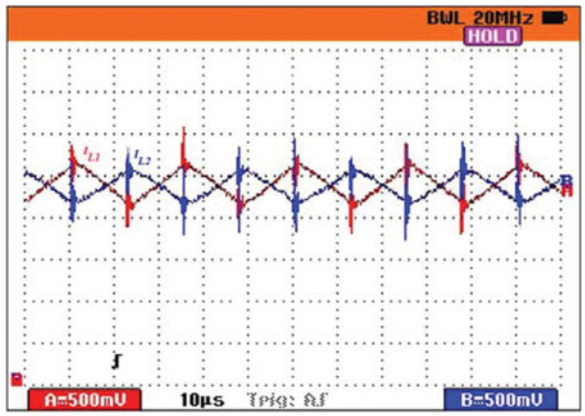

Fig. 27. Steady-state inductor currents of the MDIBC (40 mV/A).

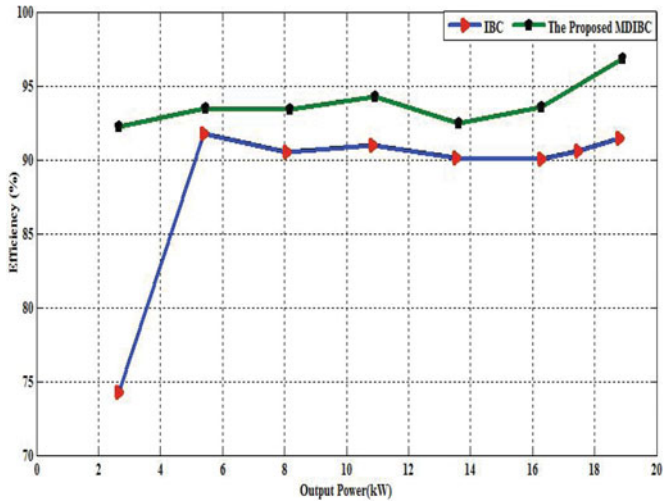

Fig. 28. Efficiency of the proposed MDIBC and the two-channel IBC (at $V_{\rm in} = 200$ V, $V_{\rm out} = 400$ V, and $F_s = 20$ kHz).

proves efficiency, but also improves the performance of the dc system.

VIII. Conclusion

In this research, a novel MDIBC has been proposed for FCHEVs in order to optimize the drive system. The generalized SSM and the loss model have been derived for the PWM dc/dc converters operating in CCM. This paper presents a DDC for designing the dual-loop control strategy to control the dc/dc converters. The digital PI compensators are used and designed using a bode diagram to achieve the required phase margin and critical frequency. Furthermore, a DSP-based digital control for a 30-kW MDIBC and IBC is presented in this paper. The real-

time code for the complete scheme is automatically generated using embedded target and real-time workshop (RTW). The simulation and experimental results have demonstrated that the inductor size and the capacitor size of the MDIBC are reduced by two times compared to the IBC. Moreover, the current and voltage ripples are reduced by two times compared with the IBC topology. Therefore, the proposed converter seems to be very promising in high-power FC systems to extend their lifespan as well as battery systems. It is important to point out that the proposed converter can improve efficiency and reduce the size of the passive components, leading to high reliability compared with other dc/dc converter topologies.

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