Letters

Analysis on Center-Tap Rectifier Voltage Oscillation of *LLC* Resonant Converter

Ki-Bum Park, Byoung-Hee Lee, Gun-Woo Moon, and Myung-Joong Youn

***Abstract*—The *LLC* resonant converter employing a center-tap rectifier can suffer from a high voltage oscillation across rectifier diodes owing to a leakage inductance of a transformer secondary. The amplitude of this voltage oscillation is varied according to design parameters, parasitic components, and operation regions, i.e., below-resonant region and above-resonant region. To reduce the diode voltage stress, this paper analyzes the voltage oscillation mechanism and presents the design consideration.**

***Index Terms*—*LLC* resonant converter and rectifier voltage oscillation.**

I. Introduction

THE *LLC* resonant converter shown in Fig. 1 is one of the most popular topologies for its simple structure, zero-voltage switching (ZVS) of primary switches, zero-current switching (ZCS) of secondary rectifier diodes. A large number of literature deal with a design guideline considering magnetic components, switching frequency F_S variation range, efficiency, and size [1]–[4]. However, till now, the rectifier voltage oscillation problem across center-tap rectifier has rarely been discussed [5], [6].

In general, isolated-type converters employing an inductive output filter suffer from a voltage ringing across a rectifier stage since a leakage inductance of a transformer and a junction capacitance of rectifier diodes are interacted after a current commutation of a rectifier [7], [8]. This voltage oscillation increases a voltage stress on the secondary diodes. A snubber is generally required to suppress this additional voltage stress, however, it could degrade the efficiency.

In the *LLC* resonant converter, three types of output stages are commonly adopted in the secondary side according to applications, i.e., voltage-doubler rectifier, full-bridge rectifier, and center-tap rectifier, as shown in Fig. 2. In case of the full-bridge rectifier and the voltage-doubler rectifier, the diode voltage stress is clamped to the output voltage V_O, which makes them suitable for high output voltage applications. On the other hand, in case of the center-tap rectifier, which is normally adopted for low output voltage applications, the diode voltage stress in steady state is approximately twice the output voltage, $2V_O$. However, since there is no clamping path for the voltage stress on the diodes, a rather high voltage oscillation could be occurred at switching transitions, as shown in the simulation waveforms in Fig. 3 and the experimental waveforms in Fig. 4, owing to a leakage inductance of the transformer secondary L_{Ks}. Moreover, at times, an imbalance of resonant currents caused by a little discrepancy between L_{Ks1} and L_{Ks2} could make the voltage oscillation more severe in one diode. By simply adopting snubbers, the diode voltage stress can be suppressed, but a loss

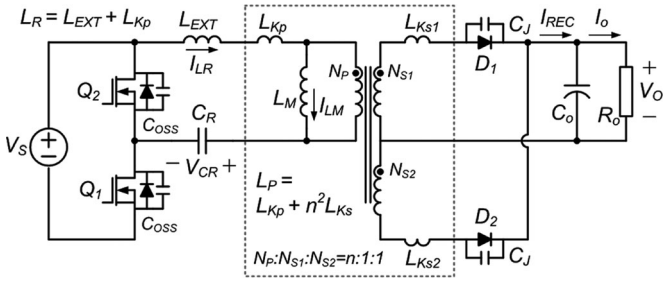

Fig. 1. Circuit diagram of *LLC* resonant converter with center-tap rectifier including parasitic components.

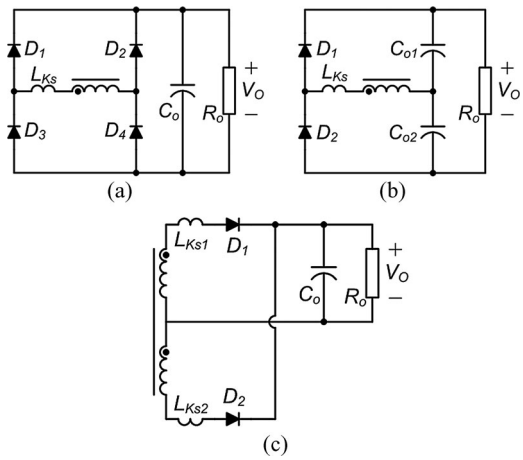

Fig. 2. Rectifiers for *LLC* resonant converter. (a) Full-bridge rectifier. (b) Voltage-doubler rectifier. (c) Center-tap rectifier.

Manuscript received April 3, 2011; revised October 27, 2011; accepted December 31, 2011. Date of current version March 16, 2012. This paper was presented in the IEEE Energy Conversion Congress and Exposition, September 2009, San Jose, CA, entitled Analysis and Design of LLC Resonant Converter Considering Rectifier Voltage Oscillation. Recommended for publication by Associate Editor R. Zane.

K.-B. Park is with the Power Electronic Systems Group, ABB Corporate Research, CH-5405 Baden Dättwil, Switzerland (e-mail: ki-bum.park@ch.abb.com).

B.-H. Lee, G.-W. Moon, and M.-J. Youn are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Yuseong-Gu, Daejeon 305-701, Korea (e-mail: bhlee@angel.kaist.ac.kr; gwmoon@ee.kaist.ac.kr; mmyoun@ee.kaist.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2012.2186614

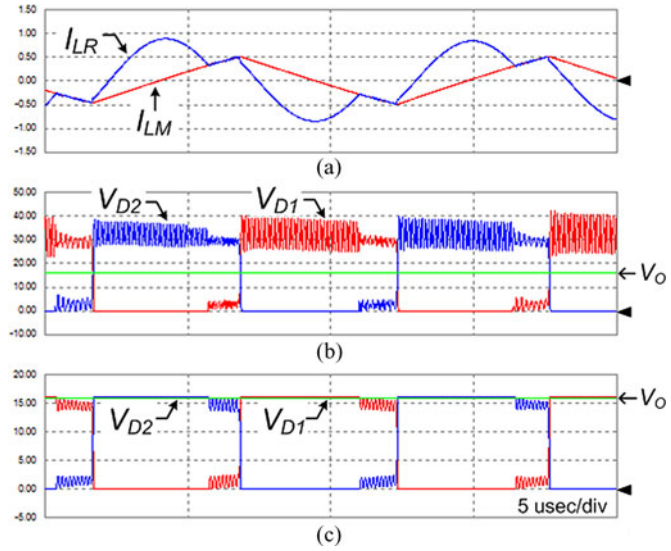

Fig. 3. PSIM simulation waveform of *LLC* resonant converter. (a) Primary current. (b) Rectifier diode voltages with center-tap rectifier; the voltage stress is more than twice V_O. (c) Rectifier diode voltages with full-bridge rectifier; the voltage stress is clamped to V_O.

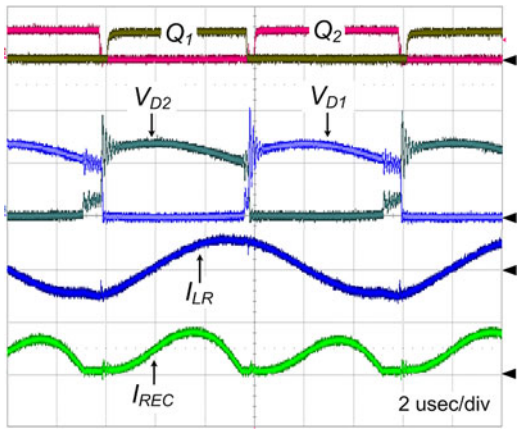

Fig. 4. Experimental waveform of *LLC* resonant converter with center-tap rectifier.

occurs. To reduce the voltage stress on the center-tap rectifier without snubbers, this Letter deals with a rectifier voltage oscillation of the *LLC* resonant converter and provides a design consideration for a small voltage oscillation.

II. Analysis of Rectifier Voltage Oscillation

Generally, the voltage oscillation across rectifier diode is caused by an interaction between a transformer leakage inductance and parasitic capacitances at switching transitions [7], [8]. This oscillation is ignited by the energy stored in the leakage inductance and other sources. To analyze the rectifier voltage oscillation in the *LLC* resonant converter, therefore, it is necessary to find out the initial currents of leakage inductors and other sources that can affect the oscillation when the rectifier diode is turned OFF at the switching transitions.

Fig. 1 shows the *LLC* resonant converter including parasitic components, i.e., the switch output capacitance: $C_{\rm OSS}$; the transformer primary leakage inductance: L_{Kp}; the secondary leakage inductance: L_{Ks1} and L_{Ks2}; and the diode junction capacitance: C_J. For the sake of the voltage oscillation analysis in the secondary side, the equivalent circuit reflected to the secondary side is used, as shown in Fig. 5, where $V_{Ss} = V_S/n$, $V_{CRs} = V_{CR}/n$, $C_{\rm OSSs} = n^2 C_{\rm OSS}$, $L_{Ms} = L_M/n^2$, $L_{Rs} = L_R/n^2$, $C_{Rs} = n^2 C_R$, and $I_{LMs} = nI_{LM}$. Since V_O can be considered as a voltage source during switching transitions, each side of the center-tap rectifier can be separated with its own V_O and repositioned.

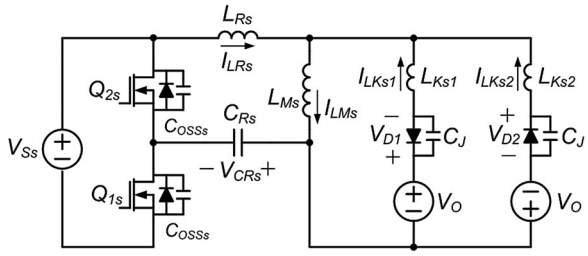

Fig. 5. Equivalent circuit of Fig. 1 during switching transition, which is reflected to secondary.

Normally, the operation can be divided into two regions according to a ratio of the resonant frequency F_R to F_S, i.e., the below-resonant (BR) region [$F_R > F_S$] and the above-resonant (AR) region [$F_R < F_S$]. With regard to the secondary side, the major difference between two regions is that the rectifier current is discontinuous in the BR region and critically continuous in the AR region. Therefore, the current commutation mechanism of the rectifier between two regions is different and the rectifier voltage oscillation mechanisms would also be different. The detailed operation focused on the diode voltage oscillation is described as follows. For the sake of analysis, it is assumed that the converter is operated around F_R and thereby an average of V_{CRs} is about V_O.

A. BR Region [$F_R > F_S$]

The key waveforms and equivalent circuits for the BR region are presented in Figs. 6 and 7, respectively. During t_1–t_2, the resonant operation transfers the power to the output through the rectifier diode D_1. At t_2, I_{D1} reaches zero and some voltage oscillation is occurred across D_1 and is expressed as in (1). This oscillation is proportional to $V_{CRs}(t_2)$, i.e., the ripple of V_{CR}, and is small enough not to affect the peak voltage stress of the diode. Although the ripple of V_{CR} could be increased as Q ($= \sqrt{L_R/C_R}/R_O$) is increased, the upcoming oscillation is more dominant with respect to the voltage stress on rectifier diodes.

$$V_{D_1}(t) \approx V_{CRs}(t_2)\{1 - \cos(\omega_1(t - t_4))\}$$
$$\omega_1 = \frac{1}{\sqrt{C_J(2L_{Rs} + L_{Ks})}}. \quad (1)$$

During t_2–t_3, only I_{LM} flows in the primary and both D_1 and D_2 are OFF-state. At t_3, Q_1 is turned OFF and the equivalent circuit shown in Fig. 7(a) is constructed. During this switching transition, all the parasitic capacitances, i.e., $C_{\rm OSS}$ and C_J, take part in the operation. V_{CRs} can be considered as a constant

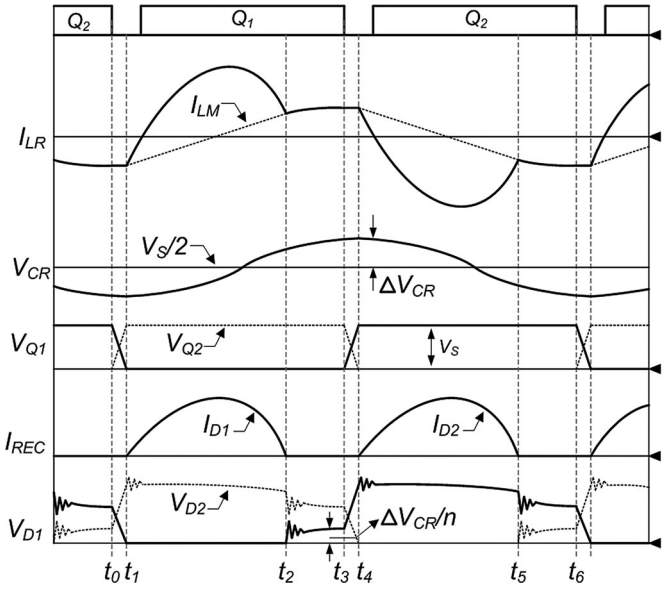

Fig. 6. Key waveform in BR region.

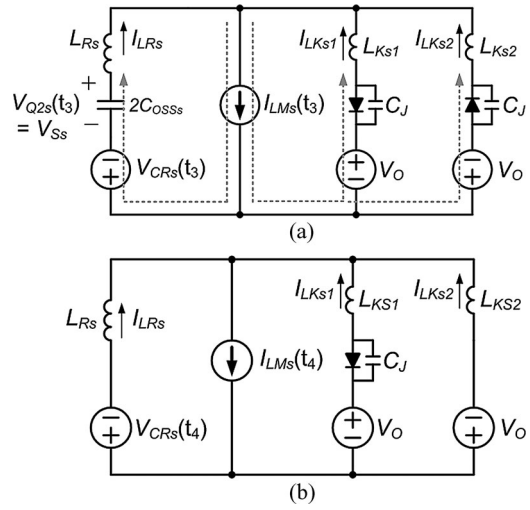

Fig. 7. Equivalent circuit for BR region. (a) t_3–t_4. (b) $t_4 \sim$.

voltage source since C_{Rs} has a sufficiently large capacitance compared to C_{OSSs} or C_J. Similarly, I_{LM} can be considered as a constant current source. In this mode, I_{LMs} flows through C_{OSSs} and C_J, as presented by the dotted line, i.e., both C_{OSSs} and C_J are charged simultaneously. Therefore, V_{Q1} and V_{D1} are increased linearly by the current source. $I_{LKs1}(t_4)$ and $I_{LKs2}(t_4)$ can be determined by the capacitance ratio of C_{OSSs} to C_J, which is expressed as in (2). For the sake of analysis, messy minor oscillation terms are ignored and only the most essential factors are considered

$$I_{LKs1}(t_4) = I_{LKs2}(t_4) \approx I_{LMs}(t_3)\frac{C_J}{2C_{\mathrm{OSSs}} + 2C_J}. \quad (2)$$

At t_4, both the antiparallel diode of Q_2 and D_2 conduct, and the equivalent circuit is changed, as shown in Fig. 7(b). The voltage oscillation is excited by the initial currents of leakage inductors presented in (2) and by the ripple of V_{CRs}, ΔV_{CRs}, as well. The

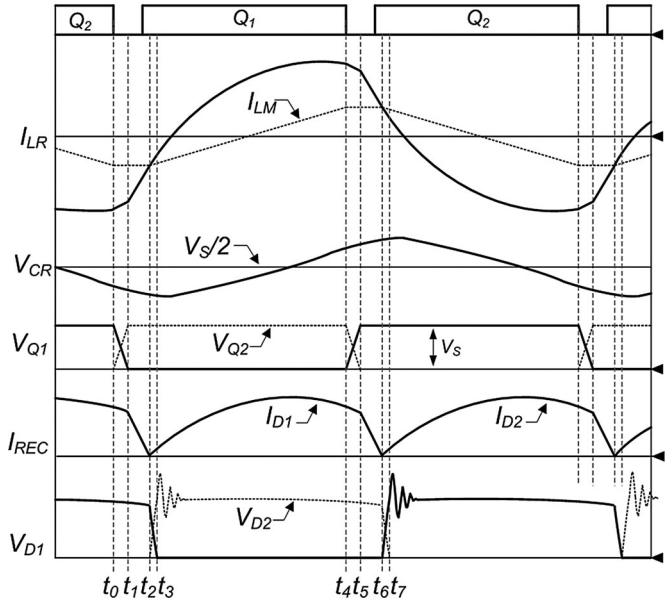

Fig. 8. Key waveform in AR region.

voltage oscillation across D_1 can be approximately expressed as in (3). It is noted that various design parameters and parasitic components affect the voltage oscillation

$$\begin{aligned} V_{D1}(t) \approx{}& V_{D1}(t_4) + I_{LMs}(t_3)\frac{\sqrt{C_J}}{2\left(C_{\mathrm{OSSs}} + C_J\right)} \\ &\times \sqrt{L_{Ks}\left(1 + \frac{L_{Rs}}{L_{Rs} + L_{Ks}}\right)}\sin\left(\omega_2(t - t_4)\right) \\ &+ \Delta V_{CRs}(t_4)\frac{L_{Ks}}{L_{Rs} + L_{Ks}}\left\{1 - \cos\left(\omega_2(t - t_4)\right)\right\} \\ \omega_2 ={}& \sqrt{\frac{L_{Rs} + L_{Ks}}{C_J L_{Ks}\left(2L_{Rs} + L_{Ks}\right)}}. \end{aligned} \quad (3)$$

B. AR Region [$F_R < F_S$]

The key waveforms and equivalent circuits for the AR region are presented in Fig. 8 and 9, respectively. The most noticeable operation of switching transition in the AR region compared to the BR region is that Q_1 is turned OFF while D_1 is still conducting, which lead to different oscillation factors.

After Q_1 is turned OFF at t_4, I_{LR} discharges C_{OSS} and V_{Q2} is decreased to zero. Then, I_{LR} and I_{D1} are decreased. When I_{D1} reach zero at t_6, the equivalent circuit shown in Fig. 9(a) is constructed, where $I_{LMs}(t_6)$ can cancel out the initial value of I_{LRs}. Unlike the BR region, C_{OSS} does not take part in the oscillation. $V_{D1}(t)$ and $V_{D2}(t)$ can be expressed as in (4) and (5), respectively. At t_7, $V_{D2}(t)$ reaches zero and the equivalent circuit is changed, as shown in Fig. 9(b). The voltage oscillation is excited by $I_{LKs1}(t_7)$ and $I_{LKs2}(t_7)$ presented in (6) and by ΔV_{CRs} as well. If the reverse-recovery current of the diode I_{RR} is considered, it would cause an additional oscillation term. Consequently, $V_{D1}(t)$ containing all these voltage oscillation

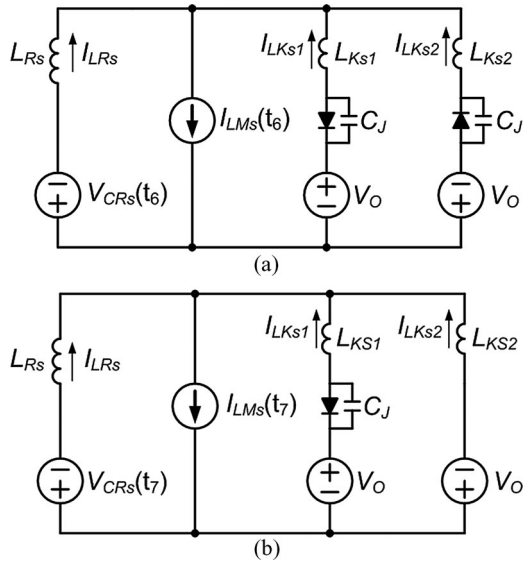

Fig. 9. Equivalent circuit for AR region. (a) t_6–t_7. (b) $t_7 \sim$; the same equivalent circuit with Fig. 7(b) except for different initial values .

factors can be approximately obtained as in (7)

$$V_{D1}(t) \approx (2V_O + \Delta V_{CRs}(t_6))\{1 - \cos(\omega_1(t - t_6))\} \quad (4)$$

$$V_{D2}(t) \approx 2V_O - V_{D1}(t) \quad (5)$$

$$I_{LKs1}(t_7) = I_{LKs2}(t_7) \approx (2V_O + \Delta V_{CRs}(t_6)) \times \sqrt{\frac{C_J}{2L_{Rs} + L_{Ks}}} \quad (6)$$

$$V_{D1}(t) \approx 2V_O + (2V_O + \Delta V_{CRs}(t_6)) \times \sqrt{\frac{L_{Ks}}{L_{Rs} + L_{Ks}}} \sin(\omega_2(t - t_7)) + \Delta V_{CRs}(t_7) \times \frac{L_{Ks}}{L_{Rs} + L_{Ks}} \{1 - \cos(\omega_2(t - t_7))\} + I_{RR}\sqrt{\frac{L_{Ks}}{C_J}\left(1 + \frac{L_{Rs}}{L_{Rs} + L_{Ks}}\right)} \sin(\omega_2(t - t_7)). \quad (7)$$

III. Design Consideration

As described in the previous section, the diode voltage oscillation mechanisms between two resonant regions are different and their voltage oscillation factors can be obtained as in Table I. Even though these might not be precise values since they are approximated, they can predict the tendency of the rectifier voltage oscillation. It is noted the main oscillation sources in BR region are I_{LMs} and ΔV_{CRs} at the switching transition; in the case of AR region, V_O, ΔV_{CRs} at the switching transition, and I_{RR} are the main sources. More details in terms of the design parameters and parasitic components are as follows.

A. BR Region

As for $V_{\mathrm{osc\_BR1}}$, since the first term $I_{LMs}(t_3)$, which is mainly determined by L_M, directly affects the oscillation, it should be small, i.e., L_M should be large. However, a large L_M compared with L_R would increase the inductor ratio K, i.e., L_M/L_R, which leads to an increase in a F_S variation range according to an input voltage or a load change [1]–[3]. In addition, lowering $I_{LMs}(t_3)$ gives a negative effect on ZVS, i.e., a longer dead time between switches is required to ensure ZVS. Regarding the second term, which consists of parasitic capacitances, smaller C_J is preferred to a small oscillation. However, it is determined by the diode selection. Instead, C_{OSS} can be increased by paralleling additional capacitor to the switches; however, a larger C_{OSS} gives detrimental effect on ZVS. In case of the third term, which consists of inductances, L_{Ks} should be small.

In order to reduce the diode voltage oscillation caused by $V_{\mathrm{osc\_BR2}}$, ΔV_{CRs} or the secondary leakage inductance ratio K_L, i.e., $L_{Ks}/(L_{Rs} + L_{Ks})$, should be small. Since ΔV_{CRs} is proportional to a load condition, a larger oscillation may occur as load increases.

B. AR Region

In AR region, $V_{\mathrm{osc\_AR1}}$ and $V_{\mathrm{osc\_AR2}}$ have the same effect with $V_{\mathrm{osc\_BR2}}$ of BR region, i.e., small values for ΔV_{CRs} and K_L are desirable. As for $V_{\mathrm{osc\_BR3}}$, which is caused by the reverse-recovery phenomenon, I_{RR} itself or L_{lkg}/C_J should be small. In order to reduce I_{RR}, *di/dt* of the diode at the switching transition should be reduced. Therefore, if this term affects the voltage oscillation severely, larger L_R will be beneficial by alleviating *di/dt*.

C. Common Solution

Among the voltage oscillation factors in Table I, only L_{Ks} is the common factor. Therefore, minimizing L_{Ks} is the foremost choice to reduce the voltage oscillation across rectifier diodes over a wide operation range. In other words, the transformer should have a small leakage inductance and the required resonant inductance L_R should be adjusted by the additional L_{EXT} in the primary for a small diode voltage oscillation. Smaller ΔV_{CRs} is also beneficial over both AR and BR regions; however, it is determined primarily by the resonant tank design.

Frequently, a transformer of an *LLC* resonant converter is implemented using a separated bobbin to get a large leakage inductance for a resonant inductor without any external inductor [3]. However, in this case, L_{Ks} as well as L_{Kp} becomes large, which gives a detrimental effect on the diode voltage oscillation. Therefore, a separated bobbin is not desirable in terms of a rectifier voltage oscillation.

IV. Experimental Results

To verify the presented analysis and the design consideration, a 84 W prototype of the *LLC* resonant converter is implemented for a laptop adapter application [9]. The design parameters are presented in Table II. Here, a synchronous rectifier (SR) is

TABLE I
RECTIFIER VOLTAGE OSCILLATION FACTORS OF *LLC* RESONANT CONVERTER

BR region	AR region
$V_{osc\_BR1}: I_{LMs}(t_3)\frac{\sqrt{C_J}}{C_{OSSs}+C_J}\sqrt{L_{Ks}\left(\frac{2L_{Rs}+L_{Ks}}{L_{Rs}+L_{Ks}}\right)}$ $V_{osc\_BR2}: \Delta V_{CRs}(t_4)\frac{L_{Ks}}{L_{Rs}+L_{Ks}}$	$V_{osc\_AR1}: \left(2V_O+\Delta V_{CRs}(t_6)\right)\sqrt{\frac{L_{Ks}}{L_{Rs}+L_{Ks}}}$ $V_{osc\_AR2}: \Delta V_{CRs}(t_7)\frac{L_{Ks}}{L_{Rs}+L_{Ks}}$ $V_{osc\_AR3}: I_{RR}\sqrt{\frac{L_{Ks}}{C_J}\left(\frac{2L_{Rs}+L_{Ks}}{L_{Rs}+L_{Ks}}\right)}$

TABLE II
EXPERIMENTAL PARAMETERS

Part	Value
Input voltage V_S	350 ~ 405 V
Output voltage V_O	16.8 V
Output Power P_O	84 W (I_O = 5 A)
Resonant frequency F_R	130 kHz
Transformer turn ratio n	10.8 (N_P:N_{S1}:N_{S2} = 54:5:5)
Transformer magnetizing inductor L_M	1 mH (core : RM8)
Transformer leakage inductor L_P	$L_{Kp} + n^2L_{Ks}$ = 5 uH
External resonant inductor L_{EXT}	25 uH (MPP, outer diameter = 12.7 mm, μ_r = 60)
Resonant capacitance C_R	47 nF
Switch Q_1 and Q_2	IPD60R385 (V_{DSS} = 600 V, R_{ds} = 0.35 Ω, C_{OSS}=38pF)
Rectifier diodes D_1 and D_2 (SR)	IRF7855 (V_{DSS} = 60 V, R_{ds} = 9.4 mΩ, C_J = 440pF)
Controller	L6599
SR driver	IR1167

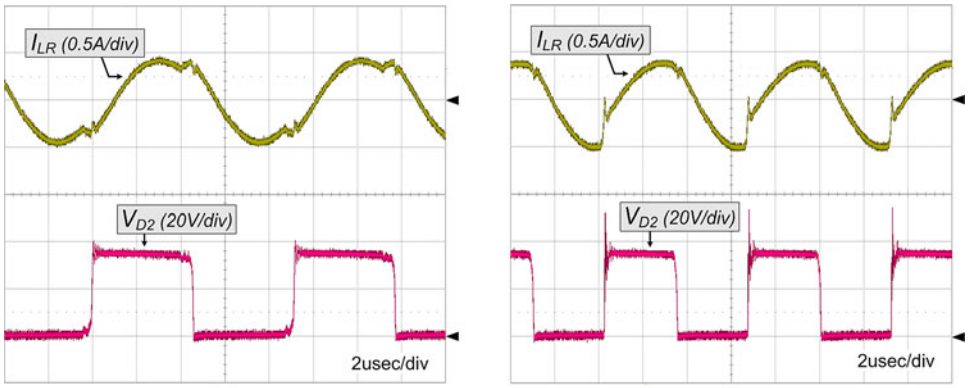

Fig. 10. Experimental results with $L_{\rm EXT} = 25\ \mu$H and $C_R = 47$ nF. (a) BR region with $V_S = 380$ V. (b) AR region with $V_S = 400$ V.

utilized to reduce the conduction loss. The resonant tank is designed with $K = 33$, $Q_{\max} = 0.08$, and $F_R = 130$ kHz.

As mentioned in the previous section, minimizing L_{Ks} is a common solution to reduce the rectifier voltage oscillation over a wide operation range. Moreover, it does not affect the resonant tank design. To minimize L_{Ks}, the transformer is implemented by an interleaved winding [10]. Then, the additional $L_{\rm EXT}$ is inserted into the primary side to adjust F_R to a designed value.

Fig. 10 shows the experimental waveforms in the BR and AR regions. With this design, although the voltage oscillation is well suppressed in the BR region, it still remains in the AR region. Normally, a synergy effect by a reverse recovery of diode makes the voltage oscillation more severe. Therefore, the voltage oscillation in the AR region, where a diode current is decreased rapidly during switching transitions tends to be higher compared with that in the BR region, where ZCS of diode is achieved, though it depends on various parameters. In this experiment, a little difference between L_{Ks1} and L_{Ks2} causes a small imbalance of I_{LR} in the AR region, which could lead to a more severe voltage oscillation in D_2.

In order to alleviate the effect of I_{RR}, which is caused by the body diode of SR, $L_{\rm EXT}$ is changed to a larger inductance, 50 μH, so that *di/dt* of the diode current can be reduced. Then, to maintain the same F_R, C_R is changed to 24 nF. With a reduced I_{RR}, the voltage oscillation in AR region is considerably suppressed while the oscillation in the BR region remains

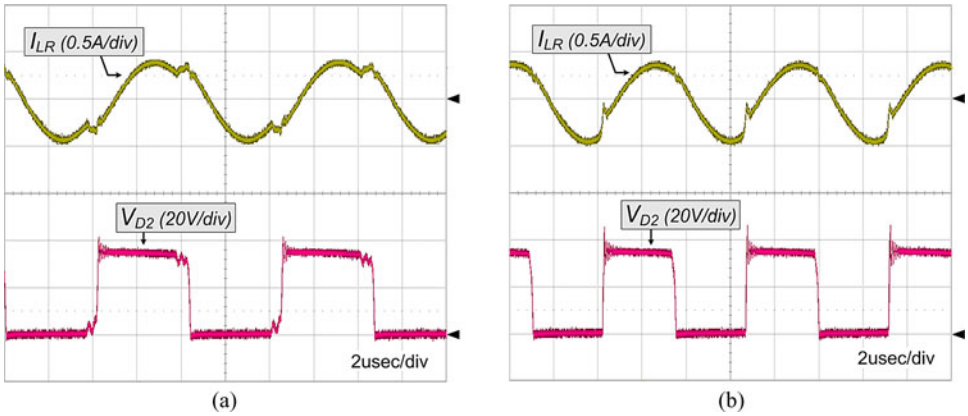

Fig. 11. Experimental results with $L_{\mathrm{EXT}} = 50\ \mu$H and $C_R = 24$ nF. (a) BR region with $V_S = 380$ V. (b) AR region with $V_S = 400$ V.

still small, as shown in Fig. 11. However, increasing L_{EXT} and reducing C_R affect the resonant tank design, i.e., it increases $Q(=\sqrt{L_R/C_R}/R_O)$ and reduces $K\ (= L_M/L_R)$. Since an increased Q could reduce a maximum voltage gain, an output voltage regulation capability should be checked out [1]–[3]. On the other hand, a reduced K decreases a F_S variation range, i.e., it is changed from 110–155 kHz to 121–154 kHz. It is noted that adjusting the voltage oscillation factors on top of minimizing L_{Ks} to reduce the voltage oscillation further sometimes requires a change of the resonant tank design.

V. Conclusion

The *LLC* resonant converter employing the center-tap rectifier can suffer from a high voltage oscillation across the secondary diodes. It is noted that the amplitude of the voltage oscillation is varied according to design parameters, parasitic components, and operation regions. Minimizing a leakage inductance of a transformer secondary would not affect the resonant tank design and could be a foremost choice for a small voltage oscillation over a wide operation range. The separated bobbin, which is widely used to obtain a large leakage inductance for a resonant inductor, is not desirable in terms of a rectifier voltage oscillation because it also increases a secondary leakage inductance. In other words, the transformer should have a small leakage inductance and the required resonant inductance should be adjusted by an additional inductor in the primary for a small diode voltage oscillation.

To further reduce the voltage oscillation in a certain operating region, i.e., BR or AR region, the corresponding voltage oscillation factors obtained in this paper should be managed to be a smaller value. It is noted that a change of the resonant tank design is often required to suppress the voltage oscillation factor, which could affect the converter performances. To accommodate a design procedure, therefore, a careful tradeoff should be made between changing the resonant tank design and just utilizing snubbers. On the other hand, the obtained voltage oscillation factors would be useful for rough prediction of a change of the voltage oscillation during a tuning process of a plant.

References

[1] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. IEEE Appl. Power Electron. Conf.*, 2002, pp. 1108–1112.

[2] L. Bing, L. Wenduo, L. Yan, F. C. Lee, and J. D. van Wyk, "Optimal design methodology for LLC resonant converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2006, pp. 533–538.

[3] H.-S. Choi, "Design consideration of half bridge LLC resonant converter," *J. Power Electron.*, vol. 7, no. 1, pp. 13–20, Jan. 2007.

[4] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 1321–1329, May 2009.

[5] A. Kats, G. Ivensky, and S. Ben-Yaakov, "Application of integrated magnetics in resonant converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 1997, pp. 925–930.

[6] Y. Zhang, D. Xu, and M. Chen, "LLC resonant converter from 48 V to 0.9 V VRM," in *Proc. IEEE Power Electron. Spec. Conf.*, 2004, pp. 1848–1854.

[7] S. Y. Lin and C. L. Chen, "Analysis and design for RCD clamped snubber used in output rectifier of phase shifted full-bridge ZVS converters," *IEEE Trans. Ind. Electron.*, vol. 45, no. 2, pp. 358–359, Apr. 1998.

[8] K.-B. Park, C.-E. Kim, G.-W. Moon, and M.-J. Youn, "Voltage oscillation reduction technique for phase-shift full-bridge converter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2779–2790, Oct. 2007.

[9] B.-C. Kim, K.-B. Park, C.-E. Kim, B.-H. Lee, and G.-W. Moon, "LLC resonant converter with adaptive link-voltage variation for a high-power-density adapter," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2248–2252, May 2010.

[10] L. H. Dixon, "Transformer and inductor design for optimum circuit performance," in *Proc. Unitrode Power Supply Design Seminar*, 2002, pp. 4-1–4-28.