# Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters

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Abstract—This paper presents the Bee optimization method for harmonic elimination in a cascaded multilevel inverter. The main objective in selective harmonic elimination pulsewidth modulation strategy is eliminating low-order harmonics by solving nonlinear equations, while the fundamental component is satisfied. In this paper, the Bee algorithm (BA) is applied to a 7-level inverter for solving the equations. The algorithm is based on the food foraging behavior of a swarm of a honeybees and it performs a neighborhood search combined with a random search. This method has higher precision and probability of convergence than the genetic algorithm (GA). MATLAB software is used for optimization and comparison of GA and BA. Simulation results show superiority of BA over GA in attaining accurate global minima and higher convergence rate. Also, its performance in 10 times run is the same as in 1 time run. Finally, for verifying purposes, an experimental study is performed.

*Index Terms*—Bee algorithm (BA), genetic algorithm (GA), multilevel inverter, selective harmonic elimination PWM (SHEPWM).

# I. INTRODUCTION

ODAY, there are many applications for multilevel inverters, such as flexible ac transmission system (FACTS) equipment [1], high voltage direct current lines [2], and electrical drives [3]. There are three conventional structures for multilevel inverters: diode-clamped [4], flying capacitor [5], and cascaded multilevel inverter with separate dc sources [6]. For improving inverter performance and output quality, different methods have been suggested. The first of them is using various switching strategies, such as sinusoidal or "subharmonic" natural pulsewidth modulation (SPWM), selective harmonic elimination PWM (SHEPWM), space-vector modulation (SVM), optimized harmonic-stepped waveform (OHSW) [7], [8], and optimal minimization of THD (OMTHD) [9]. The second method is using a low-pass filter in the output of inverters to eliminate high-order harmonics. Finally, the third approach, is using multilevel structures in order to reduce harmonics and THD. The

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SHEPWM strategy has also been used in multilevel inverters. In this method, the objective is elimination of low-order harmonics, while the fundamental harmonic is satisfied. If this goal cannot be obtained, the highest possible harmonics optimization is desired. In this approach, by solving S equations, (S-1) loworder harmonics from the fifth order can be eliminated and the fundamental component is satisfied. Solving SHEPWM nonlinear equations is a major problem in obtaining switching angles. So far, several methods have been suggested which can be categorized into two sets. The first group is based on satisfying the equations. The Newton-Raphson (N-R) method is one of these [10]. The disadvantage of iterative methods is their dependence on an initial guess and divergence problems are likely to occur for large numbers of inverter levels. Also, they can only find one set of solutions. In addition, using the MATLAB function fsolve, all roots can be obtained based on the Gauss-Newton method [11].

A mathematical method based on theory of resultant is proposed in [12]. This method can only find all possible solutions for those feasible Modulation index M solutions that exist. However, it is complicated and time-consuming and requires new expression when voltage level or input dc voltage is changed. Also, the Homotopy algorithm [13] is used to determine one set of solutions.

Since the first group does not suggest any optimum solutions for infeasible M, the second group of methods have been applied based on evolutionary algorithms. These methods can not only find solutions, where low-order harmonics can be completely eliminated, but they can also find solutions for infeasible M; the second group introduces optimum angles so that the equations are minimized. These methods are simple and can be used for problems with any number of levels. They are free from derivation. GA is one of the methods that have been used in the literature [14], [15]. In addition, particle swarm optimization [7], bacterial foraging algorithm [16], and ant colony [17] methods have been introduced. GA is widely used and is simpler and more applicable.

In this paper, the bee algorithm (BA) is applied to minimize low-order harmonics, as well as to satisfy the desired fundamental component. Results including the probability of reaching to a global solution and the effect of running times are compared with those obtained by GA. Results confirm the effectiveness of the proposed algorithm and its superiority over GA. Experimental results are presented to confirm the simulation results.

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unit generates a quasi-square waveform by phase-shifting the switching timings of its positive and negative phase legs.

## B. Selective Harmonic Elimination PWM

A 7-level inverter waveform shown in Fig. 2 has three variables  $\theta_1$ ,  $\theta_2$ , and  $\theta_3$ , where  $V_{dc1}$ ,  $V_{dc2}$ , and  $V_{dc3}$  are assumed to be equal. Considering equal amplitude of all dc sources, the Fourier series expansion of the output voltage waveform, shown in Fig. 1, will be written as

$$V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t)$$
(1)

where  $V_n$  is the amplitude of the *n*th harmonic. Switching angles are limited between zero and  $\pi/2$  ( $0 \le \theta_i < \pi/2$ ). Because of odd quarter-wave symmetric characteristic, harmonics with even order become zero. Consequently,  $V_n$  becomes

$$V_n = \begin{cases} \frac{4V_{\rm dc}}{n\pi} \sum_{i=1}^{S} \cos\left(n\theta_i\right) & \text{for odd ns} \\ 0 & \text{for even ns.} \end{cases}$$
(2)

The objective of SHEPWM is to eliminate the lower order harmonics while remaining harmonics are removed with filter. In this paper, without loss of generality, a 7-level inverter is chosen as a case study to eliminate its low-order harmonics (fifth and seventh). It is needless to take the triplen harmonics into consideration, since they will vanish in three-phase applications. So, to satisfy fundamental harmonic and eliminate fifth and seventh harmonics, three nonlinear equations with three angles are provided in

$$V_{1} = \frac{4V_{dc}}{\pi} [\cos(\theta_{1}) + \cos(\theta_{2}) + \cos(\theta_{3})]$$

$$V_{5} = \frac{4V_{dc}}{5\pi} [\cos(5\theta_{1}) + \cos(5\theta_{2}) + \cos(5\theta_{3})]$$

$$V_{7} = \frac{4V_{dc}}{7\pi} [\cos(7\theta_{1}) + \cos(7\theta_{2}) + \cos(7\theta_{3})].$$
(3)

In (3),  $V_5$  and  $V_7$  are set to zero in order to eliminate fifth and seventh harmonics, respectively. For obtaining various switching angles a new index, titled modulation index, is defined to be a representative of  $V_1$ :

$$M \stackrel{\Delta}{=} \frac{V_1}{12V_{\rm dc}/\pi} \qquad (0 \le M \le 1) \,. \tag{4}$$

Here, M is between 0 and 1 to cover different values of  $V_1$ .

Thus, by substituting (4) into (3), (5) can be derived and for a 7-level inverter the goal is to solve the following set of equation

$$M = \frac{1}{3} \left[ \cos \left(\theta_1\right) + \cos \left(\theta_2\right) + \cos \left(\theta_3\right) \right]$$
  

$$0 = \cos \left(5\theta_1\right) + \cos \left(5\theta_2\right) + \cos \left(5\theta_3\right)$$
  

$$0 = \cos \left(7\theta_1\right) + \cos \left(7\theta_2\right) + \cos \left(7\theta_3\right).$$
(5)

Now, three switching angles, namely  $\theta_1$ ,  $\theta_2$ , and  $\theta_3$ , must be found with respect to the range of M.



Fig. 1. Cascaded multilevel inverter with separate dc sources.



Fig. 2. The output voltage waveform of a 7-level inverter.

### **II. MULTILEVEL INVERTERS**

# A. Multilevel Inverter Topology

A cascaded multilevel inverter (see Fig. 1) has advantages that have been presented in [18]. Few components, the absence of extra clamping diodes or voltage balancing capacitors, and easy adjustment of the number of output voltage levels are some of them. Switching devices turn ON and OFF only once per cycle to overcome the switching loss problem.

The cascaded multilevel inverter consists of a series of Hbridge (single-phase full-bridge) inverter units. Each full-bridge can generate three different voltage outputs:  $+V_{dc}$ , 0, and  $-V_{dc}$ . However, all three multilevel inverters can produce staircase waveform as shown in Fig. 2. The number of output phase voltage levels in a cascaded multilevel inverter is 2S + 1, where S is the number of dc sources. For example, phase voltage waveform for a 7-level cascaded multilevel inverter with three isolated dc sources (S = 3) is shown in Fig. 2. Each H-bridge



Fig. 3. Basic flowchart of BA.

## **III. BEE ALGORITHM**

The Bee algorithm is an optimization algorithm based on the natural foraging behavior of honeybees to find the optimal solution [19], [20].

A bee colony consists of three kinds of bees: employed bees, on-looker bees, and scout bees. Employed bees carry information about place and amount of nectar in a particular food source. They transfer the information to on-looker bees with dance in the hive. The time of dance determines the amount of nectar in a food source. An on-looker chooses a food source based on the amount of nectar in a food source. A good food source attracts more on-looker bees to itself. Scout bees seek in search space and find new food sources. Scout bees control the exploring process, while employed and on-looker bees play an exploiting role.

In this algorithm, food sources are considered as possible solutions to a problem. The food source is a D-dimensional vector, where D is the number of optimization variables. The amount of nectar in a food source determines the value of fitness.

The basic flowchart of BA is shown in Fig. 3. In step 1, random initial food sources are generated. The number of initial food sources is half of the bee colony. In step 2, employed bees are sent to the food sources to determine the amount of nectar

and calculate its fitness. For each food source, there is only one employed bee. So, the number of food sources is equal to the number of employed bees. In addition, the employed bees modify the solutions, saved in memory, by searching in the neighborhood of its food source. The employed bees save the new solution if its fitness is better than the older one. Employed bees go back to the hive and share the solutions with the onlooker bees. In step 3, on-looker bees, which are another half of the colony, select the best food sources using a probability-based selection process. Food sources with more nectar attract more on-looker bees. On-looker bees are sent to the selected food sources. The on-looker bees improve the chosen solutions and calculate its fitness. Similar to employed bees, the on-looker bees save a new solution if its fitness is better than an older solution. In step 4, the food sources that are not improved for a number of iterations are abandoned. So, the employed bee is sent to find new food sources as a scout bee. The abandoned food source is replaced by the new food source. Finally, in step 5, the best food source is memorized. The maximum number of iterations is set as a termination criterion which is checked at the end of iteration. If it is not met, the algorithm returns to step 2 for the next iteration.

# IV. IMPLEMENTATION

For achieving switching angle, the BA program is written using MATLAB software. The size of population of BA is 100. In addition, the number of iterations for each run is 200 and assumed as a termination criterion. Constructed fitness function and its limitations are shown, respectively, in

$$f = \min_{\theta_i} \left\{ \left( 100 \frac{V_1^* - V_1}{V_1^*} \right)^4 + \sum_{s=2}^S \frac{1}{h_s} \left( 50 \frac{V_{h_s}}{V_1} \right)^2 \right\};$$
  
$$i = 1, 2, \dots, S \quad (6)$$

subject to

$$0 \le \theta_i \le \frac{\pi}{2} \tag{7}$$

where  $V_1^*$  is the desired fundamental harmonic, S is the number of switching angles, and  $h_s$  is the order of sth viable harmonic at the output of a three-phase multilevel inverter, e.g.,  $h_2 = 5$ and  $h_3 = 7$ .

In this section, switching angles are found such that low-order harmonics (fifth and seventh) are eliminated and the magnitude of the fundamental harmonic reaches to its desirable value, i.e.,  $V_1^*$ .

If the fundamental harmonic violates its set point by more than 1%, the first term of (6) fines it by a power of 4. Because of the use of the power of 4, corresponding penalties for any deviations under 1% get a negligible value. The second term of (6) neglects harmonics under 2% of fundamental. But, when any harmonic exceeds this limit, the objective function is subject to a penalty by power of 2. Finally, each harmonic ratio is weighted by inverse of its harmonic order, i.e.,  $1/h_s$ . By this weighting method, reducing the low-order harmonics gets higher importance.



Fig. 4. Optimum value of the objective function versus M.



Fig. 5. CDF curve obtained by BA.

The algorithm is run 1, 2, 5, and 10 times and the best solution based on the minimum fitness function is selected.

Fig. 4 shows the amount of fitness function with respect to the range of modulation index (0–1) with step 0.01, when the program is run once and 10 times.

For feasible points, the program can successfully arrive at the solutions, as it is indicated by objective values less than  $10^{-2}$ . For some modulation indices, more than one solution may exist. The program encounters with one of them. The probability of converging to global minimum for 10 times run is greater than 1 time run.

The cumulative distribution function (CDF) describes the probability that a real-valued random variable X with a given probability distribution will be found at a value less than or equal to x. In other words, it can be expressed by

$$CDF(x) = P(X < x).$$
(8)

The probability of reaching to a value below or equal to a specified fitness function is shown in the CDF curve. For example,



Fig. 6. Optimal switching angles versus M.



Fig. 7. Percentages of fundamental, low-order harmonics, and THD.

CDF  $(10^{-7})$  of BA for one time run is about 48%. This means in 48% of *M* range, the fitness is below or equal to  $10^{-7}$ . Fig. 5 illustrates the CDF curve of the fitness function for 1, 2, 5, and 10 times runs. As shown in Fig. 5, CDF values for 1, 2, 5, and 10 times run are very close to each other. So, the result in one time run is trustworthy and BA can reach to global minima in the first run and it is no longer necessary to run codes.

Figs. 6 and 7 show the situation of switching angles, harmonic conditions, and THD versus M. Line voltage THD is calculated by an accurate method, presented in [21]. If a region has a low fitness function, all low-order harmonics are maintained close to 0. For other ranges, the value of harmonics is significant so the equations cannot be solved. In both states, because of penalty, considered in fitness function, the fundamental harmonic is near the desired value. Reduction in value of low-order harmonics leads to a decrease in THD value.

To show the effectiveness of BA, GA is employed as a reference. For comparison, GA with the same BA parameters is implemented. The parameters of both algorithms are shown in

 TABLE I

 COMPARISON OF PARAMETERS BETWEEN BA AND GA

Parameters	BA	GA
Population Size	100	100
Number of iteration in each run	200	200
Number of runs	1,2,5,10	1,2,5,10
Running time	1000sec	700sec
Code complexity	moderate	low
Probability of reach to global minima	high	moderate







Fig. 9. Comparison of BA and GA in two times run.



Fig. 10. Comparison of BA and GA in five times run.



Fig. 11. Comparison of BA and GA in 10 times run.

TABLE II COMPARISON BETWEEN  $CDF(10^{-7})$  of BA and GA

Number of run	BA	GA
1-run	48.51	3.97
2-run	48.58	10.19
5-run	48.64	25.68
10-run	48.68	30.63

Table I. BA codes have more complexity and running time in comparison with GA. In fact, this complexity implies greater running time. Although BA has more complexity and run time, in BA the probability of reaching to global minima for all run number run is more greater. In Fig. 8, the CDF curve of BA is compared with that of GA for one time run. Also, CDF for 2, 5,

and 10 times runs is shown in Figs. 9–11. In all figures, the CDF for BA is greater than that for GA and this confirms the priority of BA over GA and shows that the probability of BA for reaching to global optimal is more than that of GA. For example, in Table II, CDF  $(10^{-7})$  of both algorithms for 1, 2, 5, and 10 times run is shown. However, when a fitness function is below  $10^{-2}$ , the corresponding angles are considered as solution, but here

TABLE III Switching Angles for M = 0.8

М	$\theta_1$	$\theta_2$	$\theta_3$
0.8	11.5042	28.7170	57.1061



Fig. 12. Structure of the experimental prototype.



Fig. 13. Output phase voltage.

 $x = 10^{-7}$  is selected to be more reliable. As shown in Table II, for all run numbers, the CDF of BA is more than the CDF of GA. So, BA has better performance for finding solutions.

## V. EXPERIMENTAL RESULT

For verifying BA solutions, a 3-phase 2-kW hardware prototype 7-level inverter as shown in Fig. 12 is built. It consists of three full-bridge inverters that are connected in a series form. DC source voltage of each H-bridge inverter is constant and is selected to be 12 V. Also, the frequency of the output is assumed to be 50 Hz.



Fig. 14. Harmonic spectrum of experimental output phase voltage plotted with FFT analysis of Simulink.



Fig. 15. Output line voltage.

Switching angles are obtained offline by BA for the range of M. The angles are loaded in an ATMEGA32 AVR<sup>®</sup> microcontroller as a lookup table. For each M, ATMEGA32 finds switching angles from the lookup table. ATMEGA32 transfers the switching signals to optocoupler 6N137 for isolation of insulated gate bipolar transistor (IGBT) from ATMEGA32. Finally, the signal is transferred to IGBT driver 7667 that is connected to IGBT and supplies  $Q_{ge}$  that is required for turning IGBT ON.

Fig. 13 shows the output phase voltage for M = 0.8. Switching angles are shown in Table III. According to Fig. 6, this point is feasible. The data in Fig. 13 are extracted from the Tektronix TDS1002B oscilloscope and related frequency spectrum is plotted with FFT analysis of the Simulink/Powergui block. Fig. 14 which shows the frequency spectrum confirms the results.

Fig. 15 shows the output line voltage. Fig. 16 shows the frequency spectrum of this waveform. Low-order harmonics as well as triplen harmonics are removed.



Fig. 16. Harmonic spectrum of experimental output line voltage plotted with FFT analysis of Simulink.

### VI. CONCLUSION

In this paper, elimination of low-order harmonics using SHEPWM strategy is investigated. BA is applied to solve the equations. Simulation results show accuracy and ability of BA for convergence objectives. Also, solutions have near probability to attain global minimum for 1, 2, 5, and 10 times runs and this probability is higher than the same runs for GA. Finally, to verify BA solutions, experimental results are presented which validate the accuracy of the proposed method.

#### REFERENCES

- Q. Song and W. Liu, "Control of a cascade STATCOM with star configuration under unbalanced conditions," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 45–58, Jan. 2009.
- [2] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.
- [3] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
- [4] N. Hatti, K. Hasegawa, and H. Akagi, "A 6.6-kV transformerless motor drive using a five-level diode-clamped PWM inverter for energy savings of pumps and blowers," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 796–803, Mar. 2009.
- [5] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1517–1526, Jun. 2010.
- [6] A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diodeclamped H-bridge cells," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 51–65, Jan. 2011.
- [7] A. Kaviani, S. H. Fathi, N. Farokhnia, and A. Ardakani, "PSO, an effective tool for harmonics elimination and optimization in multilevel inverters," in *Proc. 4th IEEE Conf. Ind. Electron. Appl.*, May 25–27, 2009, pp. 2902– 2907.
- [8] W. Fei, X. Ruan, and B. Wu, "A generalized formulation of quarter-wave symmetry SHE-PWM problems for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1758–1766, Jul. 2009.
- [9] M. T. Hagh, H. Taghizadeh, and K. Razi, "Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2259–2267, Oct. 2009.
- [10] W. Fei, X. Du, and B. Wu, "A generalized half-wave symmetry SHE-PWM formulation for multilevel voltage inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3030–3038, Sep. 2010.

- [11] T. Tang, J. Han, and X. Tan, "Selective harmonic elimination for a cascade multilevel inverter," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 2006, vol. 2, pp. 977–981.
- [12] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 459–469, Mar. 2006.
- [13] M. G. Hosseini-Aghdam, S. H. Fathi, and G. B. Gharehpetian, "Elimination of harmonics in a multilevel inverter with unequal DC sources using the homotopy algorithm," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 4–7, 2007, pp. 578–583.
- [14] R. Salehi, N. Farokhnia, M. Abedi, and S. H. Fathi, "Elimination of low order harmonics in multilevel inverter using genetic algorithm," *J. Power Electron.*, vol. 11, no. 2, pp. 132–139, Mar. 2011.
- [15] M. S. A. Dahidah and V. G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1620– 1630, Jul. 2008.
- [16] R. Salehi, B. Vahidi, N. Farokhnia, and M. Abedi, "Harmonic elimination and optimization of stepped voltage of multilevel inverter by bacterial foraging algorithm," *J. Electr. Eng. Technol.*, vol. 5, no. 4, pp. 545–551, 2010.
- [17] K. Sundareswaran, K. Jayant, and T. N. Shanavas, "Inverter harmonic elimination through a colony of continuously exploring ants," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2558–2565, Oct. 2007.
- [18] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
- [19] D. T. Pham, S. Otari, A. Adidy, M. Mahmuddin, and H. Al-Jabbouli, "Data clustering using the bees algorithm," in *Proc. 40th College Int. pour la Recherche en Productique Int. Manuf. Syst. Semin.*, 2007.
- [20] L. Ozbakir, A. Baykasoglu, and P. Tapkan, "Bees algorithm for generalized assignment problem," *Appl. Math. Comput.*, vol. 215, pp. 3782–3795, 2010.
- [21] N. Farokhnia, H. Vadizadeh, S. H. Fathi, and F. Anvariasl, "Calculating the formula of line voltage THD in multilevel inverter with unequal DC sources," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3359–3372, Aug. 2011.



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