# Cascade Dual Buck Inverter With Phase-Shift Control

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***Abstract*—This paper presents a new type of cascade inverter based on dual buck topology and phase-shift control scheme. The proposed cascade dual buck inverter with phase-shift control inherits all the merits of dual buck type inverters and overcomes some of their drawbacks. Compared to traditional cascade inverters, it has much enhanced system reliability thanks to no shoot-through problems and lower switching loss with the help of using power MOSFETs. With phase-shift control, it theoretically eliminates the inherent current zero-crossing distortion of the single-unit dual buck type inverter. In addition, phase-shift control and cascade topology can greatly reduce the ripple current or cut down the size of passive components by increasing the equivalent switching frequency. A cascade dual buck inverter has been designed and tested to demonstrate the feasibility and advantages of the system by comparing single-unit dual buck inverter, 2-unit and 3-unit cascade dual buck inverters at the same 1 kW, 120 V ac output conditions.**

***Index Terms*—Cascade inverter, dual buck inverter, phase-shift control.**

## I. Introduction

AMONG various multilevel voltage-source inverters, the most commonly used and commercially available ones are the neutral-point-clamped inverter, flying capacitor inverter, and cascade H-bridge inverter [1]–[4]. The cascade type inverters are capable of reaching higher output voltage level by using commercially standard lower voltage devices and components. They also feature a modular design concept which makes maintenance less burdensome [1]–[10]. The cascade inverters are well suited for utility interface of various renewable energy sources, such as photovoltaics, fuel cells, battery energy storage, and electric vehicle drives, where separate dc sources naturally exist [11]–[21]. However, because most current cascade inverters are based on a series connection of several single voltage source inverters (VSI) with two active devices in one leg, they suffer from shoot-through problems, the most dominating failure of VSI. In addition, for the hard-switched cascade inverters operating at higher dc bus voltage, they lose the benefit of using power MOSFETs as the active switching devices for efficiency improvement and fast switching speed when they are available at certain voltage and power level. For example, when the cell dc bus voltage goes up to 300 V to 600 V, high voltage power MOSFETs (600 V to 900 V level, like CoolMOS or MDmesh series) cannot be adopted to work at hard-switched situations like traditional cascade H-bridge inverters because of the reverse recovery issues of the body diode [34]–[38] unless soft-switching techniques are employed [39]–[41].

This paper proposes a new cascade dual buck inverter based on single dual buck inverter topology to better address the issues mentioned above. The dual buck type inverters are still VSI, but with the unique topology and operation, they do not have the shoot-through worries, which leads to greatly enhanced reliability [22]–[24]. Thanks to the lack of shoot-through worries of each building block, the cascade dual buck inverter features improved system reliability compared to other cascade inverters. In addition, the cascade dual buck inverter does not have the dead time related issues of conventional VSI-based cascade inverters, which can easily push the duty cycle to the theoretical limit and fully transfer the energy to load through total PWM. In addition, the cascade dual buck inverter can be hard-switched while utilizing the benefits of power MOSFETs at certain power levels.

Phase-shift control is widely used for cascade inverters because it is easy to implement with digital controllers and it equivalently increases the switching frequency by the number of cascade units, which reduces the output voltage and current ripple [25]–[27]. For the cascade dual buck inverter, phase-shift control is adopted as well. Besides the common benefits, it solves another problem for this unique cascade topology. One of the inherent drawbacks of single dual buck inverters is the current zero-crossing distortion, which will be explained in detail in Section III. Fortunately, with the help of phase-shift control, cascade dual buck inverter theoretically eliminates the zero-crossing distortion from zero to full load conditions.

The paper first shows different topologies of the proposed cascade dual buck inverters and their operation principles. This paper takes single-phase cascade dual buck half-bridge inverter as the analytical and design subject to demonstrate the feasibility and advantages of cascade dual buck inverters. The phase-shift control scheme is analyzed by comparing single-unit dual buck inverter and 2-unit cascade dual buck inverter. The closed-loop control for cascade dual buck inverter has been designed and implemented. A 1 kW, 120 V ac output cascade dual buck inverter system has been built to validate the proposed topology and control by comparing the experimental test results of single-unit dual buck inverter, 2-unit and 3-unit cascade dual buck inverters.

## II. Topology and Operation Principle

The single-unit dual buck inverter has two basic forms, dual buck half-bridge inverter [22], [24] and dual buck full-bridge inverter [23]. The proposed cascade dual buck inverter has

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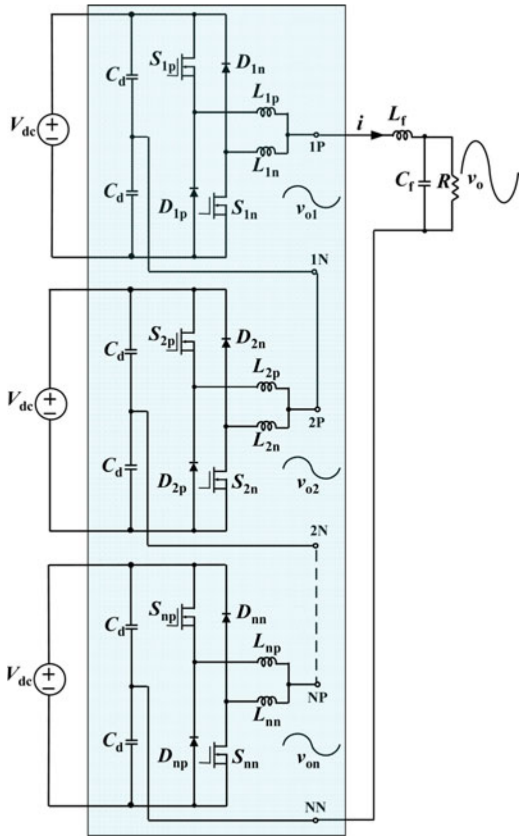


Fig. 1. Topology of cascade dual buck half-bridge inverter.

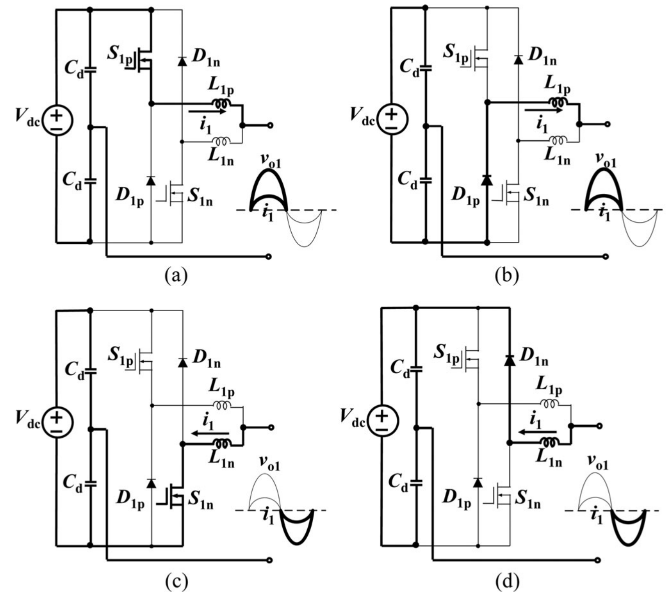


Fig. 2. Operation modes of single-unit dual buck half-bridge inverter. (a) Positive current, $S_{1\mathrm{p}}$ turned ON. (b) Positive current, $D_{1\mathrm{p}}$ free-wheeling. (c) Negative current, $S_{1\mathrm{n}}$ turned ON. (d) Negative current, $D_{1\mathrm{n}}$ free-wheeling.

two types accordingly: cascade dual buck half-bridge inverter, shown in Fig. 1, and cascade dual buck full-bridge inverter, shown in Fig. 3. This paper will focus on the analysis, design, and testing of the cascade dual buck half-bridge inverter to demonstrate the feasibility and advantages of cascade dual buck inverters.

In [24], the control strategy for two dual buck half-bridge inverters in series output to obtain higher voltage was proposed. However, the two dual buck inverters shared the same dc power supply, had two sets of filter inductor and capacitor, and the connection was only effective for two units. The proposed inverter in this paper features a different series connection concept, the cascading, which has separate dc power supplies for each cell, and is extended to $N$ unit connection, and shares the same filter components.

Fig. 1 shows the topology of the proposed cascade dual buck half-bridge inverter. It consists of $N$ units of single dual buck half-bridge inverter. Each unit is composed of two power MOSFETs and two fast recovery diodes. Each unit has two output ports, $i$P and $i$N (i $= 1, 2, \ldots, N$). To realize the cascade topology, the $i$N port of the $i$th unit is connected with the $(i+1)$P port of the $(i+1)$th unit, and port 1P and NN are used as the output ports.

$S_{\mathrm{ip}}$ and $D_{\mathrm{ip}}$ are a working pair, and operate at the positive half-cycle of output current $i$. $S_{\mathrm{in}}$ and $D_{\mathrm{in}}$ are another working pair, and operate at the negative half-cycle of output current $i$. The single unit operation modes are shown in Fig. 2 [22], [24]. For the cascade dual buck inverter, if phase-shift control is not adopted, we can switch all the units exactly the same way as single-unit inverter. This means the PWMs for $S_{\mathrm{ip}}$ and $S_{\mathrm{in}}$ are the same. However, this will bring the zero-crossing distortion problem of single-unit dual buck inverters into the cascade topology. In addition, without phase-shift control, the cascade topology loses the benefits of increased equivalent switching frequency and reduced output current ripple. Therefore, the proposed cascade dual buck inverter utilizes the phase-shift control technique to eliminate the zero-crossing distortion problem of single unit dual buck inverter and at the same time achieve higher equivalent switching frequency thus cutting down output current ripple. The detailed analysis of phase-shift control of cascade dual buck inverter will be presented in Section III.

Fig. 3(a) shows the topology of single-unit full-bridge dual buck inverter [23]. For the cascade dual buck full-bridge inverter shown in Fig. 3(b), we can put $N$ units of this single full-bridge dual buck inverter in series just like cascade dual buck half-bridge inverter in Fig. 1. The operation principle of cascade dual buck full-bridge inverter with phase-shift control will be similar to cascade dual buck half-bridge inverter, and will not be discussed in this paper.

## III. Phase-Shift Control Analysis

One of the significant characteristics of a single-unit dual buck type inverter is that the switch is selectively working based on the direction of output current. From the operation modes of single-unit half-bridge dual buck inverter in Fig. 2, we can clearly see that when $i_1$ is positive, $S_{1\mathrm{p}}$ and $D_{1\mathrm{p}}$ are the working pair, and when $i_1$ is negative, $S_{1\mathrm{n}}$ and $D_{1\mathrm{n}}$ are the working pair. However, this distinctive operation leads to its inherent drawback, current zero-crossing distortion, which will be explained in detail below. This issue can be passively mitigated by turning

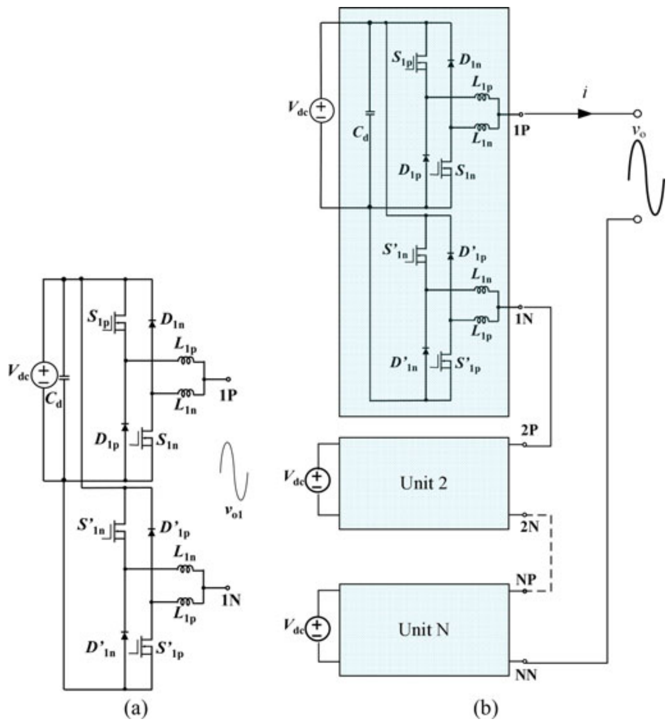


Fig. 3. Single-unit dual buck full-bridge inverter serving as one cell for cascade dual buck full-bridge inverter. (a) Single-unit dual buck full-bridge inverter. (b) Cascade dual buck full-bridge inverter.

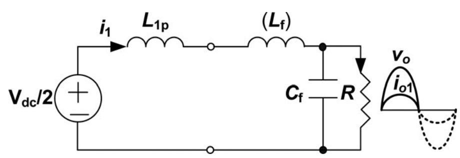


Fig. 4. Equivalent circuit of single-unit half-bridge dual buck inverter when $S_{1\mathrm{p}}$ is ON.

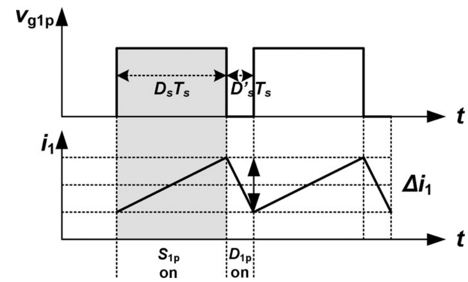


Fig. 5: Gate signal of $S_{1\mathrm{p}}$ and current $i_1$ through output inductor of single-unit half-bridge dual buck inverter.

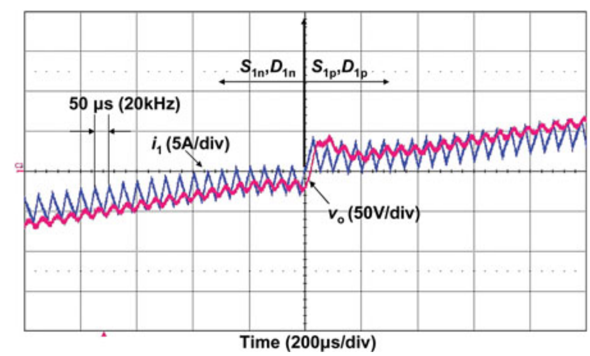


Fig. 6. Experimental result of single-unit half-bridge dual buck inverter at zero crossing period.

on both $S_{1\mathrm{p}}$ and $S_{1\mathrm{n}}$ near zero-crossing period. However, this remedy is against the operating principle and the best feature of the dual buck type inverter, which is high reliability by avoiding turning on both active switches at the same time. In addition, this passive measure results in higher switching losses because at zero-crossing period two switches are switching while the original goal of dual buck inverter is to have only one switch operating at any given time.

Thankfully, cascade topology solves the issue of zero crossing distortion by using phase-shift control scheme. With phase-shifted PWM fed to different cascade units, current zero-crossing distortion is theoretically eliminated. In addition, the phase-shift control greatly increases the equivalent switching frequency by $N$ times that of single-unit inverter, which leads to significantly lower current ripple or smaller passive filter components.

In order to illustrate the phase-shift control, single-unit half-bridge dual buck inverter and 2-unit cascade half-bridge dual buck inverter are analyzed. Fig. 4 shows the equivalent circuit of single-unit half-bridge dual buck inverter when $S_{1\mathrm{p}}$ is ON. Fig. 5 shows the gate signal of $S_{1\mathrm{p}}$ and the current through output inductor $i_1$. The shaded area of Fig. 5 corresponds to the operation mode shown by Fig. 4.

The current ripple of $i_1$ can be derived from Fig. 4 and Fig. 5 as follows:

$$\Delta i_1 = \frac{(0.5V_{\mathrm{dc}} - v_o)D_s T_s}{L_{1p} + L_f} \tag{1}$$

where $D_s$ is the duty cycle of the switch $S_{1p}$, $0.5 \leq D_s \leq 1$(Bipolar SPWM), and $T_s = \frac{1}{f_s}$, and $f_s$ is the switching frequency of $S_{1\mathrm{p}}$.

At zero-crossing period, $D_s$ is approaching 0.5. Therefore, the current ripple of $i_1$ at zero-crossing region is not zero. The same analysis applies to the negative half-cycle current. After the two half-cycle currents with switching frequency component are filtered by output capacitor $C_f$, the current $i_{\mathrm{o}1}$ gets its average component. It connects the averages of positive half-cycle current and negative half-cycle current at zero-crossing period. Because both half-cycle current averages at zero crossing are not zero, there is a jump from the negative average to the positive average, which is the current zero-crossing distortion. Since the load is resistive, the output voltage $v_o$ has the same shape as $i_{\mathrm{o}1}$, and thus has the distortion. In light load condition, the resistance is much larger, so the zero-crossing distortion of the output voltage is amplified by the multiplication of the distorted current and the load resistance.

Fig. 6 shows the experimental result of output current $i_1$ and output voltage $v_o$ across the load at zero-crossing period of single-unit dual buck inverter.

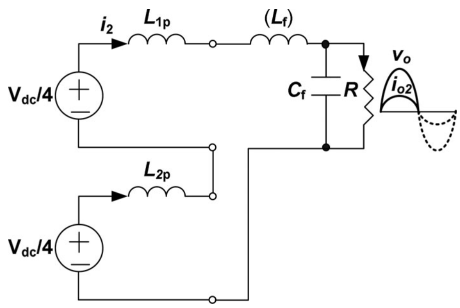


Fig. 7. Equivalent circuit of 2-unit cascade half-bridge dual buck inverter when $S_{1\mathrm{p}}$ and $S_{2\mathrm{p}}$ are both ON.

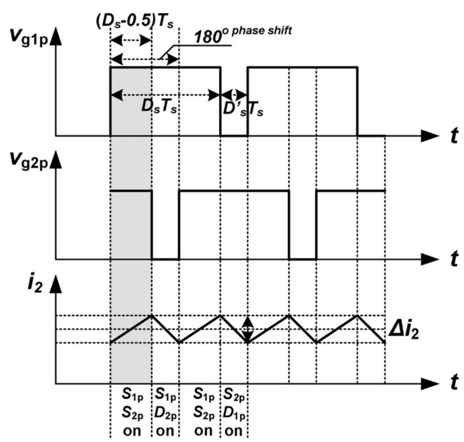


Fig. 8. Gate signals of $S_{1p}$, $S_{2p}$, and current $i_2$ through output inductor of 2-unit cascade half-bridge dual buck inverter.

TABLE I
CURRENT RIPPLE DERIVATION FOR 3, 4, AND 5-UNIT CASCADE DUAL BUCK INVERTERS

| unit \ current ripple | $\Delta i_j$ |
|---|---|
| 3 | $\Delta i_3 = \frac{(\frac{2}{2\cdot 3}V_{dc} - v_o)(D_s - \frac{1}{3})T_s}{3L_{1p} + L_f}$ |
| 4 | $\Delta i_4 = \frac{(\frac{3}{2\cdot 4}V_{dc} - v_o)(D_s - \frac{2}{4})T_s}{4L_{1p} + L_f}$ |
| 5 | $\Delta i_5 = \frac{(\frac{3}{2\cdot 5}V_{dc} - v_o)(D_s - \frac{2}{5})T_s}{5L_{1p} + L_f}$ |

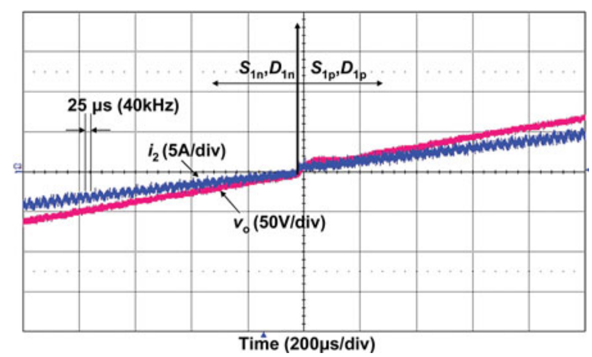


Fig. 9. Experimental result of 2-unit cascade half-bridge dual buck inverter at zero crossing period.

Fig. 7 shows the equivalent circuit of 2-unit cascade half-bridge dual buck inverter when $S_{1p}$ and $S_{2p}$ are both ON. Fig. 8 shows the gate signals of $S_{1\mathrm{p}}$ and $S_{2\mathrm{p}}$, and the current through output inductor $i_2$. The shaded area of Fig. 8 corresponds to the operation mode shown by Fig. 7. The 2-unit phase-shift angle is 180° (phase-shift angle is 360°/N). In order to generate the same output voltage $v_o$, the 2-unit cascade inverter needs two dc sources with $0.5V_{\mathrm{dc}}$ each.

The current ripple of $i_2$ can be derived from Figs. 7 and 8 as follows:

$$\Delta i_2 = \frac{(0.25V_{\mathrm{dc}} + 0.25V_{\mathrm{dc}} - v_o)(D_s - 0.5)T_s}{L_{1p} + L_{2p} + L_f}. \quad (2)$$

If $L_{1p} = L_{2p}$, (2) can be rewritten as

$$\Delta i_2 = \frac{(0.5V_{\mathrm{dc}} - v_o)(D_s - 0.5)T_s}{2L_{1p} + L_f}. \quad (3)$$

In order to find the generalized equation of current ripple with phase-shift control for $n$-unit cascade half-bridge dual buck inverter, a similar process of derivation has been conducted for a sufficient number of samples, from 3-unit inverter up to 5-unit inverter. The results are shown in Table I and it is under the assumption that $L_{1p} = L_{2p} = \cdots = L_{np}$.

From Table I, the generalized form of current ripple for $n$-unit cascade half-bridge dual buck inverter can be derived in the following:

$$\Delta i_n = \frac{(((\lceil (n+1)/2 \rceil /2n)V_{\mathrm{dc}} - v_o)(D_s - (\lceil (n-1)/2 \rceil /n))T_s}{nL_{np} + L_f} \quad (4)$$

where $\lceil x \rceil$ is the ceiling function, and is defined as the smallest integer not less than $x$

$$\lceil x \rceil = \min \{m \in \mathbb{Z} | m \geq x\} \quad (5)$$

where $x$ is a real number, m is an integer, and $\mathbb{Z}$ is the set of integers.

As can be seen from (4), at zero-crossing period, $D_s$ is very close to 0.5, and thus the current ripple at zero-crossing region is greatly reduced compared to single-unit inverter. Theoretically, when $n$ is the even number, there is no current distortion at zero-crossing point because $\lceil (n-1)/2 \rceil /n$ is equal to 0.5. It is obvious with the increase of the number of cascade units, the current ripple becomes smaller and smaller.

Fig. 9 shows the experimental result of output current $i_2$ and output voltage $v_o$ across the load at zero-crossing period of 2-unit dual buck inverter with phase-shift control. There is practically no current distortion.

From Figs. 6 and 9, we can see that the equivalent switching frequency of 2-unit cascade inverter with phase-shift control is doubled, which leads to current ripple cut-down. From (1) and

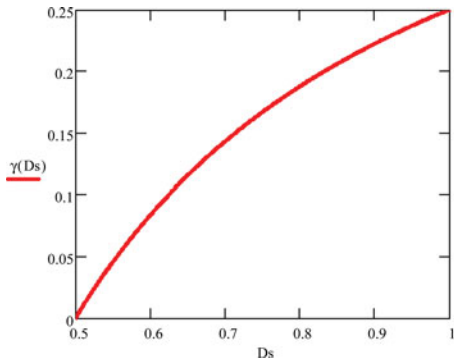


Fig. 10. Current ripple ratio between single-unit dual buck inverter and 2-unit cascade dual buck inverter.

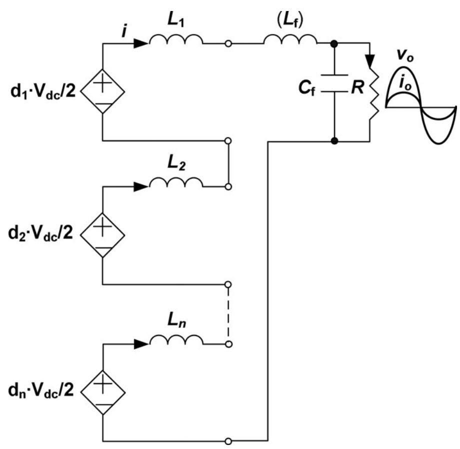


Fig. 11. The average model of N-unit cascade half-bridge dual buck inverter.

(3), the current ripple ratio is

$$\gamma = \frac{\Delta i_2}{\Delta i_1} = \frac{D_s - 0.5}{D_s} \cdot \frac{L_{1p} + L_f}{2L_{1p} + L_f}. \quad (6)$$

Since $L_{\rm ip}$ is already serving as the filter inductor, and if $L_f = 0$, (6) can be analyzed as

$$\gamma = \left(1 - \frac{0.5}{D_s}\right) \cdot 0.5 \le 25\%. \quad (7)$$

Fig. 10 shows the current ripple ratio curve under different duty cycles. From Fig. 10 we can see that at zero-crossing, the ratio reaches the lowest, zero, and climbs up when $D_s$ increases. Even as $D_s$ approaches 1, the maximum ratio is only 25%.

## IV. Closed-Loop System Control Design

In order to demonstrate the feasibility and advantages of cascade dual buck inverter, the closed-loop control is derived and designed below for a 1 kW, 120 V ac standalone system shown in Fig. 1.

Fig. 11 shows the average model of N-unit cascade half-bridge dual buck inverter. $d_j$ $(j = 1, \ldots, n)$ is the duty cycle of each corresponding unit and $L_j$ $(j = 1, \ldots, n)$ is the output inductor of each unit

$$\begin{aligned} L_j &= L_{jp} \quad i > 0 \\ L_j &= L_{jn} \quad i < 0. \end{aligned} \quad (8)$$

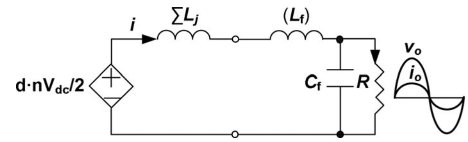


Fig. 12. The equivalent average model of N-unit cascade half-bridge dual buck inverter.

From Fig. 11, we have the following relation

$$(d_1 + d_2 + \cdots + d_n) \cdot \frac{V_{\rm dc}}{2} = \frac{d_1 + d_2 + \cdots + d_n}{N} \cdot \frac{NV_{\rm dc}}{2} \quad (9)$$

$d_j$ can be different from each other. However, to maintain the power balance of each cascade unit, it is desirable to have equal $d_j$. So if $d_1 = d_2 = \cdots = d_n = d$, (9) can be rewritten as

$$(d_1 + d_2 + \cdots + d_n) \cdot \frac{V_{\rm dc}}{2} = d \cdot \frac{NV_{\rm dc}}{2}. \quad (10)$$

From (10) and Fig. 11, it is easy to derive the equivalent average model of N-unit cascade dual buck inverter shown in Fig. 12, where $\Sigma L_j = L_1 + L_2 + \cdots + L_n$.

Define $L = \Sigma L_j + L_f$, and we have the following equation from Fig. 12:

$$d(t) \cdot \frac{NV_{\rm dc}}{2} - v_o(t) = L\frac{di(t)}{dt}. \quad (11)$$

Transform (11) to $s$ domain, we have

$$i(s) = \frac{1}{sL}\left(d(s) \cdot \frac{NV_{\rm dc}}{2} - v_o(s)\right). \quad (12)$$

So the transfer functions from duty cycle $d$ to current $i$ and voltage $v_o$ to current $i$ are as follows:

$$G_{id}(s) = \frac{i(s)}{d(s)} = \frac{\frac{NV_{\rm dc}}{2}}{sL} \quad (13)$$

$$G_{iv}(s) = \frac{i(s)}{v_o(s)} = \frac{1}{sL} \quad (14)$$

where $G_{id}(s)$ is the control-to-output transfer function and $G_{iv}(s)$ is an uncontrolled feed-forward term. By introducing admittance compensation controller $G_{\rm AC}$(s), shown in Fig. 13, the undesirable term can be cancelled out, which brings in smoother zero-current start-up and reduced current steady-state error [31], [32].

Fig. 13 shows the control block diagram of N-unit cascade half-bridge dual buck inverter operating at standalone mode. The closed-loop design adopts dual-loop design, the inner current loop with a simple proportional controller $G_P$(s) to achieve fast dynamic response with enough stability margin and the outer voltage loop with a PR controller $G_{\rm PR}$(s) to ensure a higher loop gain at fundamental frequency reducing the steady-state voltage error [28]–[30]. For this 1 kW, 120 V ac output cascade inverter system, the controllers are designed as follows.

For the PR controller in (15), $k_p$ is the proportional gain, $k_r$ is the resonant gain, and $\omega_c$ is the equivalent bandwidth of the resonant controller. In principle, the bandwidth $\omega_c$ needs to be as small as possible to obtain a highly selective bandwidth, but for digital implementation, it is quite difficult to realize

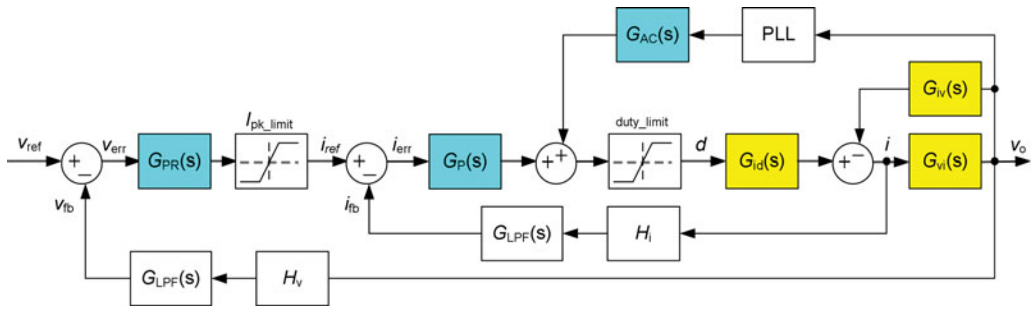


Fig. 13. Control block diagram of N-unit cascade half-bridge dual buck inverter operating at standalone mode.

a small $\omega_c$. The controller gain at fundamental frequency can be increased by increasing either $k_p$ or $k_r$. On the other hand, $k_p$ and $k_r$ cannot be too high because this will impair system stability [29], [30], [42]. With all the considerations above, the parameters for PR controller in this design have been chosen as

$$G_{\rm PR}(s) = k_p + \frac{2\omega_c k_r s}{s^2 + 2\omega_c s + \omega_1^2} \quad (15)$$

where $k_p = 0.02, k_r = 12, \omega_c = 10$.

A current loop in a dual-loop system is designed to have a high loop bandwidth with enough stability margin rather than to reduce the current steady-state error by providing a high gain at fundamental frequency [42]. In this design, a simple proportional controller will meet the requirement

$$G_P(s) = 0.05. \quad (16)$$

In [32], the equivalent dc bus voltage is $V_{\rm dc}$ for single unit inverter system, and thus the outcome of admittance compensation term is the reciprocal of $V_{\rm dc}$. From Fig. 13, we can clearly see that the equivalent dc bus voltage for the cascade dual-buck inverter is $NV_{\rm dc}/2$. Therefore, the admittance compensation transfer function is obtained as follows:

$$G_{\rm AC}(s) = \frac{1}{NV_{\rm dc}/2} \quad (17)$$

In order to close the outer voltage loop, shown in Fig. 13, $G_{vi}$(s) is derived below based on the model in Fig. 12

$$G_{vi}(s) = \frac{1}{sC_f + 1/R}. \quad (18)$$

$G_{\rm LPF}$(s) is second-order low pass filter with cut-off frequency 5 kHz and a damping ratio 0.7.

With the designed controllers above, the Bode plot of both compensated inner current loop gain and compensated outer voltage loop gain is shown in Fig. 14. As can be seen, the current loop has the cross-over frequency 1.2 kHz with gain margin 15.3 dB and phase margin 70.7°. The voltage loop has the cross-over frequency 209 Hz with phase margin 87.2°, and at 60 Hz fundamental frequency it has a gain of 35.5 dB to reject the steady state error.

Fig. 15 shows the PWM generation flow chart based on the current reference signal from Fig. 13. Fig. 16 shows the experimental results for PWM generation based on the sequence from Fig. 15. It can be seen that the PWMs for $S_{\rm ip}$ and $S_{\rm in}$ never overlap, which means this cascade dual buck inverter is shoot-through free. The phase-shifted PWMs are simple to implement by digital controller by just adding an incremental angle to the adjacent cascade unit.

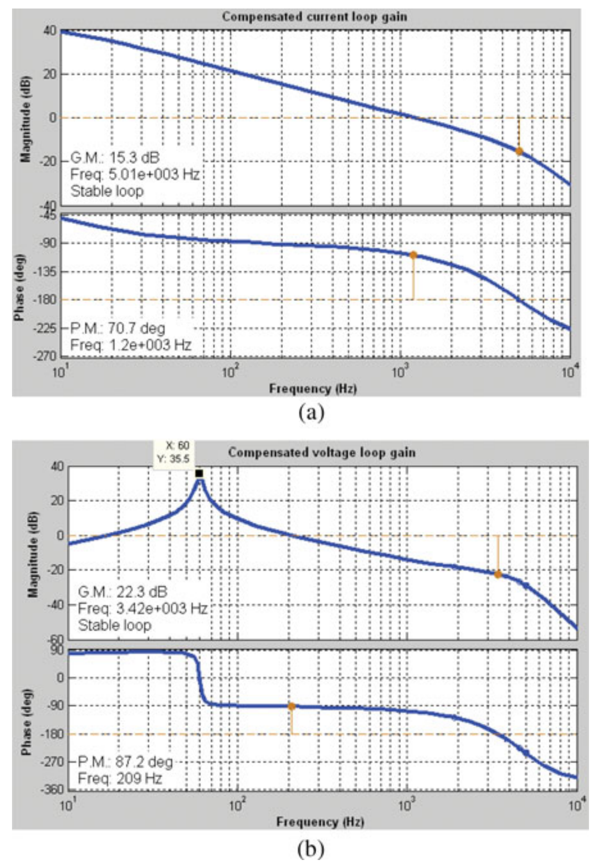


Fig. 14. Bode plot of compensated inner current loop gain and outer voltage loop gain. (a) Bode plot of compensated current loop gain. (b) Bode plot of compensated voltage loop gain.

## V. Comparative Experimental Results

To prove the viability and merits of the proposed cascade dual buck inverter with phase-shift control, a 1 kW, 120 V ac output cascade dual buck half-bridge inverter system in standalone operation was designed and tested. The system structure of the experiment is the same as in Fig. 1, and the control scheme applied is shown in Figs. 13 and 15. The system controller and PWM generation are conducted by TI floating point

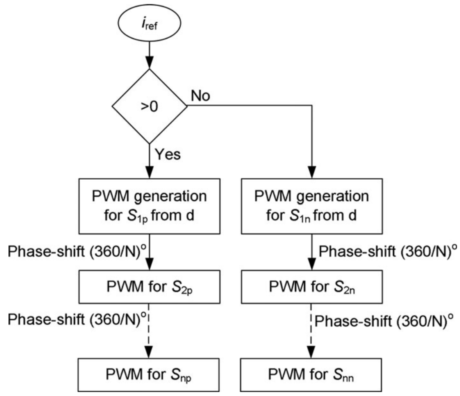


Fig. 15. PWM generation for all switches of N-unit cascade half-bridge dual buck inverter with phase-shift control.

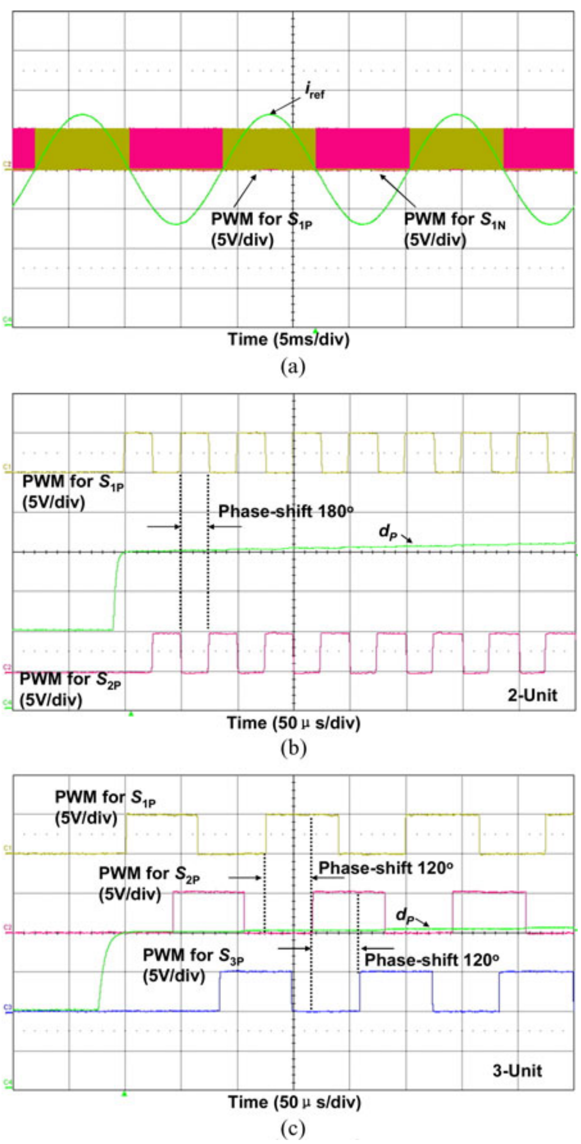


Fig. 16. Experimental results of PWM generation for N-unit cascade half-bridge dual buck inverter with phase-shift control. (a) PWM generation for $S_{1p}$ and $S_{1n}$ based on $i_{\mathrm{ref}}$ direction. (b) PWM phase-shift of $S_{1p}$ and $S_{2p}$ for 2-unit cascade dual buck inverter. (c) PWM phase-shift of $S_{1p}$, $S_{2p}$, and $S_{3\mathrm{p}}$ for 3-unit cascade dual buck inverter.

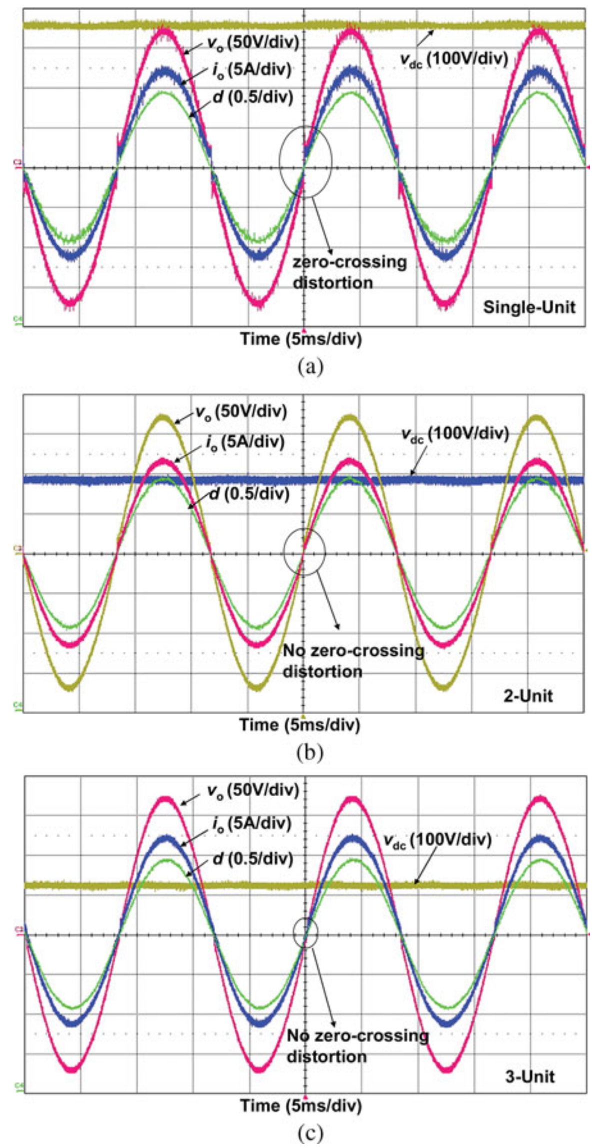


Fig. 17. Output current $i_o$, ac and dc voltage waveforms for single-unit, 2-unit cascade, and 3-unit cascade inverter system at 1 kW. (a) Single-unit inverter. (b) 2-unit cascade inverter. (c) 3-unit cascade inverter.

DSP TMS320F28335. The switching frequency of the devices is set to be 20 kHz. Because the cascade dual buck inverter adopts phase-shifted PWM control, the equivalent switching frequency of the inverter is 40 kHz for 2-unit and 60 kHz for 3-unit cascade inverters, respectively. The MOSFET is selected as STY80NM60 N with on-resistance 35 mΩ, and the diode is RURG3060 with reverse recovery time 55 ns. The passive components are selected as follows: $L_{jp} = L_{jn} = 250$ μH, $L_f = 1$ mH, $C_f = 2.4$ μF, and $C_d = 1.2$ mF. The system has the ability of serving as single-unit, 2-unit, and 3-unit systems. For comparison, tests were conducted with single-unit, 2-unit, as well as 3-unit systems. All the output power of three tests is 1 kW, and output ac voltage is 120 V RMS. For single-unit system, $V_{\mathrm{dc}}$ is 360 V, and for 2-unit cascade system, $V_{\mathrm{dc}}$ is 180 V, and for 3-unit cascade system, $V_{\mathrm{dc}}$ is 120 V.

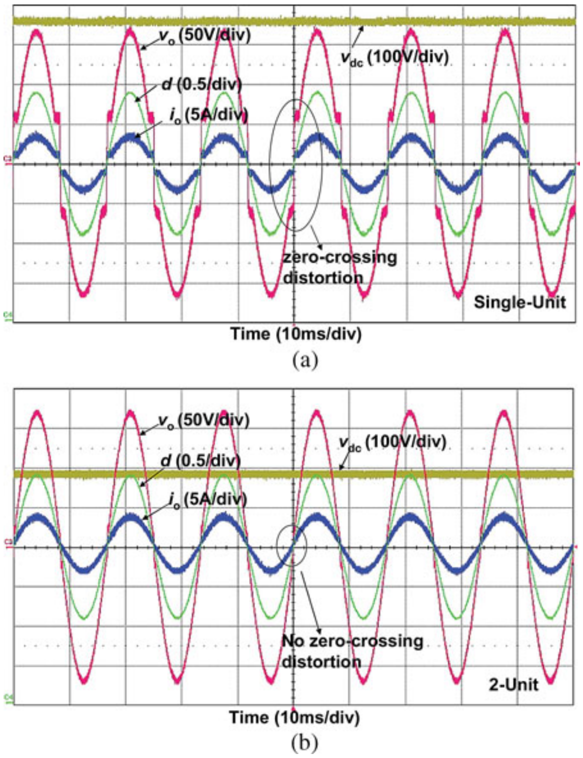


Fig. 18. Output current $i_o$, ac and dc voltage waveforms for single-unit, 2-unit cascade inverter system at 300 W. (a) Single-unit inverter. (b) 2-unit cascade inverter.

TABLE II
THD Measurement for Both Single-Unit and Cascade Dual Buck Inverters

| | 1kW | | 300W | |
|---|---|---|---|---|
| | $v_o$ | $i_o$ | $v_o$ | $i_o$ |
| 1-unit | 2.6% | 2.4% | 10.3% | 10.0% |
| 2-unit | 0.9% | 0.8% | 1.7% | 1.5% |
| 3-unit | 0.9% | 0.8% | 1.5% | 1.2% |

Fig. 17 shows the output current $i_o$ through load and voltage waveforms of single-unit dual buck inverter, 2-unit cascade dual buck inverter, and 3-unit cascade dual buck inverter at 1 kW output. It is clear that with phase-shift control for 2-unit system and 3-unit system, the current zero-crossing distortion was almost eliminated. However, the single-unit zero-crossing is severe.

The distortion problem is more obvious in light load conditions for single-unit inverter. Fig. 18 shows the comparison between single-unit inverter and 2-unit cascade inverter at 300 W output. The aggravated current and voltage distortion with very high THD will be intolerable and impose a risk for the load operation. In contrast, the cascade dual buck inverter with phase-shift control does not have this distortion at light load either. The THD is measured for both single-unit inverter and cascade dual buck inverter under full load and light load conditions. The result is shown in Table II. As can be seen, the THD at 300 W for single-unit inverter is 10% while for cascade dual buck inverter it is only around 1%.

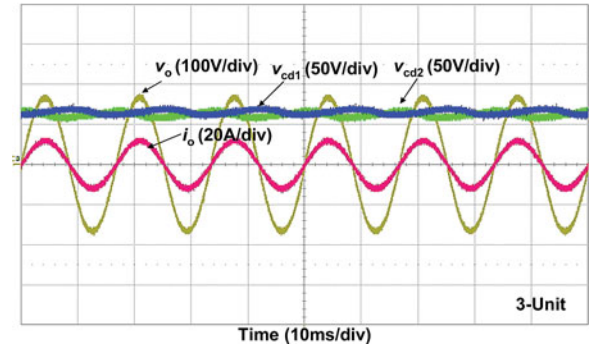


Fig. 19. Voltage waveforms across split capacitors for 3-unit cascade dual buck half-bridge inverter system at 1 kW.

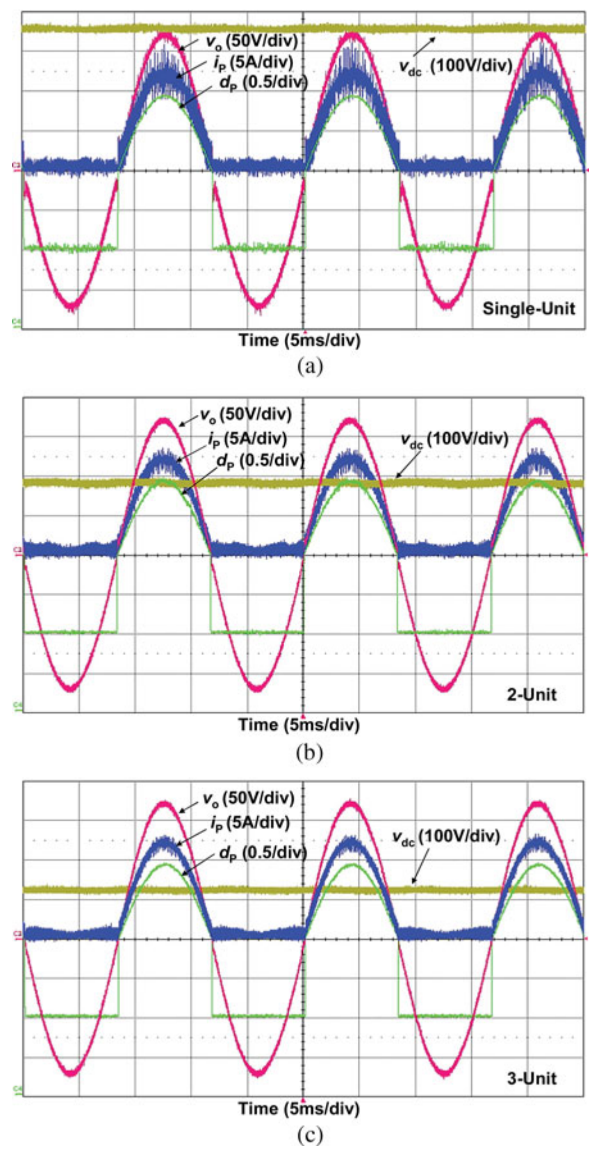


Fig. 20. Output positive half-cycle current $i_P$, ac and dc voltage waveforms for single-unit, 2-unit cascade, and 3-unit cascade inverter system at 1 kW. (a) Single-unit inverter. (b) 2-unit cascade inverter. (c) 3-unit cascade inverter.

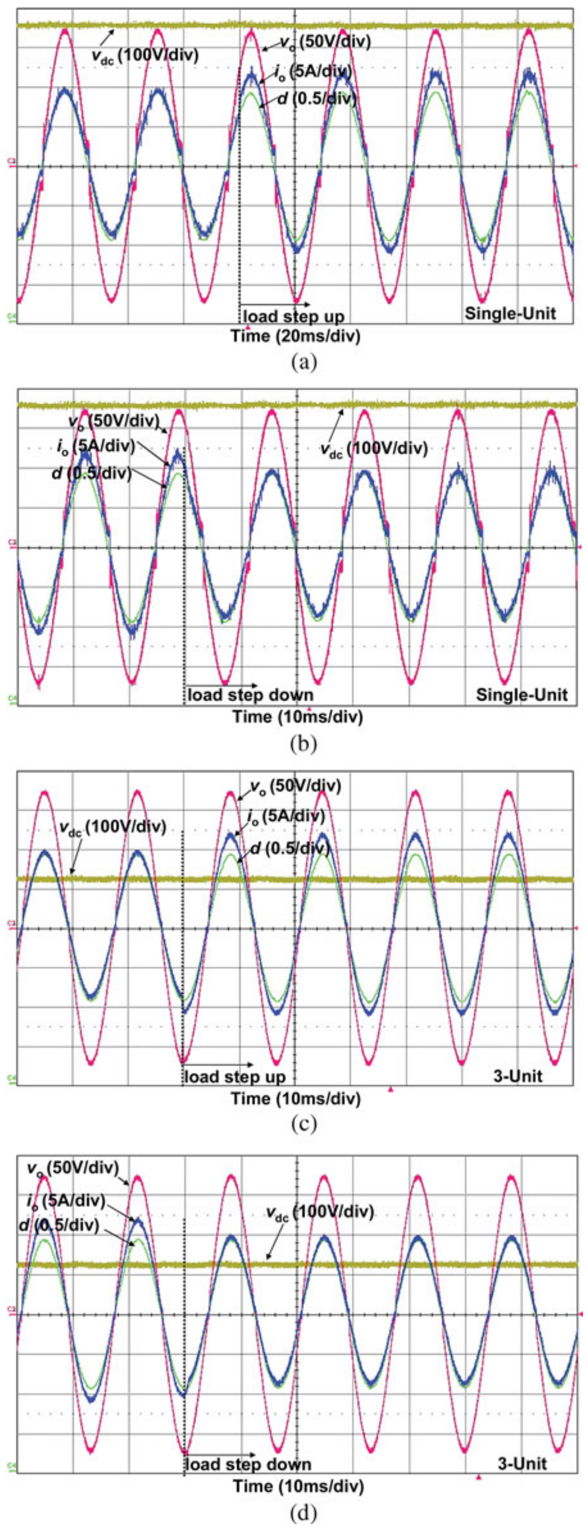


Fig. 21. Load step-up and step-down tests for single-unit inverter and 3-unit cascade inverter system. (a) Load step-up test for single-unit inverter. (b) Load step-down test for single-unit inverter. (c) Load step-up test for 3-unit cascade inverter. (d) Load step-down test for 3-unit cascade inverter.

Fig. 19 shows the voltage $v_{\rm cd1}$ and $v_{\rm cd2}$ across the split capacitors from one cell of 3-unit cascade dual buck half-bridge inverter. For the cascade dual buck half-bridge inverter, the split capacitors are needed for each cascade unit. It can be seen that the voltage of the capacitors is naturally balanced. In some cases, if the voltage across the capacitors is unbalanced, due to use of different types of capacitors, different ESR or other factors, a voltage balance compensator might be considered [33] to solve the issue. The cascade dual buck full-bridge inverter is a better alternative to save two split capacitors and totally avoid the issue.

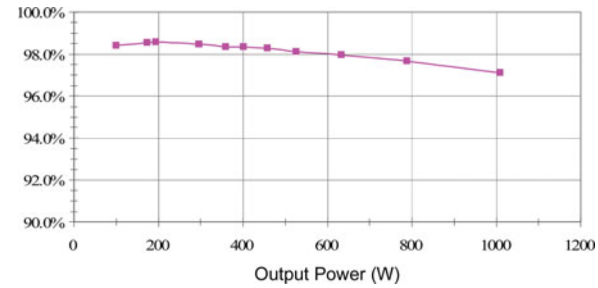


Fig. 22. Efficiency measurement under different power output conditions.

Fig. 20 shows the positive half cycle output current $i_p$ through inductor and voltage waveforms of single-unit dual buck inverter, 2-unit cascade dual buck inverter and 3-unit cascade dual buck inverter. $d_p$ is the duty cycle for current positive half-cycle. This shows the unique operating feature of single-unit dual buck inverter is inherited by cascade dual buck inverter. Every dual buck unit in the cascade system maintains the no-shoot-through characteristic, and thus leads to a more robust and reliable cascade inverter system than traditional voltage source based cascade inverter.

Fig. 21 shows the output current and voltage waveforms of single-unit inverter and 3-unit cascade dual buck inverter under load step conditions. Load step-up and step-down tests were done to show the fast dynamics and good stability of the designed control system for cascade dual buck inverter. Even though single-unit system can withstand load change, its inherent zero-crossing distortion will affect the control system and be harmful to the load.

Fig. 22 shows the measured efficiency curve under different power output conditions for cascade dual buck half-bridge inverter.

## VI. Conclusion

A new series of cascade dual buck inverters has been proposed based on single-unit dual buck inverters. The cascade dual buck inverter has all the merits of traditional cascade inverters, and improves on its reliability by eliminating shoot-through worries and dead-time concerns. With the adoption of phase-shift control, the cascade dual buck inverter solves the inherent current zero-crossing distortion problem of single-unit dual buck inverter.

To prove the effectiveness of the proposed topology and control scheme, a cascade dual buck half-bridge inverter system operating at standalone mode with 1 kW, 120 V ac output capability has been designed and tested. By comparison of experimental results of single-unit dual buck inverter with 2-unit and

3-unit cascade dual buck inverters, the viability and advantages of the cascade dual buck inverter are validated.

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