Derivation, Analysis, and Implementation of a Boost–Buck Converter-Based High-Efficiency PV Inverter

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***Abstract*—In this paper, a single-phase grid-connected transformerless photovoltaic inverter for residential application is presented. The inverter is derived from a boost cascaded with a buck converter along with a line frequency unfolding circuit. Due to its novel operating modes, high efficiency can be achieved because there is only one switch operating at high frequency at a time, and the converter allows the use of power MOSFET and ultrafast reverse recovery diode. It also features a robust structure because the phase leg does not have a shoot-through issue. This paper begins with theoretical analysis and modeling of this boost–buck converter-based inverter. And the model indicates that small boost inductance will lead to an increase in the resonant pole frequency and a decrease in the peak of Q, which results in easier control and greater stability. Thus, interleaved multiple phases structure is proposed to have small equivalent inductance; meanwhile, the ripple can be decreased, and the inductor size can be reduced as well. A two-phase interleaved inverter is then designed accordingly. Finally, the simulation and experiment results are shown to verify the concept and the tested efficiency under 1-kW power condition is up to 98.5%.**

***Index Terms*—Grid-tied, high efficiency, inverter, photovoltaic (PV).**

I. Introduction

PHOTOVOLTAIC (PV) power supplied to the utility grid is gaining more and more attention nowadays [1]–[6]. Numerous inverter circuits and control schemes can be used for PV power conditioning system (PCS). For residential PV power generation systems, single-phase utility interactive inverters are of particular interest [7]–[11]. This type of application normally requires a power level lower than 5 kW [8], [12] and a high input-voltage stack that provides a dc voltage around 400 V. However, depending on the characteristics of the PV panels, the total output voltage from the PV panels varies greatly due to different temperature, irradiation conditions, and shading and clouding effects. Thus, the input voltage of a residential PV inverter can vary widely, for example, from 200 to 500 V, and can be quite different from the desirable 400-V level. Therefore, a dc–dc converter with either step-up function or step-down function or even both step-up and step-down functions is needed before the dc–ac inverter stage. Such a dc–dc converter in conjunction with a dc–ac inverter arrangement has been widely used in the state-of-the-art PV PCS.

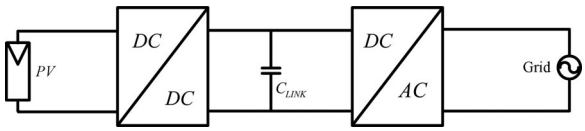

Fig. 1. Conventional two-stage PV.

Fig. 1 shows the block diagram of the PV PCS which has two-stage high-frequency power conversion in cascaded configuration with dc link in the middle [13]–[17]. In this structure, the dc-bus voltage should be boosted from the PV array, and the dc–ac stage can be a voltage-source-type high-frequency inverter. Another option is to use a line-commuted inverter along with an isolated dc–dc stage [18]–[21]. Also, many nonisolated single-stage boost or buck–boost derived inverter topologies have been developed [22]–[25]. Their major drawbacks are limitation of input-voltage range and/or requirement of two input sources [26], [27]. With recent changes in electric code that allows ungrounded PV panels, it is possible to replace the isolated dc–dc with nonisolated or transformerless dc–dc [28]. Without the transformer, the dc–dc stage will be more reliable and cost effective [29]. If the dc–dc stage can produce a rectified sinusoidal output, then the dc–ac stage only needs to operate in line frequency by simply determining the polarity of the dc–dc output.

In this paper, a boost–buck-type dc–dc converter is proposed as the first stage with regulated output inductor current, and a full-bridge unfolding circuit with 50- or 60-Hz line frequency is applied to the dc–ac sage, which will unfold the rectified sinusoid current regulated by the dc–ac stage into a pure sinusoidal current, as shown in Fig. 2. Since the circuit runs either in boost or buck mode, its first stage can be very efficient if the low conduction voltage drop power MOSFET and ultrafast reverse recovery diode are used. For the second stage, because the unfolding circuit only operates at the line frequency and switches at zero voltage and current, the switching loss can be omitted. The only loss is due to the conduction voltage drop, which can

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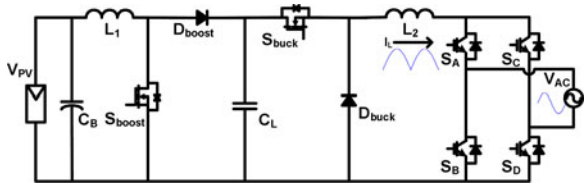

Fig. 2. Boost–buck-based PV inverter.

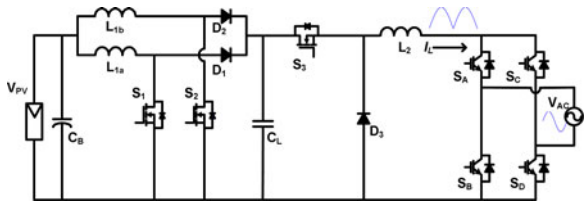

Fig. 3. Interleaved-boost-cascaded-with-buck (IBCB) PV inverter.

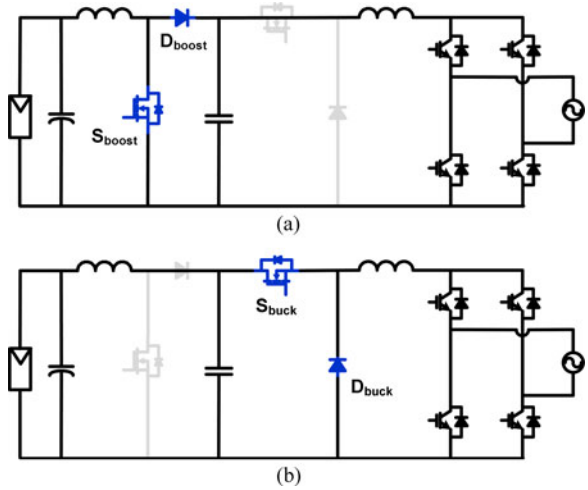

Fig. 4. (a) Boost mode. (b) Buck mode.

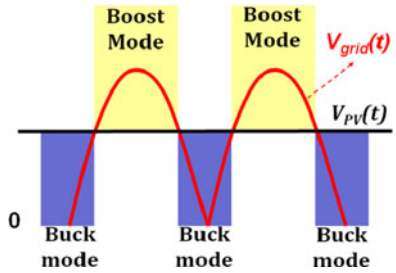

Fig. 5. Operation mode.

be minimized with the use of low on-drop power devices, such as thyristor or slow-speed insulated gate bipolar transistor (IGBT). In this version, IGBT is used in the unfolding circuit because it can be easily turned ON and OFF with gating control. Since only the boost dc–dc converter or buck dc–dc converter operates with high-frequency switching all the time in the proposed system, the efficiency is improved [30]. Also, because there is only one high-frequency power processing stage in this complete PCS, the reliability can be greatly enhanced [31]. Finally, after analyzing its model, as shown in Fig. 3, an interleaved-boost-cascaded-with-buck (IBCB) converter is proposed to increase the resonant pole frequency by the use of a smaller boost inductor value, which improves both control and stability. Analysis of a middle capacitor and CCM/DCM operation condition is also presented.

II. Operation Principle

A. Boost Mode

When the PV panel's voltage is lower than the instantaneous grid voltage, it will operate in boost mode, in which $S_{\rm boost}$ will be switched ON and OFF and $S_{\rm buck}$ will be always ON, and the buck part of the circuit will act as an output filter as shown in Fig. 4(a).

In this mode, the duty cycle of $S_{\rm boost}$ can be found as

$$D_{\rm boost} = 1 - \frac{V_{\rm in}}{V_o} \tag{1}$$

where $200 \le V_{\rm in} \le 340$ and $V_o = 340 \sin \omega t$; then, it is easy to obtain

$$0 \le D_{\rm boost} \le 1 - \frac{V_{\rm in}}{340}. \tag{2}$$

B. Buck Mode

When the PV panel's voltage is higher than the instantaneous grid voltage, it will operate in buck mode, in which $S_{\rm buck}$ will be switched ON and OFF and $S_{\rm boost}$ will be always OFF, and the boost part of the circuit will act as an input filter as shown in Fig. 4(b).

In this mode, the duty cycle of $S_{\rm buck}$ can be found as

$$D_{\rm buck} = \frac{V_o}{V_{\rm in}} \tag{3}$$

where $200 \le V_{\rm in} \le 500$ and $V_o = 340 \sin \omega t$; then, it is easy to obtain

$$\text{if } 340 \le V_{\rm in} \le 500 \text{ then } 0 \le D_{\rm buck} \le \frac{340}{V_{\rm in}} \tag{4}$$

$$\text{if } 200 \le V_{\rm in} \le 340 \text{ then } 0 \le D_{\rm buck} \le 1. \tag{5}$$

Thus, if the PV panel's voltage is lower than the grid's peak voltage, the PV inverter will switch between buck mode and boost mode depending on the instantaneous grid voltage as shown in Fig. 5. However, if the PV panel's voltage is higher than the grid's peak voltage, it will always run at buck mode. Instead of a dc bus in the middle, the voltage across the capacitor C_L in boost/buck PV inverter varies with the grid, if PV panel's voltage is lower than the grid's peak voltage as shown in Fig. 6. However, if PV panel's voltage is higher than grid's peak voltage, C_L's voltage will be the same as the PV panel's voltage.

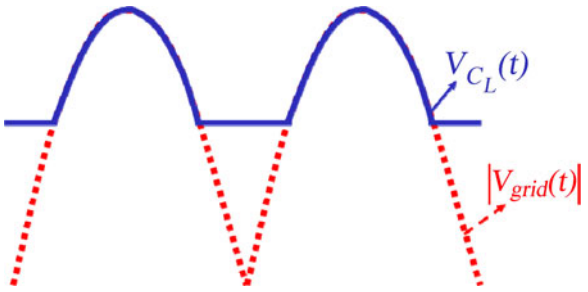

Fig. 6. Capacitor C_L's voltage.

III. Modeling and Universal Control of the Inverter

A. Modeling Analysis of the Inverter

In order to achieve unity power factor, L_2's current needs to be controlled as a rectified sinusoidal shape. The pulsewidth modulation (PWM) switch models have been established for this PV inverter both in buck mode and in boost mode as shown in Fig. 7(a) and (b) with parasitic parameters considered. The PV panel is simplified as a dc-voltage source and the grid with bridge switches is simplified as a rectified sinusoidal voltage source. Although the output voltage is rectified sinusoidal instead of constant output, it can also be treated as "steady state," since the output voltage is changing with line frequency that is much smaller than switching frequency. Under steady-state condition, the transfer functions of both modes can be obtained as equations (3) and (6) by KVL and KCL

$$\begin{cases} \hat{i}_{L1}\cdot D + I_1\hat{d} = \hat{i}_{L1} + \hat{i}_{L2C} \\ D\left(\dfrac{V_c}{D}\hat{d} - \hat{i}_{L2C}Z_{L2C}\right) + \hat{i}_{L2C}Z_{L2C} = \hat{i}_{L1}Z_{L1e} \end{cases} \tag{6}$$

where, (7)–(11), as shown at the bottom of this page.

During buck mode, L_2's current can be treated as normal buck converter's output inductor current which can be easily controlled. However, it is critical to control L_2's current in boost mode because the control target in this mode is its output filter's inductor current. Thus, the compensator for boost mode needs to be designed first and then applied to buck mode. In practice, if the boost mode is stable and well controlled, buck mode will be stable and well controlled as well. The loop gains of boost mode at different operating points are shown in Fig. 8. It clearly shows that the right half plane (RHP) zero and double pole make 270° phase delay, which makes it difficult to be compensated. Thus, the compensated crossover frequency needs to be before double-pole's frequency of the boost mode and make sure the peak Q value to be lower than 0 dB. And, in order to have a compensator which is good for every operation point, the compensator design is based on the worst conditions, which is defined as a condition with the highest $Q_{\rm pk}$ and the earliest phase drop. In our case, worst condition happens when the input voltage is the lowest

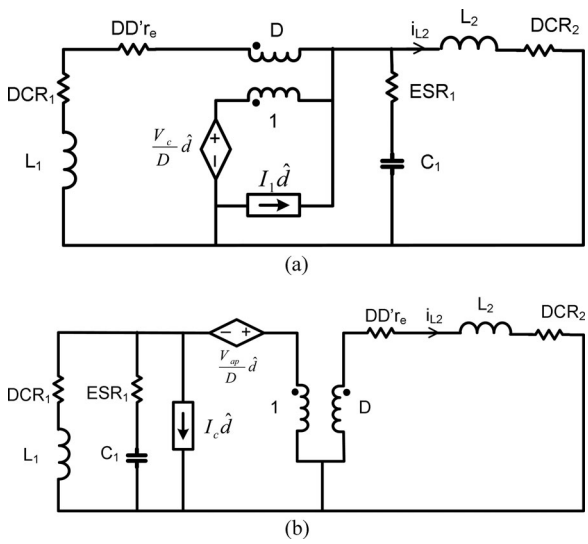

Fig. 7. (a) Model of boost mode. (b) Model of buck mode.

$$\hat{i}_{L2} = \hat{i}_{L2C}\frac{Z_C}{Z_{L2}+Z_C}, \quad Z_{L2C} = \frac{Z_C Z_{L2}}{Z_{L2}+Z_C}, \quad I_1 = -I_{L1}, \quad V_c = -V_o, \quad r_e = \mathrm{DCR}_2 \,\|\mathrm{ESR}_1 \tag{7}$$

$$G_{id\_\mathrm{boost}} = \frac{-(sL_1 + \mathrm{DCR}_1 + D'Dr_e)\cdot I_{L1} + V_o\cdot D'}{(1+sC_1\mathrm{ESR}_1)(sL_2+\mathrm{DCR}_2)D'^2 + (sL_1+\mathrm{DCR}_1+D'Dr_e)[(1+sC_1\mathrm{ESR}_1)+(s^2C_1L_2+sC_1\mathrm{DCR}_2)]} \cdot (1+sC_1\mathrm{ESR}_1) \tag{8}$$

$$Z_{LC}(I_2\hat{d} + D\hat{i}_2) = \frac{V_{\rm in}}{D}\hat{d} - Z_{Le}\cdot D\hat{i}_2 \tag{9}$$

$$\begin{aligned} Z_{LC} &= (sL_1+\mathrm{DCR}_1)\,\|((1/sC_1)+\mathrm{ESR}_1), \quad r_e = \mathrm{DCR}_1\,\|\mathrm{ESR}_1, \quad Z_{Le} = s\frac{L_2}{D^2} + \frac{\mathrm{DCR}_2}{D^2} + \frac{D'}{D}r_e \\ &= s\frac{L_2}{D^2} + \frac{\mathrm{DCR}_2}{D^2} + \frac{D'}{D}(\mathrm{DCR}_1\,\|\mathrm{ESR}_1) \end{aligned} \tag{10}$$

$$G_{\mathrm{id\_buck}} = \frac{s^2C_1L_1(V_{\rm in}-I_2D\cdot\mathrm{ESR}_1)+s\left[V_{\rm in}C_1\cdot(\mathrm{ESR}_1+\mathrm{DCR}_1)-I_2D(L_1+C_1\cdot\mathrm{ESR}_1\cdot\mathrm{DCR}_1)\right]+V_{in}-I_2D\cdot\mathrm{DCR}_1}{D^2\cdot\left[s^3C_1L_1\frac{L_2}{D^2}+s^2C_1\left(L_1\cdot\mathrm{ESR}_1+\frac{L_2}{D^2}\cdot(\mathrm{ESR}_1+\mathrm{DCR}_1)+L_1\left(\frac{\mathrm{DCR}_2}{D^2}+\frac{D'}{D}r_e\right)\right)+s\left(\frac{L_2}{D^2}+C_1(\mathrm{ESR}_1+\mathrm{DCR}_1)\left(\frac{\mathrm{DCR}_2}{D^2}+\frac{D'}{D}r_e\right)+L_1+C_1\cdot\mathrm{ESR}_1\cdot\mathrm{DCR}_1\right)+\frac{\mathrm{DCR}_2}{D^2}+\frac{D'}{D}r_e+\mathrm{DCR}_1\right]}. \tag{11}$$

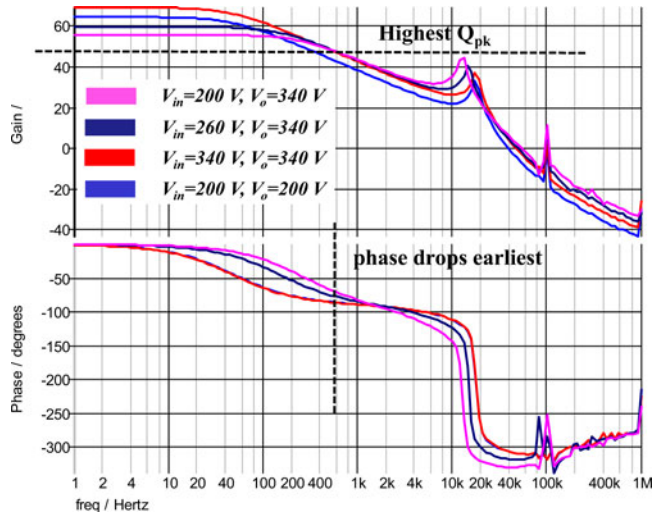

Fig. 8. Loop gain of boost mode at different operating points.

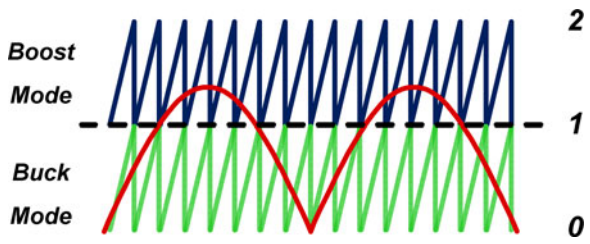

Fig. 9. Analog control for smooth transition.

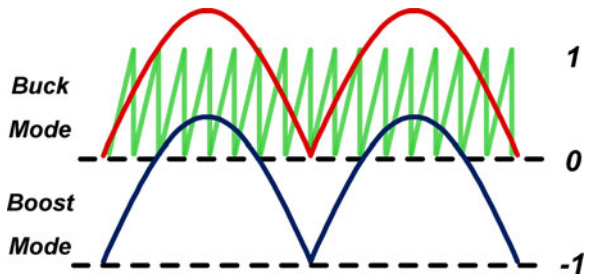

Fig. 10. Digital control for smooth transition.

defined value of 200 V and the output voltage is the peak voltage of the grid, 340 V.

In order to achieve smooth waveform in transition between boost and buck modes, an offset of the sawtooth ramp right on top of the buck-mode PWM modulator needs to be applied to boost mode as shown in Fig. 9. The high gain of buck mode can be realized by shrinking the amplitude of the ramp for buck mode. As a result, universal control for both modes can be achieved. If a digital signal processor (DSP) is employed as a controller, smooth transition between the two modes can be achieved in various ways by taking advantage of flexible algorithm implementation. For example, in our test-bed system, the signal after compensator is deducted by a unit as shown in Fig. 10 in order to achieve smooth transition between the two modes.

Table I lists the transfer function derivation results for both boost and buck modes. It can be seen that the inductor value is the dominant factor to the resonant frequency, or double-pole frequency. If L_1 can be reduced, the double-pole position, which is considered as the frequency wall of bandwidth, will be pushed to higher frequency. Moreover, the gain will increase as well, and also the Q factor will be reduced accordingly as shown in Fig. 11(a), which benefits the high-bandwidth design for the boost mode. However, decreasing L_2 will keep the same double-pole position and have higher Q factor, which would not help controller design. As a result, small L_1 and large L_2 are preferred from the design point of view.

B. Interleaved Scheme and Implementation Method

If the switching frequency can be increased so that a smaller inductance is utilized, the system will be easier to compensate and more stable. However, the efficiency may decrease in this case. In order to keep high efficiency and stability, an interleaved-boost-cascaded-with-buck converter is proposed. Fig. 12 shows the complete circuit diagram. The model of such a circuit is similar to that of the circuit shown in Fig. 4, so the same model derived in this section can be used for compensator design. The maximum power point tracking can be implemented as an outer loop with lower bandwidth control, providing the magnitude of the output current reference [32]–[35]. Figs. 13 and 14 show analog and digital control diagram.

IV. Analysis of the Middle Capacitor and CCM/DCM Operation

A. Middle Capacitor C_L Analysis

The middle capacitor C_L also impacts Q factor and double-pole frequency. Large C_L leads to small Q but low-frequency double pole. Also from the power decoupling point of view, as shown in Fig. 15, large C_L leads to large pulsating input power which means large C_{in} is needed to decouple the power, which is not expected. In our case, 2 μF is chosen for C_L

$$\begin{aligned} p_o(t) &= v_o(t)\cdot i_{L_2}(t) = V_o \sin\omega t \cdot I_{L_2}\sin\omega t \\ &= V_o \cdot I_{L_2}\frac{1-\cos 2\omega t}{2} \end{aligned} \tag{12}$$

$$\begin{aligned} p_c(t) &= C_L\frac{dv_c(t)}{dt}\cdot v_c(t) \\ &= \begin{cases} C_L\dfrac{d\left(V_o\sqrt{1-\cos 2\omega t/2}\right)}{dt}\cdot V_o\sqrt{\dfrac{1-\cos 2\omega t}{2}} \\ \qquad\qquad\qquad\qquad \text{if } V_{\text{PV}} < v_o(t) \\ C_L\dfrac{dV_{\text{PV}}}{dt}\cdot V_{\text{PV}} = 0 \qquad \text{if } V_{\text{PV}} > v_o(t) \end{cases} \end{aligned} \tag{13}$$

TABLE I
BODE PLOT PARAMETERS DERIVATION

BOOST MODE		BUCK MODE		
Double-pole position	Q	Double-pole position	Double-zero position	Q
$s=\pm\sqrt{\frac{L_2D'^2+L_1}{C_1L_1L_2}}j$	$Q\approx\frac{\sqrt{\left(L_2\cdot D'^2+L_1\right)L_1}}{D'^4C_1L_2}$ ESR_1	$s=\pm\sqrt{\frac{L_2+L_1\cdot D^2}{C_1L_1L_2}}j$	$s=\frac{\left[I_2D\cdot L_1/V_{in}-C_1\cdot(ESR_1+DCR_1)\right]\pm\sqrt{4C_1L_1}j}{2C_1L_1}$	$Q\approx\frac{\sqrt{L_1\left(2L_2+L_1\cdot D^2\right)}}{C_1L_2}$ ESR_1+DCR_1

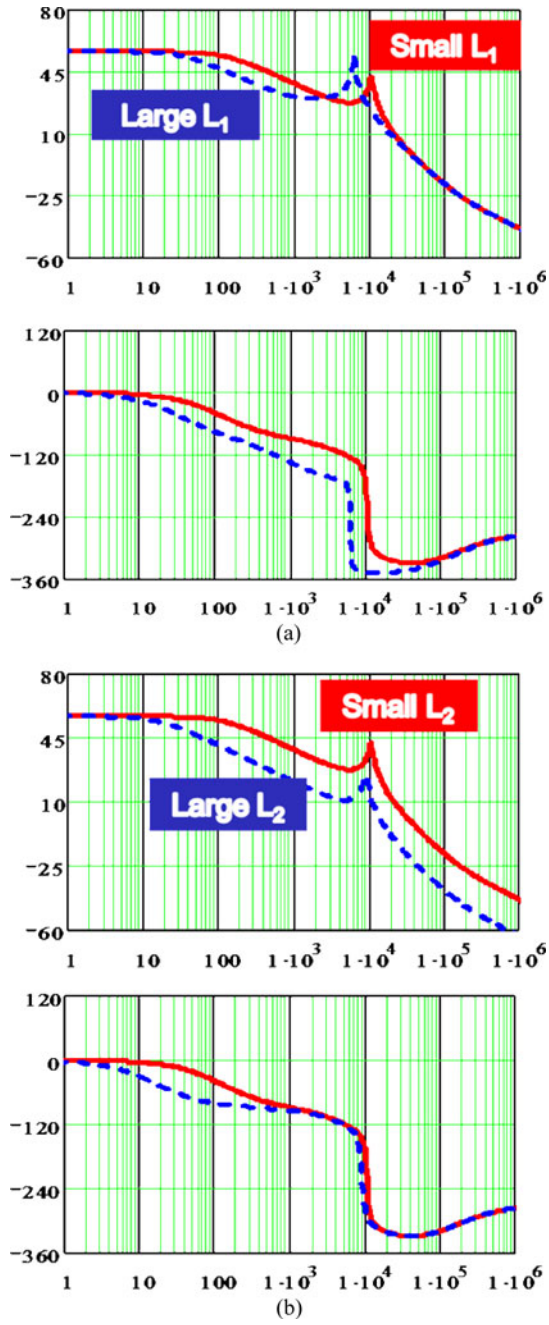

Fig. 11. (a) Boost inductance L_1's impact on boost mode bode plot $G_{\mathrm{id\_boost}}$. (b) Buck inductance L_2's impact on boost mode bode plot $G_{\mathrm{id\_boost}}$.

$$p_{\mathrm{in}}(t)=p_c(t)+p_o(t)$$
$$=\begin{cases} C_L\dfrac{d\left(V_o\sqrt{(1-\cos 2\omega t/2)}\right)}{dt}\cdot V_o\sqrt{\dfrac{1-\cos 2\omega t}{2}} \\ \qquad +V_o\cdot I_{L_2}\dfrac{1-\cos 2\omega t}{2} & \text{if } V_{\mathrm{PV}}<v_o(t) \\ V_o\cdot I_{L_2}\dfrac{1-\cos 2\omega t}{2} & \text{if } V_{\mathrm{PV}}>v_o(t). \end{cases} \tag{14}$$

B. CCM, DCM, and Boundary Condition Analysis

During the buck mode, the input current can be treated as the input filter's inductor's current whose ripple is much reduced from the filtering effect. Similarly, during the boost mode, the output current can be treated as the output filter's inductor's current whose ripple is also much mitigated. Due to this dual filter effect, the DCM mode operation is very rare in the proposed circuit.

In fact, the circuit is always running in CCM mode for the input current in buck mode and output current in boost mode. This also indicates that DCM or boundary mode can happen only in buck mode for output current and in boost mode for input current. Then, it can be analyzed as a normal buck–boost converter. The boundary condition can be derived based on the input current ripple for boost mode and the output current ripple for buck mode as follows:

$$\Delta I_{\mathrm{in}}=\frac{1}{2}\cdot\frac{\Delta T}{L}\cdot V=\frac{1}{2}\cdot\frac{(1/f_{sw})\cdot(1-(V_{\mathrm{in}}/V_o))}{L_{1a}}\cdot V_{\mathrm{in}}$$
$$=\frac{1}{20}\cdot\frac{V_{\mathrm{in}}\cdot V_o-V_{\mathrm{in}}^2}{V_o} \tag{15}$$
$$\Delta I_o=\frac{\Delta T}{L}\cdot V=\frac{(1/f_{sw})\cdot(1-(V_o/V_{\mathrm{in}}))}{L_2}\cdot V_o$$
$$=\frac{1}{20}\cdot\frac{V_{\mathrm{in}}\cdot V_o-V_o^2}{V_{\mathrm{in}}}. \tag{16}$$

Based on the aforementioned equations, it is easy to derive that the maximum ripple of an input current happens if $V_{\mathrm{in}}=200$ V and $V_o=340$ V, then $\Delta I_{\mathrm{in\_max}}=4.12$ A. And the maximum ripple of output current happens if $V_{\mathrm{in}}=500$ V and $V_o=250$ V, then $\Delta I_{o\_\max}=6.25$ A. Thus, the boundary power for different input voltages can be obtained as shown in Fig. 16(a) and (b).

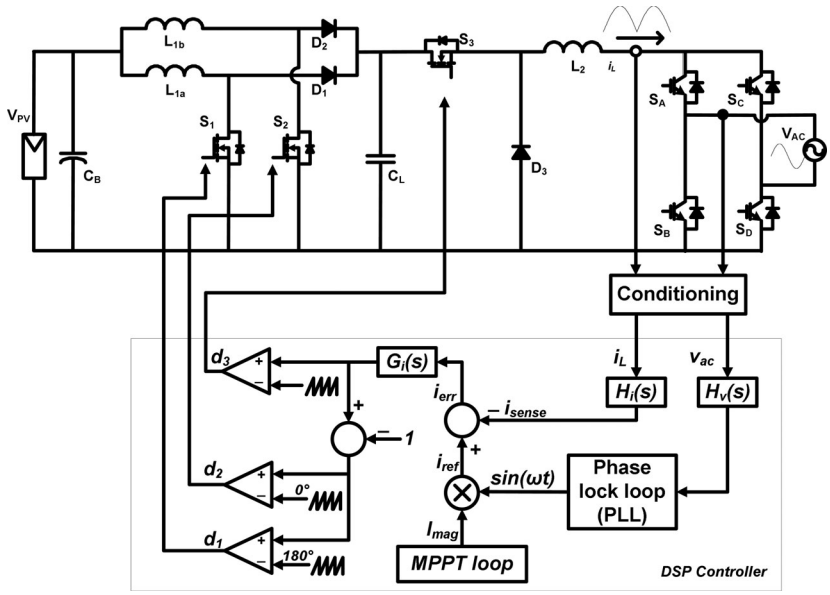

Fig. 12. Circuit diagram of the proposed PV inverter.

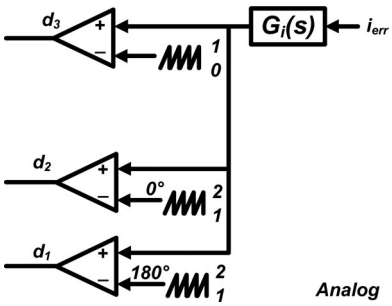

Fig. 13. Analog control diagram.

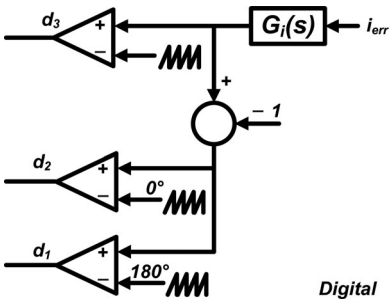

Fig. 14. Digital control diagram.

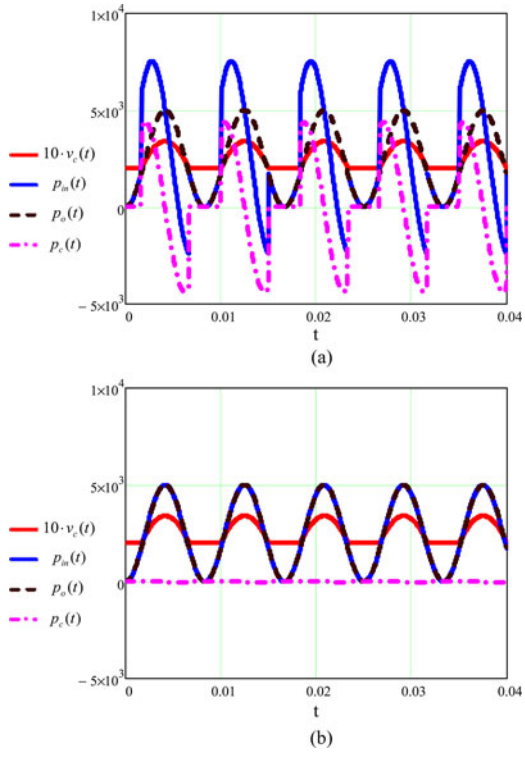

Fig. 15. (a) Pulsating power on input, output, and C_L when C_L is 200 μF. (b) Pulsating power on input, output, and C_L when C_L is 2 μF.

It is obvious from Fig. 16(a) and (b) that the input current will go to DCM under very light power condition, which is even lower than 10% of the rated power. And the output current will go to DCM under light power condition as well, which is lower than 20% of the rated power at most of the input voltage. If DCM is not desired, burst mode can be implemented under light power condition [36].

V. Simulation and Experimental Results

The proposed PV inverter along with its closed-loop controller has been simulated in PSIM. Fig. 17(a) and (b) compares the simulation results with different input-voltage conditions. In Fig. 17(a), the input voltage $V_{\rm in}$ is assumed to be 200 V. As can be seen in the figure, buck or boost switch does not work simultaneously. $S_{\rm boost}$ works when $V_{\rm in}$ is smaller than the

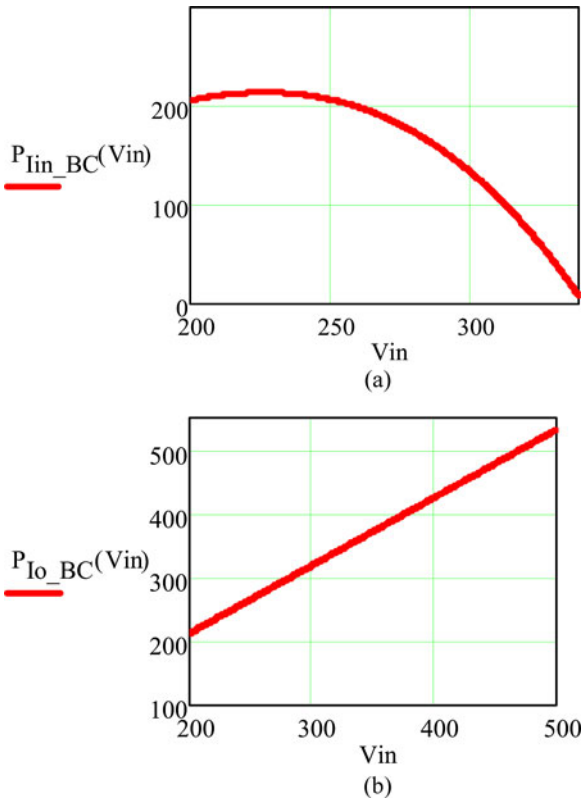

Fig. 16. (a) Boundary power condition for an input current with different input voltages. (b) Boundary power condition for output current with different input voltages.

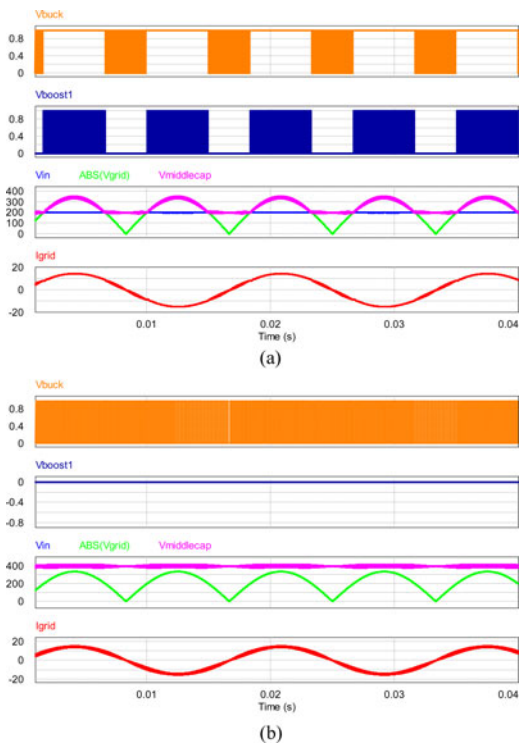

Fig. 17. (a) Simulation results with small input voltage. (b) Simulation results with large input voltage.

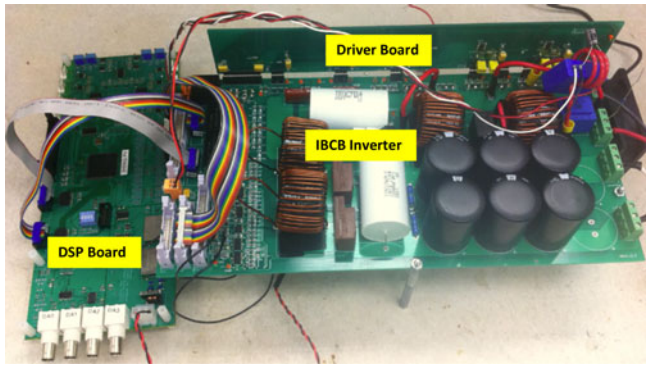

Fig. 18. Test-bed hardware prototype.

TABLE II
DESIGN PARAMETERS

Rated Power	2.5 kW
Grid Voltage	208 V_{ac} / 240 V_{ac}
Grid frequency	60 Hz
Input Voltage	200 – 500 V
Switching frequency	50 kHz

instantaneous grid voltage and $S_{\rm buck}$ works when $V_{\rm in}$ is larger than the instantaneous grid voltage. In this case, the ripple current of L_2 during boost mode is smaller than that during buck mode, because L_2 performs as the output filter's inductor of boost converter but performs a normal output inductor of buck converter. Fig. 17(b) shows the simulation results when the input voltage is 400 V. Unlike the previous case, there is no boost mode, and only $S_{\rm buck}$ is working. The voltage on the middle capacitor C_L always is equal to the input voltage since $D_{\rm boost}$ is always conducting.

Fig. 18 shows the photograph of the test-bed hardware prototype. Tables II and III list the design parameters and component selection. DSP TMS320F28335 from Texas Instruments has been implemented in the system. Fig. 19 shows the PWM and the reference control signals. Fig. 20(a) shows the testing results when $V_{\rm in}$ is smaller than the peak of the output voltage and Fig. 20(b) shows the testing results when $V_{\rm in}$ is greater than the peak of the output voltage.

Other than the proposed structure and control method, testing with different control methods with different voltages on C_L has been conducted. Instead of making the middle capacitor C_L's voltage the same as the grid voltage during boost mode, we should control its voltage constant higher than the grid voltage as shown in Fig. 21. With 1-kW power, the efficiency curves

TABLE III
COMPONENTS SELECTION

L_{1a}, L_{1b}	200 μH
L_2	400 μH
C_B	2 mF
C_L	2 μF
S_1, S_2, S_3	SPW47N60C3
D_1, D_2, D_3	C3D20060D
S_A, S_B, S_B, S_D	FGH30N60LSD

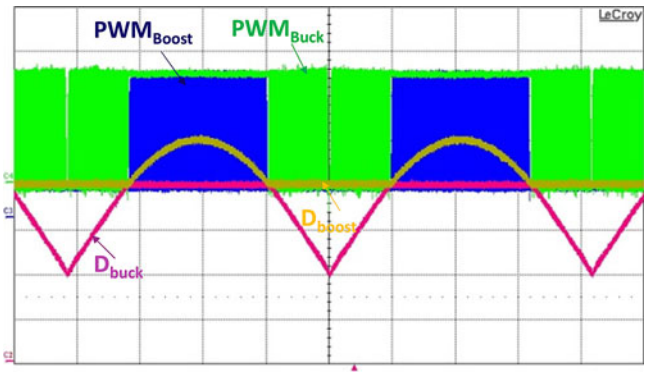

Fig. 19. Experiment results of PWM signals.

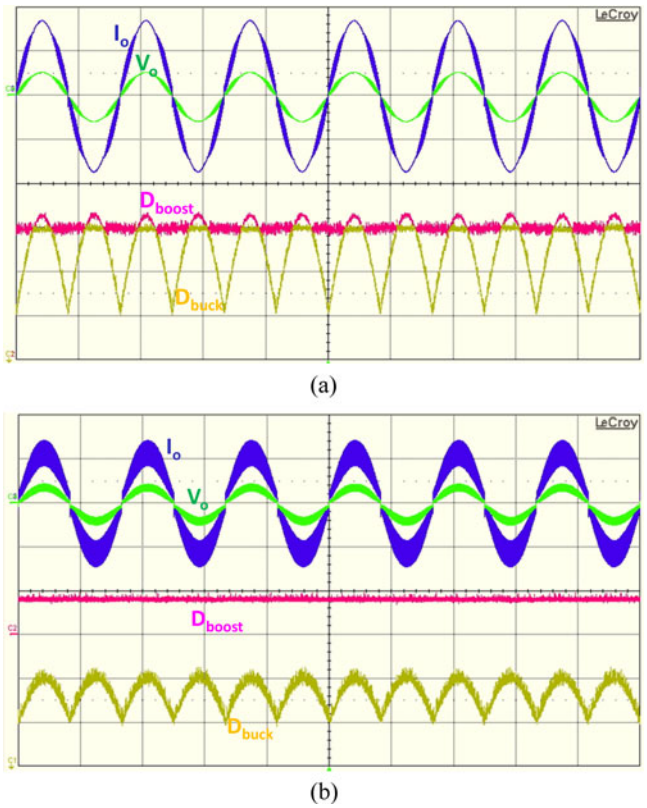

Fig. 20. (a) Experimental results with small input voltage. (b) Experimental results with large input voltage.

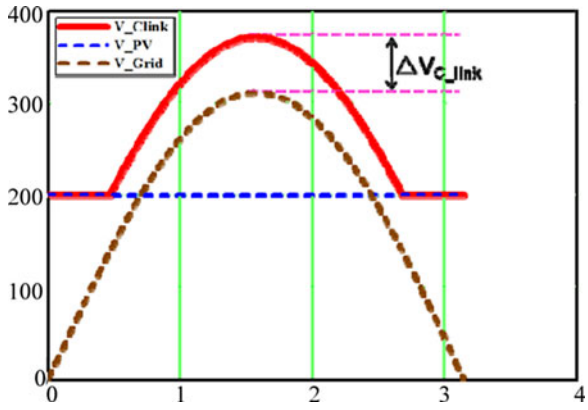

Fig. 21. Voltage on C_L for other tested control methods.

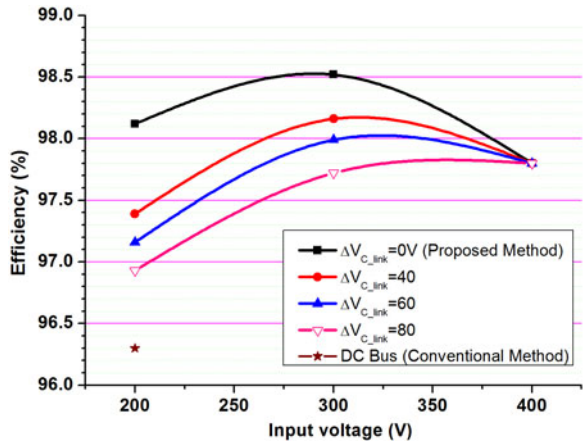

Fig. 22. Efficiency curve of boost–buck stage with 1-kW power.

of different input voltages are shown in Fig. 22, which include the proposed solution, different $\Delta V_{C\_\mathrm{link}}$, and constant V_{C_link}. The results indicate that the peak efficiency reaches 98.5% of the proposed control method. If the conventional two-stage with dc-link control method is used, the first stage's efficiency is only 96.3% at 200 V input voltage. Although the testing is conducted without the unfolding circuit, the loss in this part is small, only around 8 W loss for 1-kW power. If CoolMOS are used in the unfolding circuit, the loss in this part will only be 2.4 W for 1-kW power. Thus, the overall efficiency is still high.

VI. SUMMARY

The derivation of a highly efficient robust residential PV inverter based on a boost-cascaded-with-buck converter along with an unfolding circuit has been presented. The first-stage converter operates in either boost or buck mode, so high efficiency can be achieved. A multiphase interleaved boost stage is proposed to increase the resonant pole frequency by the use of a smaller inductor value. As a result, the control loop bandwidth can be pushed further up to enhance the robustness of the complete system. The proposed circuit along with its controller has been designed, simulated, and tested with a hardware prototype. Finally, the results indicate that the efficiency of the

proposed solution is around 2% higher than the conventional solution under the same condition.

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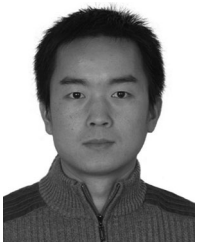

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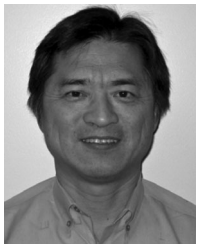

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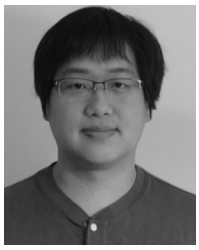

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