# Digitally Implemented Average Current-Mode Control in Discontinuous Conduction Mode PFC Rectifier

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***Abstract*—This paper proposes a digital average current-mode control method in discontinuous conduction mode (DCM) power factor correction rectifier. The proposed control technique does not estimate, but directly senses the average value of the inductor current in each switching cycle. It is implemented by means of a conventional current sensing circuit and a microcontroller. The calculation burden of the microcontroller is the same with that of conventional two-loop-controlled converter because the additional calculation process is not required. The control method achieves lower total harmonic distortion and higher power factor than the conventional technique. Experimental results with a 200-W prototype verify the feasibility and performance of the proposed control method.**

***Index Terms*—Average current-mode control, digital control, discontinuous conduction mode (DCM), power factor correction (PFC), variable-duty-cycle control.**

## I. Introduction

DISTORTED line current from nonresistive load causes problems such as power loss, noise, line voltage distortion, and reduced line utilization [1]. Regulations on harmonic current limit such as IEC61000-3-2 [2] and the internal specifications of many electronic equipment manufacturers are generally considered to alleviate these problems. Active power factor correction (PFC) front-end rectifier based on switch-mode power supply with its input filter is one solution to minimizing the harmonic current and meeting the regulations. By employing proper control scheme, the active PFC rectifier emulates the resistive load and achieves low line current distortion.

In low to medium power application, where rms inductor current is fairly low, discontinuous conduction mode (DCM) as well as critical conduction mode (CRM, also referred to as boundary conduction mode or transition mode) is widely used due to its low switching loss, low diode reverse recovery current, and small inductor size. Its constant switching frequency and inherent current sharing capability are also advantageous when interleaving more than one module [3], [4], while variable switching frequency of CRM requires maximum frequency limitation and sophisticated interleaving technique.

Distorted input current, however, can be the major drawback to DCM if the control method is not properly considered. As a conventional control law for DCM, constant-duty-cycle control (also referred to as open-loop control or voltage follower control) is widely used for its simplicity because the controller needs a low-bandwidth voltage loop and no current loop, which does not require current sensing and control circuit [5]–[7]. The average inductor current is naturally distorted with this control method because the duty cycle is virtually fixed and not compensated within a half line cycle. In addition, nonzero inductor current at the beginning of the switching cycle, which is perturbed by the resonance between the parasitic capacitance of the switch and main inductor, is not controlled and may act as another source of input current distortion [8].

A typical solution used to reduce the current distortion of the DCM PFC rectifier is variable-duty-cycle control, which is the counterpart of the conventional constant-duty-cycle control [9]–[14]. The variable-duty-cycle control not only overcomes the problem of distorted input current [9], but also mitigates the output voltage ripple and rms inductor current [10]. It is generally realized by modifying the voltage loop of the constant-duty-cycle control by utilizing an input voltage feedforward and additional calculation circuit. An analog calculation circuitry for square-root operation and multiplication is added in [10] and [11]. As the tradeoff of the decreased current distortion, the control circuits become complicated. Ye and Jovanović [12] digitally realized the analog control scheme in [11] and eliminated complicated analog calculation circuits, while the calculation burden of digital controller is increased. One-cycle control method shown in [9] enables the variable-duty-cycle control with the two resettable integrators and input voltage feedforward network instead of the square-root operator and multiplier. Synthesizing a certain harmonic component of the line frequency in the voltage loop is another modification for variable-duty-cycle control, which requires additional phase detector and phase-locked loop for line input voltage [13], [14]. The common feature of the aforementioned realizations of variable-duty-cycle control for DCM PFC rectifier is that the average value of the inductor current is not sensed but estimated, which leads to complicated control circuits or the calculation algorithm. Furthermore, these implementations cannot eliminate the current distortion caused by the perturbed initial inductor current in a unit switching period as explained in [8].

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Instead of modifying the voltage loop, adding a current loop with an inductor current sensing circuit is considered as an alternative to implementing variable-duty-cycle control of DCM PFC rectifier. The current loop can effectively suppress current distortion by the initial inductor current perturbation [15]. However, digitally sampling the inductor current in DCM operation is not as straightforward as it is in continuous conduction mode (CCM) [16]. In DCM, the sampled inductor current needs to be corrected to properly represent the average inductor current per switching period [17], [18]. The digital controller should deviate the sampling instant within the switching period and calculate a correction factor to determine the average inductor current, which consumes considerable resources of the controller. Sampling the inductor current more than once in a switching cycle may help to achieve precise average inductor current, though it requires a high-performance A/D converter for high-rate sampling [19].

In this paper, an average current-mode control for DCM PFC rectifier is digitally implemented to realize the variable-duty-cycle control. With a direct sensing of the average inductor current, the high-bandwidth current loop dramatically reduces the input current distortion. It uses the conventional sensing circuit and fixed sampling instant to sample the average inductor current. The sampling occurs once per switching cycle, which does not need high-rate sampling A/D converter. The control algorithm of the proposed control implementation requires the same calculation burden with that of conventional two-loop-controlled converter, and additional computation such as correction factor calculation is not necessary.

This paper consists of the following sections. In Section II, circuit configuration, mode analysis, and operation of the sensing circuit as well as the two-loop control strategy are given. With the mathematical expression of properly controlled inductor current shape, it is explained how the variable-duty-cycle control can achieve lower current distortion than constant-duty-cycle control. Section III illustrates design procedure of the proposed control implementation. It includes the design of boost inductance, sensing capacitance, and digitally realized control loops. Experimental results with 200-W prototype hardware are presented in Section IV. Conclusions are presented in Section V.

## II. Control Technique for DCM PFC Rectifier

### A. Operation of Average Sensing Circuit

The proposed control technique follows the general structure of the conventional two-loop control to build an average current-mode control, as shown in Fig. 1. The average sensing circuit, the shaded box in Fig. 1, gives the average inductor current in each switching cycle to establish the current-mode control. The sampling of the average inductor current occurs once in a switching period like other controller inputs such as rectified input voltage and output voltage. It does not need high-rate sampling, which samples twice or more per switching period; thus, it can save the resources of the digital controller.

Circuit configuration and operational waveform of the average sensing circuit are shown in Fig. 2. As shown in Fig. 2(a), the circuit looks the same as the conventional current sensing

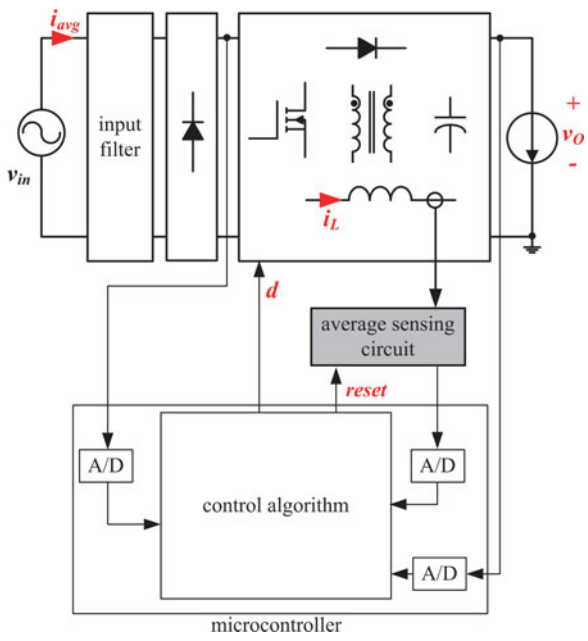


Fig. 1. Proposed control technique applied to the PFC rectifier for digital average current-mode control.

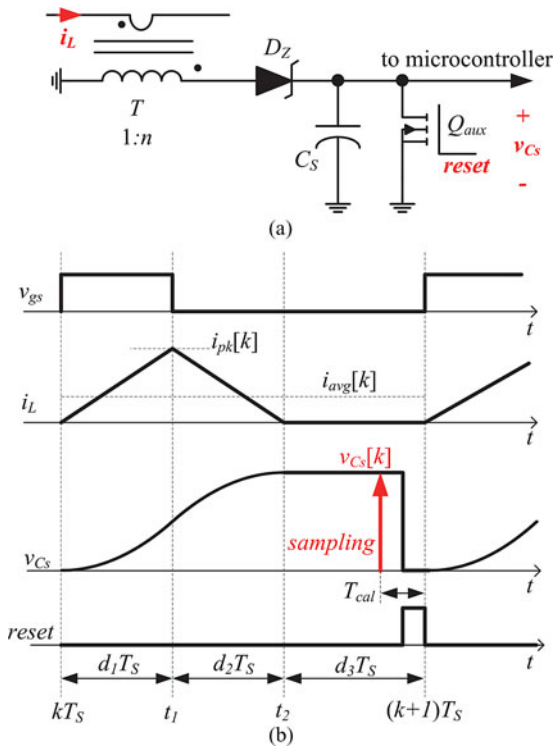


Fig. 2. Average sensing circuit. (a) Circuit structure. (b) Operational waveforms.

circuit utilized in charge current-mode control [20], but its operation differs in the proposed control. In the charge current-mode control, the sensing capacitor voltage $v_{Cs}$ represents the average switch current per switching cycle by integrating the switch current during ON-time. The voltage is reset to zero right after the main switch turns off by the inversed main gate signal.

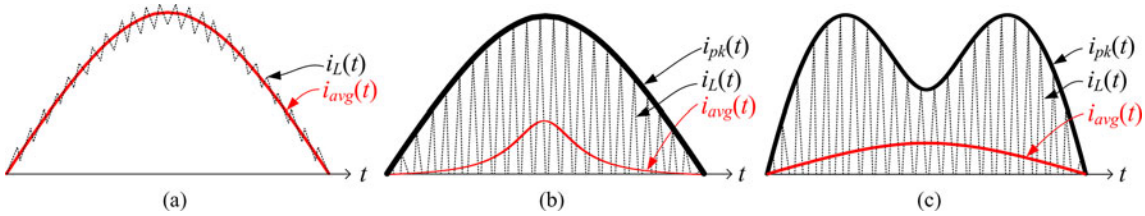


Fig. 3. Comparison of current waveform shapes. (a) Average current-mode-controlled CCM. (b) Constant-duty-cycle-controlled DCM. (c) Variable-duty-cycle-controlled DCM.

In the proposed control, on the other hand, the same circuit is utilized to integrate not the switch current, but both the switch and the diode current. The integrating interval of the sensing circuit is extended to near the end of the switching cycle by delaying the timing of the reset signal. Fig. 2(b) shows the typical waveform of the proposed average sensing circuit operation in DCM PFC rectifier. $v_{gs}$, $i_L$, *reset*, and $T_S$ are the gate signal for main switch, the inductor current, the gate signal for auxiliary switch $Q_{\rm aux}$ in average sensing circuit, and the switching period, respectively. $d_1$ and $d_2$ are the duty ratios for the switch conduction interval and diode conduction interval in the power stage. To take advantage of the analog integrating circuit and avoid the high-rate sampling, the circuit integrates the scaled inductor current in the sensing capacitor $C_S$ and samples $v_{Cs}$ once in the switching cycle. In the first interval in $k$th switching cycle, $kT_S < t < t_1$, the main switch is in ON-state. $i_L$ increases linearly and $v_{Cs}$ increases in parabolic way because the linear term of $i_L$ is integrated, as expressed in the following:

$$v_{C_s}(t) = \frac{1}{nC_S}\int_{kT_S}^{t} i_L(t)dt. \tag{1}$$

In (1), $n$ is the turn ratio of the current transformer. In the second interval, $t_1 < t < t_2$, the main switch is in OFF-state. $i_L$ decreases and the sign of the parabolic curve of $v_{Cs}$ is inverted. In the third interval, $t_2 < t < (k+1)T_S$, of which the time duration is $d_3T_S$, $i_L$ becomes zero and the sampled value $v_{Cs}[k]$ fully represents the average inductor current, as follows:

$$v_{C_s}[k] = \frac{T_S}{nC_S}\left[\frac{1}{T_S}\int_{kT_S}^{(k+1)T_S} i_L(t)dt\right] = \frac{T_S}{nC_S} i_{\rm avg}[k]. \tag{2}$$

The term in the braces in (2) is the average inductor current in the $k$th switching cycle $i_{\rm avg}$. Thus, $v_{Cs}[k]$ represents the scaled value of the average inductor current. $Q_{\rm aux}$ in the average sensing circuit turns on after the sampling to discharge $C_S$ before the next switching period.

Sampling $v_{Cs}[k]$ in the third interval occurs when the remaining time of the switching cycle is $T_{\rm cal}$. $T_{\rm cal}$ is the minimum required time that includes A/D conversion and reset of $v_{Cs}$, and calculation and update of the duty cycle for the next switching cycle. Because the resetting time of $v_{Cs}[k]$ becomes negligible by selecting $Q_{\rm aux}$ with low ON-state resistance, $T_{\rm cal}$ is effectively fixed by the calculation time according to the control algorithm programmed in the microcontroller. Therefore, the sampling time can also be fixed within the switching cycle. The sampling time and the inductance design to secure sufficient $T_{\rm cal}$ will be explained later.

### B. Current Waveforms in DCM PFC Rectifier

Fig. 3 compares the inductor current waveforms of average current-mode-controlled CCM, constant-duty-cycle-controlled DCM, and variable-duty-cycle-controlled DCM over a half line period. The continuous-time-domain current waveforms such as $i_{\rm pk}(t)$ and $i_{\rm avg}(t)$ in Fig. 3 are the approximated ones of the discrete-time-domain waveforms $i_{\rm pk}[k]$ and $i_{\rm avg}[k]$, assuming that the switching frequency of the rectifier is much higher than the line frequency. The waveforms of average current-mode-controlled CCM PFC rectifier in Fig. 3(a) resemble the sinusoid of the line voltage because the switching ripple of $i_L$ is relatively small. However, unlike in CCM rectifier, the envelope of the inductor current in DCM PFC rectifier should not look like a sinusoid to demonstrate low current distortion. In Fig. 3(b), constant-duty-cycle control constructs the envelope of the inductor current $i_{\rm pk}(t)$ to be sinusoidal. However, the resultant filtered inductor current or the line current $i_{\rm avg}(t)$ is highly distorted. Analysis of line current distortion according to line voltage in constant-duty-cycle-controlled DCM is given in [4]. In contrast to Fig. 3(b), Fig. 3(c) shows that in variable-duty-cycle-controlled DCM, $i_{\rm avg}(t)$ follows the sinusoidal curve though $i_{\rm pk}(t)$ does not.

If the average inductor current per switching cycle is controlled to be proportional to the sinusoidal input voltage by the variable-duty-cycle control, $i_{\rm pk}(t)$ can be derived from the duty ratios $d_1$ and $d_2$, as expressed in (3) and (4)

$$d_1 = \frac{Li_{\rm pk}(t)}{|v_{\rm in}(t)|\,T_S} \tag{3}$$

$$d_2 = \frac{Li_{\rm pk}(t)}{(v_O - |v_{\rm in}(t)|)\,T_S} \tag{4}$$

where $L$, $v_O$, and $v_{\rm in}(t)$ are inductance in power stage, output voltage, and line voltage, respectively. $i_{\rm avg}(t)$ is derived from the geometry of the waveform shown in Fig. 2(b) with unknown constant $X$, as shown in the following:

$$i_{\rm avg}(t) = \frac{1}{2}(d_1+d_2)i_{\rm pk}(t) = X\sin\omega_L t \tag{5}$$

where $v_{\rm in}(t)$ is assumed to be the pure sine wave with peak value $V_{\rm pk}$ and line period $T_L = 2\pi/\omega_L$, which is expressed in the following:

$$v_{\rm in}(t) = V_{\rm pk}\sin\omega_L t. \tag{6}$$

Substituting (3), (4), and (6) into (5) yields the following:

$$i_{\rm pk}(t) = \sqrt{\frac{2T_S V_{\rm pk} X}{L}}\sqrt{1-\frac{V_{\rm pk}\sin\omega_L t}{v_O}}\sin\omega_L t. \tag{7}$$

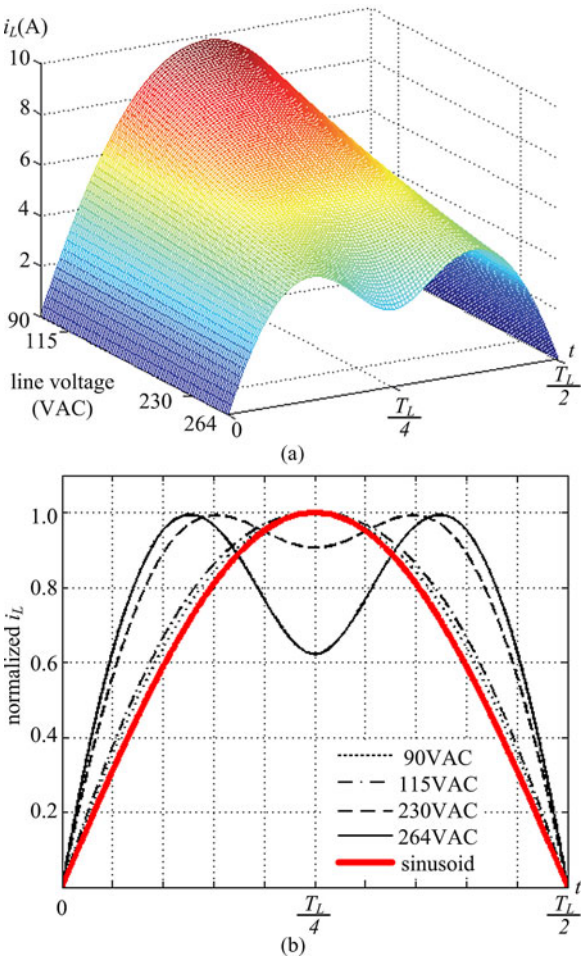


Fig. 4. (a) $i_{\rm pk}$ curves of variable-duty-cycle-controlled DCM PFC rectifier for various line voltages. (b) Normalized $i_{\rm pk}$ curves compared with the sine wave.

The unknown constant $X$ is derived by considering input power. If $P_{\rm in}$, $P_O$, and $\eta$ are input power, output power, and efficiency of the rectifier system, respectively, i.e., input filter and rectifier, the following can be achieved:

$$P_{\rm in} = \frac{P_O}{\eta} = I_{\rm rms} V_{\rm rms} = \frac{1}{2} V_{\rm pk} X. \tag{8}$$

$I_{\rm rms}$ and $V_{\rm rms}$ in (8) represent rms of line current and line voltage in a half line cycle, respectively. Rearranging and substituting (8) into (7) yields the following:

$$i_{\rm pk}(t) = 2\sqrt{\frac{T_S P_O}{\eta L}}\sqrt{1 - \frac{V_{\rm pk}\sin\omega_L t}{v_O}}\sin\omega_L t. \tag{9}$$

Fig. 4(a) compares various $i_{\rm pk}(t)$ curves in case the variable-duty-cycle-controlled DCM rectifier outputs 400 V and 200 W, assuming that the efficiency of the rectifier system is unity. The maximum inductor current occurs at the midpoint of the half line period when line voltage is lower than 188.6 Vac. When the line voltage is higher than 188.6 Vac, a local minimum forms in the middle of the curve and the maximum current occurs twice in the half line period. Detailed derivation of maximum $i_{\rm pk}(t)$ is discussed in Section III-A. Fig. 4(b) shows the normalized $i_{\rm pk}(t)$ with the pure sinusoid. Low line voltages such as 90 and 115 Vac demonstrate $i_{\rm pk}(t)$ curves, which are slightly changed from the sine wave. On the contrary, curves for high line voltages such as 230 and 264 Vac are highly deviated and show the local minimum in the middle of the half line period. This is because the second square-root term in (9) is not a constant, but a function of $\sin\omega_L t$. The deviation of the term over half line cycle becomes dominant when the line voltage is high, i.e., $V_{\rm pk}/v_O$ is high. Considering that the pure sinusoid is the $i_{\rm pk}$ waveform of the conventional constant-duty-cycle-controlled rectifier, the performance improvement of the proposed control technique may be trivial with low line voltages like 90 or 115 Vac. However, it can be emphasized if the high line voltage such as 230 or 264 Vac is applied.

## III. Rectifier Design With the Proposed Control Technique

Practical implementation of the proposed average current-mode variable-duty-cycle control to boost PFC rectifier is shown in Fig. 5. Loop configuration of the proposed control follows the general two-loop control with the input voltage feedforward. Output of the voltage compensator $G_V$ and the sensed rectified input voltage are multiplied together and compared with the sensed average inductor current. Current compensator $G_C$ output is again compared with the counter value of the pulse width modulation (PWM) generator and provides the gate signals to the power stage.

### A. Inductance Design

A large inductance of $L$ is effective because it decreases the rms current in DCM PFC rectifier. However, the maximum limit of the inductance $L_{\rm crit}$ exists to maintain the DCM operation throughout the line cycle and load variation. Otherwise, the rectifier operation may go into CCM and lose control even though the control loop is designed to be stable. Specifically, the time duration of the third interval $d_3 T_S$ should be considered in the inductance design because the sampling of $v_{Cs}$ and calculation of the next duty cycle is executed in the third interval. Fig. 6 illustrates the shrinkage of $d_3 T_S$ according to the increase of $L$. Assuming the same level of $i_{\rm avg}[k]$, $d_3 T_S$ becomes shorter when $L$ is larger because the slopes of $i_L$ become more gradual.

$L_{\rm crit}$ is derived in the following to properly reset $v_{Cs}$ and obtain sufficient calculation time $T_{\rm cal}$: $d_{3\rm min}$, the minimum duty ratio of the third switching interval, is expressed in (10) by considering (3), (4), (6), and (9)

$$d_{3_{\rm min}} = 1 - (d_1 + d_2) = 1 - \frac{2}{V_{\rm pk}}\sqrt{\frac{L_{\rm crit} P_O}{\eta T_S}} \times \frac{1}{\sqrt{1 - (V_{\rm pk}/v_O)\sin\omega_L t}}. \tag{10}$$

Equation (10) notes that $d_{3\rm min}$ occurs in the middle of the half line cycle, i.e., $\sin\omega_L t = 1$. $d_{3\rm min}$ is plotted as the function of $L_{\rm crit}$ for various line voltages and $P_O$ in Fig. 7, assuming that $T_S$ is 15.385 $\mu$s (reciprocal of 65 kHz) and $\eta$ is a unity. The

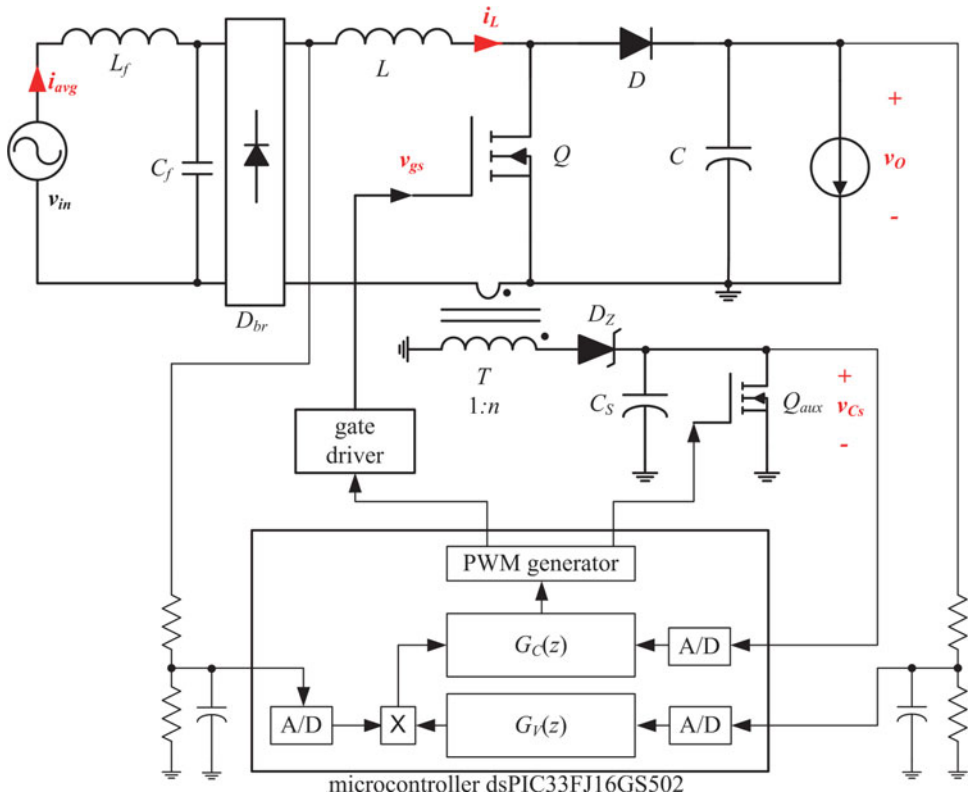


Fig. 5. Implementation of the proposed control technique to boost PFC rectifier.

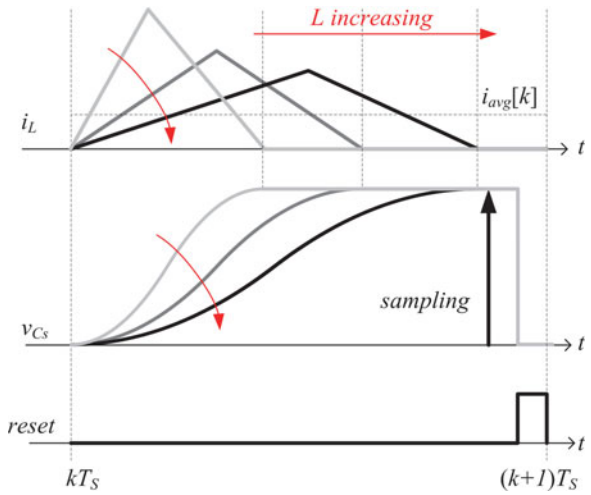


Fig. 6. Decrease of $d_3 T_S$ according to the increase of $L$.

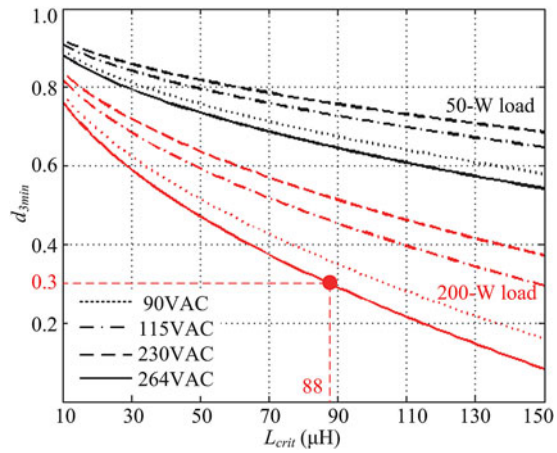


Fig. 7. $d_{3\min}$ as the function of $L$ to determine the critical inductance $L_{\rm crit}$.

worst case for $d_{3\min}$ is high line voltage and full load situation, which is represented by the solid curve at the bottom.

Selection of $d_{3\min}$ affects the design of $L_{\rm crit}$, and consequently, the maximum and the rms inductor currents. The maximum inductor current in a half line period, $I_{\rm pk\_max}$, is derived by differentiating and equating (9)

$$\frac{d}{d\omega_L t} i_{\rm pk}(t) = \sqrt{\frac{T_S P_O}{\eta L}} \frac{(\cos\omega_L t)\,(2-(3V_{\rm pk}/v_O)\sin\omega_L t)}{\sqrt{1-(V_{\rm pk}/v_O)\sin\omega_L t}} = 0. \tag{11}$$

For $0 < t < (T_L/2)$, one obvious solution for (11) is when $\cos\omega_L t = 0$ or $\omega_L t = \pi/2$. The other solutions exist only when $(2/3)(v_O/V_{\rm pk}) < 1$, considering the term in the second parentheses of the numerator in (11). If $v_O$ is 400 V and $(2/3)(v_O/V_{\rm pk}) > 1$, i.e., $V_{\rm rms} < 188.6$ V, (9) has the maximum at $\omega_L t = \pi/4$ and does not have any local minimum. If $V_{\rm rms} > 188.6$ V, (9) has the local minimum at $\omega_L t = \pi/4$ and the maximums occur at $\omega_L t = \sin^{-1}(2/3)(v_O/V_{\rm pk})$. Substituting $\omega_L t = \pi/2$ and $\omega_L t = \sin^{-1}(2/3)(v_O/V_{\rm pk})$in (9) according to the condition of $V_{\rm pk}$, $I_{\rm pk\_max}$ is mathematically expressed

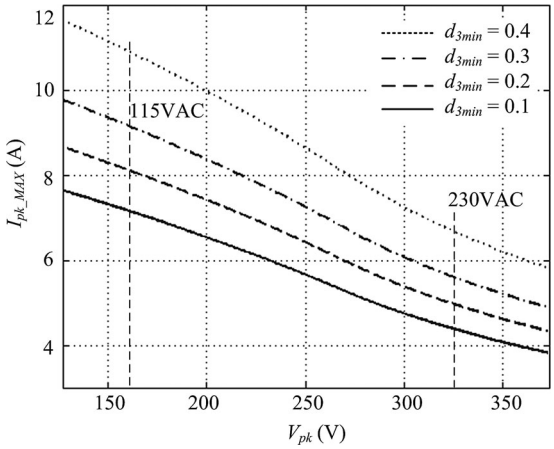


Fig. 8. $I_{\mathrm{pk\_max}}$ versus $V_{\mathrm{pk}}$ for various $d_{3\mathrm{min}}$.

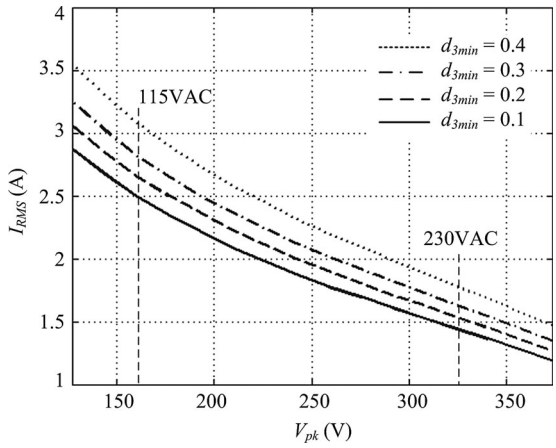


Fig. 9. $I_{\mathrm{rms}}$ versus $V_{\mathrm{pk}}$ for various $d_{3\mathrm{min}}$.

in (12)

$$I_{\mathrm{pk\_max}} = 2\sqrt{\frac{T_S P_O}{\eta L}}\sqrt{1-\frac{V_{\mathrm{pk}}}{v_O}} \quad \left(\text{if } \frac{2}{3}\frac{v_O}{V_{\mathrm{pk}}} > 1\right) \tag{12a}$$

$$I_{\mathrm{pk\_max}} = \frac{4}{3\sqrt{3}}\sqrt{\frac{T_S P_O}{\eta L}}\frac{V_{\mathrm{pk}}}{v_O} \quad \left(\text{if } \frac{2}{3}\frac{v_O}{V_{\mathrm{pk}}} < 1\right). \tag{12b}$$

The rms inductor current in a half line period $I_{\mathrm{rms}}$ should also be considered in $d_{3\mathrm{min}}$ design. $I_{\mathrm{rms}}$ is expressed, as in the following, according to the analysis in [10], assuming that the rectifier efficiency is a unity

$$I_{\mathrm{rms}} = \frac{V_{\mathrm{pk}} T_S}{L}\sqrt{\frac{2}{T_L}\int_0^{T_L/2}\frac{V_O\, d_1(t)^3 \sin^2\omega_L t}{3(V_O - V_{\mathrm{pk}}\sin\omega_L t)}dt} \tag{13}$$

where $d_1(t)$ is given in (14) by combining (3), (6), and (9)

$$d_1(t) = \frac{2}{V_{\mathrm{pk}}}\sqrt{\frac{LP_O}{\eta T_S}}\sqrt{1-\frac{V_{\mathrm{pk}}}{V_O}\sin\omega_L t} \tag{14}$$

The critical inductances for several $d_{3\mathrm{min}}$ such as 0.1, 0.2, 0.3, and 0.4 are determined as 62, 88, 112, and 144 $\mu$H, respectively, from the worst-case curve in Fig. 7, the one for 264 Vac and 200 W. $I_{\mathrm{pk\_max}}$ and $I_{\mathrm{rms}}$ for the selected critical inductances and line voltages are plotted in Figs. 8 and 9, respectively, assuming that the rectifier outputs maximum power 200 W. Figs. 8 and 9, respectively, show that $I_{\mathrm{pk\_max}}$ and $I_{\mathrm{rms}}$ are proportional to $d_{3\mathrm{min}}$. Therefore, selecting large $d_{3\mathrm{min}}$ increases the peak and the rms inductor current. However, the effect of $d_{3\mathrm{min}}$ on $I_{\mathrm{rms}}$ is less considerable than that on $I_{\mathrm{pk\_max}}$. For example, for increase of $d_{3\mathrm{min}}$ from 0.1 to 0.4, $I_{\mathrm{rms}}$ rises by 0.33 A, while $I_{\mathrm{pk\_max}}$ is increased by 2.4 A in 230 Vac operation.

In this paper, $T_{\mathrm{cal}}$ requires approximately 4 $\mu$s to properly calculate and update the duty cycle, which spends 26% of the unit switching cycle. With 4% margin, $d_{3\mathrm{min}}$ is set to be 0.3 and $L_{\mathrm{crit}}$ is determined as 88 $\mu$H, as indicated in Fig. 7. Fig. 10 shows the variation of $d_3$ throughout the half line cycle with the resultant $L$ when full load is applied. In correspondence with the curves in Fig. 7, 264 Vac curve demonstrates the smallest $d_{3\mathrm{min}}$ on the middle of the line cycle, followed by 90, 115, and 230 Vac curves by the ascending order of $d_{3\mathrm{min}}$.

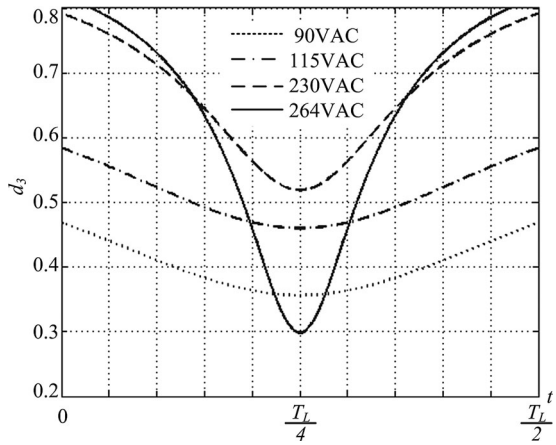


Fig. 10. Variation of $d_3$ within a half line cycle when $L$ is 88 $\mu$H.

### B. Sensing Capacitance and Current Sensing Gain

Sensing capacitance in the average sensing circuit $C_S$ is directly related to the performance of the proposed control technique. The range of $C_S$ is limited by practical reasons. Small $C_S$ may not be appropriate because $v_{Cs}$ may exceed the maximum input voltage of the microcontroller. Large $C_S$ is either not feasible because $v_{Cs}$ may not be reset correctly and the A/D conversion resolution for $v_{Cs}$ may become insufficient. The capacitance is recommended to be within the range from a few tens to a few hundreds of nanofarads.

The minimum boundary of $C_S$ is not dependent on the inductance $L$, but on the average inductor current in a unit switching cycle. One can notice from Fig. 6 that $v_{Cs}$ at the sampling instant is constant though $L$ changes. The boundary is determined by considering the maximum average inductor current in a half line cycle $I_{\mathrm{avg\_max}}$ and the maximum input voltage of the microcontroller $V_{Cs\_\mathrm{max}}$ as expressed in the following:

$$\frac{T_S}{nC_S} I_{\mathrm{avg\_max}} < V_{Cs\_\mathrm{max}}. \tag{15}$$

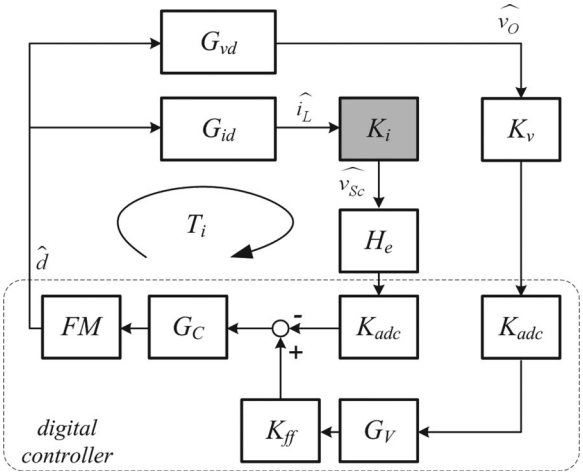


Fig. 11. Small-signal diagram of the proposed control technique.

If power factor of the rectifier is a unity and the waveform $i_{\rm avg}(t)$ is sinusoidal, $I_{\rm avg\_max}$ and $I_{\rm rms}$ have the relationship shown in the following:

$$I_{\rm rms} = \frac{1}{\sqrt{2}} I_{\rm avg\_max} \tag{16}$$

and substituting (16) into (8) achieves the following:

$$I_{\rm avg\_max} = \frac{\sqrt{2} P_O}{\eta V_{\rm rms\_min}} \tag{17}$$

where $V_{\rm rms\_min}$ in (12) is the minimum rms line input voltage. From (15) and (17), the minimum $C_S$ can be defined as follows:

$$C_S > \frac{\sqrt{2} T_S P_O}{n \eta V_{Cs\_max} V_{\rm rms\_min}}. \tag{18}$$

In this paper, the minimum $C_S$ is 293 nF by considering $T_S$, $n$, $P_O$, $V_{\rm Cs\_max}$, $\eta$, and minimum line voltage as 15.385 $\mu$s, 50, 200 W, 3.3 V, a unity, and 90 Vac, respectively.

The current sensing gain of the average sensing circuit is constant and does not change in the frequency domain. Though the proposed sensing circuit integrates the inductor current, the integrating operation does not continue over consecutive switching cycles. Thus, in contrast to standard analog integrators, the sensing circuit does not have any frequency-dependent dynamics such as analog integrators. The effect of the average sensing circuit on the small-signal modeling appears as the fixed gain $K_i$, which is the shaded box in Fig. 11. $K_i$ is defined to be $T_S/nC_S$ as the coefficient of $i_{\rm avg}[k]$ in (2).

### C. Control Loop Implementation

Control loops are realized by the algorithm programmed in the microcontroller Microchip dsPIC33FJ16GS502. Current loop gain $T_i$ is defined as in Fig. 11 and the following:

$$T_i = G_{\rm id} K_i H_e K_{\rm adc} G_C {\rm FM} \tag{19}$$

where $G_{\rm id}$ is open-loop control-to-inductor current transfer function $\widehat{i_L}/\hat{d}$. $H_e$, $K_{\rm adc}$, $G_C$, and FM are sampling effect, internal A/D conversion gain, current compensator gain, and PWM modulator gain of the digital controller, respectively. $T_i$ is similar to the characteristic of the conventional CCM average current-mode-controlled converter [21], [22].

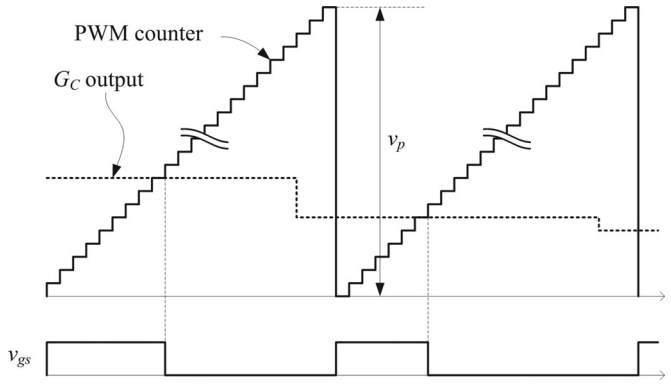


Fig. 12. Current compensator output and PWM counter to derive the modulator gain FM.

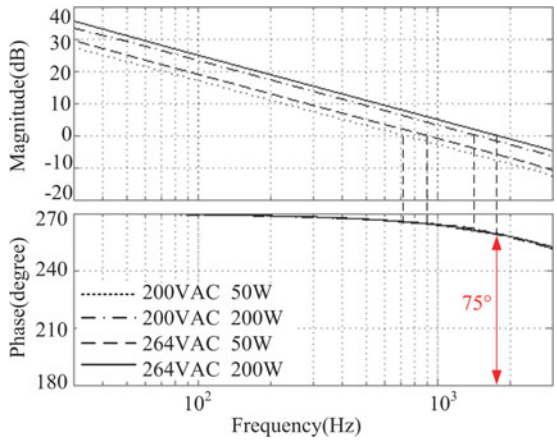


Fig. 13. Bode plots of the current control loop $T_i$ for 200–264 Vac line voltage.

A/D conversion gain and PWM modulator gain are dependent on the characteristic of the microcontroller. By the feature of the internal A/D converter and conversion algorithm of dsPIC33FJ16GS502, $K_{\rm adc}$ is defined as follows:

$$K_{\rm adc} = \frac{1}{V_{Cs\_max}} = 0.303. \tag{20}$$

PWM modulator gain is only dependent on the maximum value of the counter in PWM generator in microcontroller. In the analog average current-mode control, the modulator gain is the complicated function of switching frequency, current compensator, modulator ramp slope, and sensed inductor current slope [23]. In the digital control, however, FM is simply a reciprocal of $v_p$ shown in Fig. 12 because the output of $G_C$ does not fluctuate when it is compared with the PWM counter. The unit step of the counter is set by the PWM clock signal as 1.04 ns and 14 793 steps are required to realize 65-kHz switching frequency. FM is determined by the following based on Q-15 data format

$${\rm FM} = \frac{1}{14793/(2^{15}-1)} = 2.215. \tag{21}$$

$G_{\rm id}$, which can be derived from the averaged circuit model [24], [25], shows flat gain up to half of the switching frequency.

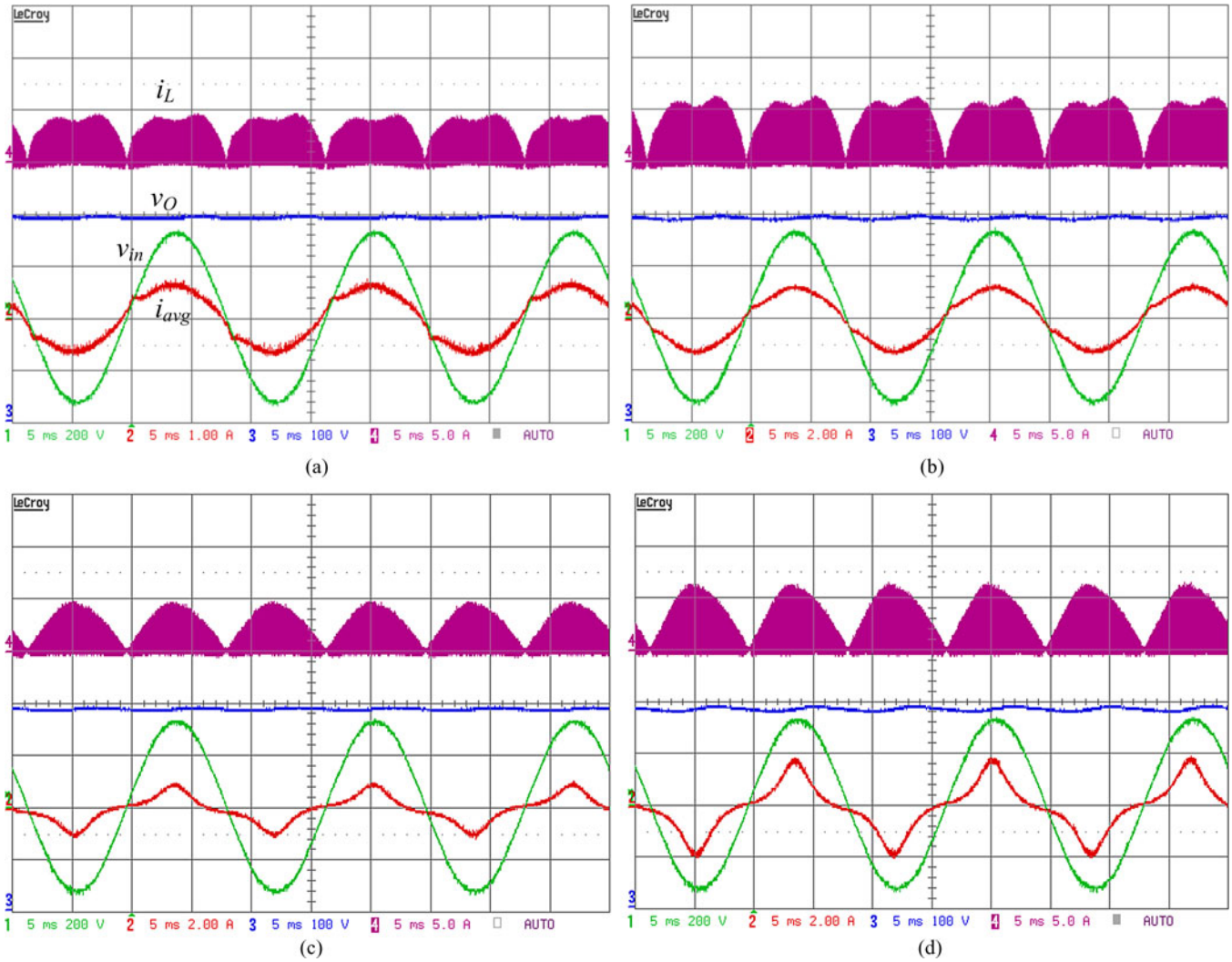


Fig. 14. Steady-state waveforms of the proposed and conventional control methods when line voltage is 230 Vac ($i_L$ 5 A/div). (a) Proposed control with 50% load ($i_{\rm avg}$ 1 A/div). (b) Proposed control with 100% load ($i_{\rm avg}$ 2 A/div). (c) Conventional control with 50% load ($i_{\rm avg}$ 2 A/div). (d) Conventional control with 100% load ($i_{\rm avg}$ 2 A/div).

Current compensator $G_C$ is first designed in $s$ domain to have an integrator with single pole to attenuate the HF noise, as shown in the following:

$$G_C(s) = \frac{\omega_i}{s}\frac{1}{1+(s/\omega_p)}. \tag{22}$$

$G_C(s)$ is interpreted into $z$ domain with zero-order-hold discretization method with the sampling frequency 65 kHz. Resultant $G_C(z)$ is shown in the following:

$$G_C(z) = \frac{a_0 + a_1 z^{-1}}{1 + b_1 z^{-1} + b_2 z^{-2}}. \tag{23}$$

Integrator gain $\omega_i$ and single pole $\omega_p$ in (22) are determined to set the bandwidth and phase margin of $T_i$ to 1 kHz and 75° for universal line voltage and entire load range. For example, $\omega_i$ and $\omega_p$ are 143 Hz and 20 kHz, respectively, in $s$ domain, and the corresponding $a_0$, $a_1$, $b_1$, and $b_2$ in (23) are 0.007772, 0.004123, −1.145, and 0.1447, respectively, for 200–264 Vac line voltage. Resultant $T_i$ curves are shown in Fig. 13.

As the voltage loop compensation, $G_V$ is designed through the similar steps of $G_C$ design. The rectified input voltage and the output voltage are sensed through the resistive voltage divider shown in Fig. 5. Their sampling instant and A/D conversion gain of $v_O$ in voltage loop are the same as those of $v_{Cs}$ in current loop. Capacitors in the resistive dividers are for noise reduction and sufficiently small not to affect the dynamic characteristics of the control loops. In Fig. 11, $K_v$ and $K_{\rm ff}$ in the voltage loop represent the divider gain of the output voltage and the feedforward gain of the input voltage, respectively. $G_V$ is designed to let the voltage loop $T_v$ have 10-Hz bandwidth and 90° phase margin to attenuate the half-of-line-period ripple.

The calculation procedure for loop compensation algorithm contains only two vector inner products for each loop and single multiplying operation for sensed input voltage and voltage compensator output. It requires the same calculation burden with conventional digitally controlled CCM PFC rectifier. There is no additional square root, multiplying, or dividing operation, which spends a lot of the resources of the microcontroller.

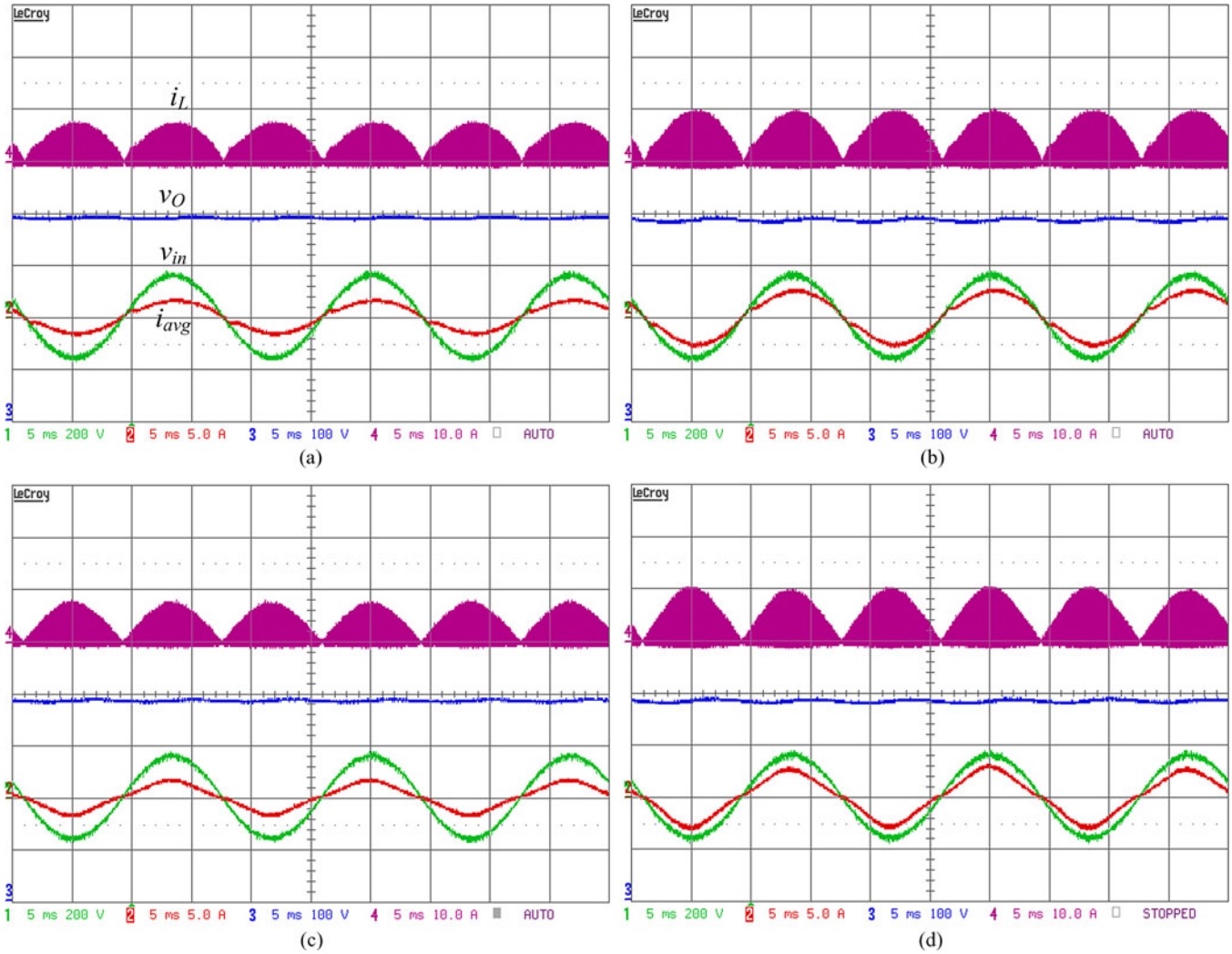


Fig. 15. Steady-state waveforms of the proposed and conventional control methods when line voltage is 115 Vac ($i_L$ 10 A/div, $i_{\rm avg}$ 5 A/div). (a) Proposed control with 50% load. (b) Proposed control with 100% load. (c) Conventional control with 50% load. (d) Conventional control with 100% load.

## IV. Experimental Results

The proposed current control technique is verified by a 200-W laboratory prototype, as shown in Fig. 5. $v_O$ is regulated to be 400 V with the universal line input voltage range and the load range of 50–200 W. Circuit components and parameters that are not mentioned in previous sections are stated in the following.

1) $L_f$: 250 $\mu$H.
2) $C_f$: 1 $\mu$F.
3) $D_{br}$: D25XB60.
4) $L$: 70 $\mu$H.
5) $Q$: STW20NM50.
6) $D$: FSF10A60.
7) $C$: 220 $\mu$F.
8) $D_Z$: 1N4744.
9) $C_S$: 660 nF.
10) $Q_{\rm aux}$: FDD8770.
11) Resistive input voltage sensing gain: 0.0089.

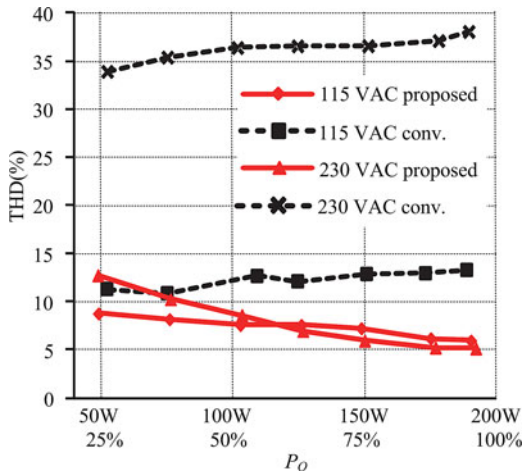


Fig. 16. THD comparison between the proposed and the conventional constant-duty-cycle control.

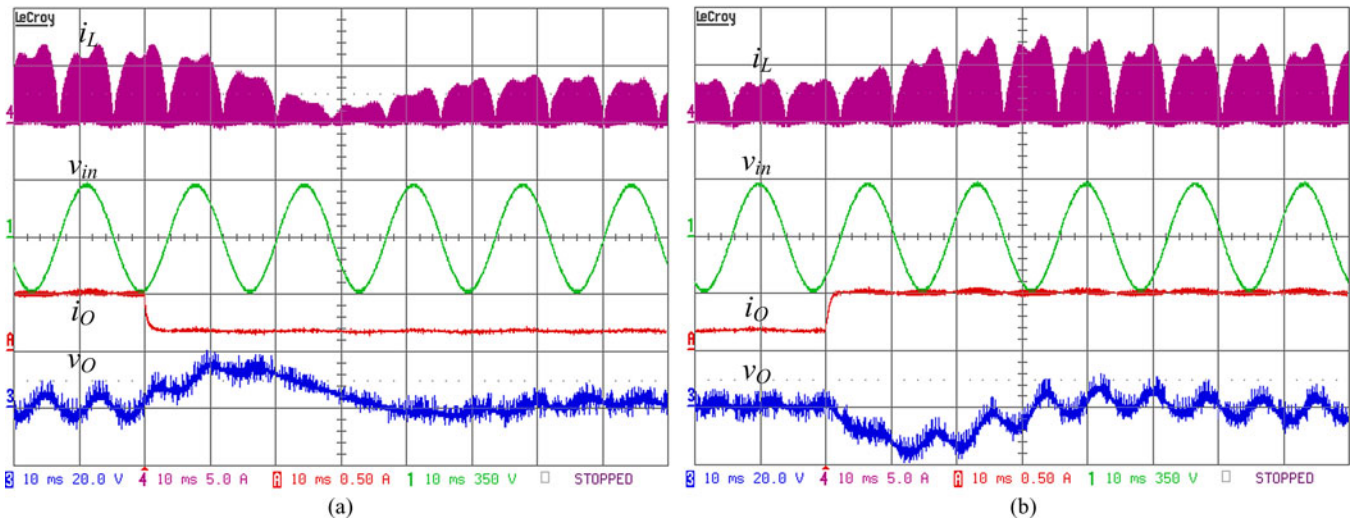


Fig. 17. Operation of the proposed control technique in load transition when line voltage is 230 Vac ($v_O$ ac coupled, 10 V/div). (a) When the load steps from 25% to 100%. (b) When the load steps from 100% to 25%.

12) Resistive output voltage sensing gain: 0.0025.
13) Switching frequency: 65 kHz.
14) Gate driver: TC4420.
15) Line frequency: 60 Hz.

It should be noted that the smaller sensing capacitor $C_S$ is preferred considering the efficiency of the rectifier. In case the line voltage is specified as high range, such as 200–264 Vac, $C_S$ smaller than 660 nF should be selected.

Fig. 14 illustrates the current waveforms in steady state when the load is 100 W, and 200 W when line voltage is 230 Vac. As shown in the Fig. 14(a) and (b), the line current of the proposed control follows the sinusoidal shape, as analyzed in Section II, and the variable-duty-cycle-controlled inductor current demonstrates the local minimum in the middle of the half line period. The reason the inductor current shape in a half line cycle is not symmetrical is that the output of the voltage compensator $G_V$ is not fixed. However, the effect of the asymmetry on the current distortion is negligible. For comparison, Fig. 14(c) and (d) shows the waveforms of the constant-duty-cycle-controlled DCM PFC. The inductor current looks like a sinusoid, but the line current is highly distorted in the middle of the half line period. The same comparison in case the line voltage is 115 Vac is also shown in Fig. 15. In Fig. 15, the proposed control method still shows smaller current distortion than constant-duty-cycle control. The inductor currents of the two control method seem to have similar waveform with each other, but the filtered line current waveforms demonstrate different distortion.

Total harmonic distortion (THD) measurement results for various loads and rms line voltages are shown in Fig. 16. All the data are collected by Yokogawa WT210 harmonics measurement functions. The proposed control shows smaller THD than the conventional constant-duty-cycle control. According to the power increase, the proposed control further decreases the THD, while constant-duty-cycle control increases it. The impact on THD improvement between the control methods is larger in 230 Vac than in 115 Vac, as analyzed in Section II.

Fig. 17 shows the operation of the proposed control when the load steps from 100% to 25% and vice versa when 230 Vac is applied. The proposed control shapes the inductor current in the transient operation as well. From the ac-coupled waveform of $v_O$, the overshoot and undershoot do not exceed 10 V.

## V. Conclusion

A digital average current control method for DCM PFC rectifier to achieve low current distortion has been proposed. The main feature of the proposed control method is that the average inductor current is directly sensed to eliminate additional calculation in the microcontroller. The control method achieves smaller current distortion than the conventional constant-duty-cycle control method by employing a conventional sensing circuit. Circuit operation, inductor current shaping, and rectifier design procedure have been analyzed and explained with mathematical expressions. The proposed control technique has been verified and compared with the conventional approach based on the experimental results achieved with a 200 W prototype. Waveforms and measured data have proven the performance improvement of the proposed control method.

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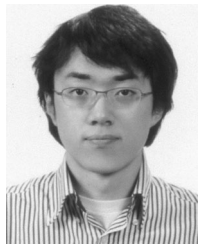

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