Efficiency Optimization in Digitally Controlled Flyback DC–DC Converters Over Wide Ranges of Operating Conditions

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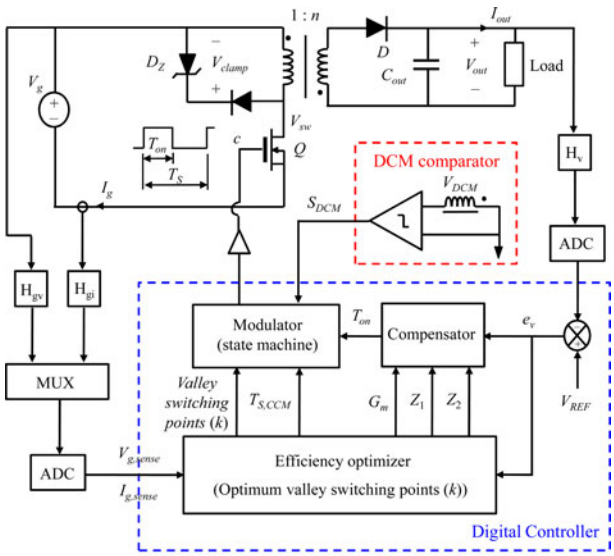
***Abstract*—This paper presents an approach to efficiency optimization in digitally controlled flyback dc–dc converters over wide ranges of operating conditions. Efficiency is characterized and optimized based on power loss modeling and multivariable nonlinear constrained optimization over power-stage and controller parameters. A valley switching technique is adopted to reduce MOSFET turn-on switching loss in discontinuous conduction mode. An optimization procedure is formulated to minimize power loss weighted over a range of operating points, under a cost constraint. A lookup table-based digital controller is applied to achieve on-line efficiency optimization by programming switching frequencies and operating modes based on the efficiency optimization processes. The proposed on-line efficiency optimization approach is verified by experimental results on a low cost 65 W flyback dc–dc prototype.**

***Index Terms*—Digital control, flyback converter, frequency hopping, lookup table, on-line efficiency optimization, valley switching.**

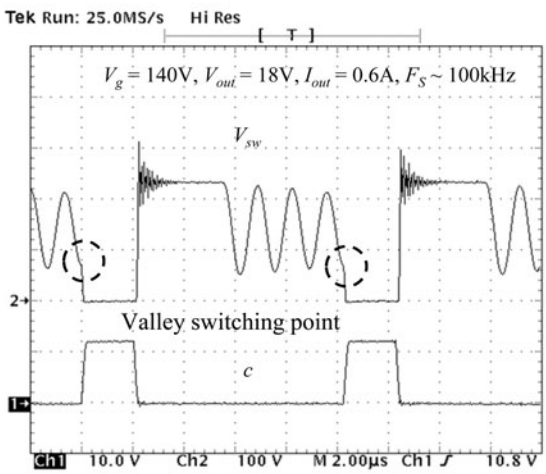
I. Introduction

THE basic flyback power converter shown in Fig. 1(a) is widely adopted in low power applications that require transformer isolation, typically up to about 100 W, because of its simplicity and low cost. Also, high efficiency over wide ranges of operating conditions has become increasingly important in order to respond to the demands of energy efficient programs and initiatives.

One approach to achieving this objective is a quasi-resonant (QR) control with valley switching, which offers decreased switching losses compared to constant-frequency discontinuous-conduction (DCM) or continuous-conduction mode (CCM) operation [1]–[4]. When the flyback converter operates in DCM, ringing due to the resonance between the magnetizing inductance L_M and the switching-node capacitance $C_{\rm sw}$, is observed when the switch Q and the output diode D are both OFF. The valley switching technique forces the switch to turn ON at the minimum switching-node voltage $V_{\rm sw}$. An example of valley switching is shown in Fig. 1(b).



(a)



(b)

Fig. 1. (a) Conventional flyback dc–dc converter. (b) Example of control with valley switching.

More advanced flyback topologies have been proposed to improve efficiency. For example, the active-clamp flyback converter features soft switching and recycling of the

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energy stored in the leakage inductance L_{lk} [5]–[8]. Another approach is to replace the diode with a synchronous rectifier, thus reducing the dominant conduction loss in relatively low output voltage applications [9]–[11]. However, these modifications come at increased cost. One of the objectives in this paper is to examine efficiency optimization opportunities subject to cost constraints corresponding to the basic flyback configuration of Fig. 1(a).

A number of switched-mode power supply design optimization approaches have been described in the literature [12]–[17]. The approach proposed in this paper is based on three main ideas: 1) a relatively simple, but sufficiently detailed loss model capable of representing the main loss mechanisms over wide ranges of operating points; 2) an objective function that allows minimization of the power loss weighted over a range of operating points, under a cost constraint; and 3) combined design-time optimization and controller optimization, taking advantage of a digital controller capability to set the operating mode and the switching frequency to the optimum values for any given operating point [18].

In the area of off-line dc–dc converters, such as the flyback converter shown in Fig. 1(a), "green mode" analog controllers featuring multimode operation have been introduced [19]–[21]. Such approaches are often tied to specific power converter topologies or assume certain power stage parameters. In the area of digital dc–dc control, approaches have been proposed to achieve on-line efficiency optimization, e.g., by adjusting deadtimes [22]–[24], by multimode operation [23], [25], by adjusting the supply voltage for compensation of the propagation delay variations due to the variations of intrinsic parameter and operating condition [26], or by a real-time prediction of the load current [27]. Such on-line efficiency optimization techniques are attractive but require more complex controllers and may not perform well in the presence of dynamically changing operating conditions.

In addition to the concurrent optimization over power-stage-design parameters and controller parameters [18], this paper proposes a digital control approach using a relatively simple lookup table to achieve on-line efficiency optimization as shown in Fig. 1(a) [28]. This paper is organized as follows. Section II summarizes power loss modeling, together with a model validation by comparisons with experimental results. Section III discusses details of the optimization procedure. Section IV describes how the digital controller is implemented and programmed based on the optimization results. Section V presents analytical and experimental results of static performance, while Section VI addresses dynamic operation of the controller, including demonstrations of smooth mode transitions and consistent transient responses over various operating conditions. Conclusions are presented in Section VII.

II. Power Loss Modeling

Sufficiently detailed loss models are necessary in order to perform efficiency optimization over design and controller parameters. The approaches to loss modeling adopted in this paper, which are based on well known or published results, are briefly summarized in this section, together with experimental validation results. A constant operating temperature of 60 °C is assumed in all models.

A. Conduction Losses

Conduction losses are modeled on approximate converter waveforms from an ideal-switch converter model. The transistor Q on resistance $R_{\rm on}$, as well as the diode D forward voltage drop V_F, and series resistance R_D are taken from the component data sheets.

B. Switching Loss Due to Switching-Node Capacitance

At the end of each switching period, the energy stored in the nonlinear switching-node capacitance is dissipated when the switch is turned ON. Assuming that the controller employs valley switching in DCM, the switching-node voltage $V_{\rm sw}$ is estimated as follows in DCM:

$$V_{\rm sw} = V_g - \frac{V_{\rm out} + V_F}{n} e^{-\alpha N_{\rm cycle} T_{\rm OSC}} \tag{1}$$

$$\alpha = \frac{R_r}{2L_M} \tag{2}$$

$$N_{\rm cycle} = \text{round}\left(\frac{D_3 T_S}{T_{\rm OSC}}\right) + 0.5 \tag{3}$$

where $T_{\rm OSC}$ is the oscillation period of the ringing, R_r is the damping resistance, T_S is the switching period, and $D_3 T_S$ is the length of the subinterval when both the MOSFET Q and the output diode are OFF. In CCM

$$V_{\rm sw} = V_g + \frac{V_{\rm out} + V_F}{n}. \tag{4}$$

The switching-node capacitance consists of a nonlinear drain-to-source capacitance of the MOSFET, and a winding capacitance of the transformer. The loss is modeled as

$$P_{\rm sw} = \frac{1}{2} C_w V_{\rm sw}^2 F_S + E(V_{\rm sw}) F_S \tag{5}$$

where C_w is the winding capacitance, $F_S = 1/T_S$ is the converter switching frequency, and $E(V_{\rm sw})$ is the energy stored in the MOSFET drain-to-source capacitance as a function of the switching-node voltage, which is available from the MOSFET data sheet. The winding capacitance is calculated by measuring the ringing period.

C. Switching Loss Due to Leakage Inductance

The leakage inductance is analytically modeled from the transformer winding structure as described in [29]. The loss associated with the dissipative snubber shown in Fig. 1(a) is modeled as

$$P_{\rm clamp} = \frac{1}{2} L_{\rm lk} I_{Q,\rm peak}^2 \frac{n V_{\rm clamp}}{n V_{\rm clamp} - V_{\rm out}} F_S \tag{6}$$

where $V_{\rm clamp}$ is the snubber Zener voltage and $I_{Q,\rm peak}$ is the peak MOSFET current.

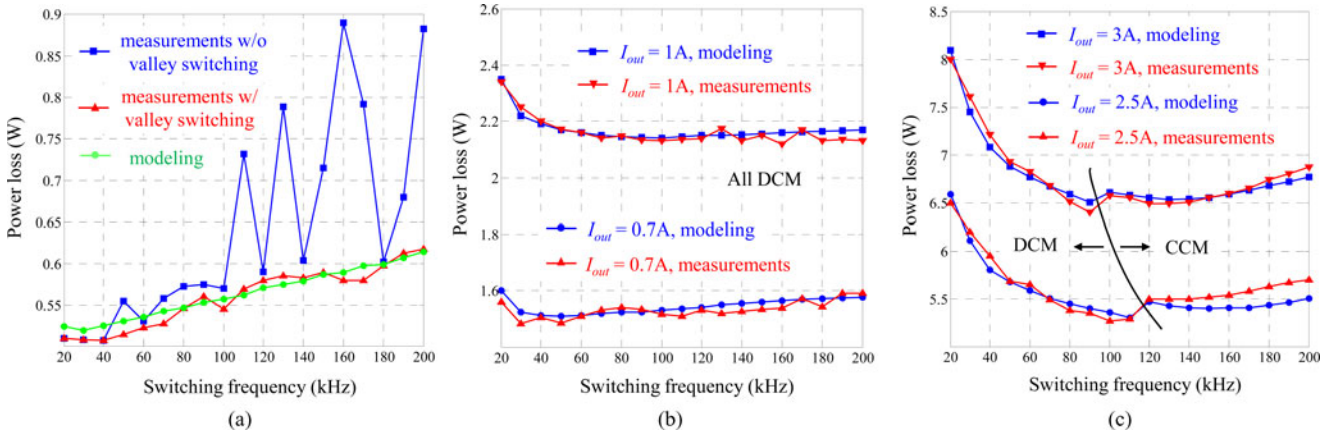

Fig. 2. Power loss characterization at light, intermediate, and heavy loads. Comparison of results based on loss modeling and based on experiments. (a) Power loss as a function of frequency at $V_g = 130$ V and $I_{\rm out} = 0.25$ A. (b) Power loss as a function of frequency at $V_g = 200$ V and $I_{\rm out} = 0.7$ A and $I_{\rm out} = 1$ A. (c) Power loss as a function of frequency at $V_g = 200$ V and $I_{\rm out} = 2.5$ A and $I_{\rm out} = 3$ A.

D. Transformer Proximity Loss and Core Loss

The 1-D model of the proximity loss is constructed using the approach presented in [30]. The magnetomotive force (MMF) distribution in each transformer winding layer is found in time domain and decomposed into sinusoidal harmonics by Fourier series analysis. The power loss density is then computed for each harmonic, and power loss densities over all harmonics are summed to find the proximity loss in each layer.

The air-gap of the transformer may have a significant influence on the AC winding resistance due to the fringing effects [31], [32]. However, these effects have not been included because of difficulties in incorporating necessary 2-D or 3-D finite element analysis in the optimization process.

The core losses are calculated using the improved generalized Steinmetz equation, which allows for arbitrary (nonsinusoidal) waveforms [33].

E. Comparisons With Experimental Efficiency Characterization

The experimental setup consists of a 65 W flyback dc–dc converter power stage interfaced to a Virtex IV FPGA development board used as a digital controller, a programmable dc power supply, an electronic dc load, and efficiency characterization routines implemented in MATLAB on a PC.

The parameters of the power stage prototype are $V_g = 130$ V $\sim$ 300 V, $V_{\rm out} = 18$ V, $I_{\rm out} = 50$ mA $\sim$ 3 A, $n = 0.22$, $L_M = 270$ μH, $L_{lk} = 5.2$ μH, $C_{\rm out} = 4500$ μF, $V_{\rm clamp} = 150$ V, and $H_v = 0.07$. For the transformer, a PQ 26/25 core of PC44 power ferrite (TDK) is used and the primary side is wound with $N_1 = 32$ turns of 0.5 mm TEX-E wire, while the secondary side has $N_2 = 7$ turns of three parallel AWG24 wires. The 600 V, 11 A MOSFET (Infineon, SPP11N60C3) and 2 $\times$ 10 A, 120 V dual Schottky diode (STMicroelectronics, STPS20120CT) are selected as the switch Q and the output diode D, respectively.

During efficiency characterization, the MATLAB/PC controls the dc power supply and the dc load as well as the switching frequency of the converter, and measures the input and output power. The digital controller regulates the output voltage via switch on-time, and communicates with MATLAB to receive the switching period command and commands to turn ON or OFF the valley switching, and to send regulation status, on-time and DCM/CCM status. Valley switching is implemented using a state-machine in the digital controller, similar to [34]. If valley switching is enabled, the digital controller detects DCM comparator signal $S_{\rm DCM}$ to measure and store the oscillation period of the ringing $T_{\rm OSC}$. After the switching period set from MATLAB expires, the state machine waits for $S_{\rm DCM}$ transition and extends the switch off-time by $T_{\rm OSC}/4$ such that the switch turns ON at the minimum switching-node voltage in DCM.

In order to collect the efficiency data, the switching frequency was swept from 20 to 200 kHz with a 10-kHz step, with or without valley switching at various load currents (50–3 A) and input voltages (130–300 V).

To validate the loss modeling, Fig. 2 shows a comparison of the power losses predicted by the model with the results obtained from the experimental characterization. The loss modeling predicts the total power dissipation within 5% of the measurement results. It should be noted how the valley switching results in significantly decreased power losses as shown in Fig. 2(a), which is desirable for improved efficiency in DCM operation. At light loads, since the switching loss due to the switching-node capacitance is more significant compared to other losses, power losses measured without valley switching are in most cases much larger than those measured with valley switching. At certain switching frequencies [e.g., 60, 100, 120, 140, and 180 kHz, as shown in Fig. 2(a)], the transistor is turned ON very close to the valley switching point even if no active valley switching control is employed, which is why the measured losses with or without valley switching are nearly the same at these switching frequencies. At intermediate loads, the power loss curves are relatively flat over

the entire switching frequency range because the output diode conduction loss and the loss due to the leakage inductance are dominant.

III. Efficiency Optimization in Flyback DC–DC Converters

A. Efficiency Optimization Procedure

A flyback converter design requires many tradeoffs and iterations with a large number of design variables. The first step of the optimization procedure is to determine the external specifications of the converter (e.g., range of operating conditions, $V_{g,i}$ and $I_{\mathrm{out,j}}$) and component limits used as constraints in the optimization. The core size, core material, output capacitor, and output diode are defined as the constraints in this optimization, and are kept the same as in the power stage prototype used for the loss model validation in Section II. Other constraints are defined for the selection of wires in the transformer, magnetizing inductance, and the clamp voltage V_{clamp} in the snubber. Round wires are used for transformer windings and a window area is filled such that copper losses due to the DC resistances are minimized as described in [35]. The magnetizing inductance is determined for the core not to be saturated using

$$L_M I_{Q,\mathrm{peak}} < N_1 B_{\max} A_C \tag{7}$$

where N_1 is the number of turns on the primary side, $B_{\max}$ is the maximum flux density, and A_C is the cross-sectional area of the given core. The maximum possible clamp voltage V_{clamp} is selected based on the voltage rating of the selected MOSFET to minimize the leakage inductance loss given by (6). The interleaved transformer is employed in the optimization process because the leakage inductance can be significantly reduced compared to the noninterleaved transformer [31]. Furthermore, it is assumed that the controller employs valley switching at all DCM operating points.

Fig. 3 shows a flowchart of the optimization procedure, which is divided into two optimization processes. The most inner loop is the switching frequency optimization (i.e., the controller optimization) for a given set of design parameters and for a given set of operating points of interest. In the outer loop (i.e., the design optimization), the variable design parameters include the turns ratio n, the number of turns on the primary side N_1, and the MOSFET Q.

The objective function f is defined as a weighted sum of the converter losses over the set of operating points

$$f = \sum_{i,j} \alpha_{i,j} \frac{P_{\mathrm{loss}}(i,j)}{P_{\mathrm{out}}(i,j)} \tag{8}$$

$$\sum_{i,j} \alpha_{i,j} = 1. \tag{9}$$

Note that the loss $P_{\mathrm{loss}}(i,j)$ at an operating point (i,j) is normalized by the output power at the same operating point and weighted by a factor $\alpha_{i,j}$. The weight factors $\alpha_{i,j}$ determine the importance of efficiency at each operating point. The process employs MATLAB function (fmincon) for multivariable nonlinear constrained optimization. The end results of the optimization procedure are the design parameters of the power stage and the optimum switching frequency to be implemented in the controller. This is particularly well suited for digital controller realization, where the optimum switching frequency can be easily programmed as a function of the operating point.

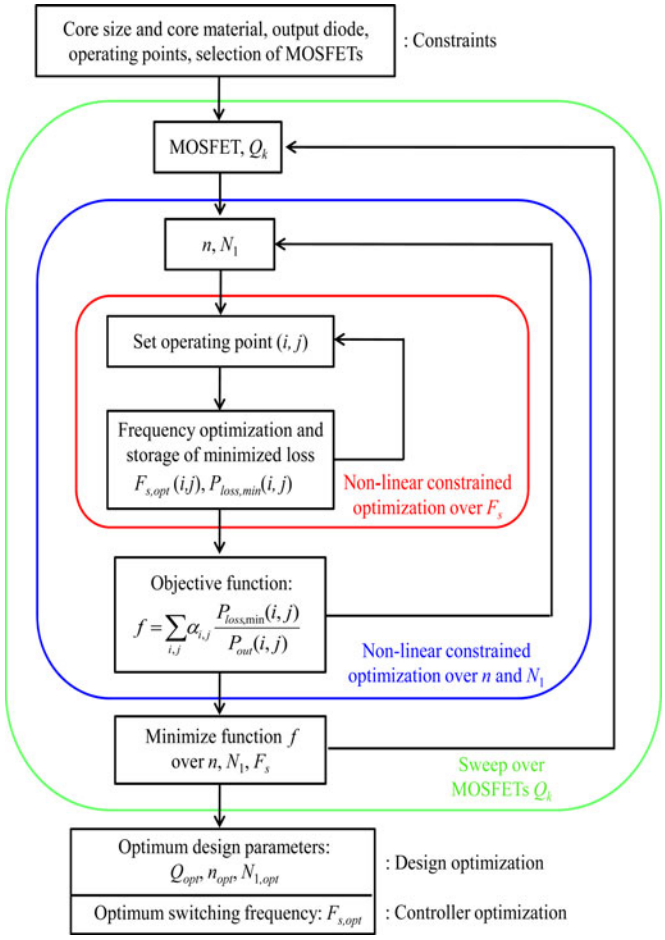

Fig. 3. Block diagram of efficiency optimization procedure. The optimum design parameters (n, N_1 and MOSFET) and optimum switching frequency F_S as functions of operating point (V_g, I_{out}) can be found simultaneously based on experimentally verified power loss models and multivariable nonlinear constrained optimization process.

B. Optimization Results

Fig. 4 shows nine operating points considered and summarizes three cases taken as examples of the optimization procedure. The first case is that nine operating points (combinations of minimum, intermediate, and maximum input voltage and minimum, intermediate, and maximum load current) are selected and equally weighted ($\alpha_{i,j} = 1/9$). The choice of the weights corresponds to a design where efficiency at each operating point is considered equally important. Equivalently, in this case, the total power loss is minimized under the assumption that the time the converter spends at an operating point is inversely proportional to the output power. In the other two optimization examples, only one operating point is considered, $\alpha_{1,1} = 1$, or $\alpha_{3,2} = 1$, respectively.

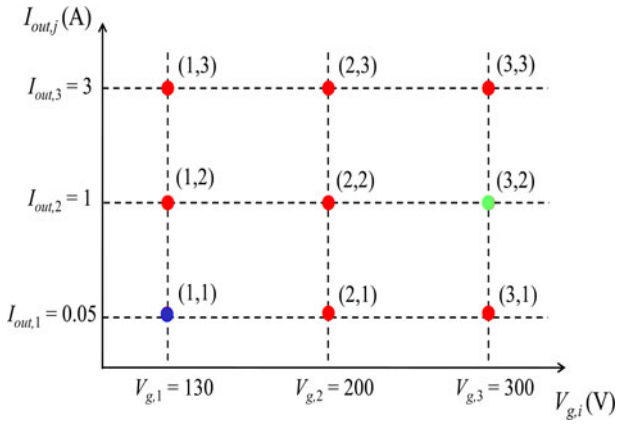

Fig. 4. Three optimization examples. Case 1 ($\alpha_{i,j} = 1/9$), case 2 ($\alpha_{1,1} = 1$), and case 3 ($\alpha_{3,2} = 1$).

TABLE I
RANGES OF DESIGN PARAMETERS

Parameters	Ranges for optimization
MOSFET	600V, 06A (SPP06N60C3, $ 0.836) 600V, 11A (SPP11N60C3, $ 1.383) 800V, 06A (SPP06N80C3, $ 1.310) 800V, 11A (SPP11N80C3, $ 1.860)
n	0.15 ~ 0.50
N_1	20 ~ 50
F_S	20kHz ~ 400kHz

The ranges of design parameters and switching frequency are presented in Table I. Two types of Infineon 600 V MOSFETs and two types of 800 V MOSFETs were considered. The voltage and current ratings of the considered MOSFETs, together with unit costs (Digi-Key Corporation), are shown in Table I. Minimum and maximum boundaries of the turns ratio are 0.15 and 0.50, respectively. The number of turns on the primary side is between 20 and 50. The switching frequency range covers DCM and CCM operations at most of the considered operating points.

Table II shows the optimized power stage design parameters for the three examples. Note that the optimum design parameters are different in the three cases because of the different weight factors. In all cases, the 800 V, 6 A MOSFET was selected, the cost of which is lower compared to the 600 V, 11 A and 800 V, 11 A MOSFETs. The MOSFET having a higher voltage rating results in reduced switching loss because it allows a higher clamp voltage, which decreases the loss (6) associated with the leakage inductance. Furthermore, the MOSFET with a higher on resistance and a smaller output capacitance results in lower losses in these examples. The largest loss reduction effect can be attributed to the reduction in the leakage inductance value by about one-half due to the interleaved transformer windings.

Table III presents maximum efficiencies obtained from the optimization processes, together with a comparison of the optimum switching frequencies. Compared to case 1, cases 2 and 3 result in the best efficiencies at the particular operating points (1, 1) and (3, 2), respectively.

TABLE II
RESULTS OF DESIGN OPTIMIZATION

	Optimum design: case 1 ($\alpha_{i,j} = 1/9$)	Optimum design: case 2 ($\alpha_{1,1} = 1$)	Optimum design: case 3 ($\alpha_{3,2} = 1$)
MOSFET	800V, 6A (SPP06N80C3)	800V, 6A (SPP06N80C3)	800V, 6A (SPP06N80C3)
n	0.20	0.16	0.25
N_1	34	32	36
L_M	360μH	320μH	405μH
L_{lk}	2.6μH	2.4μH	2.7μH
V_{clamp}	400V	400V	400V
Transformer	Interleaved	Interleaved	Interleaved
Wire number in primary side	AWG#23	AWG#22	AWG#23
Wire number in secondary side	AWG#15	AWG#14	AWG#16
Number of layers in primary side	2	2	2
Number of layers in secondary side	1	1	1

Fig. 5 shows efficiency characterizations for the optimization case 1 (equal weights for all nine considered operating points): (a)–(c) comparisons between the optimization and experimental results and (d)–(f) optimum switching frequency as a function of load current with different input voltages. The optimization results predict the efficiency within 0.3% and the switching frequency within 10 kHz under various operating conditions. Efficiencies greater than 92% are achieved under most operating conditions except at very light loads.

Several interesting features of the optimum switching frequencies and operating mode can be deduced from the optimization and efficiency characterization results. The optimum switching frequency at light loads is in the vicinity of the lowest allowed switching frequency (20 kHz) because of dominant switching losses due to the switching-node capacitance. The optimum frequency at heavy and intermediate loads is close to the DCM/CCM boundary (i.e., close to the critical frequency) because the valley switching does not occur in CCM and the switching loss due to the switching-node capacitance increases abruptly as the converter moves from the DCM/CCM boundary to CCM. The optimum frequency drops below the DCM/CCM boundary frequency as the load drops below a value that depends on the input voltage. Another interesting point is that the best efficiency can be achieved in CCM at low input voltages and at heavy loads, as shown in Fig. 5(d), when conduction losses are more dominant.

IV. OPTIMUM CONTROLLER PARAMETERS BASED ON THE PROPOSED EFFICIENCY OPTIMIZATION APPROACH

As described in Section III, the proposed optimization technique results in the optimum power stage design parameters under a cost constraint, and optimum controller parameters: operating modes and switching frequencies. The optimum controller parameters can be programmed in the digital controller, which presents a simpler and more general approach compared to other on-line efficiency optimization approaches. A block

TABLE III
MAXIMUM EFFICIENCIES AND OPTIMUM SWITCHING FREQUENCIES IN THREE CASES AT NINE OPERATING CONDITIONS

	Optimum design: case 1 ($\alpha_{i,j} = 1/9$)		Optimum design: case 2 ($\alpha_{1,1} = 1$)		Optimum design: case 3 ($\alpha_{3,2} = 1$)	
	η_{max} (%)	$F_{s,opt}$ (kHz)	η_{max} (%)	$F_{s,opt}$ (kHz)	η_{max} (%)	$F_{s,opt}$ (kHz)
130V, 50mA (1,1)	91.2	20	91.2	20	91.1	20
130V, 1A (1,2)	93.4	150	93.4	210	93.3	100
130V, 3A (1,3)	92.8	100	92.6	140	92.7	70
200V, 50mA (2,1)	88.6	20	88.7	20	88.4	20
200V, 1A (2,2)	92.6	140	92.7	180	92.7	110
200V, 3A (2,3)	92.7	70	92.5	110	92.6	80
300V, 50mA (3,1)	83.5	20	83.7	20	83.1	20
300V, 1A (3,2)	92.0	30	91.7	40	92.1	30
300V, 3A (3,3)	92.6	90	92.5	140	92.6	60

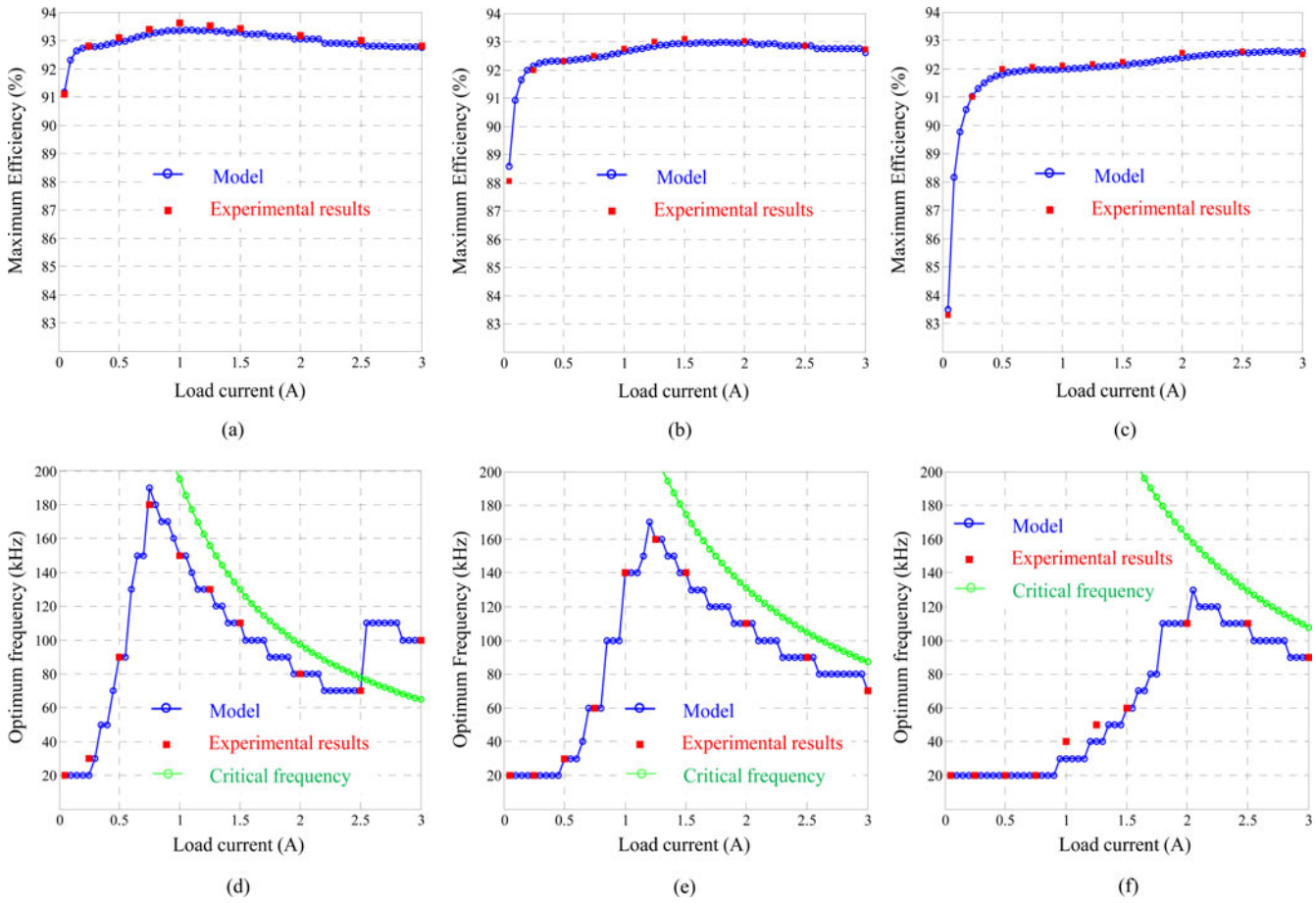

Fig. 5. (a)–(c) Optimum efficiency and (d)–(f) optimum switching frequency as functions of load current for case 1 optimum design with three different input voltages (130, 200, and 300 V). (a) Optimum efficiency as a function of load current at 130 V. (b) Optimum efficiency as a function of load current at 200 V. (c) Optimum efficiency as a function of load current at 300 V. (d) Optimum switching frequency as a function of load current at 130 V. (e) Optimum switching frequency as a function of load current at 200 V. (f) Optimum switching frequency as a function of load current at 300 V.

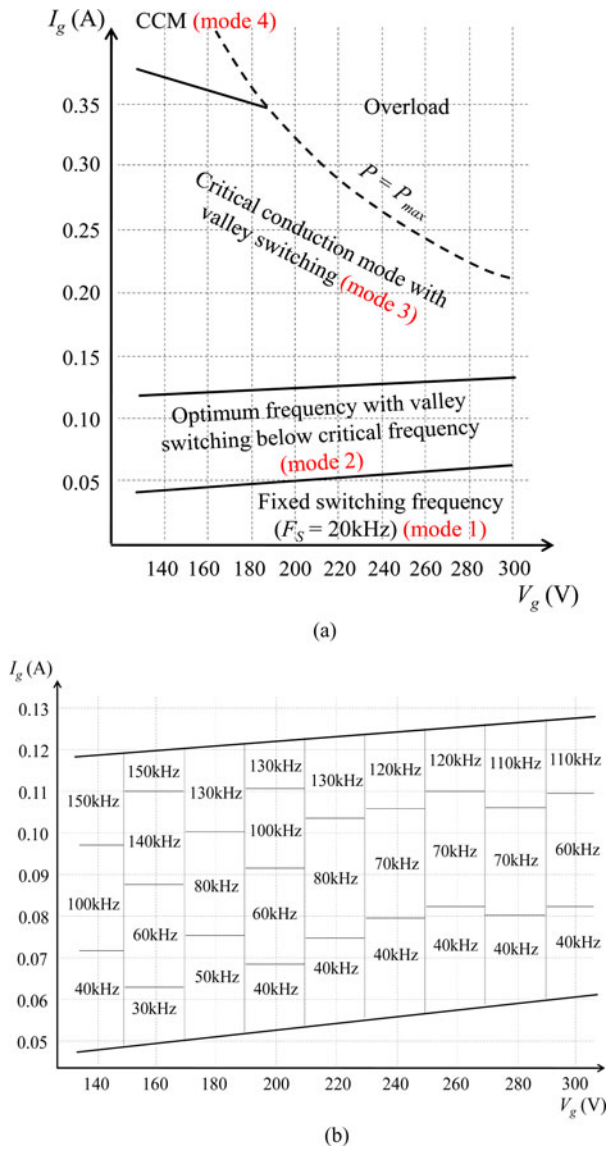

Fig. 6. (a) Optimum operating modes 1–4 as functions of operating conditions (input voltage and input current). (b) Optimum switching frequency stored in the lookup table for mode 2. In contrast to Fig. 5, note that the optimum controller parameters are characterized over a range of input current instead of output current, because the input current is used to detect the operating conditions as shown in Fig. 1(a).

diagram of the controller around a conventional flyback dc–dc converter is shown in Fig. 1(a).

In this paper, the controller is implemented based on the results for optimization case 1 where all operating points are equally weighted. The four operating modes and optimum switching frequencies obtained from the optimization approach are shown as functions of operating conditions (input voltage V_g and input current I_g) in Fig. 6(a) and (b). Note that in Fig. 6, the optimum controller parameters are characterized over a range of input current instead of the output load current, which was indicated as the operating condition in Fig. 5. This is because the input current is used to detect the operating conditions as shown in Fig. 1(a). The near-linear mode boundaries simplify the lookup table in the controller. The modes include operation at a

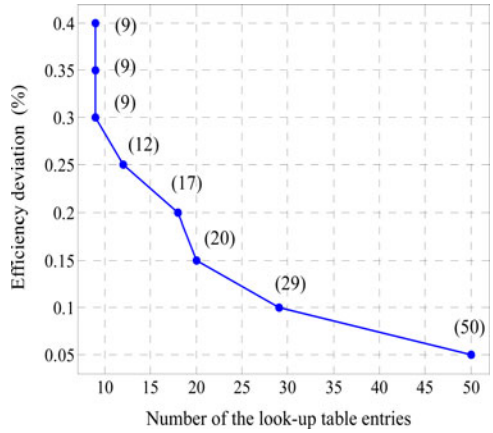

Fig. 7. Efficiency deviation as a function of the number of lookup table entries.

minimum fixed switching frequency (20 kHz) (mode 1), a switching frequency with valley switching (below a critical switching frequency) stored in a lookup table (mode 2), operation close to the critical conduction mode with valley switching (mode 3), and operation in CCM at optimum switching frequencies stored in a lookup table (mode 4). The switching frequency lookup table in mode 2 is designed such that the optimum switching frequency is assigned at the center of each slot and efficiency at the boundaries related to input current is deviated around 0.1% from the optimum efficiency. As shown in Fig. 6(b), the lookup table size is relatively small, having 29 entries. Fig. 7 presents the efficiency deviation as a function of the number of lookup table entries, and indicates that granularity of the lookup table is a tradeoff between the table size and the efficiency loss due to operation away from the optimum switching frequency.

V. Static Operation of the Controller

As commonly observed in other approaches based on valley switching, undesirable frequency hopping can occur in mode 2, where the target switching frequency is set in the lookup table as a function of input voltage and input current. The controller tends to jump between different switching frequencies corresponding to different numbers of DCM oscillation periods. This behavior is undesirable because of increased output voltage ripple and possible audible noise. In this section, it is shown how the frequency hopping problem is caused by two different mechanisms, and solutions are proposed, together with digital controller implementation and corresponding experimental results.

A. Frequency Hopping Mechanisms

For valley switching implementation, the state-machine is programmed such that the switch turns ON at the first valley switching point after the optimum switching period $T_{S,\mathrm{OPT}}$ stored in the lookup table. However, the valley switching point does not pass the boundary of the optimum switching period consistently at certain operating conditions, resulting in the frequency hopping by one DCM oscillation period in mode 2, as shown in Fig. 8.

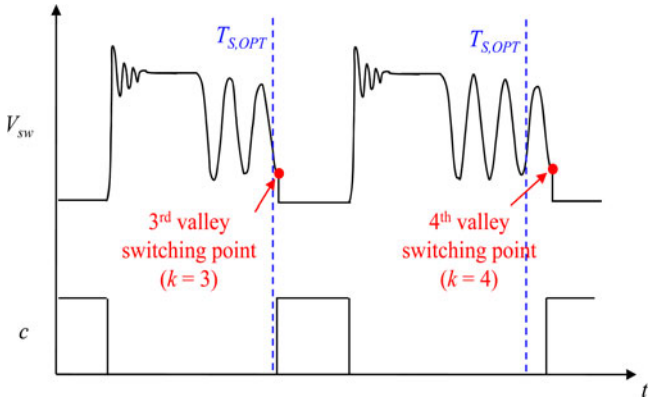

Fig. 8. Example of frequency hopping mechanism 1 (switching-node voltage $V_{\rm sw}$ and control signal (c))—jumping from third valley switching point ($k = 3$) to fourth valley switching point ($k = 4$).

An approach to addressing this frequency hopping mechanism in an analog control scheme has been proposed in [36], using an adaptive blanking time control. In this control scheme, two blanking times ($T_{\rm limit1}$ and $T_{\rm limit2}$) and a window detection time T_C are properly determined and the blanking times are adaptively changed under certain load conditions.

The digital controller allows a relatively simple approach to eliminating the frequency hopping mechanism #1, by storing the optimum valley switching points $k_{\rm opt}$ in the lookup table instead of the optimum switching periods or frequencies. The state-machine can be easily modified such that the valley switching points are counted. The switch turns ON at the valley switching point $k_{\rm opt}$ stored in the lookup table. The optimum valley switching points are obtained from the power loss model used for the efficiency optimization presented in Section III. Another advantage of this approach is that an even smaller lookup table can be obtained compared to the lookup table storing the optimum switching period [see Fig. 6(b)]. Fig. 9 shows the optimum operating modes and the modified lookup table for mode 2 in terms of the optimum valley switching points $k_{\rm opt}$ with measured switching frequencies in each slot. The measured switching frequencies corresponding to the optimum valley switching points are comparable to the optimum switching frequencies obtained from the controller optimization. Valley switching is not employed in mode 1 because at long switching periods the oscillation decays, so valley switching benefits are lost. Instead, in mode 1, the converter operates at a preset minimum switching frequency (20 kHz).

As implied by the lookup table shown in Fig. 9, the valley switching points are abruptly changed at specific values of the input current or the input voltage. Smooth changes of optimum valley switching points depend on the size of each slot in the lookup table. The smaller the size of the slots, the smoother the changes are across the slots. When the input current or the input voltage is at a slot boundary, switching frequency hopping is observed due to jumps in the selected values of $k_{\rm opt}$. To address this frequency hopping mechanism, hysteresis bands are added at the lookup table slot boundaries, and the difference between switch on-times of adjacent slots is added or subtracted

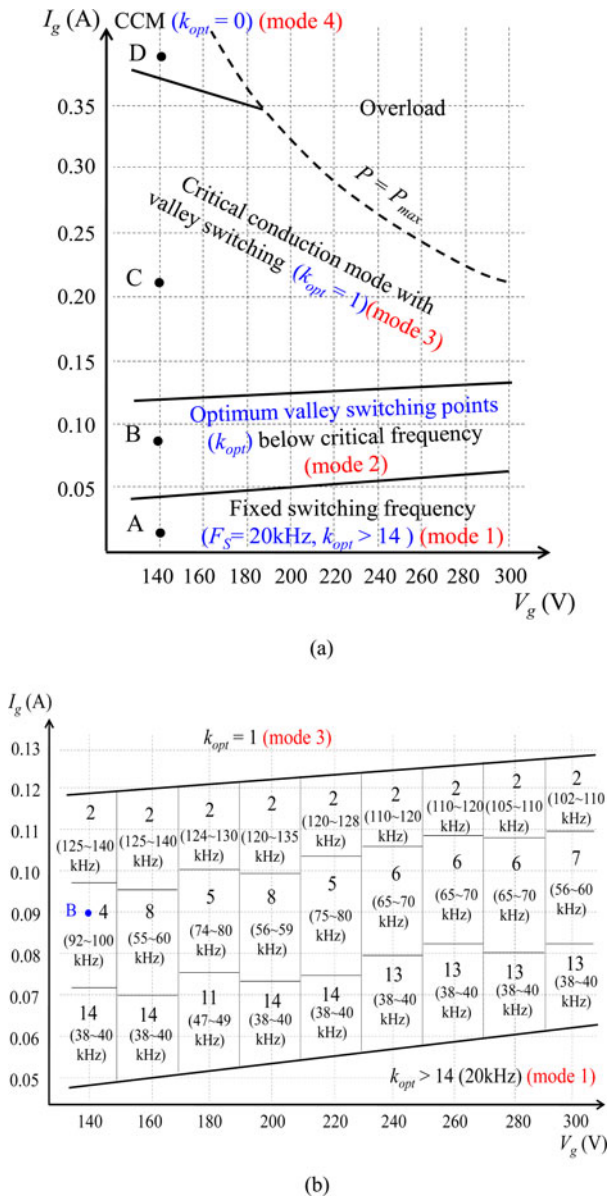

Fig. 9. (a) Optimum operating modes 1–4 as functions of operating conditions (input voltage and input current). (b) Optimum valley switching points $k_{\rm opt}$ stored in the lookup table for mode 2.

depending on the direction of variations in operating conditions I_g and V_g to minimize disturbance caused by the change in $k_{\rm opt}$.

B. Digital Controller Implementation and Experimental Results

As shown in Fig. 1(a), the feedback control loop consists of sensing and A/D conversion of the output voltage, a compensator which computes the switch on-time $T_{\rm on}$ once per switching cycle, and a variable-frequency modulator implemented as a state machine. The input current, along with the input voltage, is sensed once per switching period, using a relatively slow, low-resolution A/D converter. The sensed values are low-pass filtered using an analog *RC* filter to obtain averaged values indicative of the operating point. The bandwidth of the *RC* filter

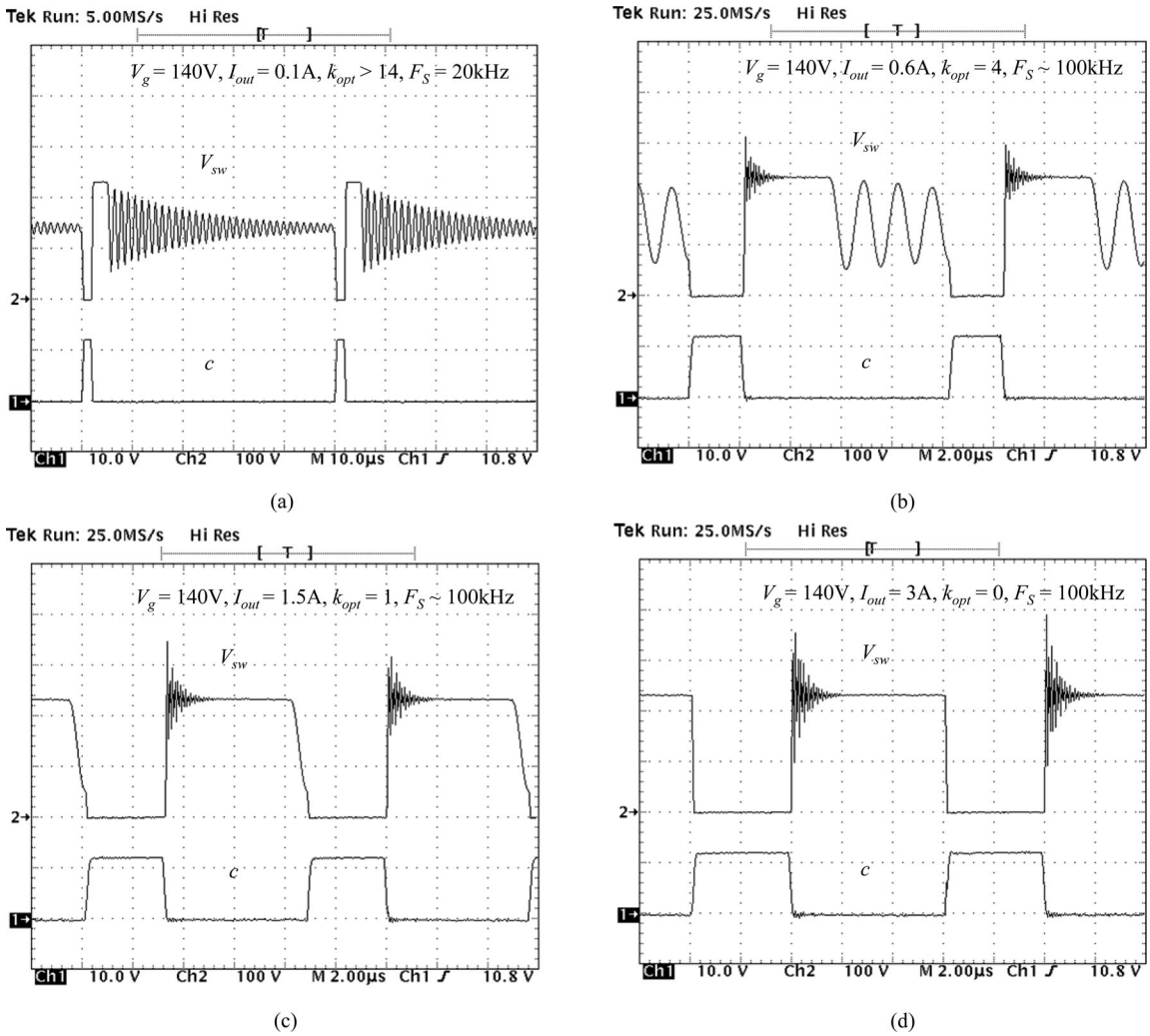

Fig. 10. Steady-state waveforms [switching-node voltage $V_{\rm sw}$ and control signal (c)] measured at points A–D in Fig. 9. (a) Waveforms at point A (mode 1). (b) Waveforms at point B (mode 2). (c) Waveforms at point C (mode 3). (d) Waveforms at point D (mode 4).

is determined as a compromise between speed of efficiency optimization actions and sensitivity of the controller. The efficiency optimizer block includes a lookup table which outputs the optimum valley switching points $k_{\rm opt}$ for modes 1–3, and the optimum switching periods $T_{S,\rm CCM}$ for mode 4. In order to achieve smooth mode transitions and consistent dynamic responses, the compensator parameters (gain G_m, zeros Z_1, Z_2) are also updated by the efficiency optimizer block. The compensator parameters are selected from small-signal modeling analysis over various operating conditions, as discussed further in Section VI.

Fig. 10 presents measured steady-state waveforms of the switching-node voltage $V_{\rm sw}$ and control signal c at the representative operating points A–D in Fig. 9(a) and (b), showing how the controller properly selects the operating modes and the valley switching points $k_{\rm opt}$.

Fig. 11 indicates comparisons of efficiencies as functions of the load current with three different input voltages (140, 220, and 300 V), for three cases. In case 1 efficiency is based on the results of the proposed efficiency optimization using power loss modeling and multivariable nonlinear constrained optimization [18]. Case 2 has an experimentally measured efficiency with the optimized 65 W flyback prototype using the proposed digital controller to achieve on-line efficiency optimization. Case 3 has an experimentally measured efficiency of the same 65 W flyback prototype with the constant switching frequency (100 kHz). As shown in Fig. 11, the model-based optimization and actual experimental results are consistent at all operating points (within 0.3%), except at very light loads due to a loss in the resistive voltage divider used for input voltage sensing, which was not included in the loss model. Efficiency of the optimized prototype with the digital controller (case 2) exceeds 92% at all operating points over approximately 3:1 range of input voltages and 10:1 range of loads. Comparisons of efficiencies between cases 2 and 3 show how the proposed digital controller performs with the converter to achieve on-line efficiency optimization. Compared to the efficiency measured with the optimized prototype having fixed-frequency operation (case 3), the lookup table based

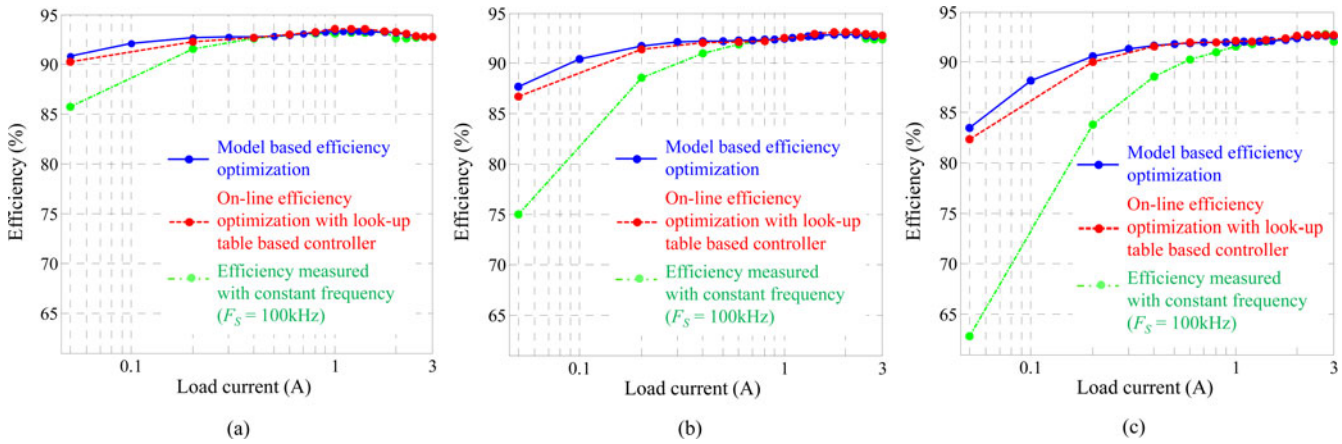

Fig. 11. Comparison of efficiency results at 3 different input voltages (140, 220, and 300 V). (a) $V_g = 140$ V. (b) $V_g = 220$ V. (c) $V_g = 300$ V.

controller improves efficiencies over all operating conditions, especially at very light loads. So, the controller with the lookup table simply facilitates implementation of the concurrent power-stage/controller optimization approach.

VI. Dynamic Operation of the Controller

With a discrete-time compensator having fixed parameters (gain G_m, zeros Z_1 and Z_2), it is not possible to accomplish the target cross-over frequency with adequate phase margin at all operating points. Instead, gain scheduling is applied, with compensator coefficient loaded from the lookup table depending on the operating conditions. An extension (*k*-control) is introduced to improve large-signal transient responses over mode boundaries, and to limit the peak current stress during transients. In this section, small-signal modeling and analysis are presented to determine the gain-scheduled compensator and *k*-control parameters, together with experimental results.

A. *k*-Control Scheme

As described in Section V, the optimum valley switching points $k_{\rm opt}$ stored in the lookup table change abruptly with variations in the sensed input voltage and input current, which may affect large-signal transient responses. When a large step-up load transient is applied to the converter operating at light load and low switching frequency (in mode 1), the compensator increases $T_{\rm on}$ significantly above the steady-state value, which may result in excessive transistor peak currents. To improve large-signal transient responses, a simple extension, named the "*k*-control," is applied. The *k*-control allows for dynamic changes of the valley switching points during transients. Fig. 12 shows how the *k*-control scheme is implemented in the optimizer block. The *k*-control loop can be easily added to the main output voltage control loop with the same gain-scheduled compensator. An increment Δk in the number of the valley switching points k is introduced based on the scaled output voltage error ($e_v = V_{\rm REF} - H_v V_{\rm out}$), $\Delta k = \alpha \cdot e_v$, where $\alpha < 0$. For example, consider again the case when a large step-up load transient is applied

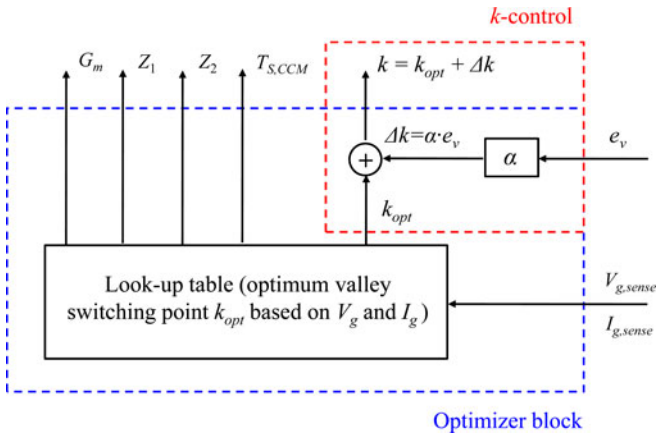

Fig. 12. *k*-Control implementation.

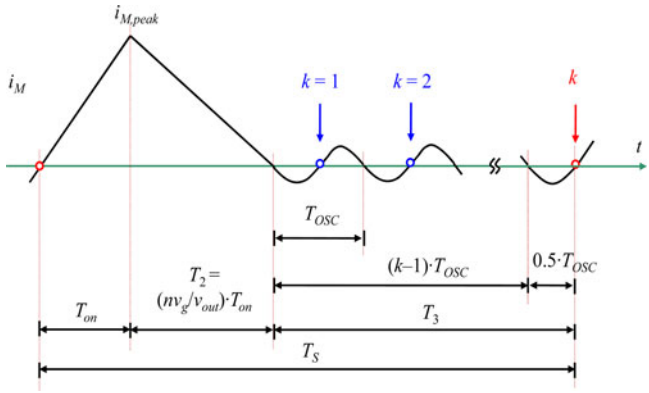

Fig. 13. Magnetizing current i_M with valley switching points k in DCM.

to the converter operating at light load (in mode 1). As the output voltage drops, e_v increases, and $\Delta k < 0$ is added to $k_{\rm opt}$ from the lookup table. As a result, k is reduced and the switching frequency increases, so that the compensator brings the voltage back to regulation faster, while reducing $T_{\rm on}$ and peak current overshoots. In steady state, when the error e_v is 0, $\Delta k = 0$, and $k = k_{\rm opt}$ to achieve on-line efficiency optimization.

TABLE IV
SMALL SIGNAL FLYBACK DCM MODEL PARAMETERS

Input port parameters ($M = V_{out}/V_g$)		Output port parameters ($M = V_{out}/V_g$)	
r_1	$R_e(T_{ON},K)\dfrac{T_{ON}(1+n/M)+(K-0.5)T_{OSC}}{T_{ON}+(K-0.5)T_{OSC}}$	r_2	$M^2R_e(T_{ON},K)\dfrac{T_{ON}(1+n/M)+(K-0.5)T_{OSC}}{T_{ON}+(K-0.5)T_{OSC}}$
g_1	$\dfrac{1}{M^2R_e(T_{ON},K)}\dfrac{nT_{ON}}{T_{ON}(1+n/M)+(K-0.5)T_{OSC}}$	g_2	$\dfrac{2}{MR_e(T_{ON},K)}\dfrac{T_{ON}+(K-0.5)T_{OSC}+nT_{ON}/2M}{T_{ON}+(K-0.5)T_{OSC}+nT_{ON}/M}$
j_1	$\dfrac{V_g}{T_{ON}R_e(T_{ON},K)}\left\{1+\dfrac{(K-0.5)T_{OSC}}{T_{ON}(1+n/M)+(K-0.5)T_{OSC}}\right\}$	j_2	$\dfrac{V_g}{T_{ON}MR_e(T_{ON},K)}\left\{1+\dfrac{(K-0.5)T_{OSC}}{T_{ON}(1+n/M)+(K-0.5)T_{OSC}}\right\}$
k_1	$-\dfrac{1}{R_e(T_{ON},K)}\dfrac{T_{OSC}}{T_{ON}(1+n/M)+(K-0.5)T_{OSC}}$	k_2	$-\dfrac{1}{MR_e(T_{ON},K)}\dfrac{T_{OSC}}{T_{ON}(1+n/M)+(K-0.5)T_{OSC}}$

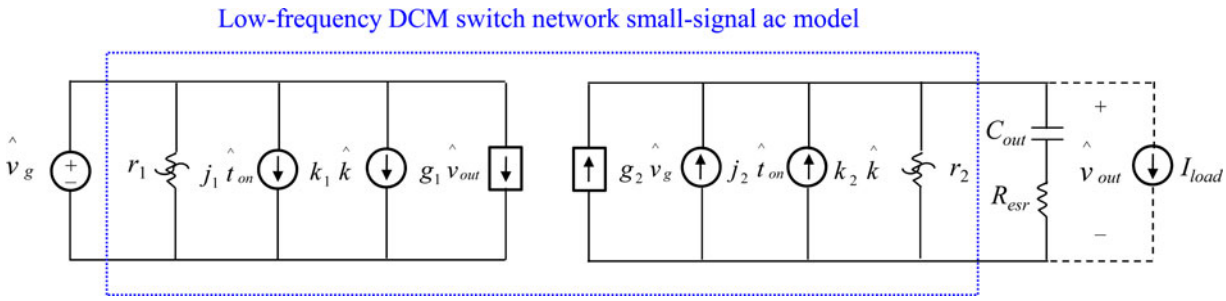

Fig. 14. Small-signal ac model of the flyback dc–dc converter operating in DCM.

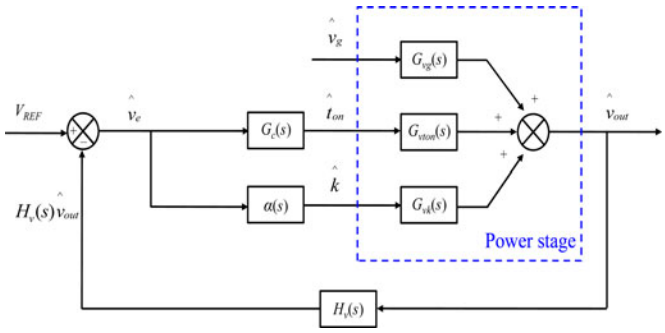

Fig. 15. Block diagram of the small-signal model of the DCM flyback converter with output voltage regulation.

B. Small-Signal Modeling in CCM (Mode 4) and DCM (Modes 1–3)

The lookup table-based controller allows the converter to operate in CCM or in DCM. The compensator design is based on small-signal modeling of the converter in both modes.

In CCM, the on-time to output voltage transfer functions $G_{\mathrm{vton}}(s)$ are found, using standard averaged small-signal models [35]. The small-signal equivalent circuit includes conduction losses due to switch on-resistance and output diode forward voltage drop, and the on-time to output voltage transfer function is found using the equivalent model.

The averaged switch network is used for small-signal analysis in DCM, which is controlled by the switch on-time T_{on} and valley switching point k for output voltage regulation and improved dynamic responses. Under the assumption that the averaged switch network is lossless, the input and output ports are modeled by the effective resistor R_e and dependent power source, respectively, with the power consumed by the effective resistance R_e transferred to the network output port (loss-free resistor model) [35]. So, the switch network input port and output port currents are modeled as

$$\langle i_1\rangle_{T_S} = \frac{\langle v_g\rangle_{T_S}}{R_e(T_{\mathrm{on}},T_S)} \tag{10}$$

$$\langle i_2\rangle_{T_S} = \frac{\langle v_g\rangle^2_{T_S}}{R_e(T_{\mathrm{on}},T_S)\langle v_{\mathrm{out}}\rangle_{T_S}} \tag{11}$$

where the effective resistance R_e is a function of the switch on-time T_{on} and switching period T_S

$$R_e(T_{\mathrm{on}},T_S) = \frac{2L_MT_S}{T_{\mathrm{on}}^2}. \tag{12}$$

As shown in Fig. 13, the switching period depends on changes of the valley switching points due to the k-control, resulting in

$$T_S(T_{\mathrm{on}},k) = T_{\mathrm{on}}\left(1+\frac{nv_g}{v_{\mathrm{out}}}\right)+(k-0.5)T_{\mathrm{OSC}}. \tag{13}$$

Therefore, the effective resistor R_e is modified as a function of the switch on-time T_{on} and valley switching point k by inserting (13) into (12) to include effects of the k-control on output voltage

TABLE V
GAIN-SCHEDULED COMPENSATOR PARAMETERS

Modes	Valley switching points	Compensator types	Parameters
1 (DCM)	$k_{opt} > 14$ (F_S = 20kHz)	PI	$G_m = 20.12\times10^{-5}$, $Z_1 = 0.994$
2, 3 (DCM)	$1 \le k_{opt} \le 14$	PI	$G_m = 10.03\times10^{-5}$, $Z_1 = 0.997$
4 (CCM)	$k_{opt} = 0$	PID	$G_m = 36.2\times10^{-5}$, $Z_1 = 0.9614$, $Z_2 = 0.9753$

regulation in the small-signal models.

$$R_e(T_{\rm on}, k) = \frac{2L_M}{T_{\rm on}^2}\left\{T_{\rm on}\left(1+\frac{nv_g}{v_{\rm out}}\right)+(k-0.5)T_{\rm OSC}\right\}. \quad (14)$$

To obtain a small-signal equivalent circuit model for the converter operating in DCM, (14) is inserted into the averaged switch model (10) and (11), and the model is perturbed and linearized. Fig. 14 shows the small-signal ac model in DCM, and Table IV presents model parameters. In this model, high frequency dynamics due to the magnetizing inductance are neglected because the output filter capacitance $C_{\rm out}$ is relatively large (4500 μF), so the target crossover frequency f_c is relatively low, around 1 kHz.

The transfer functions involved with the compensator and k-control designs are derived based on the small-signal model of the converter shown in Fig. 14. For example, the on-time to output voltage transfer function $G_{\rm vton}(s)$ is established through analysis of the model when small ac variations of the input voltage and valley switching point are set as zero. Similarly, the valley switching point to output voltage transfer function $G_{\rm vk}(s)$ is obtained by letting the ac variations of the input voltage and on-time zero.

A loop gain $T_v(s)$, which is the product of the gains around the forward and feedback paths of the control loop, is usually used to examine whether the control loop guarantees consistent transient responses over various operating conditions. Fig. 15 shows a complete block diagram of the DCM small-signal model in output voltage regulation system, including loops for the switch on-time regulation and k-control. The loop gain $T_v(s)$ is expressed as

$$T_v(s) = H_v(s)\cdot\{G_c(s)\cdot G_{\rm vton}(s)+\alpha(s)\cdot G_{\rm vk}(s)\} \quad (15)$$

where $H_v(s)$ is a scale factor used for output voltage sensing [see Fig. 1(a)], $G_c(s)$ is the gain-scheduled compensator network, and $\alpha(s)$ is the k-control gain. Note that the switch on-time regulation and k-control actions are added in the loop gain, resulting in increased crossover frequency. Therefore, the k-control is capable of improving dynamic responses.

C. Experimental Results

Table V summarizes the compensator parameters and the fixed k-control gain α is set as -1000 to achieve the target crossover frequency with adequate phase margin over different operating modes. It should be noted that the sampling rate, which in the experimental prototype equals the switching frequency, varies across operating conditions. This is taken into account in the analysis of the loop gain magnitude and phase responses. Fig. 16 shows the results for three operating points.

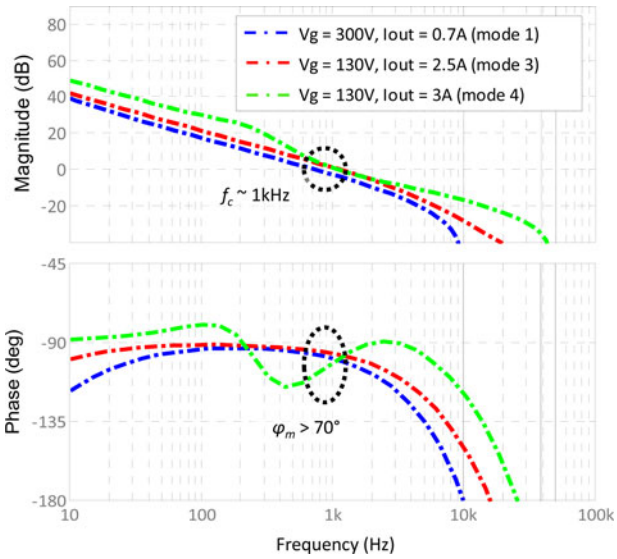

Fig. 16. Loop gain magnitude and phase responses at three operating conditions corresponding to compensator parameters presented in Table V.

TABLE VI
CONTROLLER HARDWARE REQUIREMENTS

Module	Number of gates
Gain-scheduled compensator	1854
Modulator (state machine)	2012
Optimizer (look-up table, k-control)	6863

Over all operating point corners, the gain-scheduling and k-control approaches result in relatively consistent small-signal dynamic responses with the crossover frequency around 1 kHz and the phase margin more than 70°.

For the experiment, the k-control scheme and gain-scheduled compensator parameters are programmed in the optimizer block of the controller. The A/D resolution of the output voltage error e_v is 2 mV. The k-control increment Δk is set to zero if the output voltage error e_v is between -4 mV and $+4$mV.

The hardware requirements for the controller design are presented in Table VI in terms of the equivalent number of gates reported by the Xilinx synthesis tool. The gate count for the optimizer module is larger compared to the other modules due to the implementation of the hysteresis bands. By considering the number of slots assigned to program the operating modes,

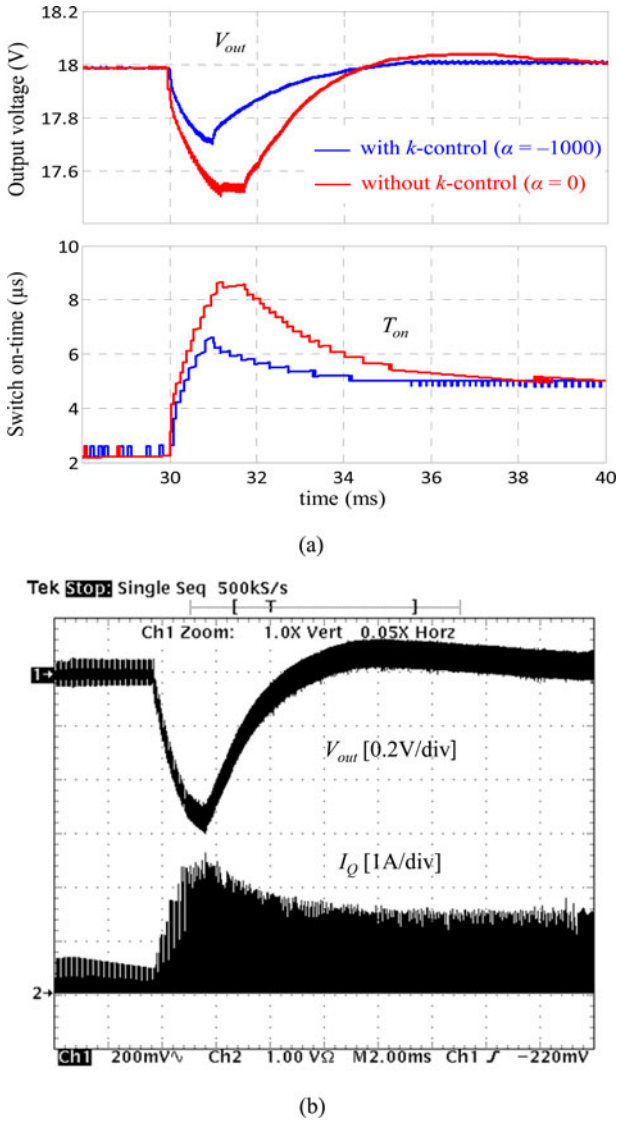

Fig. 17. Simulation and experimental results for a 0.1–2.5 A step load transient at 130 V in a case when the gain-scheduled compensator is employed without k-control ($\alpha = 0$). (a) Simulation results ($V_{\rm out}$, $T_{\rm on}$) with different k-control gains [$\alpha = 0$ (red) and $\alpha = -1000$ (blue)]. (b) Experimental results ($V_{\rm out}$ and I_Q) without k-control ($\alpha = 0$).

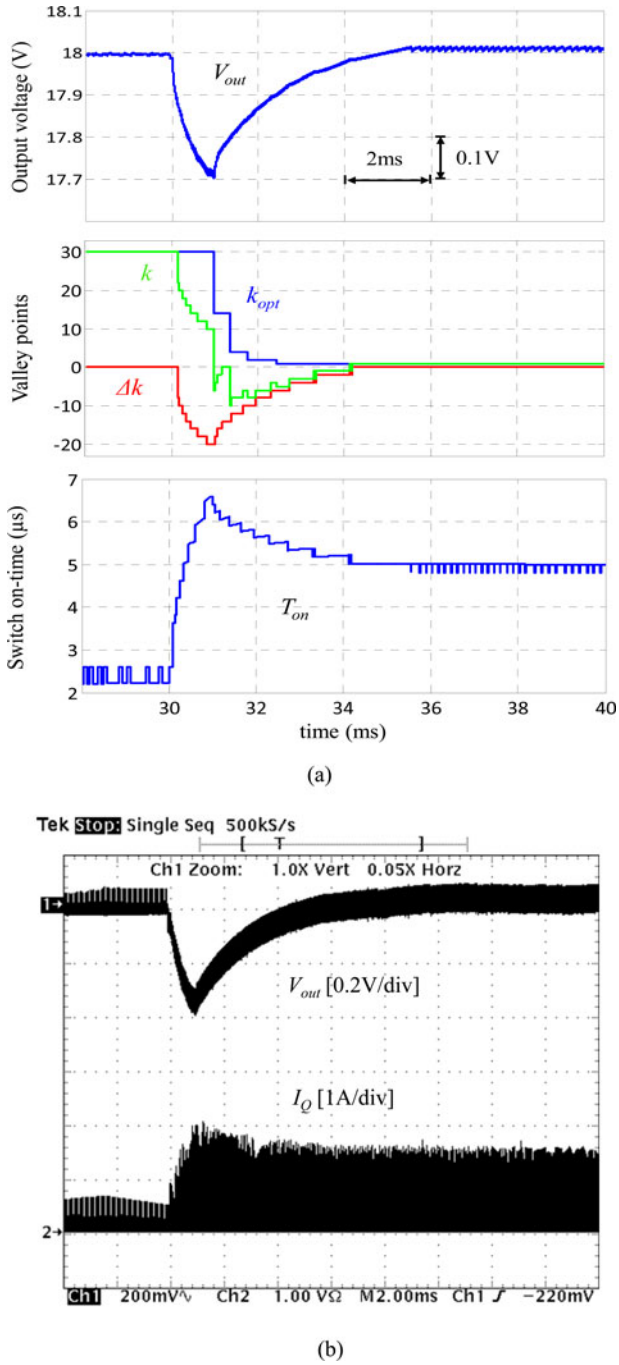

Fig. 18. Simulation and experimental results for a 0.1–2.5 A step load transient at 130 V. (a) Simulation results ($V_{\rm out}$, $k_{\rm opt}$, Δk, k, and $T_{\rm on}$). (b) Experimental results ($V_{\rm out}$ and I_Q).

and how many bits are used to store the lookup table parameters (e.g., the optimum valley switching points $k_{\rm opt}$, the controller coefficients, and the optimum switching periods in modes 1 and 4), the memory required to store the lookup tables in the optimizer module is calculated, resulting in around 320 bits.

Fig. 17 presents 0.1–2.5 A step load transient responses in a case when the converter employs only the gain-scheduled compensator shown in Table V without k-control ($\alpha = 0$). Simulation and experimental results of large-signal transient responses over different modes, including k-control ($\alpha = -1000$), are presented in Fig. 18 (0.1–2.5 A step load transient) and Fig. 19 (2.5–0.1 A step load transient). Note that the valley switching points k start equal to the optimum valley switching points $k_{\rm opt}$ and return to $k_{\rm opt}$ after the transient. As shown in the simulation results, the k-control does not degrade operation of the main output voltage control loop to regulate on-time $T_{\rm on}$ and the experimental results (output voltage $V_{\rm out}$ and MOSFET current I_Q) are well matched with the simulation results. Comparisons between Figs. 17 and 18 indicate that the k-control results in lower output voltage undershoot and faster dynamic responses, together with decreased peak switch current overshoot.

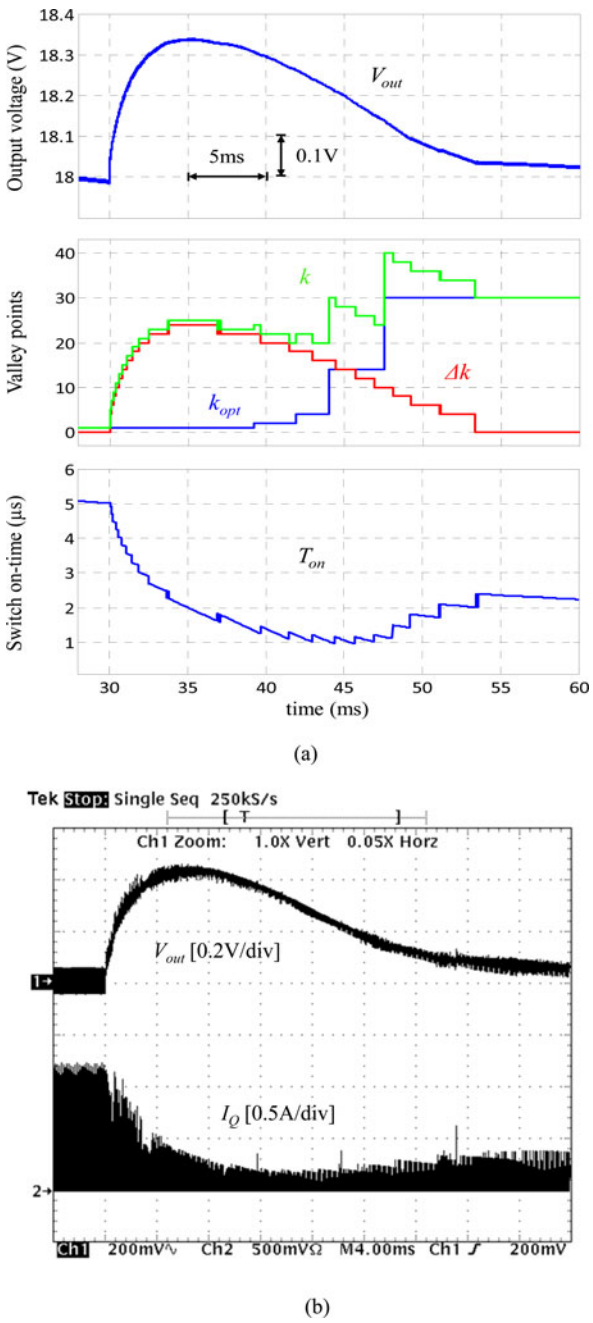

Fig. 19. Simulation and experimental results for a 2.5–0.1 A step load transient at 130 V. (a) Simulation results ($V_{\rm out}$, $k_{\rm opt}$, Δk, k, and $T_{\rm on}$). (b) Experimental results ($V_{\rm out}$ and I_Q).

VII. Conclusion

This paper describes an efficiency optimization approach for digitally controlled flyback dc–dc converters. Efficiency is characterized and optimized over wide ranges of operating conditions based on detailed power loss models and multivariable nonlinear constrained optimization. The proposed efficiency optimization approach can be separated into two processes, the design parameter optimization and the controller parameter optimization, enabling the power stage design and the controller design simultaneously, under a low-cost constraint. The optimum controller parameters are programmed in the lookup table, which implies that the same controller could be applied to different power stages. Compared to other on-line efficiency optimization techniques, the approach is simpler and less susceptible to disturbances during converter operation. Undesirable frequency hopping mechanisms, commonly observed in valley switching control schemes, are resolved by storing optimum valley switching points in the lookup table and by using hysteresis bands in the lookup table boundaries. A gain-scheduled compensator is designed based on small-signal modeling and analysis, and a simple extension, referred to as control, is proposed to improve large-signal transient responses. The optimization and experimental results for a standard low-cost 65 W flyback converter show that the controller achieves smooth mode transitions and consistent transient responses over different operating modes, and that efficiency exceeds 92% at all operating points over approximately 3:1 range of input voltages and 10:1 range of loads.

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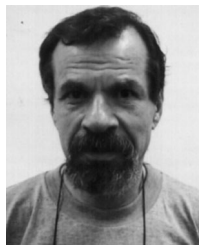

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