Fully Digitalized Implementation of PFC Rectifier in CCM Without ADC

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***Abstract*—As is generally acknowledged, the main drawback of a fully digitalized power factor correction (PFC) rectifier is that too many analog-to-digital converters (ADCs) are used, and hence, the corresponding cost is high. Consequently, in this paper, the information on the desired signal is obtained from two paired sawtoothed waves compared with the sensed signal, without the use of any ADCs. For the PFC rectifier operating in the continuous conduction mode (CCM) under average current mode control, the two proposed formulas used to calculate the average inductor current, together with the strategy for changing sampling points, are applied to accurately sample the average inductor current of the PFC rectifier. At the same time, based on the slope value of the inductor current obtained from the proposed average current calculation formula, another related formula is derived to obtain the input voltage information used to feed the partial feedforward controller. As for the sinusoidal current command, it is generated by a sinusoid table along with a zero-crossing detector. Furthermore, the information on the output voltage is obtained by one simple approximate formula. Therefore, there is no ADC required to realize the full digital control of the PFC rectifier operating in CCM.**

***Index Terms*—Average current mode control, one-comparator counter-based sampling, power factor correction (PFC) rectifier, two sawtoothed waves.**

I. Introduction

When considering the use of power electronics technologies, the main focus is on how to improve their conversion efficiency on the user side. Since the ac source of 110 or 220 V_{rms} is widely used, the energy saving can be achieved by reducing the complex power transmission between the power company and the user side via the ac–dc conversion interface. In [1]–[4], the lower the power factor (PF), the more the loss in the transmission line. The traditional ac–dc conversion interface consists of one peak rectifier and one linear regulator. Such a peak rectifier has a pulse-type input current, which contains many harmonics and whose fundamental phase deviates from the phase of the input voltage [5]. Hence, the line voltage is polluted to a certain extent. Aside from this, such a system has low efficiency since the switch operates in the linear region, and hence is not suitable for high-power applications. Consequently, the rectifier with power factor correction (PFC) [5] is presented to overcome the aforementioned disadvantages. Above all, the standard EN 61000-3-2 [6] raises the importance of the PFC rectifier in the industry.

As for the PFC control, it can be classified into three types: 1) peak current mode control; 2) average current mode control; and 3) hysteresis current mode control. Among these three, the average current mode control works with the smallest peak-to-peak inductor current and makes the PFC rectifier operate under constant switching frequency. Aside from this, the operations of the PFC control are divided into two types: analog control and digital control. Up to now, analog control has been widely used in the switching power supply.

In the literature, [7] describes how to design a PFC rectifier based on one analog pulse width modulated (PWM) control IC, named UC-3854. In the literature, [8] shows that the system tends to oscillate as the slope of the control effort is too large such that this control effort and the triangular wave will intersect at two points over one switching period. In [9], a simple circuit is added to the boost converter to increase the value of PF under high switching frequency [7]. In [10], the peak voltage detection based on an *RC* circuit is used to feedback the input current, so as to obtain the required value of PF. However, the analog control has some demerits, such as low immunity from the switching noise, low resistance to environmental variations, unsuitability for complicated control strategies, etc.

In order to solve the aforementioned problems, digital control techniques [11]–[17] are proposed. Under digital control, the DSP possesses high-speed complicated calculation capability. In [18]–[30], how to control switching power supplies based on the DSPs is shown, and [31]–[38] apply the DSPs to the control of the PFC rectifiers, particularly as the digital control shown in [31] is indispensable for the special duty cycle control strategy.

However, as is generally acknowledged, the DSP program is executed sequentially, and hence, the accompanying time elapse is long if too many complicated mathematical equations are required. The long elapse time causes the control delay to be too long, which makes the system unstable. Unlike the DSP, the field programmable gate array (FPGA) has a hardware speed similar to that of the logic gate and possesses parallel process capability. Therefore, the FPGA is gaining more and more popularity in the control of various switching power supplies [39]–[47], as exemplified in [48]–[51], which demonstrate applications of FPGAs to PFC rectifiers.

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Up to now, the analog-to-digital converter (ADC) has been indispensable for traditional digital control. There are many ADC structures [52], which possess individual applications. Basically, the selection of the ADC is based on the trade-off between sampling rate and resolution. However, a high-resolution ADC is expensive. Consequently, the one-comparator counter-based sampling technique [53] is proposed and applied to the digital control without ADC. Furthermore, the sawtoothed wave injection method [54] is proposed to enhance the sampling linearity. However, these sampling strategies without ADC are not suitable when the analog signal has large variations in amplitude. In this case, there is a large difference between sampled data and actual analog signal. In order to solve this problem, the amplitude of the sawtoothed wave to be injected is increased further, and hence, the accuracy is degraded significantly. Consequently, the one-comparator counter-based sampling technique with sawtoothed wave injection is not suitable for sampling the inductor current of the PFC rectifier.

In order to apply the concept of such a sampling technique [53], [54] to the PFC rectifier operating in CCM, two average current calculation formulas, based on the modified one-comparator counter-based sampling technique along with two paired sawtoothed waves applied, are presented herein. The proposed sampling strategy has the following features:

1) it does not require a low-pass filter, and hence, the corresponding bandwidth of the inner loop can be increased;
2) the sinusoid table, triggered by the zero-crossing detector: cooperates with the control effort created from the outer loop, so as to provide the sinusoidal current command for the average current mode control;
3) since the inductor current of the PFC rectifier varies significantly in its amplitude, the selection of average current calculation formula depends on the value of the duty cycle;
4) based on the slope value of the inductor current obtained from the proposed average current calculation, another related formula is derived so as to obtain the input voltage information used to feed the partial feedforward controller;
5) the information on the output voltage is obtained by one simple approximate formula which averages two sampled values over one switching period, so as to achieve the voltage loop control.

Therefore, there is no ADC required to realize the fully digitalized control of the PFC rectifier in CCM. In addition, the feasibility and effectiveness of the proposed sampling topology are demonstrated by experimental results.

II. Overall System Configuration

Fig. 1 shows the proposed overall system function block diagram, whereas Fig. 2 shows the main power stage used in this paper. The main power stage is constructed by one PFC rectifier. In order to make the input current in phase with the input voltage, the FPGA controller needs information on the inductor current and on the phase angle of the input voltage, and the former is achieved by the Hall sensor and the sampling circuit B, whereas the latter is achieved by the isolated transformer and the zero-crossing detector. Aside from these, the output voltage

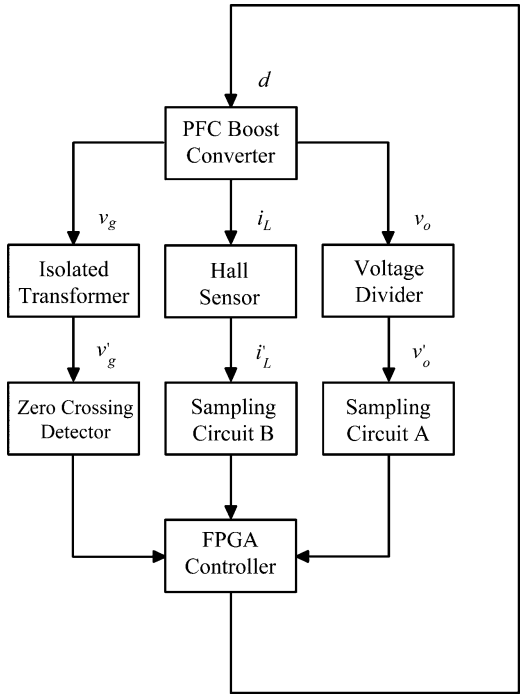

Fig. 1. Proposed overall system function block diagram.

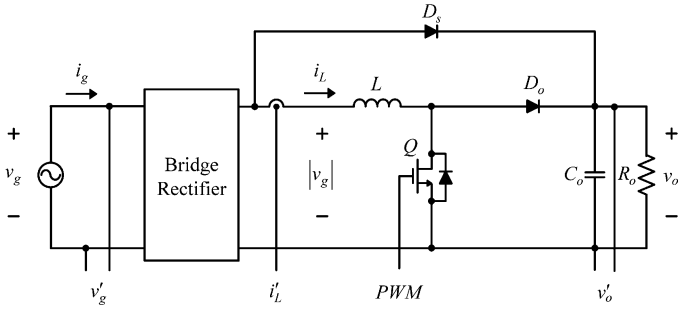

Fig. 2. Main power stage of the PFC rectifier.

information needed by the FPGA controller is achieved by the voltage divider and the sampling circuit A. Above all, the sampling circuits A and B are realized by the proposed sampling method. Therefore, the suitable duty cycle figured out from the FPGA controller is sent to the main switch Q, to not only stabilize the output voltage of this converter but also to perform the required PFC. Furthermore, the diode D_s, shown in Fig. 2, is utilized to establish the voltage across the output capacitor C_o so that the inrush current at startup can be suppressed. It is noted that in Fig. 1, the input voltage, the inductor current, and the output voltage are signified by v_g, i_L, and v_o, respectively, whereas the input voltage after the isolated transformer, the inductor current after the Hall sensor, and the output voltage after the voltage divider are represented by v'_g, i'_L, and v'_o, respectively.

III. Sampling Technique Concept

Prior to the following discussion, it is assumed that this converter operates in CCM.

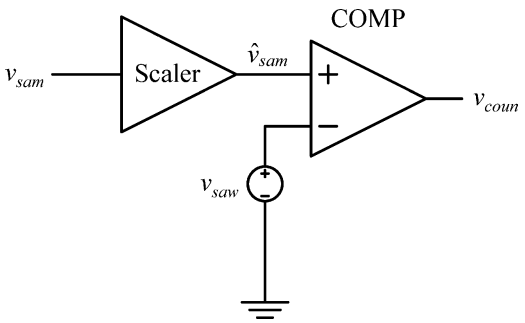

Fig. 3. Main sampling circuit.

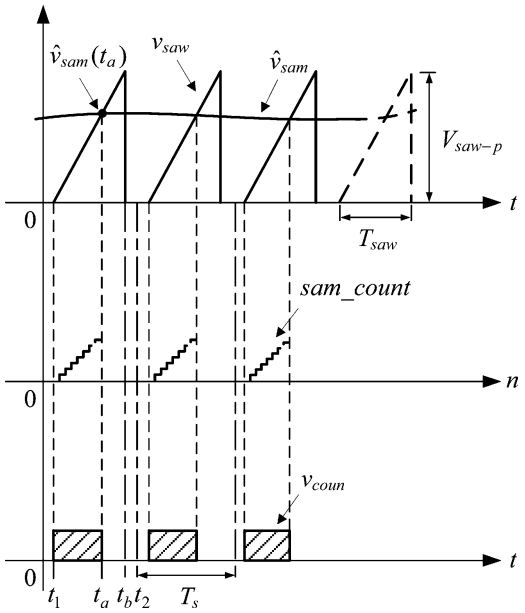

Fig. 4. Key waveforms in sampling.

A. One-Comparator Sampling

In order to sample a signal without any ADC in the digital control system, one-comparator sampling is presented herein, whose basic operating principle is as follows. Fig. 3 shows the main sampling circuit, where $v_{\rm sam}$, $\hat{v}_{\rm sam}$, $v_{\rm saw}$, and $v_{\rm coun}$ are the signal to be sampled, $v_{\rm sam}$ after the scaler, the sawtoothed wave, and the signal outputted from the comparator COMP, respectively. After this, there are some symbols to be defined prior to the following analysis: 1) one counter, named *cycle_count* with the period of T_s, is used as a function block enabling counter so as to make function blocks in Fig. 2 work; 2) the width of $v_{\rm saw}$ is expressed to be $T_{\rm saw}$; and 3) the other counter, named *sam_count*, is used as a sampling counter.

From Fig. 4, it can be seen that *sam_count*, controlled by $v_{\rm coun}$, starts counting at the instant t_1 stops counting at the instant t_a, and is repeated cycle by cycle. Since the switching noise exists in the switching power supply, the time intervals of $0{\sim}t_1$ and $t_b{\sim}t_2$ are used to reduce their effects on sampling. Therefore

$$T_s = T_{\rm saw} + t_1 + t_2 - t_b = t_2. \tag{1}$$

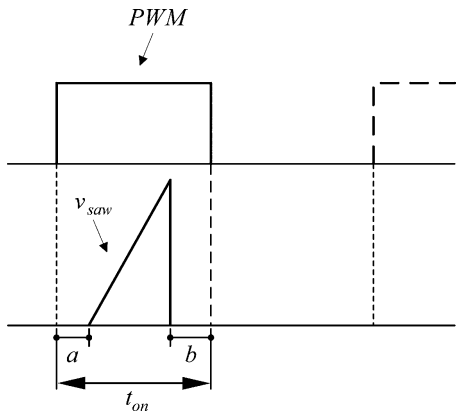

Fig. 5. Sawtoothed wave used to sample the signal during the turn-on period.

Moreover, the value of *sam_count*, used as the digital information of $v_{\rm sam}$, can be obtained to be

$$sam\_count = f_{\rm sam} \cdot (t_a - t_1) \tag{2}$$

where $f_{\rm sam}$ corresponds to the frequency of *sam_count*.

On the other hand, from the sawtooth-slope equation, the value of $\hat{v}_{\rm sam}$ at the instant t_a can be expressed to be

$$\hat{v}_{\rm sam}(t_a) = \frac{V_{\rm saw-p}}{T_{\rm saw}} \cdot (t_a - t_1) \tag{3}$$

where $V_{\rm saw\text{-}p}$ is the peak value of $\hat{v}_{\rm sam}$.

By substituting (3) into (2), we can obtain

$$sam\_count = \frac{f_{\rm sam} \cdot T_{\rm saw}}{V_{\rm saw-p}} \cdot \hat{v}_{\rm sam}(t_a). \tag{4}$$

Hence, the mapping relationship between analog and digital can be seen from (4).

B. Sampling Interval and Resolution

If the sampling frequency is synchronous with the switching frequency, then the sampling process will occur during the turn-on period $t_{\rm on}$ or the turn-off period $t_{\rm off}$. Fig. 5 shows the sawtoothed wave used to sample the signal during the turn-on period, where PWM is represented as the gate driving signal used to drive the main switch Q. In order to obtain accurate digital information on the signal during the turn-on period, the following inequality must be satisfied as shown in Fig. 5 along with Fig. 4:

$$t_{\rm on} \geq a + b + T_{\rm saw} \tag{5}$$

where a, b, and $T_{\rm saw}$ are t_1, t_2–t_b, and t_b–t_1, respectively.

Hence, the equivalent A/D resolution, AD_R, can be represented by

$$\text{AD\_R} = T_{\rm saw} \cdot f_{\rm sam} = (t_{\rm on} - a - b) \cdot f_{\rm sam}. \tag{6}$$

In Fig. 6, the analysis of the sawtoothed wave during the turn-off period is the same as that in Fig. 5.

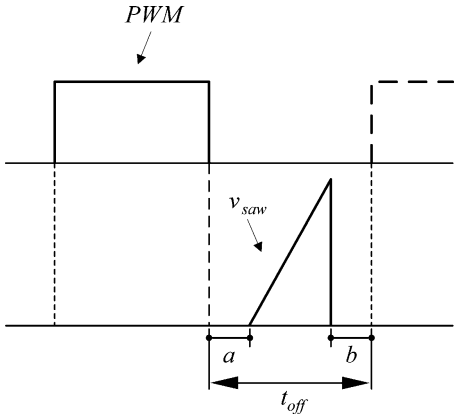

Fig. 6. Sawtoothed wave used to sample the signal during the turn-off period.

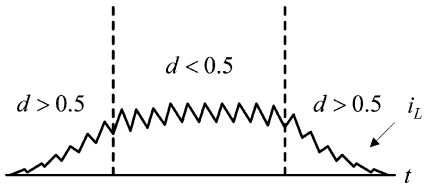

Fig. 7. Duty cycle distribution over one half-cycle.

C. One-Comparator Sampling With One Sawtoothed Wave Applied to PFC

In order to achieve high PF, the input current is controlled to follow the input voltage as tightly as possible. Hence, the duty cycle of PWM, d, will be varied significantly over one half-cycle. Assuming that the output voltage of the PFC rectifier is kept constant at V_o, the voltage conversion ratio M can be expressed to be

$$M \equiv \frac{v_o}{v_g} = \frac{V_o}{V_{g\text{-}p} \cdot |\sin(\omega_e \cdot t\ )|} = \frac{1}{1-d} \tag{7}$$

where $V_{g\text{-}p}$ is the peak value of v_g, V_o is the dc value of v_o, and ω_e is the radian frequency of v_g.

According to (7), d can be expressed to be

$$d = 1 - \frac{V_{g\text{-}p} \cdot |\sin(\omega_e \cdot t)|}{V_o}. \tag{8}$$

Based on (8), it can be seen that, as shown in Fig. 7, d is distributed over a half-cycle with the boundary condition that d is equal to 0.5. And, the corresponding instant t can be expressed to be

$$t = \frac{1}{\omega_e} \cdot \sin^{-1}\left(\frac{V_o}{2V_{g\text{-}p}}\right). \tag{9}$$

Therefore, according to Fig. 7, the sampling interval is determined by the duty cycle d. If d is larger than 0.5, the sampling process occurs during the turn-on period; otherwise, the sampling process occurs during the turn-off period. And, some constraints shown in Section III-B must be taken into account.

As generally acknowledged, if the average current mode control is used to achieve a high PF, the inductor current is desired to be sampled at the point of the average value over one switching period [8]. However, the sampled inductor current is not always at the point of the average value if the one-comparator sampling with one sawtoothed wave is applied to PFC. This can be illustrated in Figs. 8 and 9. As shown in Fig. 8, under the same duty cycle but different average values, the value of the sampled inductor current at point A is higher than the corresponding average value, but the value of the sampled inductor current at point B is lower than the corresponding average value. As shown in Fig. 9, under the same average value but different duty cycles, the value of the sampled inductor current at point A is higher than the corresponding average value, but the value of the sampled inductor current at point B is lower than the corresponding average value. Such phenomena in the average inductor currents shown in Figs. 8 and 9 cannot make the input current follow the input voltage tightly even if the inner loop is well controlled. Based on the aforementioned description, how to accurately sample the average inductor current without any ADC is presented in the following sections along with how to sample the output voltage and how to determine the peak value of the input voltage.

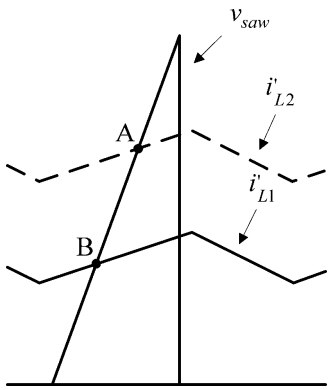

Fig. 8. Sampled inductor currents under the same duty cycle but different average inductor currents.

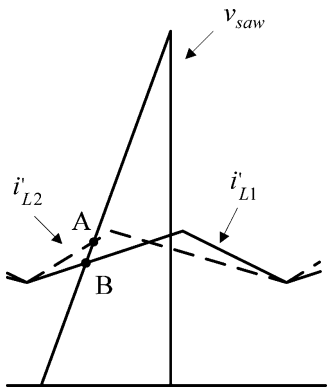

Fig. 9. Sampled inductor currents under the same average inductor current but different duty cycles.

D. Sampling Inductor Current Using Two Sawtoothed Waves

First, there are some symbols and assumptions to be described in Figs. 10 and 11, as follows: 1) m_1 and m_2 are the slopes of the magnetizing and demagnetizing inductor currents, respectively; 2) s_1 is the value of the first sampling, whereas s_2 is the value

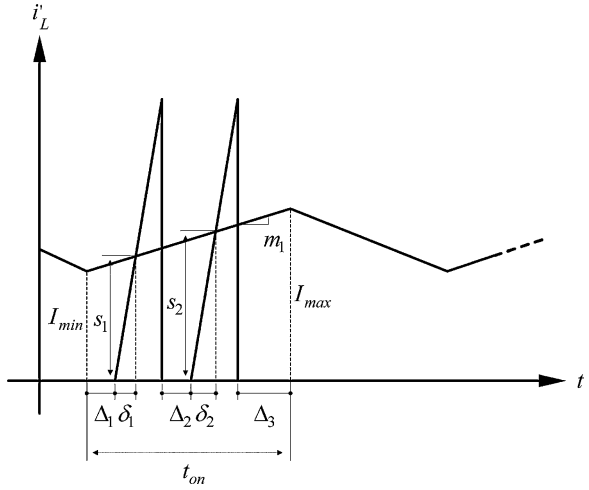

Fig. 10. Sampling using two sawtoothed waves during the turn-on period with the duty cycle not less than 50%.

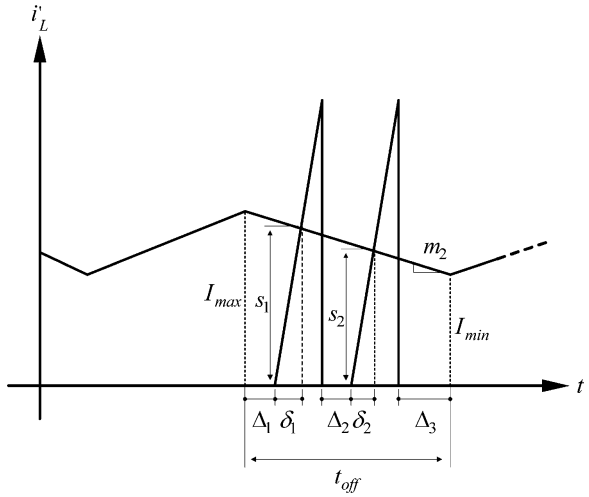

Fig. 11. Sampling using two sawtoothed waves during the turn-off period with the duty cycle less than 50%.

of the second sampling; 3) $I_{\max}$ and $I_{\min}$ are the maximum and minimum inductor currents, respectively; 4) Δ_1 and Δ_3 are the time intervals used to be immune from the switching noise due to the turn-on and turn-off instants; 5) δ_1 and δ_2 are the counting time intervals for the first and second samplings, respectively; 6) Δ_2 is left for the recovery time of the actual sawtoothed wave; and 7) this PFC rectifier operates in CCM.

In order to realize the proposed sampling method, the following inequality must be satisfied:

$$0.5T_s \geq \Delta_1 + \Delta_2 + \Delta_3 + 2T_{\text{saw}}. \tag{10}$$

Therefore, the time interval of the sawtoothed wave T_{saw} can be expressed to be

$$T_{\text{saw}} \leq 0.5 \cdot (0.5T_s - \Delta_1 - \Delta_2 - \Delta_3). \tag{11}$$

At the same time, the equivalent A/D resolution AD_R can be represented by

$$\text{AD\_R} = T_{\text{saw}} \cdot f_{\text{sam}} = 0.5 \cdot (0.5T_s - \Delta_1 - \Delta_2 - \Delta_3) \cdot f_{\text{sam}}. \tag{12}$$

From Fig. 10, the inductor current is sampled during the turn-on period with the duty cycle of not less than 50%, and hence, the slope of the magnetizing inductor current can be expressed to be

$$m_1 = \frac{s_2 - s_1}{\Delta_2 + \delta_2 + T_{\text{saw}} - \delta_1}. \tag{13}$$

Therefore, the inductor current equation can be represented by

$$i'_L = \frac{s_2 - s_1}{\Delta_2 + \delta_2 + T_{\text{saw}} - \delta_1} \cdot t + I_{\min}. \tag{14}$$

If $t = \Delta_1 + \delta_1$, the minimum inductor current $I_{\min}$ can be solved out to be

$$I_{\min} = s_1 - \frac{s_2 - s_1}{\Delta_2 + \delta_2 + T_{\text{saw}} - \delta_1} \cdot (\Delta_1 + \delta_1). \tag{15}$$

By substituting (15) into (14), (14) can be written to be

$$i'_L = \frac{s_2 - s_1}{\Delta_2 + \delta_2 + T_{\text{saw}} - \delta_1} \cdot (t - \delta_1 - \Delta_1) + s_1. \tag{16}$$

If $t = 0.5 \cdot t_{\text{on}}$, the average inductor current I'_L can be worked out to be

$$I'_L = \frac{s_2 - s_1}{\Delta_2 + \delta_2 + T_{\text{saw}} - \delta_1} \cdot \left(\frac{t_{\text{on}}}{2} - \delta_1 - \Delta_1\right) + s_1, \text{for } s_1 < s_2. \tag{17}$$

On the other hand, from Fig. 11, if the inductor current is sampled during the turn-off period with the duty cycle less than 50%, the average inductor current I'_L can be worked out via the similar method applied to (17) to be

$$I'_L = s_1 - \frac{s_1 - s_2}{\Delta_2 + \delta_2 + T_{\text{saw}} - \delta_1} \cdot \left(\frac{t_{\text{off}}}{2} - \delta_1 - \Delta_1\right), \text{for } s_1 > s_2. \tag{18}$$

Eventually, two formulas used to figure out the average inductor current, shown in (17) and (18), make the current loop of the PFC rectifier digitally controlled without any ADC required. Next, how to apply the proposed concept to the voltage loop and the partial feedforward loop is discussed, such that the full digital control of the PFC rectifier without any ADC can be realized.

E. Sampling Output Voltage Based on Two Sawtoothed Waves Information

As is generally acknowledged, the output voltage contains the low-frequency sinusoidal voltage ripple, whose amplitude is much larger than that of the switching voltage ripple. Hence, such a low-frequency voltage ripple dominates the output voltage ripple. Therefore, the output voltage ripple $\tilde{v}_o$ can be approximately expressed by

$$\tilde{v}_o \approx -\tilde{V}_{o\text{-}p} \cdot \sin(2 \cdot \omega_e \cdot t) \tag{19}$$

where $\tilde{V}_{o\text{-}p}$ is the peak value of $\tilde{v}_o$.

Since the maximum absolute variation in the output voltage ripple over one switching period $|\Delta\tilde{v}_o|_{\max}$ occurs at the zero crossing of the input voltage, $|\Delta\tilde{v}_o|_{\max}$ can be expressed to be

$$|\Delta\tilde{v}_o|_{\max} \approx \tilde{V}_{o\text{-}p} \cdot [\sin(2 \cdot \omega_e \cdot T_s) - \sin(2 \cdot \omega_e \cdot 0)]. \quad (20)$$

Since T_s is equal to 20 ns and ω_e is 377 rad/s, the resulting $|\Delta\tilde{v}_o|_{\max}$ can be signified from (20) by

$$|\Delta\tilde{v}_o|_{\max} \approx 0.015 \times \tilde{V}_{o\text{-}p}. \quad (21)$$

It is noted that the result in (21) shows that $|\Delta\tilde{v}_o|_{\max}$ is 1.5% of $\tilde{V}_{o\text{-}p}$, implying that it can be assumed that the sampled values all over one switching period are considered to be the same. Therefore, v_o' can be estimated to be

$$v_o' = 0.5 \cdot (s_1 + s_2). \quad (22)$$

Hence, the voltage-loop control can be realized without any ADC used.

F. Sampling Input Voltage Based on Two Sawtoothed Waves Information

In this paper, the partial feedforward control [9] is adopted so as to decrease the effect of variations in input voltage on the load transient response and to reduce the burden of the current loop. Therefore, the duty cycle created from the partial feedforward loop d_f can be expressed to be

$$d_f = 1 - \frac{|v_g'|}{V_o'}. \quad (23)$$

From (23), the more the $|v_g'|$, the lower the d_f. Also, based on (13), the peak value of $v_g', V_{g\text{-}p}'$, can be estimated to be

$$V_{g\text{-}p}' = \frac{s_2 - s_1}{\Delta_2 + \delta_2 + T_{\text{saw}} - \delta_1} \cdot \frac{L_g}{|sin(\omega_e \cdot t)|} |_{t=n \cdot T_s}. \quad (24)$$

Therefore, according to (24), $|v_g'|$ can be estimated to be

$$|v_g'| = V_{g\text{-}p}' \cdot |\sin(\omega_e \cdot t)|. \quad (25)$$

It is noted that $V_{g\text{-}p}'$ is updated as the zero crossing of the input voltage occurs.

Hence, the partial feedforward control can be also realized without any ADC used. That is, based on the aforementioned analysis, the PFC rectifier can be under fully digitalized control without any ADC.

IV. Experimental Results

System specifications and key component product names are tabulated in Table I. Some measured waveforms are provided to verify the effectiveness of the proposed control scheme. The parameters of the voltage loop are the proportional gain k_p of 0.035 and the integral gain k_i of 0.004, whereas the parameters of the current loop are the proportional gain k_p of 0.9, the integral gain k_i of 0.125, and the derivative gain k_d of 0.8. Hence, under the condition of the rated input voltage of 110 V_{rms}, Figs. 12 and 13 show the measured waveforms for the input voltage and current, and the distribution of the input current harmonics, at minimum and rated loads, respectively. And, the measured values of total harmonic distortion (THD), PF, and efficiency at minimum load, shown in Fig. 12, are 8%, 0.98, and 94.8%, respectively, and the measured values of THD, PF, and efficiency at rated load, shown in Fig. 13, are 2.8%, 0.993, and 94.5%, respectively. It is thus obvious that under the same input voltage, the more the load current, the lower the THD, the higher the PF, but the lower the efficiency. Also, by substituting the results in Figs. 12(b) and 13(b) into the IEC61000-3-2 Class C Standard shown in Table II, it can be seen that all the input current harmonics are below the individual maximum permissible harmonic currents. In addition, the measured values of THD, PF, and efficiency for various input voltages and loads are tabulated in Table III. From Table III it can be seen that, the higher the input voltage, the higher the efficiency, but the lower the THD and PF. On the other hand, Figs. 14 and 15 show the sampling points for the

TABLE I
System Specifications and Key Component Product Names

Input voltage (v_g)	90V_{rms} to 130V_{rms} with 110V_{rms} rated
Output voltage (V_o)	200V
Switching frequency (f_s)	50kHz
Switching period (T_s)	20μs
Rated output power ($P_{o\text{-}rated}$)	200W
Minimum output power ($P_{o\text{-}min}$)	100W
Peak value of the output voltage ripple	≤ 2V
Peak value of the sawtoothed wave ($V_{saw\text{-}p}$)	3V with Δ_1 of 1.6μs, Δ_2 of 0.4μs, Δ_3 of 1.16μs
Sampling clock (f_{sam})	200MHz
Comparator	LT1719
Digital control chip	EP2C20F484C8 with system clock of 50MHz

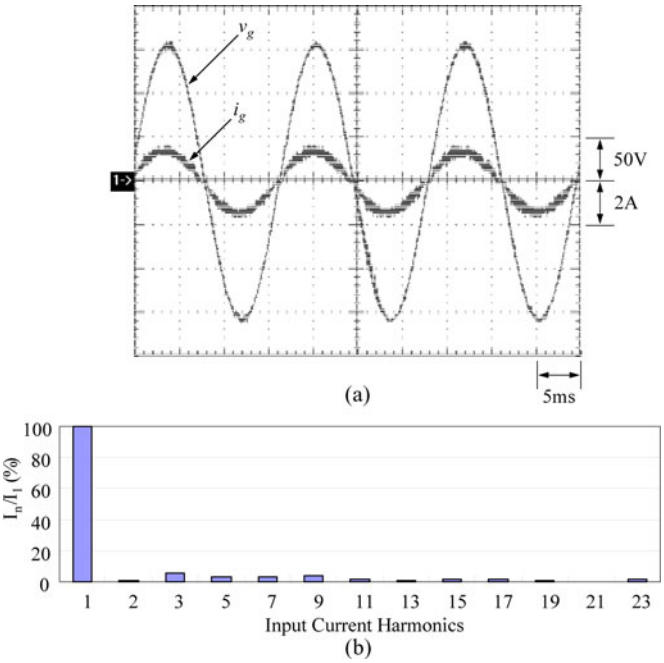

Fig. 12. Measured waveforms at minimum load. (a) Input voltage v_g and the input current i_g. (b) Distribution of the input current harmonics.

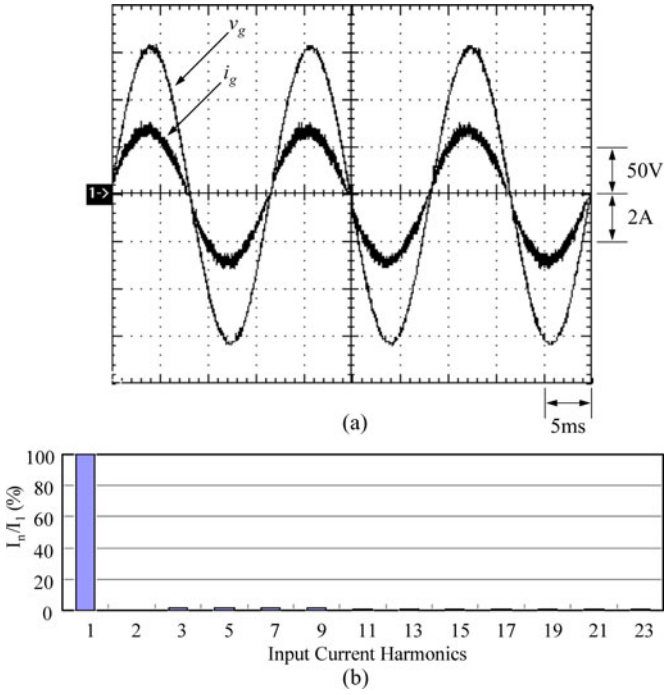

Fig. 13. Measured waveforms at rated load. (a) Input voltage v_g and the input current i_g. (b) Distribution of the input current harmonics.

TABLE II
IEC 61000-3-2 CLASS C STANDARD

Harmonic order (n)	Maximum permissible harmonic current expressed as a percentage of the input current at the nth fundamental frequency (%)
2	2
3	30 λ
5	10
7	7
9	5
$11 \le n \le 39$	3
λ is the circuit power factor	

TABLE III
THD, PF, AND EFFICIENCY FOR VARIOUS INPUT VOLTAGES AND LOADS

Input voltage of 90V_{rms}			
	Minimum load	Middle load	Rated load
THD	6.1%	4.1%	2.4%
PF	0.987	0.993	0.995
Efficiency	94.8%	94.6%	94.3%
Input voltage of 110V_{rms}			
THD	8%	4.4%	2.8%
PF	0.98	0.989	0.993
Efficiency	94.8%	94.6%	94.5%
Input voltage of 130V_{rms}			
THD	12.7%	7.1%	5%
PF	0.971	0.984	0.988
Efficiency	96%	96.7%	97%

inductor current at high and low duty cycles, whereas Fig. 16 displays the sampling points for the output voltage. From these results, shown in Figs. 14–16, it can be seen that the proposed sampling method can remove the effect of the switching noise on sampling. Fig. 17 shows the photo of the experimental setup.

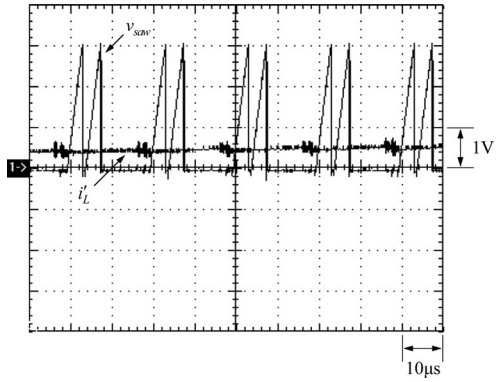

Fig. 14. Measured sampling points for the inductor current at high duty cycles.

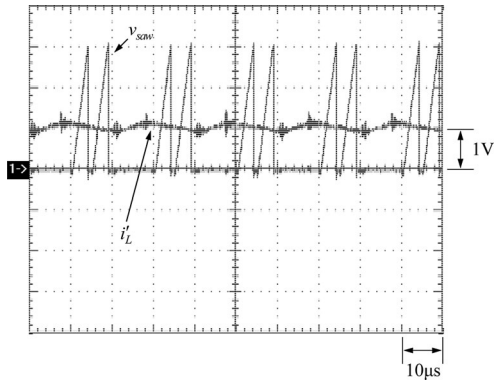

Fig. 15. Measured sampling points for the inductor current at low duty cycles.

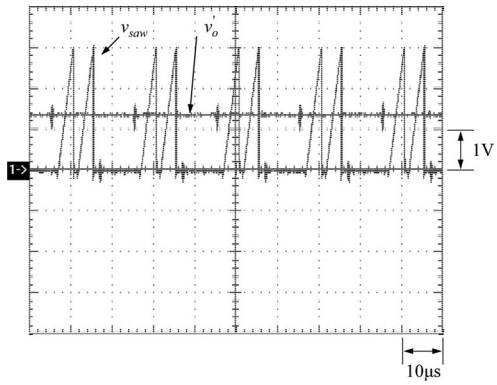

Fig. 16. Measured sampling points for the output voltage.

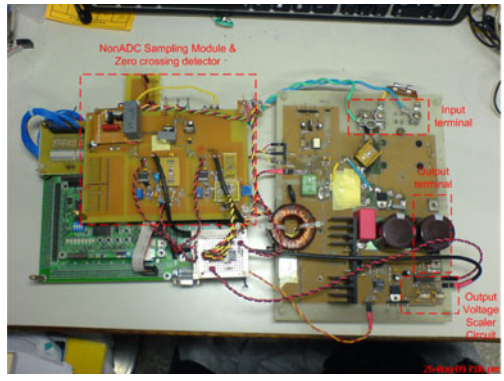

Fig. 17. Experimental setup.

V. Conclusion

Some of the features of the proposed sampling method for the PFC rectifier presented in this paper are as follows.

1) Information on the required signal is obtained via two paired sawtoothed waves compared with the sensed signal, without any ADC used.
2) For the PFC rectifier operating in CCM, two proposed formulas, together with the strategy for changing sampling points, are used to figure out the average inductor current.
3) Based on the slope value of the inductor current obtained from the average current calculation formula, another formula is derived so that the input voltage information used to feed the partial feedforward controller can be obtained.
4) The sinusoidal current command is generated by a zero-crossing detector along with a sinusoid table.
5) Information on the output voltage is obtained by one simple approximate formula.
6) There is no ADC required to realize the fully digitalized control of the PFC rectifier operating in CCM.

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