High-Efficiency DC–DC Converter With Two Input Power Sources

Rong-Jong Wai, *Senior Member, IEEE*, Chung-You Lin, and Bo-Han Chen

***Abstract*—The aim of this study is to develop a high-efficiency converter with two input power sources for a distributed power generation mechanism. The proposed converter can boost the varied voltages of different power sources in the sense of hybrid power supply to a stable output dc voltage for the load demand. An auxiliary circuit in the proposed converter is employed for achieving turn-ON zero-voltage switching (ZVS) of all switches. According to various situations, the operational states of the proposed converter can be divided into two states including a single power supply and a dual power supply. In the dual power-supply state, the input circuits connected in series together with the designed pulsewidth modulation can greatly reduce the conduction loss of the switches. In addition, the effectiveness of the designed circuit topology and the ZVS properties are verified by experimental results, and the goal of high-efficiency conversion can be obtained.**

***Index Terms*—DC–DC converter, hybrid power supply, high-efficiency power conversion, zero-voltage switching (ZVS).**

I. Introduction

In order to protect the natural environment on the earth, the development of clean energy [1]–[3] without pollution has the major representative role in the last decade. By accompanying the permission of Kyoto Protocol, clean energies, such as fuel cell (FC), photovoltaic (PV), wind energy, etc., have been rapidly promoted. Due to the electric characteristics of clean energies, the generated power is critically affected by the climate or has slow transient responses, and the output voltage is easily influenced by load variations. [4]. Thus, a storage element is necessary to ensure proper operation of clean energies. Batteries or supercapacitors are usually taken as storage mechanisms for smoothing output power, start-up transition, and various load conditions [5], [6]. The corresponding installed capacity of clean energies can be further reduced to save the cost of system purchasing and power supply. For these reasons, hybrid power conversion systems (PCS) have become one of interesting research topics for engineers and scientists at present.

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Based on power electronics technique, the diversely developed power conditioners including dc–dc converters and dc–ac inverters are essential components for clean-energy applications. Generally, one power source needs a dc–dc converter either for rising the input voltage to a certain band or for regulating the input voltage to a constant dc-bus voltage [6]–[8]. However, conventional converter structures have the disadvantages of large size, complex topology, and expensive cost. In order to simplify circuit topology, improve system performance, and reduce manufacturing cost, multi-input converters have received more attentions in recent years [9]–[18].

Liu and Chen [9] proposed a general approach for developing multi-input converters. By analyzing the topologies of converters, the method for synthesizing multi-input converters was inspired by adding an extra pulsating voltage or a current source to a converter with an appropriate connection. Wai *et al*. [11], [12] presented multi-input converters with high step-up ratios, and the goal of high-efficiency conversion was obtained. However, these topologies are not economic for the non-isolated applications because of the complexity with numbers of electrical components. Tao *et al*. [13] and Matsuo *et al*. [14] utilized multiwinding-type transformers to accomplish the power conversion target of multi-input sources. Although these topologies were designed based on time-sharing concept, the complexity of driving circuits will be increased by the control techniques in [13] and [14]. Marchesoni and Vacca [15] investigated a newly designed converter with the series-connected input circuits to achieve the goal of multiple input power sources. The installation cost of the converter with few components was certainly reduced. The feature of [15] is that the conduction losses of switches can be greatly reduced, especially in the dual power-supply state. Unfortunately, the hard-switching problem and the huge reverse-recovery current within the output diode degrade the conversion efficiency as a traditional boost converter [6]. Kwasinski [16] discussed the evolution of multiple input converters from their respective single-input versions. Based on several assumptions, restrictions, and conditions, these analyses indicate some feasible and unfeasible frameworks for multiple-input development. Li *et al*. [17] investigated a set of basic rules for generating multiple-input converter topologies, and systematically generated two families of multiple-input converters. Qian *et al*. [18] designed a novel converter topology with four power ports including two sources, one bidirectional storage port, and one isolated load port. The zero-voltage switching (ZVS) can be achieved for four main switches.

In this study, a high-efficiency ZVS dual-input converter is investigated, and this converter directly utilizes the current-source type applying to both input power sources. Based on

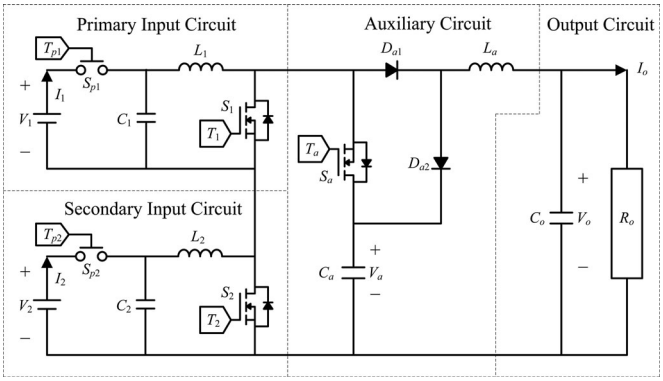

Fig. 1. Circuit topology of high-efficiency dual-input converter.

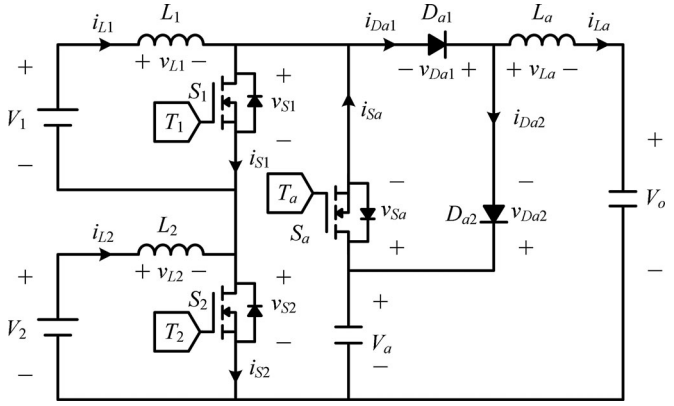

Fig. 2. Equivalent circuit.

the series-connected input circuits and the designed pulsewidth modulation (PWM) driving signals, the conduction loss of the switches can be greatly reduced in the dual power-supply state. Lee *et al*. [19] performed zero-current-transition dc–dc converters without additional current stress and conduction loss on the main switch during the resonance period of the auxiliary cell. The auxiliary cell provides zero-current-switching turn-OFF for all active switches and minimizes the reverse recovery problem of the main diode. The modified type of this representative auxiliary cell in [19] is introduced into the proposed dual-input converter to reduce the reverse-recovery currents of the diodes. An auxiliary circuit with a small inductor operated in the discontinuous conduction mode (DCM) is utilized for achieving turn-ON ZVS of all the switches, and the huge reverse-recovery current of the output diode in the traditional boost converter can be removed via the utilization of an auxiliary inductor series connected with a diode. Consequently, the proposed dual-input converter can efficiently convert two power sources with different voltages to a stable dc-bus voltage. According to the power dispatch, this converter could be operated at two states including a single power-supply state and a dual power-supply state. This study is organized into four sections. Following the introduction in Section I, the topology and operation of the proposed high-efficiency dual-input converter are presented in Section II. In Section III, experimental results are provided to validate the effectiveness of the proposed converter. Conclusions are drawn in Section IV.

II. Topology and Operation of Dual-Input Converter

Fig. 1 shows the circuit topology of the proposed ZVS dual-input converter. It contains four parts including a primary input circuit, a secondary input circuit, an auxiliary circuit, and an output circuit. The major symbol representations are summarized as follows. V_1 and I_1 denote the primary input voltage and current, respectively. V_2 and I_2 exhibit the secondary input voltage and current, respectively. S_{P1}, S_{P2}, T_{P1}, and T_{P2} express the power ON/OFF switches and their driving signals produced by the power management. C_i, L_i, S_i, and T_i $(i = 1, 2)$ represent individual capacitors, inductors, switches, and driving signals in the primary and secondary input circuit, respectively. C_a, L_a, D_{a1}, and D_{a2} are the auxiliary capacitor, inductor, and diodes of the auxiliary circuit. S_a and T_a are the auxiliary switch and its driving signal, which is generated by the PWM. C_o, V_o, I_o, and R_o describe the output capacitor, voltage, current, and equivalent load, respectively.

For the convenience of analyses, the simplified equivalent circuit is depicted in Fig. 2, and the directional definition of significant voltages and currents are labeled in this figure. The simplification in Fig. 2 is compliant with the following assumptions: 1) all power switches and diodes have ideal characteristics without considering voltage drops when these devices are conducted; 2) the capacitors C_a and C_o are large enough so that the voltage ripples due to switching are negligible and could be taken as constant voltage sources V_a and V_o; and 3) the power ON/OFF switches S_{P1} and S_{P2} are omitted. According to different power conditions, the operational states of the proposed converter can be divided into two states including a single power-supply state with only one input power source and a dual power-supply state with two input power sources. The powers produced by the voltage sources V_1 and V_2 are referred as P_1 and P_2, respectively, while the power consumed by the load is referred as P_o. If the condition of $P_1 > P_o$ $(P_2 > P_o)$ holds, the switch S_{P1} (S_{P2}) turns ON to supply the power with a single input power source V_1 (V_2). On the contrary, the switches S_{P1} and S_{P2} turn ON to supply the power with two input power sources if the conditions of $P_1 > P_o$ and $P_2 > P_o$ fail. The detailed operational stages are described as follows.

A. Single Power-Supply State

By turning off one power ON/OFF switch S_{P1} or S_{P2} for cutting off the connection between the power source and the converter, the other input power source V_2 or V_1 can supply alone for supporting the output demand. The primary input power supply is considered, for example, to explain how to operate in this state, i.e., the switch S_{P2} is always turned OFF and the switch S_2 is triggered all the while for minimizing the conduction loss. The switching period is defined as T_S. d_1 and d_a denote the duty cycles of the switch S_1 and S_a, respectively. d_d and $d_{\rm dcm}$ present the duty cycles of the dead time and the freewheeling time of the auxiliary inductor. Note that the auxiliary inductor is designed to operate in the DCM. The characteristic waveforms

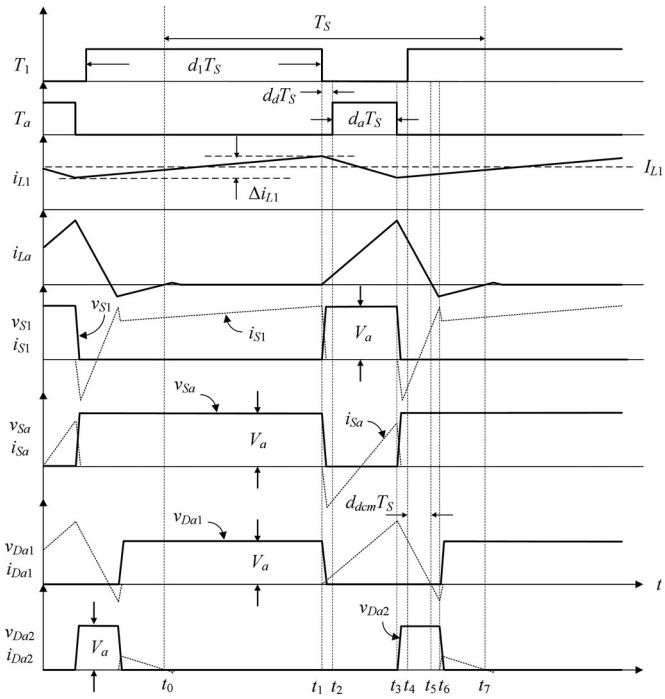

Fig. 3. Characteristic waveforms in single power-supply state.

and topological modes of the single power-supply state are depicted in Figs. 3 and 4, respectively. The complete operation modes in a switching period of the converter are discussed as follows.

Mode 1 [t_0–t_1]: At t_0, the auxiliary inductor current i_{La} returned to zero. The switch S_1 is continuously conducted and the auxiliary switch S_a is still turned OFF. The primary inductor L_1 is linearly charged by the primary input voltage V_1. The auxiliary switch voltage v_{Sa} is equal to the auxiliary capacitor voltage V_a.

Mode 2 [t_1–t_2]: At t_1, the switch S_1 is turned OFF, the switch voltage v_{S1} is rising to the auxiliary capacitor voltage V_a, and the auxiliary switch voltage v_{Sa} is decreasing to zero. The body diode of the auxiliary switch S_a is conducted for receiving the primary inductor current i_{L1} to charge the auxiliary capacitor. Therefore, the switch current i_{Sa} is negative. Besides, the auxiliary inductor current linearly increases, and its slope is dependent on the auxiliary inductor voltage v_{La}, which is equal to $V_a - V_o$. Continuously, the primary auxiliary diode D_{a1} is conducted.

Mode 3 [t_2–t_3]: At t_2, the auxiliary switch S_a is turned ON with ZVS because the body diode has been already conducted for carrying the primary inductor current i_{L1}. After the auxiliary inductor current i_{La} increases to be larger than the primary inductor current i_{L1}, the auxiliary switch current i_{Sa} becomes positive. The discharging current from the auxiliary capacitor together with the primary inductor current i_{L1} releases the stored energy to the output voltage V_o. During modes 2 to 3 ($t = t_1 - t_3$), the time interval can be written as $(d_d + d_a)T_S$. The auxiliary inductor current i_{La} and the primary inductor current i_{L1} can be expressed as

$$i_{La}(t) = \frac{(V_a - V_o)(t - t_1)}{L_a} \tag{1}$$

$$i_{L1}(t) = (I_{L1} + 0.5\Delta i_{L1}) + \frac{(V_1 - V_a)(t - t_1)}{L_1} \tag{2}$$

where I_{L1} is the average value of the primary inductor current i_{L1}, and Δi_{L1} is the corresponding peak-to-peak current ripple. Note that, the time interval (t_1–t_2) in mode 2 is extremely short so that it could be regarded as the same time in Fig. 4. At t_3, the maximum values of the auxiliary inductor current i_{La} can be calculated as

$$i_{La}(t_3) = \frac{(V_a - V_o)(d_d + d_a)T_S}{L_a}. \tag{3}$$

According to (2), the current ripple Δi_{L1} can be rewritten as

$$\Delta i_{L1} = \frac{(V_a - V_1)(d_d + d_a)T_S}{L_1}. \tag{4}$$

Mode 4 [t_3–t_4]: At t_3, the auxiliary switch S_a is turned OFF. Because the auxiliary inductor current i_{La} is greater than the primary inductor current i_{L1}, the parasitic capacitor of the auxiliary switch S_a is charged by the auxiliary inductor current i_{La} so that the auxiliary switch voltage v_{Sa} rises. At the same time, the energy stored in the parasitic capacitor of the switch S_1 will release to the output voltage V_o via the inductor current i_{La} so that the switch voltage v_{S1} decreases. The switch current i_{Sa} falls down to zero and the switch voltage v_{Sa} rises to the auxiliary capacitor voltage V_a. The body diode of the switch S_1 is conducted for carrying the differential current without strain. Besides, the auxiliary inductor voltage v_{La} is equal to $-V_o$, and the current i_{La} linearly decreases. The energy stored in the auxiliary inductor L_a starts to discharge into the output voltage V_o as freewheeling.

Mode 5 [t_4–t_5]: At t_4, the switch S_1 is turned ON with ZVS upon the condition that the auxiliary inductor current i_{La} is still larger than the primary inductor current i_{L1}. The auxiliary inductor current i_{La} continuously decreases with the slope $-V_o/L_a$. After the current i_{La} is smaller than the primary inductor current i_{L1}, the switch current i_{S1} is positive. During modes 4 to 5 ($t = t_3 - t_5$), the time interval can be written as $(d_d + d_{\rm dcm})T_S$. The auxiliary inductor current i_{La} and the primary inductor current i_{L1} can be expressed as

$$i_{La}(t) = \frac{[(V_a - V_o)(d_d + d_a)T_S - V_o(t - t_3)]}{L_a} \tag{5}$$

$$i_{L1}(t) = (I_{L1} - 0.5\Delta i_{L1}) + \frac{V_1(t - t_3)}{L_1}. \tag{6}$$

Mode 6 [t_5–t_6]: At t_5, the auxiliary inductor current i_{La} is equal to zero. Substituting $i_{La}(t_5) = 0$ into (7), the relation between the voltages V_a and V_o can be derived as

$$(V_a - V_o)(d_d + d_a) = V_o(d_d + d_{\rm dcm}). \tag{7}$$

In this mode, the parasitic capacitor of the primary auxiliary diode D_{a1} is charged by the output voltage V_o with a small reverse-recovery current.

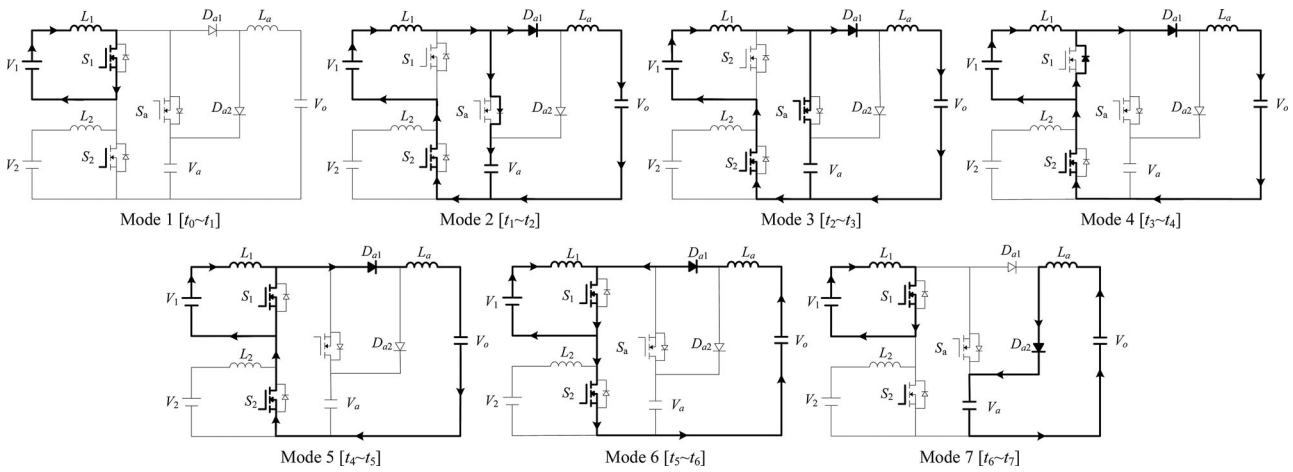

Fig. 4. Topological modes in single power-supply state.

Mode 7 [t_6–t_7]: At t_6, the diode voltage v_{Da1} is rising to the output voltage V_o, the secondary auxiliary diode D_{a2} is conducted for receiving the auxiliary inductor current i_{La} to charge the auxiliary capacitor voltage V_a, and then the auxiliary inductor current i_{La} returns to zero. In the single power-supply state with the primary input power, the switch S_{P2} is always turned OFF and the switch S_2 is triggered all the while. It means that the switch S_2 works as a synchronous rectifier for avoiding the current to flow through its body diode and reducing the power losses in modes 2–7 in Fig. 4.

According to the volt–second balance theory [20], the voltage–second production of the primary inductor L_1 in a switching period should be equal to zero. Thus, one can obtain

$$V_1(d_1 + d_d)T_S + (V_1 - V_a)(d_a + d_d)T_S = 0 \tag{8a}$$

$$V_1 = V_a(d_a + d_d). \tag{8b}$$

Assume that the dead-time duty cycle d_d is much smaller than the duty cycle of the switch d_1; the summation of the duty cycles d_1 and d_a approaches to 1. The relationships of (7) and (8b) can be represented as

$$V_o = \frac{(1-d_1)V_a}{(1+d_{\rm dcm}-d_1)} \tag{9a}$$

$$V_1 = (1-d_1)V_a \tag{9b}$$

$$\frac{V_o}{V_1} = \frac{1}{(1+d_{\rm dcm}-d_1)}. \tag{9c}$$

Because the average current of the output capacitor C_o should be zero over a switching period for a constant output voltage V_o, the balance equation can be expressed via (3) as

$$\frac{0.5(V_a - V_o)(1-d_1)T_S(1-d_1+d_{\rm dcm})}{L_a} = \frac{V_o}{R_o}. \tag{10}$$

From the algebraic operation via (9) and (10), the duty cycle and the voltage gain of the converter can be derived as

$$d_{\rm dcm} = 0.5(1-d_1)\left[\sqrt{1+\frac{8L_a}{R_oT_S(1-d_1)^2}} - 1\right] \tag{11a}$$

$$V_o = \frac{2V_1}{(1-d_1)\left[1+\sqrt{1+\dfrac{8L_a}{R_oT_S(1-d_1)^2}}\right]}. \tag{11b}$$

By the similar derivation process, the voltage gain of the single power-supply state with the secondary input power source also can be represented as

$$V_a = \frac{V_2}{(1-d_2)} \tag{12a}$$

$$V_o = \frac{2V_2}{(1-d_2)\left[1+\sqrt{1+\dfrac{8L_a}{R_oT_S(1-d_2)^2}}\right]} \tag{12b}$$

where d_2 denotes the duty cycle of the switch S_2.

B. Dual Power-Supply State

When the proposed converter is operated in the dual power-supply state with two input power sources, it can be taken as a superposition process of the primary and secondary input circuits. In this state, the summation of duty cycles d_1 and d_2 should be greater than 1, i.e., each of duty cycles d_1 and d_2 is securely greater than 0.5. Moreover, the symbols d_{a1} and d_{a2} denote the first and the second duty cycles of the switch S_a, respectively. $d_{\rm dcm1}$ and $d_{\rm dcm2}$ present the first and the second duty cycles of the freewheeling times of the auxiliary inductor. The auxiliary inductor is also designed to operate in the DCM. In order to explain the operational principle in the dual power-supply state easily, the following theoretical analysis is based on the assumption of $i_{L1} > i_{L2} > |i_{L1} - i_{L2}|$, where $|\cdot|$ is the absolute operator. The characteristic waveforms and topological modes of the dual power-supply state are depicted in Figs. 5 and 6, respectively. Note that the time intervals in modes 2, 4, 9, and 11 are extremely short so that each interval could be regarded as the same time in Fig. 5. The operation modes in this state are discussed as follows.

Mode 1 [t_0–t_1]: At t_0, the auxiliary inductor current i_{La} returned to zero. The switches S_1 and S_2 are continuously conducted. The auxiliary switch S_a is still turned OFF. The

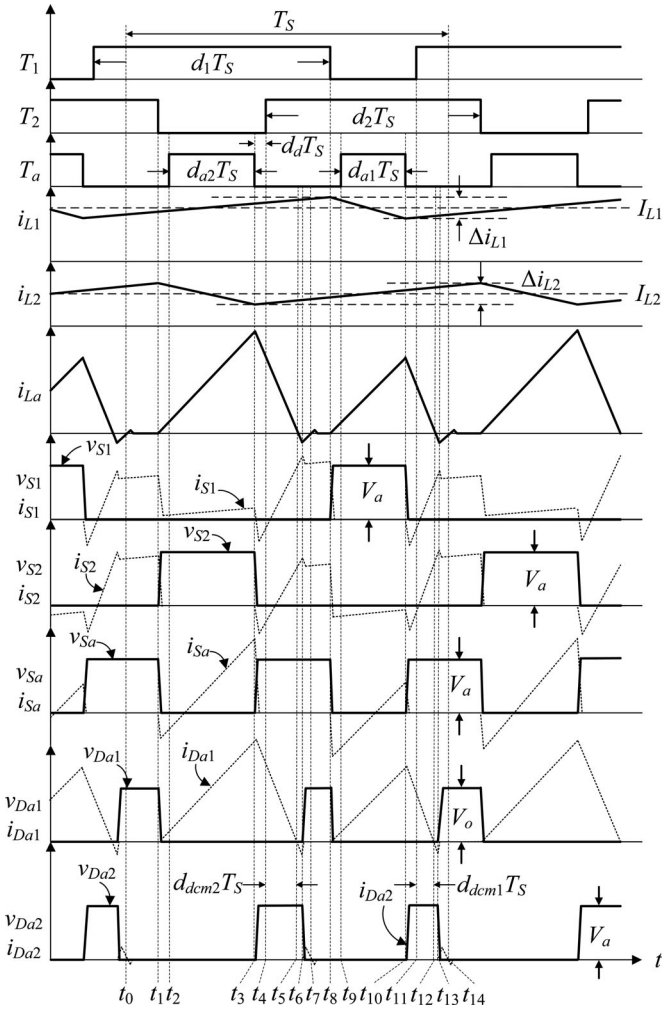

Fig. 5. Characteristic waveforms in dual power-supply state.

inductors L_1 and L_2 are linearly charged by the input voltages V_1 and V_2, respectively.

Mode 2 [t_1–t_2]: At t_1, the switch S_2 is turned OFF, the switch voltage v_{S2} is rising to the auxiliary capacitor voltage V_a, and the auxiliary switch voltage v_{Sa} is decreasing to zero. The body diode of the auxiliary switch S_a is conducted for receiving the secondary inductor current i_{L2} to charge the auxiliary capacitor. Therefore, the switch current i_{Sa} is negative. Besides, the auxiliary inductor current i_{La} linearly increases, and the slope is dependent on the auxiliary inductor voltage v_{La}, which is equal to $V_a - V_o$. Continuously, the primary auxiliary diode D_{a1} is conducted.

Mode 3 [t_2–t_3]: At t_2, the auxiliary switch S_a is turned ON with ZVS. After the auxiliary inductor current i_{La} increases to be larger than the secondary inductor current i_{L2}, the auxiliary switch current i_{Sa} becomes positive. The discharging current from the auxiliary capacitor together with the secondary inductor current i_{L2} releases the stored energy to the output voltage V_o. During modes 2 to 3 ($t = t_1 - t_3$), the time interval can be written as $(d_d + d_{a2})T_S$. The auxiliary inductor current i_{La} and the secondary inductor current i_{L2} can be expressed as

$$i_{La}(t) = \frac{(V_a - V_o)(t - t_1)}{L_a} \tag{13}$$

$$i_{L2}(t) = (I_{L2} + 0.5\Delta i_{L2}) + \frac{(V_2 - V_a)(t - t_1)}{L_2} \tag{14}$$

where I_{L2} is the average value of the secondary inductor current i_{L2}, and Δi_{L2} is the corresponding peak-to-peak current ripple. At t_3, the local maximum value of the auxiliary inductor current i_{La} can be calculated as

$$i_{La}(t_3) = \frac{(V_a - V_o)(d_d + d_{a2})T_S}{L_a}. \tag{15}$$

According to (14), the current ripple Δi_{L2} can be represented as

$$\Delta i_{L2} = \frac{(V_a - V_2)(d_d + d_{a2})T_S}{L_2}. \tag{16}$$

In addition, applying Kirchhoff's current law, the current loop equation is given by $i_{L1} = i_{S1} + i_{L2}$. The switch current i_{S1} can be expressed as $i_{L1} - i_{L2}$, and it is positive so far due to the current relationship $i_{L1} > i_{L2}$. By the topological design and switching mechanism, the conduction loss of the switch S_1 sustaining all the primary inductor current i_{L1} can be effectively reduced, especially in the low-voltage high-current clean-energy applications.

Mode 4 [t_3–t_4]: At t_3, the auxiliary switch S_a is turned OFF. Because the auxiliary inductor current i_{La} is greater than the secondary inductor current i_{L2}, the parasitic capacitor of the auxiliary switch S_a is charged by the auxiliary inductor current i_{La}, and the auxiliary switch voltage v_{Sa} rises. At the same time, the energy stored in the parasitic capacitor of the switch S_2 will release to the output voltage V_o via the inductor current i_{La}, and the switch voltage v_{S2} decreases. The switch current i_{Sa} falls down to zero and the switch voltage v_{Sa} rises to the auxiliary capacitor voltage V_a. The body diode of the switch S_2 is conducted for carrying the differential current without strain. Besides, the auxiliary inductor voltage v_{La} is equal to $-V_o$, and the current i_{La} linearly decreases. The energy stored in the auxiliary inductor L_a starts to discharge into the output voltage V_o as freewheeling.

Mode 5 [t_4–t_5]: At t_5, the switch S_2 is turned ON with ZVS upon the condition that the auxiliary inductor current i_{La} is still larger than the secondary inductor current i_{L2}. The auxiliary inductor current i_{La} continuously decreases with the slope $-V_o/L_a$. After the current i_{La} is smaller than the secondary inductor current i_{L2}, the switch current i_{S2} is positive. By the same way, the switch current i_{S1} becomes positive as well as i_{S2}. During modes 4 to 5 ($t = t_3 - t_5$), the time interval can be written as $(d_d + d_{\mathrm{dcm}2})T_S$. The auxiliary inductor current i_{La} and the secondary inductor current i_{L2} can be expressed as

$$i_{La}(t) = \frac{[(V_a - V_o)(d_d + d_{a2})T_S - V_o(t - t_3)]}{L_a} \tag{17}$$

$$i_{L2}(t) = (I_{L2} - 0.5\Delta i_{L2}) + \frac{V_2(t - t_3)}{L_2}. \tag{18}$$

Mode 6 [t_5–t_6]: At t_5, the auxiliary inductor current i_{La} is equal to zero. Substituting $i_{La}(t_5) = 0$ into (17), the relation between the voltages V_a and V_o can be derived as

$$(V_a - V_o)(d_d + d_{a2}) = V_o(d_d + d_{\mathrm{dcm}2}). \tag{19}$$

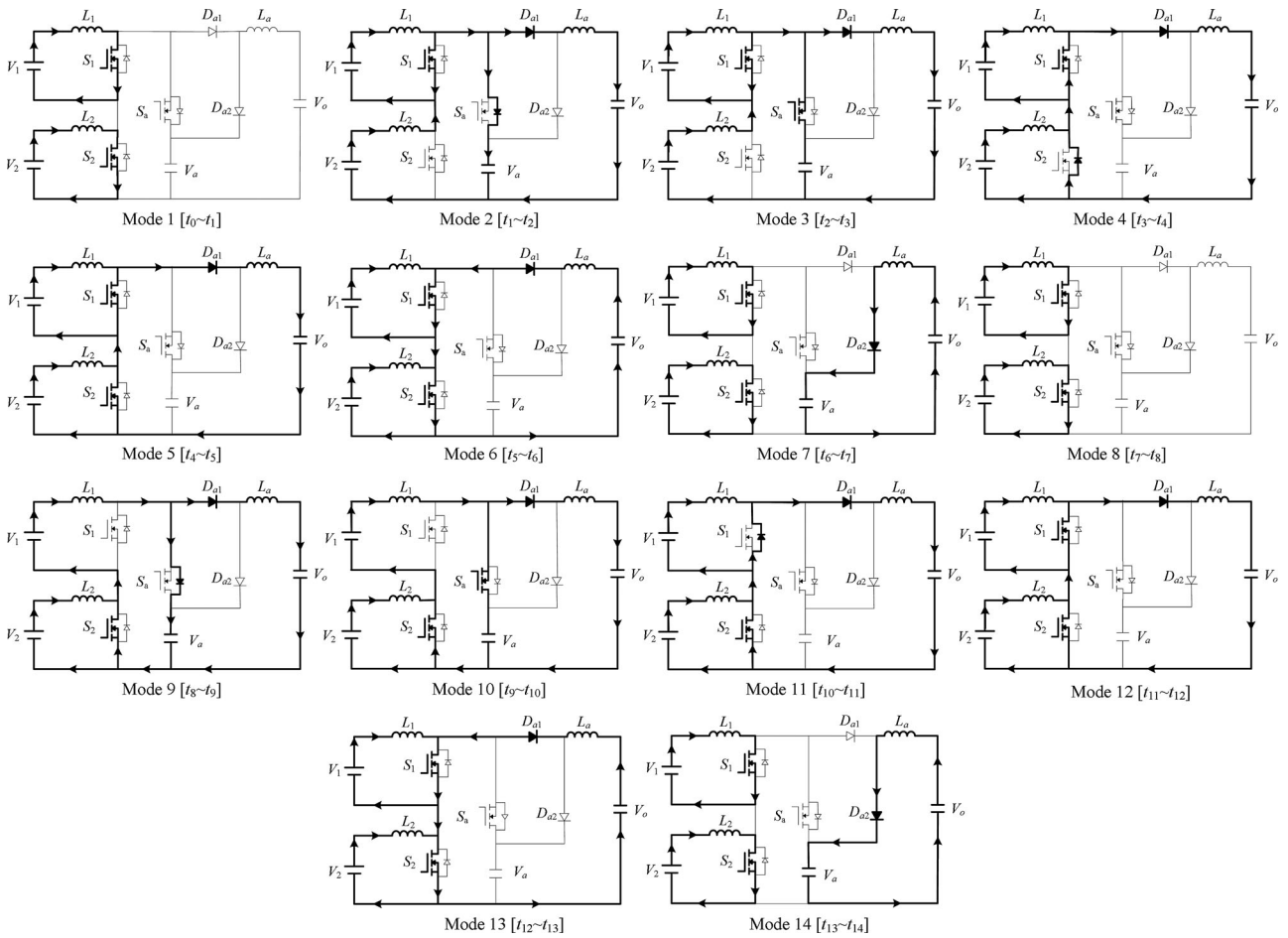

Fig. 6. Topological modes in dual power-supply state.

In this mode, the parasitic capacitor of the primary diode D_{a1} is charged by the output voltage V_o with a small reverse-recovery current.

Mode 7 [t_6–t_7]: At t_6, the diode voltage v_{Da1} is rising to the output voltage V_o, the secondary auxiliary diode D_{a2} is conducted for receiving the auxiliary inductor current i_{La} to charge the auxiliary capacitor.

Mode 8 [t_7–t_8]: At t_7, the auxiliary inductor current i_{La} returns to zero. The switches S_1 and S_2 are continuously conducted. Mode 8 is similar to mode 1.

Mode 9 [t_8–t_9]: At t_8, the switch S_1 is turned OFF, the switch voltage v_{S1} is rising to the auxiliary capacitor voltage V_a, and the auxiliary switch voltage v_{Sa} is decreasing to zero. The body diode of the auxiliary switch S_a is conducted for carrying the primary inductor current i_{L1} to charge the auxiliary capacitor. The auxiliary inductor current i_{La} linearly increases with the slope $(V_a - V_o)/L_a$. Continuously, the primary auxiliary diode D_{a1} is conducted.

Mode 10 [t_9–t_{10}]: At t_9, the auxiliary switch S_a is turned ON with ZVS. After the auxiliary inductor current i_{La} increases to be larger than the primary inductor current i_{L1}, the auxiliary switch current i_{Sa} becomes positive. The discharging current from the auxiliary capacitor together with the primary inductor current i_{L1} releases the stored energy to the output voltage V_o.

During modes 9 to 10 ($t = t_8 - t_{10}$), the time interval can be written as $(d_d + d_{a1})T_S$. The auxiliary inductor current i_{La} and the primary inductor current i_{L1} can be expressed as

$$i_{La}(t) = \frac{(V_a - V_o)(t - t_8)}{L_a} \tag{20}$$

$$i_{L1}(t) = (I_{L1} + 0.5\Delta i_{L1}) + \frac{(V_1 - V_a)(t - t_8)}{L_1}. \tag{21}$$

At t_{10}, the local maximum value of the auxiliary inductor current i_{La} can be calculated as

$$i_{La}(t_{10}) = \frac{(V_a - V_o)(d_d + d_{a1})T_S}{L_a}. \tag{22}$$

According to (21), the current ripple Δi_{L1} can be represented as

$$\Delta i_{L1} = \frac{(V_a - V_1)(d_d + d_{a1})T_S}{L_1}. \tag{23}$$

In addition, the switch current i_{S2} can be expressed as $i_{L2} - i_{L1}$, and it is negative. The conduction loss of the switch S_2 can be effectively reduced.

Mode 11 [t_{10}–t_{11}]: At t_{10}, the auxiliary switch S_a is turned OFF. Because the auxiliary inductor current i_{La} is greater than the primary inductor current i_{L1}, the parasitic capacitor of the

auxiliary switch S_a is charged by the auxiliary inductor current i_{La}. At the same time, the energy stored in the parasitic capacitor of the switch S_1 will release to the output voltage V_o via the inductor current i_{La}. The switch current i_{Sa} falls down to zero and the switch voltage v_{Sa} rises to the auxiliary capacitor voltage V_a. Similar to mode 4, both the switches' currents i_{S1} and i_{S2} are negative. The energy stored in the auxiliary inductor L_a starts to discharge into the output voltage V_o as freewheeling.

Mode 12 [t_{11}–t_{12}]: At t_{11}, the switch S_1 is turned ON with ZVS. The auxiliary inductor current i_{La} continuously decreases with the slope $-V_o/L_a$. After the current i_{La} is smaller than the primary inductor current i_{L1}, the switch current i_{S1} is positive. By the same way, the switch current i_{S2} becomes positive as well as i_{S1}. During modes 11 to 12 ($t = t_{10} \sim t_{12}$), the time interval can be written as $(d_d + d_{\rm dcm1})T_S$. The auxiliary inductor current i_{La} and the primary inductor current i_{L1} can be expressed as

$$i_{La}(t) = \frac{[(V_a - V_o)(d_d + d_{a1})T_S - V_o(t - t_{10})]}{L_a} \quad (24)$$

$$i_{L1}(t) = (I_{L1} - 0.5\Delta i_{L1}) + \frac{V_1(t - t_{10})}{L_1}. \quad (25)$$

Mode 13 [t_{12}–t_{13}]: At t_{12}, the auxiliary inductor current i_{La} is equal to zero. Substituting $i_{La}(t_{12}) = 0$ into (24), the relation between the voltages V_a and V_o can be derived as

$$(V_a - V_o)(d_d + d_{a1}) = V_o(d_d + d_{\rm dcm1}). \quad (26)$$

Mode 13 is similar to mode 6 as well as the reverse-recovery time of the primary auxiliary diode D_{a1}.

Mode 14 [t_{13}–t_{14}]: At t_{13}, the diode voltage v_{Da1} is rising to the output voltage V_o, and the secondary auxiliary diode D_{a2} is conducted for receiving the auxiliary inductor current i_{La} to charge the auxiliary capacitor.

According to the volt–second balance theory [20], the voltage–second productions of the inductors L_1 and L_2 in a switching period should be equal to zero. Thus, one can obtain

$$V_1(d_1 + d_d)T_S + (V_1 - V_a)(d_{a1} + d_d)T_S = 0 \quad (27a)$$

$$V_2(d_2 + d_d)T_S + (V_2 - V_a)(d_{a2} + d_d)T_S = 0 \quad (27b)$$

$$V_1 = (d_{a1} + d_d)V_a \quad (27c)$$

$$V_2 = (d_{a2} + d_d)V_a. \quad (27d)$$

Assume that the dead-time duty cycle d_d is much smaller than the duty cycles of the switches d_1 and d_2, the relationships of the voltages in (19), (26), (27c), and (27d) can be rewritten as

$$V_o = \frac{(1 - d_1)V_a}{(1 + d_{\rm dcm1} - d_1)} = \frac{(1 - d_2)V_a}{(1 + d_{\rm dcm2} - d_2)} \quad (28a)$$

$$V_a = \frac{V_1}{(1 - d_1)} = \frac{V_2}{(1 - d_2)} \quad (28b)$$

$$\frac{V_o}{V_1} = \frac{1}{(1 + d_{\rm dcm1} - d_1)} \quad (28c)$$

$$\frac{V_o}{V_2} = \frac{1}{(1 + d_{\rm dcm2} - d_2)}. \quad (28d)$$

Because the average current of the output capacitor C_o should be zero over a switching period for a constant output voltage V_o, the balance equation can be expressed as (29) shown at the bottom of this page.

From the algebraic operation via (28) and (29), the duty cycles and the voltage gain of the converter can be derived as

$$d_{\rm dcm1} = 0.5(1 - d_1)\left[\sqrt{1 + \frac{8L_a}{R_o T_S d_x}} - 1\right] \quad (30a)$$

$$d_{\rm dcm2} = 0.5(1 - d_2)\left[\sqrt{1 + \frac{8L_a}{R_o T_S d_x}} - 1\right] \quad (30b)$$

$$V_o = \frac{2V_1}{[(1 - d_1)(1 + \sqrt{1 + (8L_a/R_o T_S d_x)})]} = \frac{2V_2}{[(1 - d_2)\left(1 + \sqrt{1 + (8L_a/R_o T_S d_x)}\right)]} \quad (30c)$$

where the duty cycle d_x is defined as $[(1 - d_1)^2 + (1 - d_2)^2]$. From (30c), the following equation can be obtained:

$$\frac{V_1}{(1 - d_1)} = \frac{V_2}{(1 - d_2)}. \quad (31)$$

Equations (30c) and (31) state that the proposed converter can simultaneously boost both input power sources with different voltage levels to a stable output voltage via controlling the driving signals of the switches T_1, T_2, and T_a. Moreover, there exists only one pair of the duty cycles d_1 and d_2 according to specific input voltages. Note that the driving signal T_a is composed of T_1 and T_2 as shown in Fig. 5. First, one should make up the inverse signals of T_1 and T_2 as $\bar{T}_1$ and $\bar{T}_2$. Then, the inverse signals $\bar{T}_1$ and $\bar{T}_2$ are processed via delay time functions to synthesize the signals T_1' and T_2'. In the driving circuit, the control signals T_1' and T_2' are passed through logic OR gate IC to compose the driving signal T_a for the auxiliary switch.

In this study, a high-efficiency ZVS dual-input converter is investigated. The proposed converter utilizes the primary and secondary input circuits to be connected in series and operates in continuous conduction mode (CCM). The phenomenon of a high reverse-recovery current in a traditional step-up converter will be greatly alleviated via the utilization of an auxiliary inductor in series connected with a diode when the diode current falls to zero. If the primary and secondary input circuits are changed to connect in parallel, the primary inductor L_1 and the secondary inductor L_2 can be operated in DCM. In this case, the control signals for the primary and secondary input circuits are different from the ones for these two input circuits connected in

$$\frac{[(1 - d_1)(1 - d_1 + d_{\rm dcm1}) + (1 - d_2)(1 - d_2 + d_{\rm dcm2})](V_a - V_o)T_S}{2L_a} = \frac{V_o}{R_o}. \quad (29)$$

series. The control signals for the primary and secondary input circuits connected in parallel can be widely designed without regard to the series-inductor problem. Moreover, it would reduce the inductor volume and save two level shifter circuits for the floating switches. However, the primary inductor L_1 and the secondary inductor L_2 operated in DCM would cause the inductor currents i_{L1} and i_{L2} with higher peak values, so that the lifetime of the input power source (e.g., battery module or FC) will be degenerated. Besides, the DCM operation is not suitable for a high-power application.

Remark 1: As can be seen from Fig. 1, the proposed converter has the basic framework of the input part of a conventional boost converter plus an auxiliary circuit. Thus, the proposed converter can also be applied for more than two input sources, i.e., the additional power source with the same basic framework is connected in series with the original primary and secondary input circuits. As long as the control signals are appropriately designed, the turn-ON ZVS property for all switches can also be maintained. As the application to more than two input sources, the situation of inductors connected in series is also interdicted, and the allowable input voltage range of power sources will be shortened because the corresponding duty cycles are limited.

Remark 2: Although the voltage stresses over S_1, S_2, S_a, D_{a1}, and D_{a2} are higher than the output voltage in the proposed converter, the objective of high-efficiency power conversion can also be obtained because of the ZVS property for all switches and less reverse-recovery currents for all diodes. Park *et al.* [8] presented a soft-switching boost converter with an HI-bridge auxiliary resonant circuit, which made a partial resonant path for the main switch to perform soft switching under the zero-voltage condition, to obtain high-efficiency power conversion than a conventional boost converter. As far as our knowledge goes, no cascaded framework with two zero-voltage-transition boost converters has been reported. If the input terminal of the soft-switching boost converter in [8] is cascaded by the same connected way in Fig. 1 with an HI-bridge auxiliary resonant circuit to accept two input power sources, this cascaded dual-input boost converter may not maintain the soft-switching property all the time, and there are circulating currents in the resonant circuit during the resonant period. The improvements of the proposed ZVS dual-input converter in this study with comparison of the cascaded dual-input boost converter modified from [8] are as follows: 1) the ZVS property all the time; 2) no additional circulating current losses; and 3) higher power conversion efficiency.

III. Experimental Results

The proposed topology can be used to specific target applications for the high-voltage dc bus of an uninterruptible power supply or an inverter. The proposed converter can manipulate the high-efficiency power conversion with more than one input power source simultaneously to cope with the disadvantages of large size, complex topology, and expensive cost in conventional converter structure for individual power source. For an example of a hybrid PCS composed of two input power sources with an FC and a battery module, it has the following several merits: 1) it can manage the input power sources and improve system efficiency; 2) during the start of the system, the battery module powers the load to ensure that the FC cold starts easily; 3) when the load steps up, the battery module can provide the insufficient energy if the FC cannot respond quickly so that the dynamic characteristics of the entire system can be improved; and 4) the battery module can provide peak power so that the power rating of the FC can be decreased and the total cost of the whole system can be reduced.

In order to verify the effectiveness of the proposed ZVS dual-input converter, the corresponding experimental results are provided in this section. A power supply is used to emulate an FC taken as the primary power source with a maximum power of 2.5 kW, and the input voltage range is 120–170 V. Note that the summation of duty cycles d_1 and d_2 should be greater than 1 for regular operation in the dual power-supply state. Thus, each of duty cycles d_1 and d_2 should be bounded from a minimum value $d_{\min}$ to a maximum value $d_{\max}$. The minimum duty cycle $d_{\min}$ is designed to 0.55 slightly higher than a half of 1, and the maximum duty cycle $d_{\max}$ is designed to 0.83 for avoiding the lack of freewheeling time of the auxiliary inductor operating in DCM. According to the relation between input voltages and duty cycles in (31), the two input voltages should be in the same level. Therefore, the voltage range of another power supply is chosen as 120–170V for mimicking a battery module taken as the secondary power source with a maximum power of 2.5 kW. The proposed converter can boost the varied voltages of different power sources in the sense of hybrid power supply to a stable output dc voltage for the load demand. By considering the later inverter applications with 220 V_{ac}, the desired output dc voltage is set at 360 V and the maximum power of this converter prototype is 5 kW in this study. Two magnetic contactors (S-P50T), manufactured by Shihlin Company, are used to switch the power supply situation between the single power-supply state and the dual power-supply state in the proposed converter.

In the dual power-supply state, two control signals (V_{con1} and V_{con2}) are produced according to the control objectives of individual power sources for manipulating the driving signals (T_1 and T_2) in the primary input circuit and the secondary input circuit, respectively. Moreover, the driving signal T_1 is generated by comparing the control signal V_{con1} with one carrier wave (v_{tri1}), and the driving signal T_2 is generated by comparing the control signal V_{con2} with the other carrier wave (v_{tri2}). In order to satisfy the constraint on the summation of duty cycles d_1 and d_2 to be greater than 1, a phase shifter is used to make the carrier v_{tri2} with 180° phase shift in contrast to the carrier v_{tri1}. Thus, the overlap between the driving signals T_1 and T_2 can be guaranteed.

The volumes and weights of the inductors usually take the most of those in the converter, and the overall cost is also based on the prices of these passive components. Thus, the design of the inductor value becomes a key factor of the proposed converter, especially the auxiliary inductor L_a in the auxiliary circuit for proper operation. The design procedure of the inductors (L_1 and L_2) in the primary and secondary input circuits follows the conventional design method of a boost converter via considering an acceptable ripple current drawn by the

input power source [20]. In this study, the values of $L_1 = 800$ and $L_2 = 800\,\mu$H are selected. The auxiliary capacitor voltage V_a shown in (9b) and (28b) has a maximum value of 1000 V in the theoretical analysis because of the maximum duty cycle $d_{\max} = 0.83$ and the maximum input voltage $V_{1,\max} = 170$ V. Therefore, the auxiliary switch S_a is chosen as a MOSFET IXFL60N80P with a breakdown voltage of 800 V. According to mode 6 in the single power-supply state, the discontinuous conduction period ($d_{\rm dcm}T_S$) should be less than the turned-ON period of the switch (d_1T_S) in Fig. 3. By considering a maximum output power $P_o = 2.5$ kW ($R_o = 51.84\ \Omega$) with the minimum input voltage $V_{1,\min} = 120$ V and the switching period $T_S = 25\,\mu$s in the single power-supply state, the auxiliary inductor L_a should be smaller than $35\,\mu$H according to (11a) and $d_{\max} = 0.83$. Moreover, the discontinuous conduction periods $d_{\rm dcm1}T_S$ and $d_{\rm dcm2}T_S$ shown in Fig. 5 should be both smaller than the overlap period $0.5(d_1 + d_2 - 1)$, while the switches S_1 and S_2 are turned ON in the dual power-supply state. According to (30c), the value of the auxiliary inductor is chosen as $L_a = 35\,\mu$H for compensating the nonideal electric characteristic and guaranteeing the voltage gain of the proposed dual-input converter.

For solving the problem of the output voltage variations with different loads, a proportional-integral (PI) feedback controller is utilized to ensure the system stability of the proposed converter, and a digital signal processor (DSP) TMS320F2812 manufactured by Texas Instruments is adopted to achieve this goal of feedback control. The driving signals are generated by the DSP and peripheral logic circuits. At the beginning, there are some fluctuations in the output voltage according to (9) and (28) if the duty ratios d_1 and d_2 are not satisfied with (11) and (31) under the occurrence of noises and control delays. Fortunately, the output voltage fluctuation will be sensed for the feedback controller in the DSP to adaptively modify the corresponding duty ratios so that a stable output dc voltage can be ultimately obtained. The prototype with the specifications given in Table I is designed to illustrate the effectiveness of the proposed converter. The proposed converter not only can be used for a single power source to obtain high-efficiency conversion, but also can be effectively operated at the dual power-supply state. Note that under the same output power, the conduction frequency of the auxiliary circuit at the dual power-supply state exceeds the one at the single power-supply state, so that it will increase the conduction losses at the dual power-supply state. Therefore, the power conversion efficiency of the single power-supply state is higher than the one of the dual power-supply state.

TABLE I
CONVERTER COMPONENTS AND PARAMETERS

Components	Symbols	Parameters
Primary inductor	L_1	800 μH
Secondary inductor	L_2	800 μH
Auxiliary inductor	L_a	35 μH
Primary capacitor	C_1	100 μF×4
Secondary capacitor	C_2	100 μF×4
Auxiliary capacitor	C_a	4.75 μF×2
Output capacitor	C_o	40 μF×2
Switching frequency	f_S	40kHz
Switches	S_1, S_2, S_a	IXFL60N80P
Diode	D_{a1}, D_{a2}	MUR1560

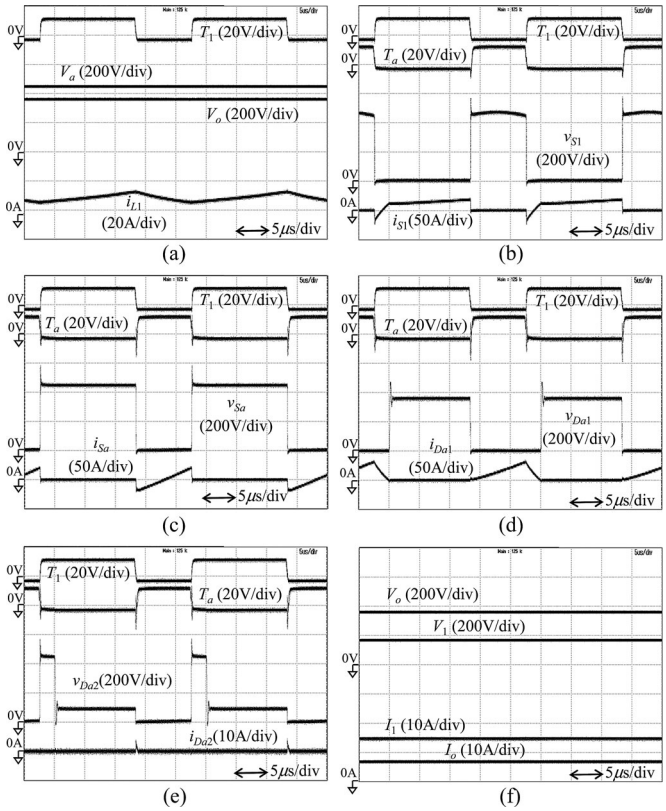

Fig. 7. (a)–(f) Experimental results at single power-supply state with closed-loop voltage control, $V_1 = 170$ V, and 2.5-kW output power.

A. Single Power-Supply State

For examining the performance of the single power-supply state with the primary input power source, the experimental results with an input voltage $V_1 = 170$ V and an output power of 2.5 kW are depicted in Fig. 7. The proposed converter under the closed-loop voltage control indeed produces a constant output voltage of 360 V via the DSP module written within a PI feedback control law. Fig. 7(a) presents the driving signal T_1, the auxiliary capacitor voltage V_a, the output voltage V_o, and the primary inductor current i_{L1}. The auxiliary capacitor voltage V_a is nearly a constant voltage of 450 V, and the output voltage V_o is kept 360 V as a stable dc output under the PI feedback control. The primary inductor current i_{L1} with an average value of 14.7 A is continuously charged and discharged in the CCM, so that the current is always positive with a small current ripple for avoiding the life-cycle degradation of the power source. The driving signals T_1 and T_a, the switch voltage v_{S1}, and current i_{S1} are depicted in Fig. 7(b). The driving signals (T_1 and T_a)

appear complementarily. By observing the switch voltage v_{S1} and current i_{S1}, the characteristic of turning on with ZVS is obvious due to the current is negative before the switch is turned ON. Fig. 7(c) shows the driving signals (T_1 and T_a), the switch voltage v_{Sa}, and current i_{Sa}. The ZVS turn ON of the switch S_a can also be achieved. The auxiliary capacitor C_a receiving the primary inductor current i_{L1} at first, then the energy is released to the output terminal by the positive current i_{Sa}. Fig. 7(d) illustrates the driving signals (T_1 and T_a), the prime auxiliary diode voltage v_{Da1}, and current i_{Da1}. It states that the diode current i_{Da1} climbs with the slope $(V_a - V_o)/L_a$ and falls with the slope V_o/L_a. Moreover, the phenomenon of a huge reverse-recovery current disappears via the utilization of an auxiliary inductor series connected with a diode when the diode current falls to zero in comparison with the traditional step-up converters. The driving signals (T_1 and T_a), the second auxiliary diode voltage v_{Da2}, and current i_{Da2} are depicted in Fig. 7(e). The second auxiliary diode D_{a2} is conducted for receiving the auxiliary inductor current i_{La} to charge the auxiliary capacitor. Fig. 7(f) shows the input/output voltage and current waveforms. When the input voltage is $V_1 = 170$ V, the output voltage V_o can be controlled to 360 V and the maximum output voltage ripple is less than 3.5 V (0.97%).

Fig. 8 shows the experimental input/output voltage and current responses of the dual-input converter at the single power-supply state due to different input voltages and varied output powers, where the response of $V_1 = 120$ V with 1143 W output power is depicted in Fig. 8(a); the response of $V_1 = 170$ V with 1143 W output power is depicted in Fig. 8(b); the response of the output power variation between 1143 and 1541 W is depicted in Fig. 8(c). From the measurable data, the conversion efficiency due to the load variation between 1143 and 1541 W is varied between 97% and 95.8% in Fig. 8(c). As can be seen from this figure, the robustness of the proposed dual-input converter with the closed-loop PI voltage control under different input voltages and varied output powers is obvious. Fig. 9 performs the conversion efficiency at the single power-supply state with the closed-loop PI voltage control. The measured conditions are set with a primary input power source of $V_1 = 170$ V and a constant output voltage of $V_o = 360$ V. From the experimental results, the maximum efficiency is measured to be about 97% due to the ZVS property of all switches.

By considering the possible applications of the proposed dual-input converter with the constant current control, Fig. 10 shows the experimental results at the single power-supply state with the closed-loop PI current control. In this experiment, the test conditions are set with $V_2 = 170$ V, 2.1-kW output power, and the desired input current $I_2 = 13$ A. In practical applications, the current of the input power source (not the inductor current) is sensed for the control utilization because the source current is smoother than the inductor current with charge/discharge slope. The proposed converter under the closed-loop current control indeed produces a constant input current of $I_2 = 13$ A via the DSP module written within a PI feedback control law. Fig. 10(a) presents the driving signal T_2, the auxiliary capacitor voltage V_a, the output voltage V_o, and the secondary inductor current i_{L2}. The auxiliary capacitor voltage V_a is nearly a constant

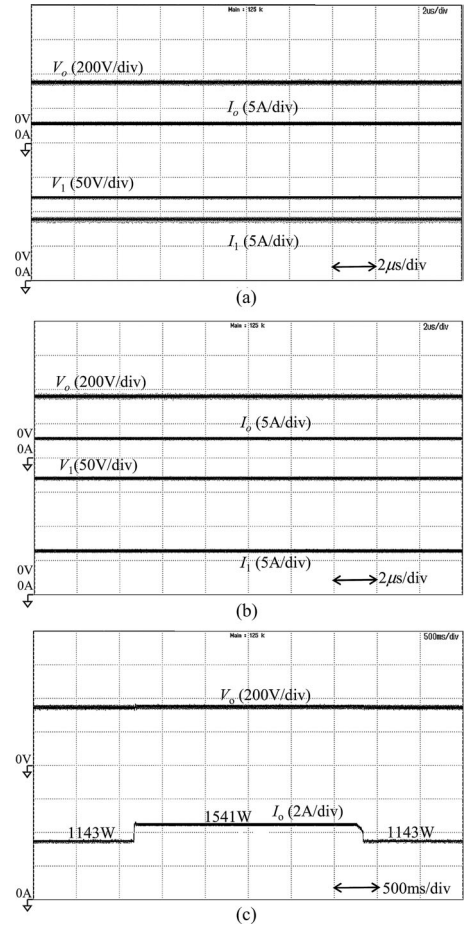

Fig. 8. (a)–(c) Experimental input/output voltage and current responses of dual-input converter at single power-supply state with closed-loop voltage control due to varied input voltage and output power. (a) $V_1 = 120$ V with 1143-W output power, (b) $V_1 = 170$ V with 1143-W output power, and (c) output power variation between 1143 and 1541 W.

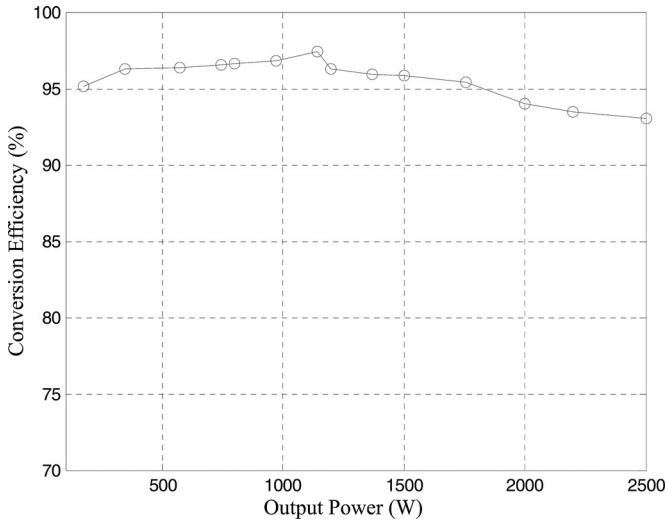

Fig. 9. Conversion efficiency at single power-supply state with closed-loop voltage control and $V_1 = 170$ V.

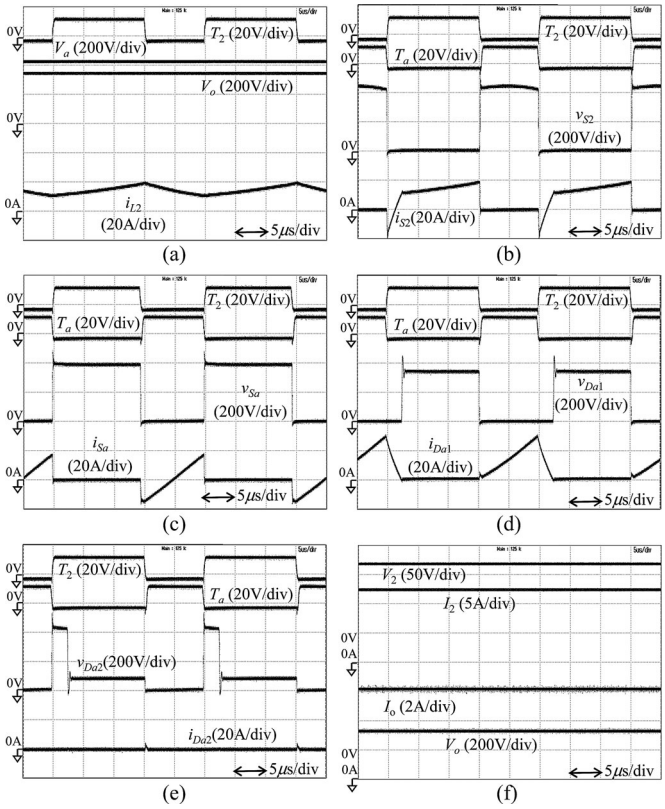

Fig. 10. (a)–(f) Experimental results at single power-supply state with closed-loop current control, $V_2 = 170$ V, and 2.1-kW output power.

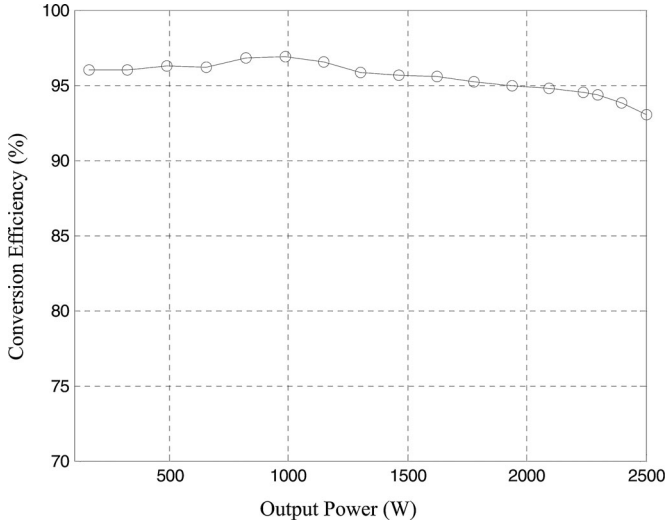

Fig. 11. Conversion efficiency at single power-supply state with closed-loop current control and $V_2 = 170$ V.

voltage of 450 V. The secondary inductor current i_{L2} is continuously charged and discharged in CCM, so that the current is always positive with a small current ripple for avoiding the life-cycle degradation of the power source. The driving signals T_2 and T_a, the switch voltage v_{S2}, and current i_{S2} are depicted in Fig. 10(b). The driving signals (T_2 and T_a) appear complementarily. By observing the switch voltage v_{S2} and current i_{S2}, the characteristic of turning ON with ZVS is obvious due to the current is negative before the switch is turned ON. Fig. 10(c) shows the driving signals (T_2 and T_a), the switch voltage v_{Sa}, and current i_{Sa}. The ZVS turn ON of the switch S_a also can be achieved. The auxiliary capacitor C_a receiving the secondary inductor current i_{L2} at first, then the energy is released to the output terminal by the positive current i_{Sa}. Fig. 10(d) illustrates the driving signals (T_2 and T_a), the prime auxiliary diode voltage v_{Da1}, and current i_{Da1}. It states that the diode current i_{Da1} climbs with the slope $(V_a - V_o)/L_a$ and falls with the slope V_o/L_a. Moreover, the phenomenon of a huge reverse-recovery current disappears via the utilization of an auxiliary inductor series connected with a diode when the diode current falls to zero in comparison with the traditional step-up converters. The driving signals (T_1 and T_a), the second auxiliary diode voltage v_{Da2}, and current i_{Da2} are depicted in Fig. 10(e). The second auxiliary diode D_{a2} is conducted for receiving the auxiliary inductor current i_{La} to charge the auxiliary capacitor. Fig. 10(f) shows the input/output voltage and current waveforms. When the input voltage is $V_2 = 170$ V, the input current I_2 can be controlled to 13 A. Fig. 11 performs the conversion efficiency at the single power-supply state with the closed-loop current control and $V_2 = 170$ V. From the experimental results, the maximum efficiency is measured to be about 96.8% due to the ZVS property of all switches. The aforementioned experimental results agree well with those obtained from theoretical analyses given in Section II-A.

B. Dual Power-Supply State

The experimental results of the proposed dual-input converter at the dual power-supply state with $V_1 = 120$ V, $V_2 = 170$ V, and a 2-kW output power are depicted in Fig. 12. By implementing the PI feedback voltage control laws in the DSP module, the goals of a stably controlled output voltage $V_o = 360$ V and a 95% high-efficiency power conversion can be concurrently achieved. Fig. 12(a) presents the driving signals (T_1, T_2, and T_a) and the output voltage V_o. The driving signals satisfy the theoretical ones as shown in Fig. 6, and the output voltage V_o can be regulated at the desired value of 360 V in the dual power-supply state. The driving signal T_1, the primary inductor current i_{L1}, the switch voltage v_{S1}, and current i_{S1} are depicted in Fig. 12(b). Moreover, the driving signal T_2, the secondary inductor current i_{L2}, the switch voltage v_{S2}, and current i_{S2} are displayed in Fig. 12(c). Both the inductors L_1 and L_2 are charged and discharged by turns in the CCM so that the currents i_{L1} and i_{L2} rise and fall above the horizontal. By observing the switch voltages and currents in Fig. 12(b) and (c), the characteristics of turning ON with ZVS of the switches S_1 and S_2 are obvious. In addition, the switch current i_{S1} is equal to the primary inductor current i_{L1} when the switch S_1 is turned on. After the switch S_2 is turned ON, the present switch current i_{S1} falls to $i_{L1} - i_{L2}$. On the other hand, the switch current i_{S2} appears negative and equal to $i_{L2} - i_{L1}$ after the switch S_1 is turned ON, it reveals that the conduction losses of the switches are indeed reduced. Fig. 12(d) shows the driving signal T_a, the auxiliary capacitor voltage V_a, the switch voltage v_{Sa}, and current i_{Sa}.

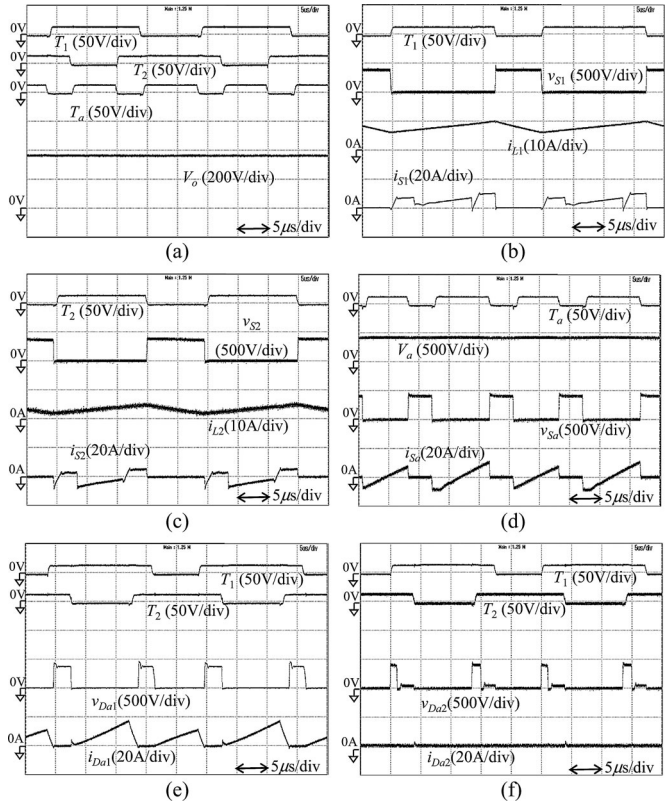

Fig. 12. (a)–(f) Experimental results at dual power-supply state with closed-loop voltage control, $V_1 = 120$ V, $V_2 = 170$ V, and 2-kW output power.

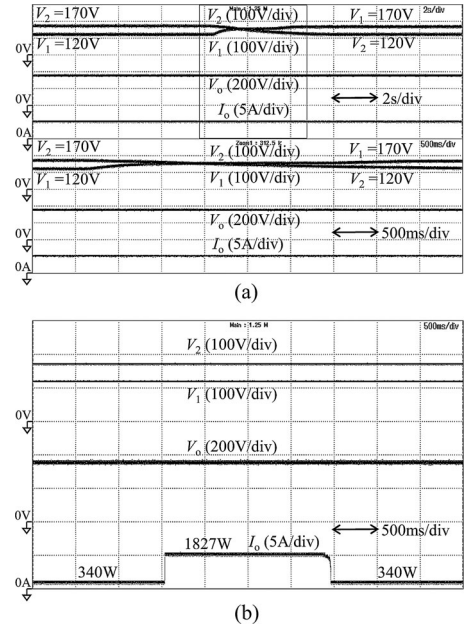

Fig. 13. (a), (b) Experimental input/output voltage and current responses of dual-input converter at dual power-supply state due to varied input voltage and output power. (a) Input voltage variation between 120 and 170 V with 1827-W output power. (b) Output power variation between 340 and 1827 W.

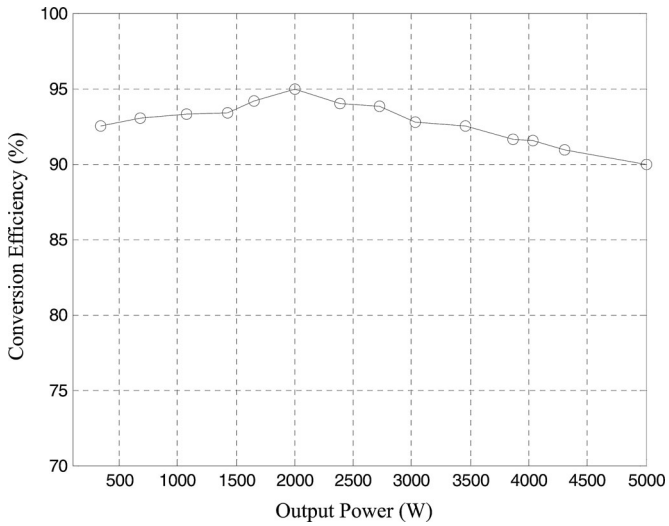

Fig. 14. Conversion efficiency at dual power-supply state with closed-loop voltage control, $V_1 = 120$ V, and $V_2 = 170$ V.

The auxiliary capacitor voltage is nearly constant agree with the assumption in Section II. The ZVS turn ON of the switch S_a with a negative starting current provides a path for the inductor current i_{L1} or i_{L2}. The different initial negative values of the current i_{Sa} indicate the peak values of the inductor currents i_{L1} and i_{L2}. Fig. 12(e) illustrates the driving signals (T_1 and T_2), the prime auxiliary diode voltage v_{Da1}, and current i_{Da1}. The diode current i_{Da1} appears linearly rising and falling in the DCM for charging the output capacitor. Fig. 12(f) performs the driving signals (T_1 and T_2), the second auxiliary diode voltage v_{Da2}, and current i_{Da2}. The second auxiliary diode D_{a2} is conducted for receiving the auxiliary inductor current i_{La} to charge the auxiliary capacitor. Fig. 13 exhibits the experimental output voltage regulation characteristics against the change of the two input voltages and load, where the response of the input voltage variation between 120 and 170 V with 1827-W output power is depicted in Fig. 13(a); the response of the output power variation between 340 and 1827 W is depicted in Fig. 13(b). From the measurable data, the conversion efficiency due to the load variation between 340 and 1827 W is varied between 92.5% and 94.7% in Fig. 13(b). As can be seen from this figure, the robustness of the proposed dual-input converter at the dual power-supply state under different input voltages and varied output powers is obvious.

Fig. 14 shows the conversion efficiency at the dual power-supply state with the closed-loop voltage control. The efficiency of the proposed converter is defined as the output power dividing by the summation of the input powers. The operation conditions are set with the primary input power source of $V_1 = 120$ V and the secondary input power source of $V_2 = 170$ V. From the experimental results, the maximum efficiency is measured to be about 95% because the conduction loss can be effectively reduced by the proposed topology and switching mechanism. The aforementioned experimental results agree well with those obtained from theoretical analyses given in Section II-B.

IV. Conclusion

This study has successfully developed a ZVS dual-input converter with hybrid power sources. The effectiveness of this converter is also verified by the experimental results. In the single power-supply state, the property of ZVS turn ON of all switches guarantees that switching losses can be reduced. In the dual power-supply state, the conduction loss can be effectively reduced by topological design of series connection of two input circuits. Besides, the reverse-recovery currents of the diodes are slight as well as the switching losses of the switches are effectively reduced. The maximum efficiency of the proposed converter operated in both operational states is higher than 95%. This new converter topology provides designers with an alternative choice to simultaneously convert hybrid power sources. In addition, the proposed high-efficiency dual-input converter also can work well in high-power level applications because the switching losses can be greatly reduced due to the ZVS property.

In general, the ground leakage current would be harmful to high-power nonisolated PV applications due to the presence of a parasitic capacitance between the PV cells and the metal frame of the PV panel, usually connected to earth. Xiao and Xie [21] focused on the leakage current suppressing method by considering all common-mode paths and presented a new full-bridge-type converter structure and a compensation strategy for half-bridge-type inverter. Yu *et al*. [22] studied a two-stage PV ac-module application including a nonisolated high step-up dc/dc converter and a newly designed H6-type dc/ac inverter to feature high efficiency over a wide load range, low ground leakage current, no need for split capacitors, and low-output ac-current distortion. If the proposed ZVS dual-input converter in this study is used for nonisolated PV applications, the ground leakage current issue due to the high-frequency voltage swing between the two negative terminals of the input sources also may cause safety and electromagnetic interference (EMI) problems because the input power sources do not share the same ground. These problems could be solved by the adoption of an EMI filter [21] for a dc power supply application or the integration with advanced inverter topologies [22] for an ac-module application in the future research.

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