High-Efficiency Modular High Step-Up Interleaved Boost Converter for DC-Microgrid Applications

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***Abstract*—In this paper, a modular interleaved boost converter is first proposed by integrating a forward energy-delivering circuit with a voltage-doubler to achieve high step-up ratio and high efficiency for dc-microgrid applications. Then, steady-state analyses are made to show the merits of the proposed converter module. For closed-loop control design, the corresponding small-signal model is also derived. It is seen that, for higher power applications, more modules can be paralleled to increase the power rating and the dynamic performance. As an illustration, closed-loop control of a 450-W rating converter consisting of two paralleled modules with 24-V input and 200-V output is implemented for demonstration. Experimental results show that the modular high step-up boost converter can achieve an efficiency of 95.8% approximately.**

***Index Terms*—DC microgrid, high step-up converter, modeling and parallel operation control.**

I. Introduction

In RECENT years, due to the public concern about global warming and climate change, much effort has been focused on the development of environmentally friendly distributed generation (DG) technologies [1]–[4]. It is well known that when many DGs are connected to utility grids, they can cause problems such as voltage rise and protection problem in the utility grid [5]–[8]. To solve these problems, new concepts of electric power systems are proposed, and dc microgrid is one of the solutions [9]–[12]. DC microgrid is suitable to use where most of the loads are sensitive dc electronic equipment. The advantage of a dc microgrid is that loads, sources, and energy storage can be connected through simpler and more efficient power electronic interfaces. Moreover, it is not necessary to process ac power quality issues. So far, dc microgrids have been used in telecom power systems, data centers system, generating stations, traction power systems, and residential houses [13]–[15]. Briefly speaking, the output voltages of most distributed energy resources such as fuel cells and photovoltaic (PV) are usually relatively low, requiring a high step-up converter for practical applications [16]–[19].

Recently, an interleaved boost converter extended by magnetically coupling a Ćuk-type auxiliary step-up circuit that charges a voltage-doubler in the output was proposed to achieve the required voltage gain [18]. As a similar solution, a sepic-integrated boost converter which provides an additional step-up gain with the help of an isolated sepic-type auxiliary step-up circuit was also proposed [19]. Nevertheless, the circuit structures of the Ćuk/sepic integrated high step-up converters are relatively complex and expensive; thus, they might be difficult to mass manufacture. In addition, considering the practical situation, the maximum output voltage and power efficiency will be affected by the parasitic effects such as winding resistances of inductors for the Ćuk/sepic integrated circuits. For small to medium power capacity (25 W $\sim$ 250 W), the forward circuit topology has less components and smaller volume than that of the Ćuk/sepic auxiliary step-up circuits, which makes the forward-type circuit another choice to implement the auxiliary circuit scheme.

The main objective of this paper is to develop a modular high-efficiency high step-up boost converter with a forward energy-delivering circuit integrated voltage-doubler as an interface for dc-microgrid system applications. In the proposed topology, the inherent energy self-resetting capability of auxiliary transformer can be achieved without any resetting winding. Moreover, advantages of the proposed converter module such as low switcher voltage stress, lower duty ratio, and higher voltage transfer ratio features are obtained. Steady-state analyses are also made to show the merits of the proposed converter topology. For further understanding the dynamic characteristic, small-signal models of the proposed converter are derived by using state-space averaging technique. For higher power applications, modules of the high step-up converters are paralleled to further reduce the input and output ripples. Analysis and control of the overall system are also made. Finally, a 450-W rating prototype system is constructed for verifying the validity of the operation principle. Experimental results show that the highest efficiency of 95.8% can be achieved.

II. Operation Principle

The proposed interleaved converter topology with high voltage transfer ratio is proposed as shown in Fig. 1. It can be seen from Fig. 1, the proposed converter consists of two-phase circuits with interleaved operation. The first phase is a boost

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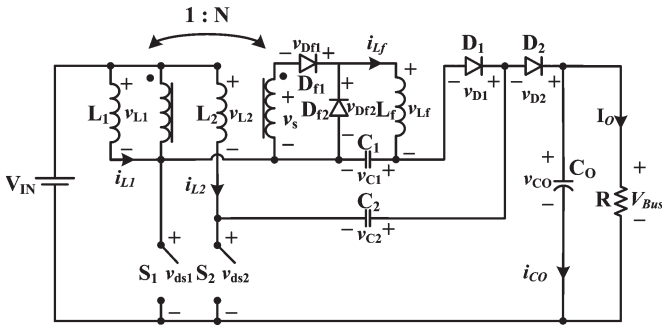


Fig. 1. Proposed modular high step-up boost converter topology.

integrating the forward-type circuit structure, which includes inductor L_1 and switch S_1 for the boost and an isolated forward energy-delivering circuit with turn ratio N. The second phase of the proposed converter is a boost circuit which contains inductor L_2, switch S_2, blocking capacitor C_2, and diode D_2 followed by the common output capacitor $C_{\rm o}$. From Fig. 1, one can see that the proposed converter is basically based on the conventional voltage-doubler [21] for the second phase circuit. However, for the first phase, in order to reduce the voltage stress of switch S_1 and diode D_1, an additional blocking capacitor C_1, is added to function as that of C_2 for the second phase. The operation principle can be described by considering the key waveforms of the proposed converter as shown in Fig. 2. For simplicity, assume that all the components in Fig. 1 including the high-frequency transformer of the forward energy-delivering circuit are assumed ideal and under steady-state condition.

As the main objective is to obtain high voltage gain and such characteristic is achieved when the duty cycle is greater than 0.5, hence, the steady-state analysis is made only for this case. It is important to point out that the proposed high step-up converter can also function for duty cycle lower than 0.5. However, with duty cycle lower than 0.5, the secondary induction voltage of the transformer is lower, and consequently, it is not possible to get the high voltage gain as that for duty ratio greater than 0.5. In addition, with duty cycle larger than 0.5, due to the charge balance of the blocking capacitor, the converter features automatic current sharing of the currents through the two interleaved phases that obviates any current-sharing control circuit [21], [27]. In comparison, when duty cycle is smaller than 0.5, the converter does not possess the automatic current-sharing capability any more, current-sharing control between each phases should be taken into account in this condition.

From Fig. 2, one can see that when the duty ratio is greater than 50%, there are four operation modes according to the ON/OFF status of the active switches. Referring to the key waveforms shown in Fig. 2, the operating principle of the proposed converter can be explained briefly as follows.

Mode 1 $[t_0 < t \leq t_1]$*:* From Fig. 2, one can see that for mode 1, switches S_1, S_2 are turned on. Diode $D_{\rm f1}$ is forward biased, while diodes $D_1, D_2, D_{\rm f2}$ are reverse biased. During this operation mode, both $i_{\rm L1}$ and $i_{\rm L2}$ are increasing to store energy in L_1 and L_2, respectively. Meanwhile, the input power is delivered to the secondary side through the isolation transformer and inductor $L_{\rm f}$ to charge capacitor C_1. Also, the

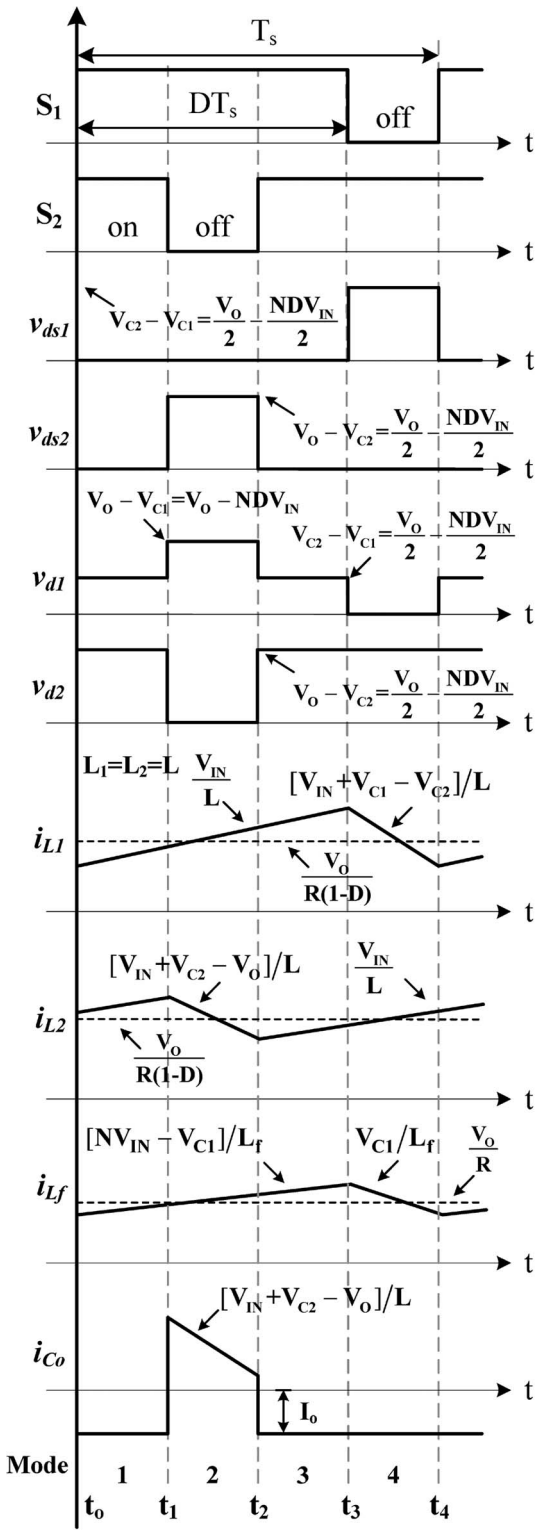


Fig. 2. Key waveforms of the proposed converter.

output power is supplied from capacitor $C_{\rm o}$. The voltage across inductances L_1 and L_2 can be represented as follows:

$$L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} = V_{\rm IN}. \tag{1}$$

Mode 2 $[t_1 < t \leq t_2]$*:* For this operation mode, switch S_1 remains conducting, and S_2 is turned off. Also, diodes D_1 and

D_{f2} remain reverse biased, D_2 and D_{f1} are forward biased. The energy stored in inductor L_2 is now released through C_2 and D_2 to the output. However, the first phase circuit including the forward-type converter remains the same. The voltage across inductances L_1 and L_2 can be represented as the following:

$$L_1\frac{di_{L1}}{dt} = V_{\rm IN} \tag{2}$$

$$L_2\frac{di_{L2}}{dt} = V_{\rm IN} + v_{C2} - V_{\rm Bus}. \tag{3}$$

Modes 3 $[t_2 < t \le t_3]$*:* For this operation mode, both S_1 and S_2 are turned on. The corresponding operating principle turns out to be the same as Mode 1.

Mode 4 $[t_3 < t \le t_4]$*:* During this operation mode, S_1 is turned off, and S_2 is turned on. Diode D_2 and D_{f1} are reverse biased, and diode D_1 is forward biased. Since diode D_{f1} is reverse biased, diode D_{f2} must turn on to conduct the inductor current $i_{\rm Lf.}$. The energy stored in L_1 is now released through C_1 and D_1 to charge capacitor C_2 for compensating the lost charges in previous modes. The energy stored in transformer is now treated to perform the self-resetting operation without additional resetting winding. Also, the output power is supplied from capacitor $C_{\rm o}$. The voltage across inductances L_1 and L_2 can be represented as follows:

$$L_1\frac{di_{L1}}{dt} = V_{\rm IN} + v_{C1} - v_{C2} \tag{4}$$

$$L_2\frac{di_{L2}}{dt} = V_{\rm IN}. \tag{5}$$

III. Steady-State Analysis

The capacitor average voltage $V_{\rm C1}$ can be derived as follows, which is equal to the average voltage across diode D_{f2}:

$$V_{C1} = V_{Df2,avg} = DNV_{\rm IN}. \tag{6}$$

The average voltage across diode D_1 can be described as

$$\begin{aligned} V_{D1,avg} &= V_{C2} - V_{C1} \\ &= (V_{C2} - V_{C1})(2D-1) \\ &\quad + (V_{\rm Bus} - V_{C1})(1-D). \end{aligned} \tag{7}$$

From (6) and (7), the capacitor voltage $V_{\rm C2}$ can be obtained as follows:

$$V_{C2} = \frac{V_{\rm Bus} + V_{C1}}{2} = (V_{\rm Bus} + DNV_{\rm IN})/2. \tag{8}$$

As to the voltage conversion ratio of the proposed converter, it can be calculated according to the volt-second balance principle of the boost inductors. From (1), (2) and (4), the volt-second balance equation for boost inductor L_1 becomes

$$\frac{V_{\rm IN}}{L_1}DT_s + \frac{(V_{\rm IN} + V_{C1} - V_{C2})}{L_1}(1-D)T_s = 0. \tag{9}$$

TABLE I
Gain and Stress Comparison for Three Converters

Gain /Stress	Two-Phase Interleaved	Voltage-Doubler	Proposed Converter
M	$\frac{1}{1-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}+ND$
$M_{\rm s}$	1	0.5	$\frac{M-ND}{2M}$
$M_{\rm D1}$	1	1	$1-\frac{DN}{M}$
$M_{\rm D2}$	1	0.5	$0.5\times(1-\frac{DN}{M})$

Thus, from (6), (8) and (9), the voltage conversion ratio M of the proposed converter can be obtained as follows:

$$M = \frac{V_{\rm Bus}}{V_{\rm IN}} = \frac{2}{1-D} + ND. \tag{10}$$

The open circuit voltage stress of switches S_1 and S_2 can be obtained directly as follows:

$$V_{S1,\max} = V_{C2} - V_{C1} \tag{11}$$

$$V_{S2,\max} = V_{\rm Bus} - V_{C2}. \tag{12}$$

It follows from (6), (8) and (10) that the same voltage stress is obtained for both active switches as follows:

$$V_{S,\max} = V_{S1,\max} = V_{S2,\max} = \frac{V_{\rm Bus}}{2} - \frac{NDV_{\rm IN}}{2}. \tag{13}$$

For convenient comparison, the normalized voltage stress of the active switches, namely M_S, can be expressed as

$$M_S = \frac{V_{S,\max}}{V_{\rm Bus}} = \frac{M-ND}{2M}. \tag{14}$$

In fact, one can see from (13) that the resulting voltage stress is obviously smaller than $V_{\rm Bus}/2$. Naturally, both conduction and switching losses can be reduced as well.

Similarly, the open circuit voltage stress of the corresponding diodes can be expressed as follows:

$$V_{D1,\max} = V_{\rm Bus} - V_{C1} = V_{\rm Bus} - DNV_{\rm IN} \tag{15}$$

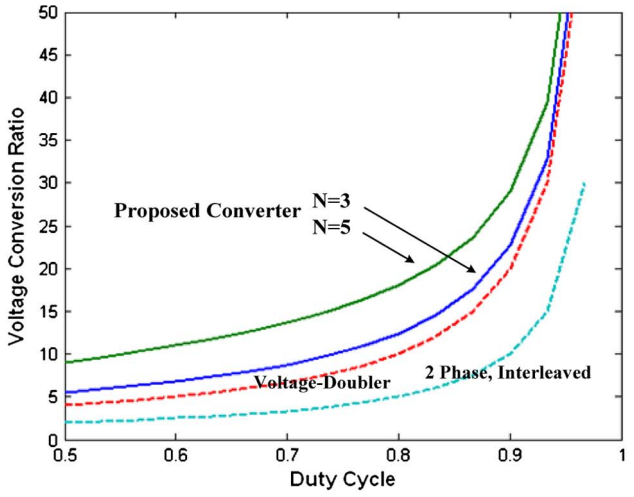
$$V_{D2,\max} = V_{\rm Bus} - V_{C2} = \frac{V_{\rm Bus}}{2} - \frac{DNV_{\rm IN}}{2}. \tag{16}$$

It follows from (15) and (16) that the corresponding normalized voltage stress becomes

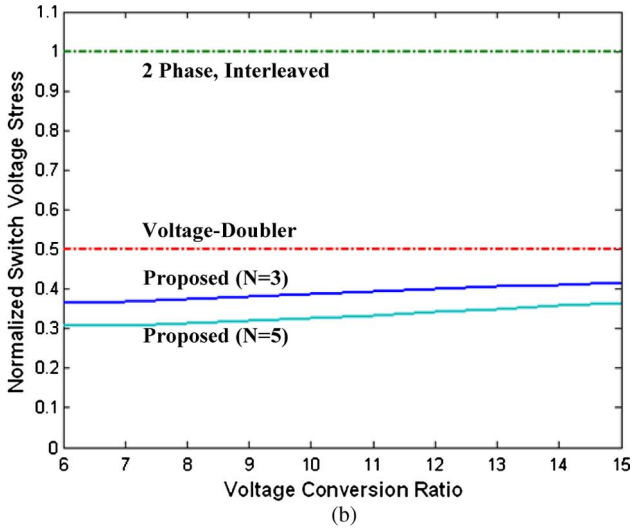
$$M_{D1} = \frac{V_{D1,\max}}{V_O} = 1 - \frac{DN}{M} \tag{17}$$

$$M_{D2} = \frac{V_{D2,\max}}{V_O} = \frac{1}{2} - \frac{DN}{2M} = \frac{M_{D1}}{2}. \tag{18}$$

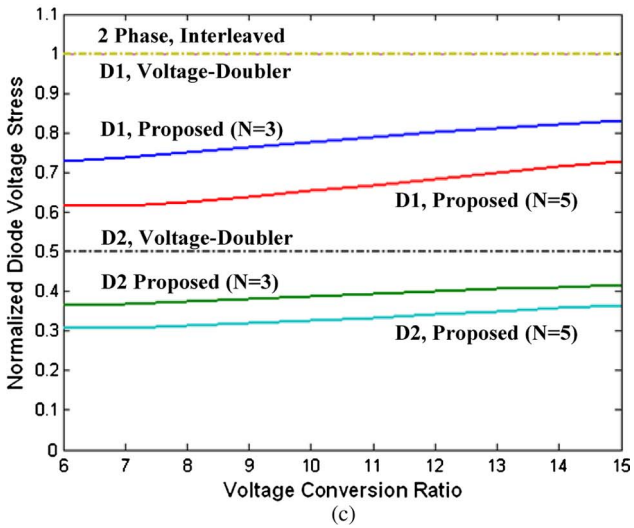
Table I summarizes the voltage gain and normalized voltage stress of key components of active as well as passive switches for reference. As an illustration, Fig. 3 shows the characteristic analyses of the proposed converter. For comparison, the voltage gains, switch stresses, and output diode stresses of the



(a)



(b)



(c)

Fig. 3. Characteristic analyses of the proposed converter: (a) voltage conversion ratio comparisons, (b) normalized switch voltage stress under different voltage conversion ratio, and (c) normalized diode voltage stress under different voltage conversion ratio.

conventional voltage-doubler [21] and the conventional two-phase interleaved boost converter [23] are also shown to provide better view.

It is seen from Fig. 3(a) that, much higher voltage gain can be achieved than that of the other two boost converters. As compared with conventional voltage-doubler and the conventional two-phase interleaved boost converter, an additional voltage gain ND can be obtained for the proposed converter by integrating the forward energy-delivering circuit. In addition, higher turn ratio N can also be chosen to get even higher voltage gain. Therefore, the proposed converter is rather suitable for use in boost-operation applications. From Fig. 3(b), one can see that the proposed converter can achieve the lowest voltage stress for the active switches. Also, it is seen that the proposed converter can achieve the lowest voltage stress for the diodes. As a result, one can expect that with proper design, the proposed converter can adopt switch components with lower voltage ratings to achieve higher efficiency.

The aforementioned steady-state continuous conduction mode (CCM) analysis of the proposed converter is described in detail. It is particularly useful for fuel cells and PV system applications. As to the discontinuous conduction mode (DCM) operation, although it is possible to yield a larger output voltage and a smaller duty cycle as compared to the CCM operation, however, the resulting output voltage is more sensitive to changes in duty cycle. Therefore, the design of the feedback circuit is more critical. In fact, the peak-to-peak input current ripple in DCM is so large as to reduce the life time of the fuel-cell stack [18], [29] and the extracted maximum power of PV system [30], the corresponding efficiency of system will be reduced as well. Therefore, the operation of the converter in DCM is not suitable for low-voltage DG system applications, and only the CCM is considered in this paper.

IV. Modeling of the Proposed Modular Converter

The state-space averaged model of the proposed converter is derived under the following assumptions: 1) power switches and diodes are ideal; 2) equivalent series resistances (ESRs) of all inductors and capacitors of proposed converter are considered to obtain a relatively precise dynamic model; 3) converter is operated under CCM, and is in steady state. First, from Fig. 2, it is straightforward to find that the corresponding weighting factors for the four operation modes are $(d-1/2)$, $(1-d)$, $(d-1/2)$, and $(1-d)$ in sequence, respectively. Thus, one can apply the state-space averaging technique to combine the state equations of different modes into the following state-space averaged equation in matrix form as shown in (19), where x is the state vector, matrices A, B, and C are constant matrices, u is the input, and y is the output

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx \end{aligned} \tag{19}$$

where

$$\begin{aligned} x^T &= [i_{L1} \quad i_{L2} \quad i_{Lf} \quad v_{C1} \quad v_{C2} \quad v_{CO}] \\ u &= [V_{\mathrm{IN}}]; \quad y = [v_O]. \end{aligned} \tag{20}$$

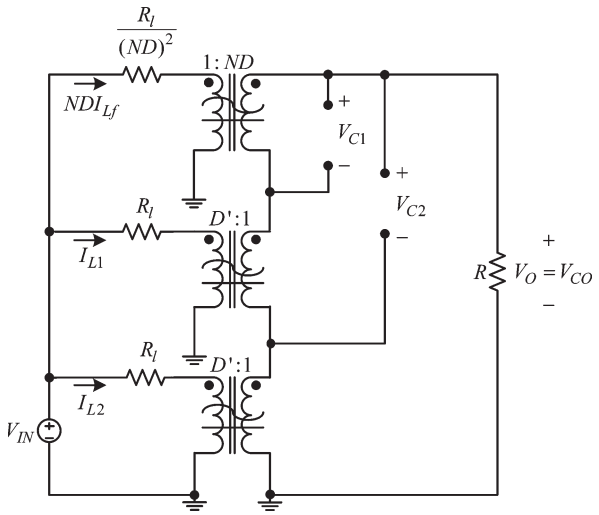


Fig. 4. Equivalent circuit of dc model of proposed converter.

The corresponding state coefficient matrices A can be expressed as (21), shown at the bottom of this page. The other state coefficient matrices are shown in

$$B^T = \begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_2} & \frac{DN}{L_f} & 0 & 0 & 0 \end{bmatrix} \tag{22}$$

$$C = \begin{bmatrix} 0 & \frac{(1-D)R \cdot R_{co}}{R+R_{co}} & 0 & 0 & 0 & \frac{R}{R+R_{co}} \end{bmatrix}. \tag{23}$$

Then, perturb the averaged state equation to yield steady state (dc) as well as dynamic (ac) linear terms and eliminate the higher order terms. Finally, the corresponding dc and ac models of the proposed converter can therefore be procured as well, respectively.

A. DC Model

To simplify the mathematics, relationships between ESRs of all inductors and capacitors are assumed to be the same. Thus, one can get the operation point of proposed converter as shown in Appendix. Considering the practical situation, main ESRs of all capacitors R_c are much smaller than load resistance ($R \gg R_c$), the equivalent circuit of the dc model can be expressed as shown in Fig. 4.

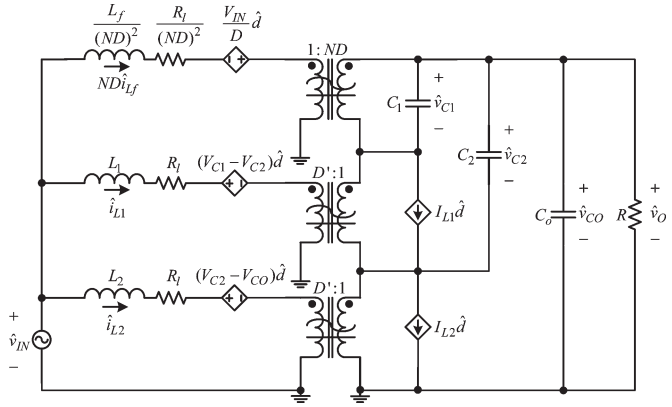


Fig. 5. Equivalent circuit of ac model of proposed converter.

B. AC Model

Similarly, the ac model of the proposed converter can be procured as follows:

$$\begin{aligned} \dot{\hat{x}} &= A'\hat{x} + B'\hat{u} + E\hat{d} \\ \hat{y} &= C'\hat{x} + F\hat{d}. \end{aligned} \tag{24}$$

In (24), matrices B', C', and F are defined in (25)–(27), respectively. The corresponding state coefficient matrices A' and E can be expressed as (28) and (29), shown at the bottom of the next page.

$$B'^T = \begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_2} & \frac{DN}{L_f} & 0 & 0 & 0 \end{bmatrix} \tag{25}$$

$$C' = \begin{bmatrix} 0 & \frac{(1-D)R \cdot R_{co}}{R+R_{co}} & 0 & 0 & 0 & \frac{R}{R+R_{co}} \end{bmatrix} \tag{26}$$

$$F = \begin{bmatrix} \frac{-R \cdot R_{co}}{R+R_{co}} I_{L2} \end{bmatrix} \tag{27}$$

Again, considering all ESRs of inductors are assumed to be the same and neglecting main ESRs of all capacitors, the equivalent circuit of the ac model of proposed converter can be illustrated in Fig. 5.

V. Parallel Operation Control

The module-paralleled converter configuration offers higher input and output ripple frequency, and increased reliability [20]–[28]. In order to satisfy the demands of low-voltage and

$$A = \begin{bmatrix} \frac{-[R_{l1}+(1-D)(R_{c1}+R_{c2})]}{L_1} & 0 & 0 & \frac{(1-D)}{L_1} & \frac{-(1-D)}{L_1} & 0 \\ 0 & \frac{-\left[R_{l2}+\left(\frac{R \cdot R_{co}}{R+R_{co}}+R_{c2}\right)(1-D)\right]}{L_2} & 0 & 0 & \frac{(1-D)}{L_2} & \frac{-R(1-D)}{L_2(R+R_{co})} \\ 0 & 0 & \frac{-R_{lf}-R_{c1}}{L_f} & \frac{-1}{L_f} & 0 & 0 \\ \frac{-(1-D)}{C_1} & 0 & \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{(1-D)}{C_2} & \frac{-(1-D)}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{(1-D)R}{C_O(R+R_{co})} & 0 & 0 & 0 & \frac{-1}{C_O(R+R_{co})} \end{bmatrix} \tag{21}$$

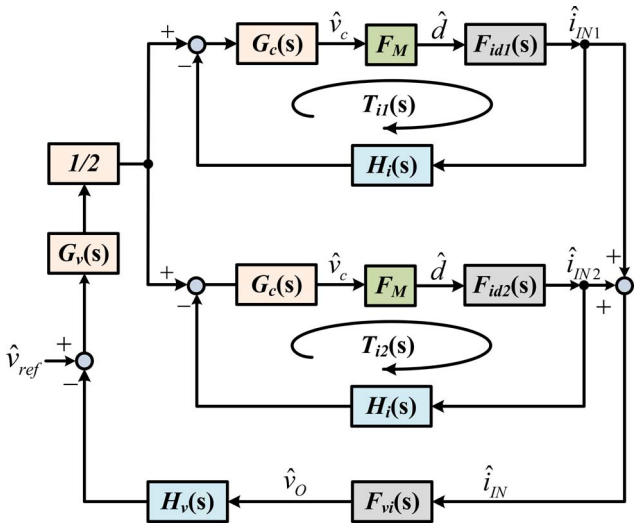


Fig. 6. Closed-loop control scheme for the module-parallel converter system.

high-current distributed power sources, a two-module parallel high step-up converter system is now given for demonstration.

For convenient design of the closed-loop controller, these two power modules are now assumed identical and with paralleled operation without the inherent circulating current phenomenon, and the simplified small-signal model of equivalent single module can therefore be obtained [20], [23], [28].

For direct control of the input current, current controller is necessary to regulate the source current at desired value. Moreover, in order to effectively reduce the input current ripple, equal current sharing between the two input inductors is necessary. On the other hand, output voltage should be well regulated during the load variations. Therefore, a closed-loop voltage controller with current sharing is designed for the proposed converter.

Fig. 6 shows the developed closed-loop control scheme for the parallel two-module high step-up converters system. It can be seen that instead of controlling the output voltage of each module, the output voltage is sensed and compared with the reference voltage. The output voltage controller generates the total input current reference for the whole system. The reference input current of each module is half of the total input current reference. Due to the single-module converter features current autobalance characteristic, equal current sharing between the four interleaved phases can be also obtained.

In the inner current control loop as shown in Fig. 6, F_M is the constant gain of the PWM generator; $G_c(s)$ represents the transfer function of current controllers, and $H_i(s)$ is the transfer function of the current sensor combined with first-order low-pass filter; $F_{id1}(s)$ and $F_{id2}(s)$ are small-signal transfer functions from duty cycle to individual input current of each module.

In the outer voltage control loop, $G_v(s)$ is the transfer function of output voltage controller, $H_v(s)$ is the transfer function of the voltage sensor combined with first-order low-pass filter. $F_{vi}(s)$ is the transfer function that relates the output voltage with the total input current of the two-module parallel converter system.

From Fig. 6, overall closed-loop transfer function of the two-module parallel converter system can be derived as

$$T(s)=\frac{\hat{v}_O}{\hat{v}_{ref}}=\frac{\frac{1}{2}T_i(s)G_v(s)F_{vi}(s)H_v(s)}{1+\frac{1}{2}T_i(s)G_v(s)F_{vi}(s)H_v(s)} \tag{30}$$

where

$$T_i(s)=\frac{G_c(s)F_MF_{id1}(s)H_i(s)}{1+G_c(s)F_MF_{id1}(s)H_i(s)}+\frac{G_c(s)F_MF_{id2}(s)H_i(s)}{1+G_c(s)F_MF_{id2}(s)H_i(s)}. \tag{31}$$

In order to provide sufficient dc gain, bandwidth, gain/phase margins for the system, two simple two-pole one-zero proportional-integral controllers are used in this paper for the current/voltage loop compensation.

The corresponding current/voltage controllers are selected as

$$\begin{cases} G_c(s)=4.03\cdot\frac{1+s/4.2\times10^2}{s(1+s/1.3\times10^4)} \\ G_v(s)=1210\cdot\frac{1+s/3.6\times10^2}{s(1+s/0.84\times10^4)} \end{cases}. \tag{32}$$

Fig. 7(a) shows the frequency response of uncompensated and compensated current loop $F_MG_c(s)F_{id1}(s)H_i(s)$, under both nominal and light-load conditions. As can be seen, this design results in a phase margin of 60°, and a gain margin of 3 dB, the crossover frequency is about 1 kHz for both nominal and light-load conditions. Fig. 7(b) shows the frequency response of uncompensated and compensated voltage

$$A'=\begin{bmatrix} \frac{-[R_{l1}+(1-D)(R_{c1}+R_{c2})]}{L_1} & 0 & 0 & \frac{(1-D)}{L_1} & \frac{-(1-D)}{L_1} & 0 \\ 0 & \frac{-\left[R_{l2}+\left(\frac{R\cdot R_{co}}{R+R_{co}}+R_{c2}\right)(1-D)\right]}{L_2} & 0 & 0 & \frac{(1-D)}{L_2} & \frac{-R(1-D)}{L_2(R+R_{co})} \\ 0 & 0 & \frac{-R_{lf}-R_{c1}}{L_f} & \frac{-1}{L_f} & 0 & 0 \\ \frac{-(1-D)}{C_1} & 0 & \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{(1-D)}{C_2} & \frac{-(1-D)}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{(1-D)R}{C_O(R+R_{co})} & 0 & 0 & 0 & \frac{-1}{C_O(R+R_{co})} \end{bmatrix} \tag{28}$$

$$E^T=\begin{bmatrix} \frac{(R_{c1}+R_{c2})I_{L1}-V_{C1}+V_{C2}}{L_1} & \frac{\left(\frac{R\cdot R_{co}}{R+R_{co}}+R_{c2}\right)I_{L2}-V_{C2}+\frac{R\cdot V_{CO}}{R+R_{co}}}{L_2} & \frac{NV_{\rm IN}}{L_f} & \frac{I_{L1}}{C_1} & \frac{I_{L2}-I_{L1}}{C_2} & \frac{-RI_{L2}}{(R+R_{co})C_O} \end{bmatrix} \tag{29}$$

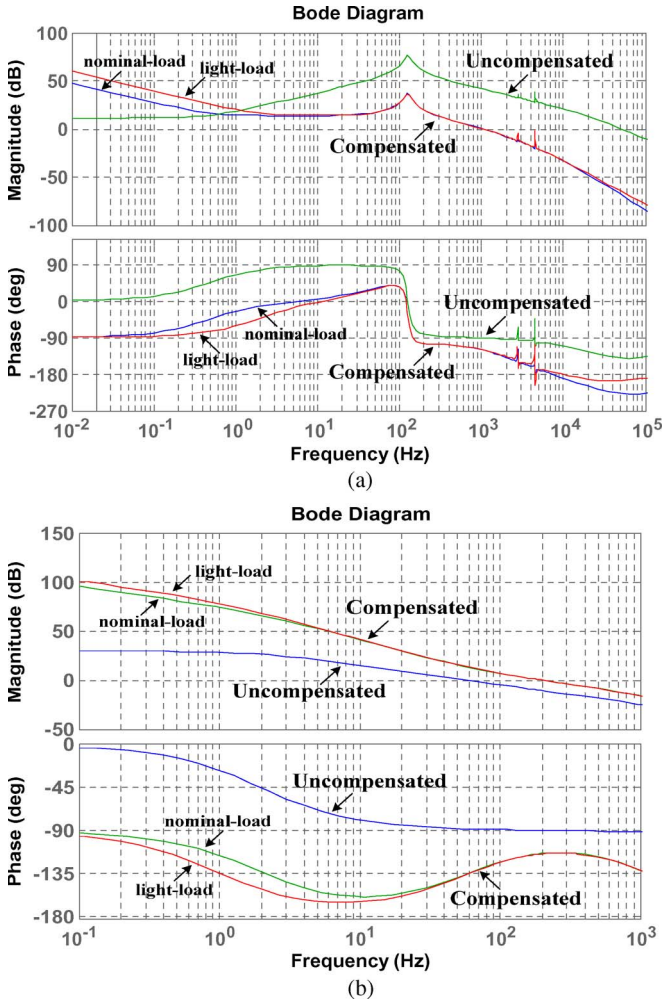


Fig. 7. Frequency responses of uncompensated and compensated (a) current loop and (b) voltage loop.

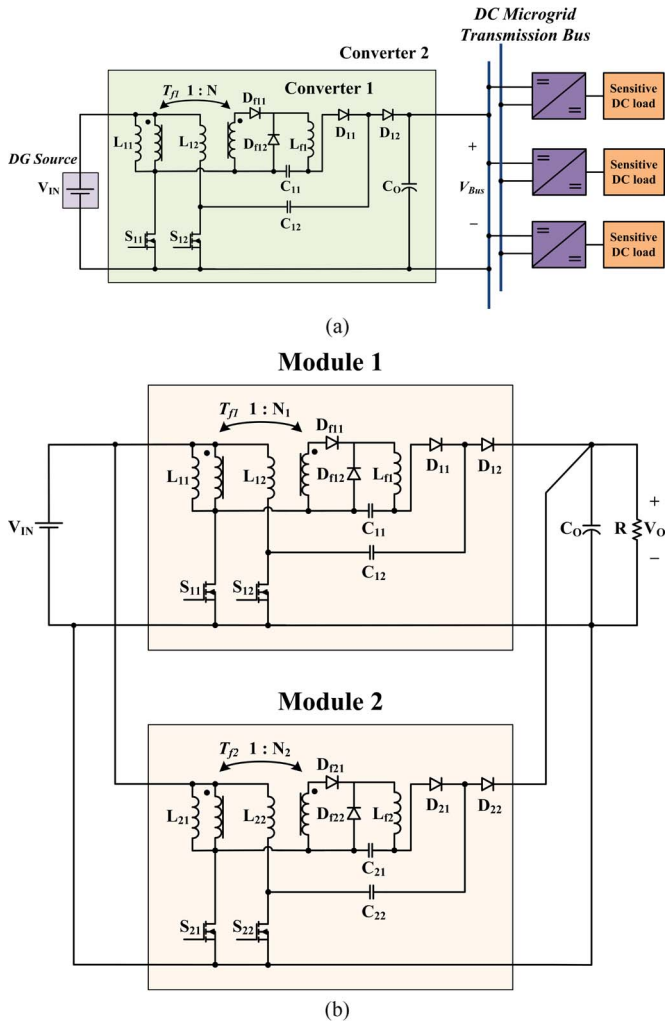


Fig. 8. Proposed high step-up converter module for dc-microgrid systems. (a) System configuration. (b) Schematic diagram for experimental prototype.

loop $G_v(s)F_{vi}(s)H_v(s)/H_i(s)$, under both nominal and light-load conditions. This design results in a phase margin of 65.6°, and a gain margin of 22.3 dB, the crossover frequency is about 200 Hz for both nominal and light-load conditions. Though the controller is designed based on two identical modules, it is applicable to the practical circuit when the two modules are not exactly the same.

VI. Experimental Results

To verify the feasibility of the proposed principle, a two-module paralleled system with the 24-V input, 200-V/450-W output, and switching frequency f_s of 50 kHz specifications was constructed as shown in Fig. 8. The corresponding circuit component parameters of the two power modules for the prototype system are selected and listed in Table II.

Fig. 9 shows the measured gate signals of the converter system. It can be seen that from Fig. 9, during one switching cycle T_s, each switch conducts for DT_s period, where D is the duty ratio, and its value is larger than 50% (nominal value: 0.68).

For the first module, switches S_{11} and S_{12} are driven with phase shift of 180°. Similarly, switches S_{21}, S_{22} of second module also use the switching state sequence like the first module. In order to interleave theses two high step-up converter modules, one shifts the phase of the second module by 90° as compared with that of the first one. Hence, it can be seen from

TABLE II
Component Parameters of the Prototype System

Component	Specification
Boost inductors ($L_{11}, L_{12}, L_{21}, L_{22}$)	CH330060, 200μH
Power transformers (T_{f1}, T_{f2})	PQ32/20, Np:Ns = 10:30
Secondary-side inductors (L_{f1}, L_{f2})	CH400060, 600μH
Primary switches ($S_{11}, S_{12}, S_{21}, S_{22}$)	IXTQ96N20P, (200V, $R_{ds(ON)}$=24mΩ)
Power diodes ($D_{11}, D_{12}, D_{21}, D_{22}, D_{f11}, D_{f12}, D_{f21}, D_{f22}$)	DSEP 8-06A
Blocking capacitors ($C_{11}, C_{12}, C_{21}, C_{22}$)	film capacitor, 3.3μF
Output capacitors (C_o)	aluminum capacitor 440μF

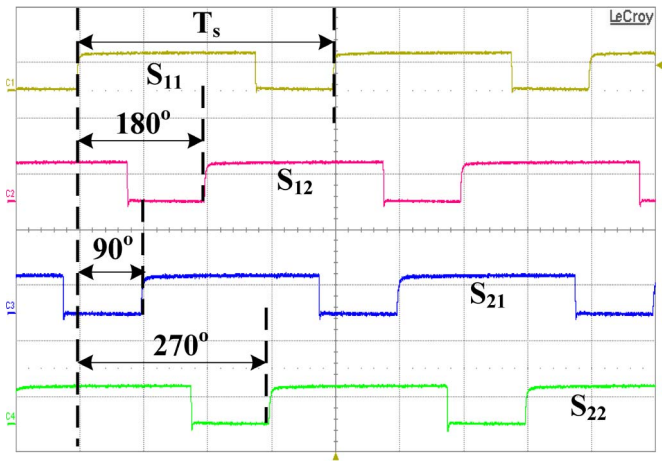


Fig. 9. Phase-shifted gate signals for the developed parallel high step-up converter modules system. (20 V/div, 5 us/div).

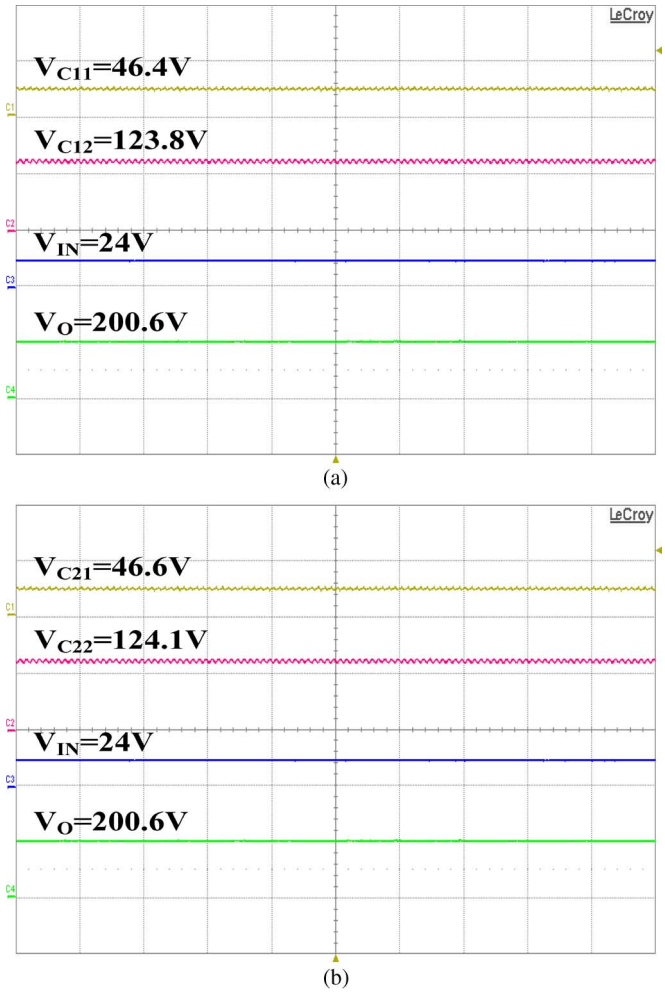


Fig. 10. Waveforms of output voltage and blocking capacitors voltage for (a) module 1, and (b) module 2. (Time: 200 us/div).

Fig. 9 that there exists 90° phase shift among all the four driving signals of power switches.

Fig. 10 records the experimental waveforms of the input voltage, output voltage of the prototype system, and voltage across blocking capacitors of each power module, respectively. As can be seen, with the proposed converter, the 200-V output

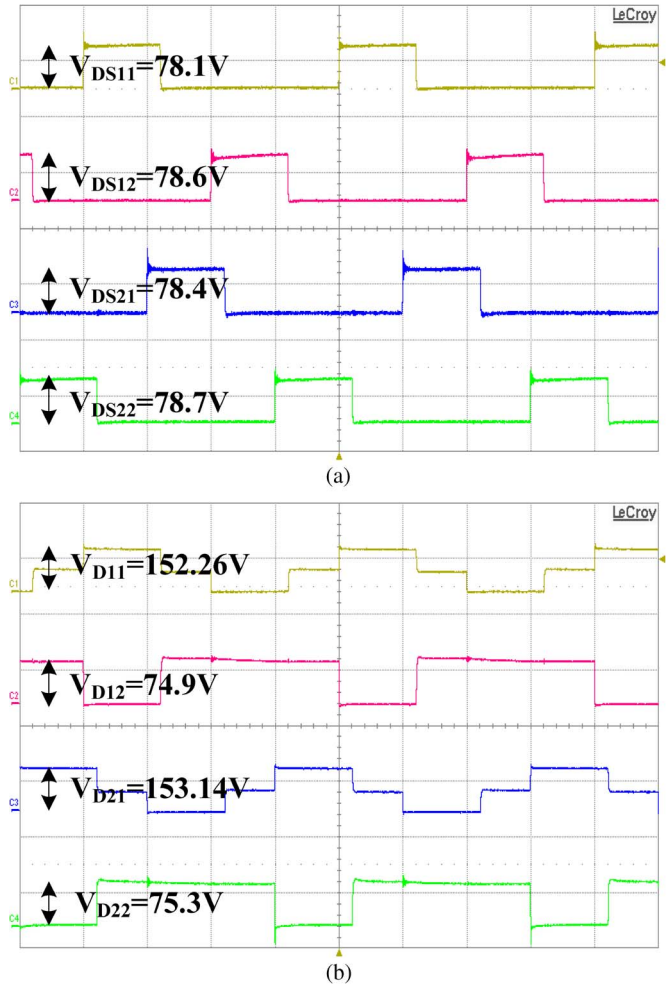


Fig. 11. Waveforms of voltage stress of (a) power switches, and (b) output diodes. (Time: 5 us/div).

voltage can be achieved with a duty ratio of about 0.68, and both blocking capacitors indeed can share most of the output voltage for reducing the voltage stress of active switches and diodes. In Fig. 11(a), one can see that the steady-state voltage stresses of both active switches are about 78 V. Obviously, the voltage stress is much smaller than the output voltage and enables one to adopt lower voltage rating devices to reduce the conduction loss as well as switching loss. Fig. 11(b) shows the voltage stress of diodes for each module, one can observe that due to the smaller duty ratio and the much lower voltage stresses of 153 V for D_{11}, D_{21} and 75 V for D_{12}, D_{22}, lower rating diodes can be adopted and the corresponding reverse-recovery problem of diodes can be alleviated. To further verify this inherent benefit of the proposed converter module, Fig. 12 shows the experimental results of the output diode stress for the conventional voltage-doubler and the proposed converter, respectively. It can be seen that, compared with the conventional voltage-doubler, the steady-state voltage stress of the output diode is reduced about 25%, and result in the reverse recovery current through the output diode is alleviated above 35%.

Fig. 13(a) shows input currents of the two modules, with the interleaved operation, the total input current ripple of the parallel converters system can be eliminated to below 50 mA.

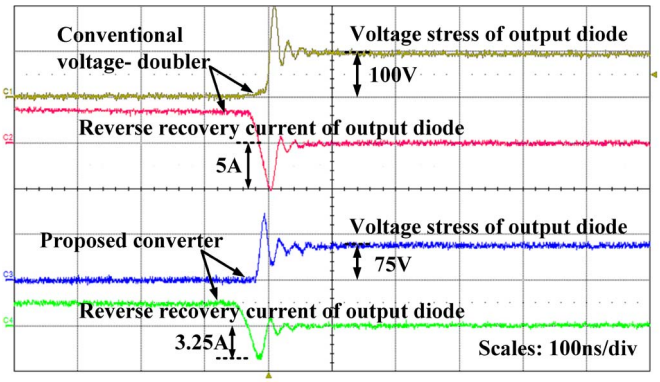


Fig. 12. Detail experimental results comparison of the output diode stress of single module between conventional voltage-doubler and proposed converter module under 200-W output power operation. (Time: 100 ns/div).

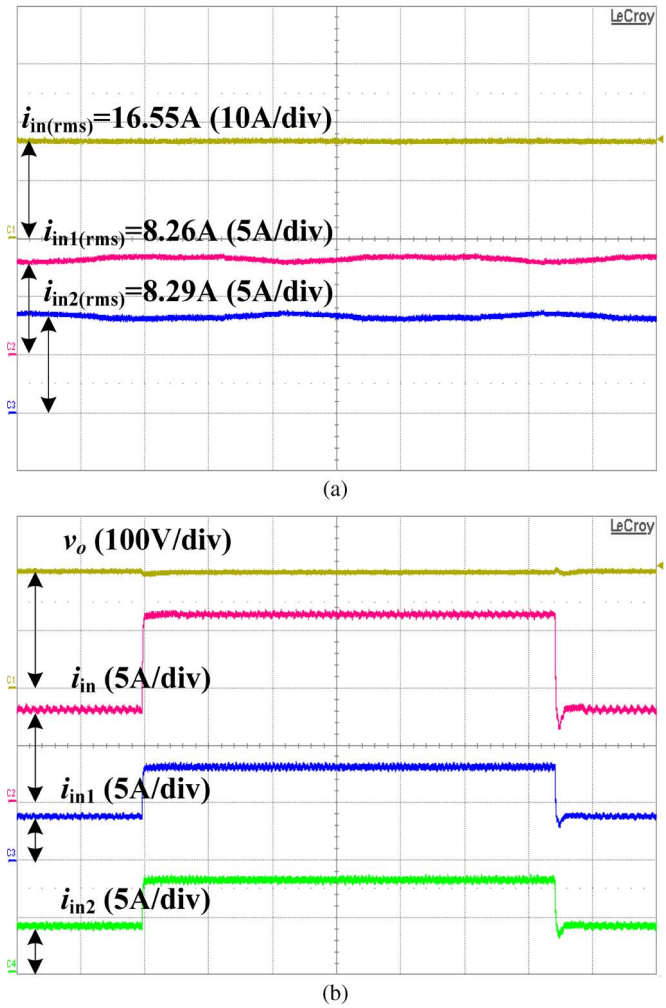


Fig. 13. Waveforms of input currents of the prototype system. (a) Steady-state operation (Time: 5 us/div). (b) Transient response for load period steps (Time: 500 ms/div).

Fig. 13(b) presents the transient response due to a step load current change between 200 W $\sim$ 400 W for the prototype system. It is seen that from Fig. 13(b), with the proposed control strategy, the overcurrent and imbalance of current distribution conditions under transient conditions can be prevented.

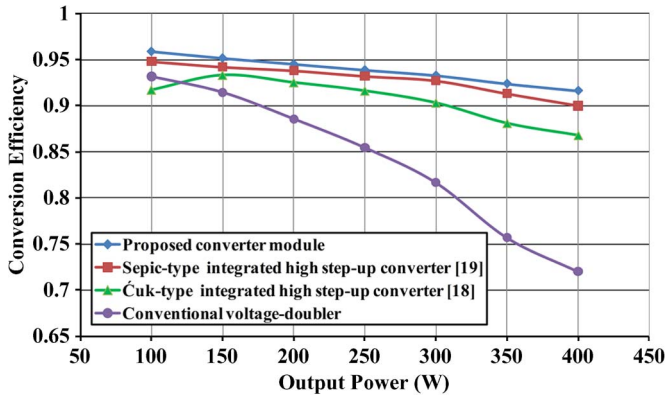


Fig. 14. Measured efficiency comparison at different loads.

The shared currents of proposed parallel system are within 5% of the averaged current over the load variation. Furthermore, in this case, the time for each currents reaching steady state is about 10 ms. Finally, the measured efficiency comparison at different loads among the conventional voltage-doubler, the Ćuk-type integrated high step-up converter [18], the sepic-type integrated high step-up converter [19], and the proposed converter module measured by using Yokogawa-WT500, is given in Fig. 14. The efficiency at 100-W light load of the proposed converter is 95.8%. There is approximately 9% efficiency improvement compared with the conventional voltage-doubler at 250 W half of load. In addition, nearly 5% and 1.5% efficiency improvement compared with the converter introduced in [18] and [19] at 400-W load condition, respectively. In the above implementation, it should be noted that the key design step is to design the transformer turn ratio that allows both a low-voltage rated device and a sufficient safe operation area. After the turn ratio is defined, the duty cycle can be appropriately determined. Consequently, the voltage rating of active switches, diodes and blocking capacitors can be easily selected. In practice, the design needs a tradeoff among the voltage stress of active switch and diode, power loss, and turns ratio. In fact, the optimal design can be carried out by processing the loss-analysis mechanism according to the switching-cycle performance [18].

VII. Conclusion

A new modular interleaved boost converter by integrating a forward energy-delivering circuit and voltage-doubler is proposed for achieving high step-up and high-efficiency objective. Steady-state analyses are then made to show the merits of the proposed converter topology. For further understanding the dynamic characteristic for the proposed converter module, steady-state and small-signal models of this converter are derived using state-space averaging technique. For higher power applications and satisfying the demands of low-voltage and high-current distributed power sources, a two-module parallel high step-up converter system is given for demonstration. Analysis and control of the proposed system are also made. Experimental results show that the proposed new high step-up boost converter module can achieve an efficiency of 95.8% approximately.

APPENDIX

The dc operation point of proposed modular converter can easily be solved with Mathematica algorithm and now listed as following (A1)–(A5), for reference:

$$\begin{aligned} V_{C1} = V_{\rm IN} \{&(-1+D)NDR\left[(-1+D)R - R_c\right] \\ &+ (R+R_c)\left[(1-D)(-2+3ND)R_c \right. \\ &\left. + 2(-1+D+ND)R_l\right]\} \\ &/ \left\{(-1+D)\left[(-1+D)R^2 \right.\right. \\ &\left. -(5-D)RR_c - (4-D)R_c^2\right] \\ &\left. + \left[(3-2D+D^2)R + (5-2D+D^2)R_c\right]R_l\right\} \end{aligned} \tag{A1}$$

$$\begin{aligned} V_{C2} = V_{\rm IN} &\left\{(-1+D)[-1-ND+ND^2]R^2 \right. \\ &+ \left[(1-D)(-1+2ND)R \right. \\ &\left. \left. -(2-D-ND+ND^2)R_c\right]R_c \right. \\ &\left. -(1-D-ND)(R+R_c)R_l\right\} \\ &/ \left\{(-1+D)\left[(-1+D)R^2 \right.\right. \\ &\left. -(5-D)RR_c - (4-D)R_c^2\right] \\ &\left. + \left[3-2D+D^2)\right](R+R_c)R_l\right\} \end{aligned} \tag{A2}$$

$$\begin{aligned} V_{CO} &= V_{\rm Bus} \\ &= V_{\rm IN}\left[(-1+D)(-2-ND+ND^2)R(R+R_c)\right] \\ &/ \left\{(1-D)\left[(1-D)R^2 \right.\right. \\ &\left. + (5-D)RR_c + (4-D)R_c^2\right] \\ &\left. + (3-2D+D^2)(R+R_c)R_l\right\} \end{aligned} \tag{A3}$$

$$\begin{aligned} I_{Lf} &= V_{\rm IN}\left[(1-D)(2+ND-ND^2)(R+R_c)\right] \\ &/ \left\{(-1+D)\left[(-1+D)R^2 \right.\right. \\ &\left. - (5-D)RR_c - (4-D)R_c^2\right] \\ &\left. + (3-2D+D^2)(R+R_c)R_l\right\} \end{aligned} \tag{A4}$$

$$\begin{aligned} I_{L1} = I_{L2} &= V_{\rm IN}\left[(2+ND-ND^2)(R+R_c)\right] \\ &/ \left\{(-1+D)\left[(-1+D)R^2 \right.\right. \\ &\left. - (5-D)RR_c - (4-D)R_c^2\right] \\ &\left. + \left[(3-2D+D^2)(R+R_c)\right]R_l\right\}. \end{aligned} \tag{A5}$$

It is worth mentioning that (A5) verifies the phase currents balance capability of the proposed converter. Because of the inherent voltage-doubler function built-in the converter topology, the current-sharing of the currents through the two interleaved phases can be obtained without any additional current-sharing control circuits. Note that the same feature, e.g., automatic current-balance characteristic, had previously been discussed [21], [26]–[28], where a novel circuit topology can be derived by integrated with the voltage-doubler and a forward energy-delivering circuit for meeting high voltage gain requirements. Furthermore, by neglecting the parasitic ESRs from (A1)–(A3), the effectiveness of the ideal voltage (6), (8), and (10) can be proved exactly.

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