High-Power Bidirectional DC–DC Converter for Aerospace Applications

R. T. Naayagi, *Member, IEEE*, Andrew J. Forsyth, *Senior Member, IEEE*, and R. Shuttleworth, *Member, IEEE*

***Abstract*—This paper contributes to the steady-state analysis of the bidirectional dual active bridge (DAB) dc–dc converter by proposing a new model that produces equations for rms and average device currents, and rms and peak inductor/transformer currents. These equations are useful in predicting losses that occur in the devices and passive components and aid in the converter design. An analysis of zero-voltage switching (ZVS) boundaries for buck and boost modes while considering the effect of snubber capacitors on the DAB converter is also presented. The proposed model can be used to predict the converter efficiency at any desired operating point. The new model can serve as an important teaching-cum-research tool for DAB hardware design (devices and passive components selection), soft-switching-operating range estimation, and performance prediction at the design stage. The operation of the DAB dc–dc converter has been verified through extensive simulations. A DAB converter prototype was designed on the basis of the proposed model and was built for an aerospace energy storage application. Experimental results are presented to validate the new model for a 7 kW, 390/180 V, 20 kHz converter operation and the ZVS boundary operation.**

***Index Terms*—DC–DC converter, dual active bridge (DAB), rms and average device currents, rms and peak inductor current, snubber capacitor, zero-voltage switching (ZVS).**

I. Introduction

AERONAUTICAL power distribution technology is moving toward dc due to the increasing proportion of dc electrical loads. As a result, the aerospace industry is promoting the use of more electrical technologies to enhance the performance and increase the reliability of aircraft systems and subsystems. The power generation capacity of the more electric Boeing 787 and Airbus A380 aeroplanes is about 1.4 MW and 850 kW, respectively [1]. In order to reduce weight, electrical power should be transmitted around the aircraft at a high voltage (HV) with low current and low conduction losses. In this context, dc power distribution system architecture is found to be the most reliable configuration for sustaining aircraft operations even under severe supply transients [1], [2]. This technology leads to simpler equipment and enables significant energy savings [2], but requires high-power-density dc–dc converter for a variety of applications such as battery-based uninterrupted power supplies to mission critical aerospace applications, e.g., actuators and avionics. The dual active bridge (DAB) topology for dc–dc conversion has been popular among researchers over the past two decades due to its high performance, high efficiency, galvanic isolation, and inherent soft-switching property [3]. These features make the DAB dc–dc converter a strong candidate for high-power-density aerospace applications. Several research papers have been published on the DAB converter performance accompanied by a comprehensive analysis [4]–[12], but hardly any paper deals with the DAB converter design. Nevertheless, design considerations for high frequency (HF) DAB converter transformers are primarily concerned with core material selection, loss minimization, and realization of controlled leakage inductances as discussed in [13] and [14].

Bidirectional power flow capability is a key feature of DAB dc–dc converters, permitting flexible interfacing to energy storage devices [15], [16]. Although the DAB converter has an inherent soft-switching attribute, it is limited to a reduced operating range depending on voltage conversion ratio and output current [15], [17]. This is a drawback for applications that operate mainly with variable or low loads as the overall converter efficiency is reduced [18]–[21]. Recently, a model was proposed [21] for the DAB converter that has been validated under certain operating conditions for low load, low efficiency, and low-power operation, but the device average and rms current models and transformer/inductor RMS current models which could serve useful for hardware design were not proposed. Moreover, such current models are not available in the existing literature for either low-power or high-power converter operation. A comparative evaluation of single- and three-phase versions of the DAB converter was performed in [22] from the perspective of operating performance and losses for bidirectional power conversion applications. The comparisons pave the way for a choice to be made between these two alternatives for any particular application. In [23], Inoue and Akagi validated DAB performance for next-generation power conversion systems using ultracapacitor-based technologies. The DAB converter dynamic performance was modeled and analyzed in [24] and [25]. Krismer *et al*. [9] and Zhou and Khambadkone [26] introduced trapezoidal and triangular modulation methods to

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R. T. Naayagi was with the Department of Engineering Systems, Medway School of Engineering, University of Greenwich, Medway ME4 4TB, U.K. She is now with the Department of Electrical and Electronics Engineering, S. A. Engineering College (affiliated to Anna University), Thiruverkadu Post, Chennai 600077, India (e-mail: naayagi04@gmail.com).

A. J. Forsyth and R. Shuttleworth are with the Power Conversion Group, School of Electrical and Electronic Engineering, The University of Manchester, Manchester M13 9PL, U.K. (e-mail: andrew.forsyth@manchester.ac.uk; roger.shuttleworth@manchester.ac.uk).

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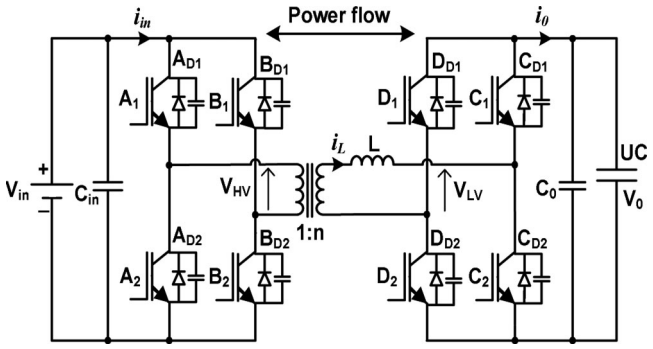

Fig. 1. Schematic of the DAB dc–dc converter.

achieve triangular and trapezoidal currents in the DAB converter ac link. This was achieved by modulating the duty cycle of the converter bridge to reduce losses over a wide operating voltage range.

The DAB converter has various potential industry applications; hence, its performance has been investigated with the latest power switching devices such as SiC [27]. This paper presents the modeling, design, development, and performance evaluation of the DAB converter shown in Fig. 1, which can act as an interface between energy storage devices such as an ultracapacitor bank and the aircraft electrical power network. Ultracapacitors constitute one form of energy storage device, which can be used to meet transient power demands and smooth the load on the generators.

In [28] and [29], Jain and Ayyanar presented a comprehensive analysis of DAB converter pulse width modulated control; however, the authors discussed only harmonic analysis for transformer rms and peak currents and stated that the exact analysis would be complicated for each voltage conversion ratio. A new steady-state model for the DAB dc–dc converter was presented in [30] and [31]. The model produced equations for device rms and average currents, and peak and RMS currents in the coupling inductor. These equations are useful in predicting the losses that occur in devices and passive components and aid in the converter design. At any operating point (e.g., for any duty ratio), the converter efficiency, losses, and device currents can be estimated easily from the model. Square-wave is the only mode of operation suitable for high-power applications and the extensive analysis presented in this paper is novel, which is duly substantiated by simulation and experimental results. The analysis is extended to soft-switching (ZVS) boundaries by considering the effect of snubber capacitors on the DAB converter. The operation of the DAB converter during transistor turn-OFF switching is discussed briefly, and the minimum current requirement for achieving ZVS under buck and boost modes is also determined. Kheraluwala *et al*. [3] describe the influence of device snubber capacitance on the ZVS region and gave a general representation of the effect of snubber on ZVS boundary. This paper extends the analysis further, and provides unique equations determining the duty ratio at which ZVS operation begins for any particular value of snubber during transistor turn-OFF under buck and boost modes. This will be useful to predict the converter capability for soft-switching operation at the design stage itself.

The rest of this paper is organized as follows. After a brief description of the operating principle of the DAB dc–dc converter, a novel steady-state model of the converter and its ZVS limits for buck and boost modes are presented in Section II. Simulation results confirming accuracy of the analysis are presented in Section III. Practical design and experimental validation of the DAB converter operation are discussed in Section IV. Finally, conclusions are drawn in Section V.

II. New Steady-State Model of DAB Converter

A. Basic Principle of Operation

Future aircraft are likely to employ electrically powered actuators for adjusting flight control surfaces and other high-power transient loads. To meet the peak power demands of aircraft electric loads and to absorb regenerated power, an ultracapacitor-based energy storage system is examined in which a bidirectional DAB dc–dc converter is used. The DAB converter shown in Fig. 1 consists of two full-bridge circuits connected through an isolation transformer and a coupling inductor *L*, which may be provided partly or entirely by the transformer leakage inductance. The full bridge on the left hand side of Fig. 1 is connected to the HV dc bus and the full bridge on the right-hand side is connected to the low-voltage (LV) ultracapacitor. Each bridge is controlled to generate an HF square-wave voltage at its terminals. By incorporating an appropriate value of coupling inductance, the two square-waves can be suitably phase shifted with respect to each other to control power flow from one dc source to another. Thus, bidirectional power flow is enabled through a small lightweight HF transformer and inductor combination, and power flows from the bridge generating the leading square-wave. Although various modes of operation of the DAB converter have been presented recently [20], [26], [28] for high-power operation, the square-wave mode is supposedly the best operating mode. This is because imposing quasi-square-wave on the transformer primary and secondary voltages results in trapezoidal, triangular, and sinusoidal waveforms of inductor current in the DAB converter ac link. These modes are beneficial for extending the low-power operating range of the converter [26]. Although these modes tend to reduce the switching losses, the voltage loss is significant due to zero voltage periods in the quasi-square-wave, which reduces the effective power transfer at high-power levels. Therefore, the contribution highlighted in this paper forms important research on the DAB converter.

The key operating waveforms of the converter during buck mode, i.e., when power flows from the HV side to the LV side are shown in Fig. 2. The voltages generated by the two full bridges, $V_{\rm HV}$ on the HV side and $V_{\rm LV}$ on the LV side, are represented as square-wave voltages with 50% duty cycle. The current flowing through the coupling inductance is i_L, $i_{AD1\text{-}A1}$ and $i_{CD1\text{-}C1}$ are the device currents on the HV and LV sides, respectively, and i_0 is the output current. The time delay between $V_{\rm HV}$ and $V_{\rm LV}$ is $dT_S/2$, where T_S is the switching period and d is the duty ratio.

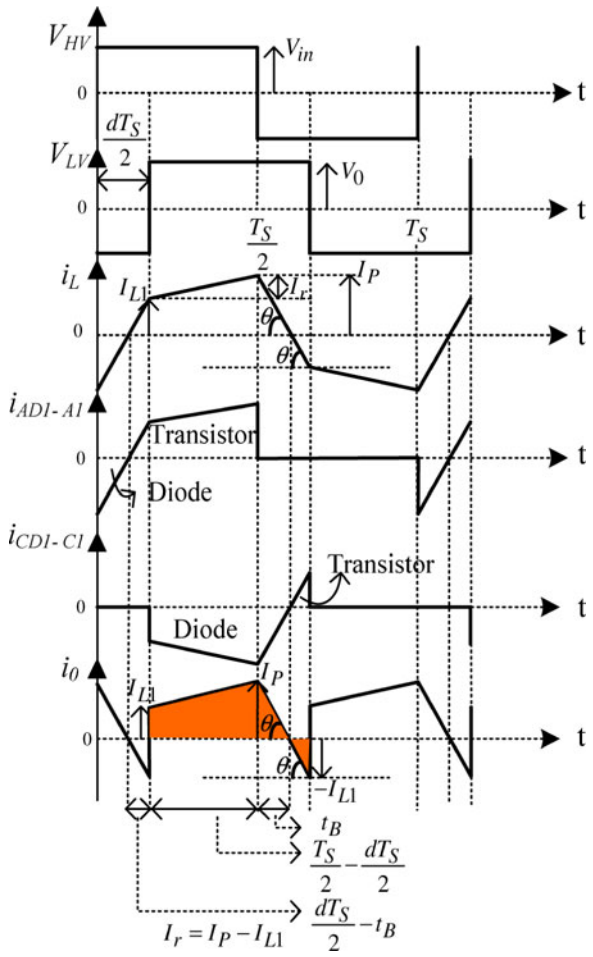

Fig. 2. Key operating waveforms of the DAB converter during buck mode.

B. Steady-State Model

Models for device rms and average currents and peak and rms currents of the coupling inductor are derived based on the assumption of lossless components and a piecewise linear waveform for i_L. The difference in voltage between the two bridges appears across the coupling inductor and the inductor current changes with an essentially constant slope; this enables expressions for inductor current peaks corresponding to different switching instants to be determined.

When the converter operates in buck mode, the voltage across inductor *L* over a half cycle is analyzed to determine the peak-to-peak change in inductor current. Expressions for inductor current are then derived for switching instants I_P and I_{L1}. The notations used in the following analysis are indicated in Fig. 2.

The current at the HV switching instant is expressed as follows:

$$I_P = \frac{T_S}{4L}\left[nV_{\text{in}} + V_0\left(2d-1\right)\right] \tag{1}$$

where *n* is the transformer turns ratio. Solving for the LV switching instant current based on the current slope during the interval $dT_S/2$ gives

$$I_{L1} = \frac{T_S}{4L}\left[nV_{\text{in}}\left(2d-1\right) + V_0\right]. \tag{2}$$

In order to find the average output (ultracapacitor) current, the current expression is required for the interval t_B: the time taken for i_L to fall to zero following the HV bridge switching instant. Since the output current waveform is piecewise linear, this can be calculated from the following:

$$\frac{I_P + I_{L1}}{(dT_S/2)} = \frac{I_P}{t_B} = \tan\theta \tag{3}$$

where θ is the angle marked on the i_0 and i_L current waveforms shown in Fig. 2. The total current change during the interval $dT_S/2$, where the current is increased from $-I_P$ to $+I_{L1}$, can be written as follows:

$$I_P + I_{L1} = \left(\frac{nV_{\text{in}} + V_0}{L}\right)\frac{dT_S}{2}. \tag{4}$$

Substituting (1) and (4) in (3), and solving for t_B gives

$$t_B = \frac{T_S\left[nV_{\text{in}} + V_0\left(2d-1\right)\right]}{4\left(nV_{\text{in}} + V_0\right)}. \tag{5}$$

Using the above equations, the area under the i_0 current waveform, shown as a shaded region in Fig. 2, is obtained. Since the waveform is periodic over half a cycle, dividing the area by the duration, which is $T_S/2$, gives the average output current of the DAB converter, which may be expressed as follows:

$$I_0 = \frac{nV_{\text{in}}T_S}{2L}\left(d - d^2\right). \tag{6}$$

Normalizing the average output current by the base value $nV_{\text{in}}T_S/2L$ gives

$$I_0' = d - d^2. \tag{7}$$

From (7), by substituting the full control range (0 to 1) for the duty ratio *d*, it can be observed that maximum power transfer occurs for a duty ratio of 0.5.

The inductor/transformer current wave shape is similar and is piecewise linear. Hence, to simplify the analysis, the waveform can be split into triangular or trapezoidal shapes over any time interval. The effective time intervals of those triangular and trapezoidal shapes were utilized to individually derive their rms currents and then summed together to obtain the total rms current equation of the DAB converter waveform. From Fig. 2, it can be observed that the inductor/transformer current is periodic and symmetrical over a cycle; hence, the rms value for a half cycle has been used to determine the corresponding value for a whole period. The instantaneous current *I*(*t*) over a half cycle is represented as follows:

$$\begin{aligned} I(t) &= \frac{I_{L1}}{(dT_S/2) - t_B}t, && 0 < t < \frac{dT_S}{2} - t_B \\ &= I_{L1} + \frac{I_r t}{(T_S/2) - t_B}, && \frac{dT_S}{2} - t_B < t < \frac{T_S}{2} - t_B \\ &= I_P - \frac{I_P t}{(T_S/2)}, && \frac{T_S}{2} - t_B < t < \frac{T_S}{2}. \end{aligned} \tag{8}$$

TABLE I
RMS CURRENT MODEL OF DEVICES IN DAB CONVERTER FOR BUCK MODE (POWER TRANSFER FROM THE HV SIDE TO THE LV SIDE)

Device	RMS current equation
HV side Transistor	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_{L1}^2+\frac{I_r^2}{3}+I_{L1}I_r\right)\right]}$
HV side Diode	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{I_P^2}{3}\times(t_B)\right]}$
LV side Transistor	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\frac{(I_{L1})^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)\right]}$
LV side Diode	$I_{RMS}=\sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_{L1}^2+\frac{I_r^2}{3}+I_{L1}I_r\right)+\frac{(I_P)^2\times t_B}{3}\right]}$

Changing the limits to their effective intervals gives

$$\begin{aligned} I(t) &= \frac{I_{L1}}{(dT_S/2)-t_B}t, \qquad 0<t<\frac{dT_S}{2}-t_B \\ &= I_{L1}+\frac{I_r t}{(T_S/2)-(dT_S/2)}, \qquad 0<t<\frac{T_S}{2}-\frac{dT_S}{2} \\ &= I_P-\frac{I_P t}{t_B}, \qquad 0<t<t_B \end{aligned} \tag{9}$$

where $I_r = I_P - I_{L1}$. Therefore, the rms equation of the inductor current is given by

$$I_{\rm rms}=\sqrt{\frac{2}{T_S}\int_0^{T_S/2} I^2(t)dt}. \tag{10}$$

Substituting $I^2(t)$ in the above equation gives $I_{\rm rms}$ as shown at the bottom of this page.

Simplifying further, the final expression for the inductor/transformer rms current during buck mode is expressed as shown (11) at the bottom of this page.

Similarly, the rms and average current model for devices on the HV and LV bridge sides of the DAB converter are derived from the waveforms shown in Fig. 2 and are listed in Tables I and II, respectively.

When the converter operates in boost mode, power flows from the LV side to HV side. A similar procedure is followed to that of the buck mode to derive the necessary model. Converter operating waveforms under boost mode are depicted in Fig. 3. The voltage across inductor L over a half cycle is analyzed to determine the peak-to-peak change in inductor current. Subsequently, expressions are derived for inductor current at switching instants I_P and I_{L1}. The expression for current at the LV switching instant I_{L1} is given as follows:

$$I_{L1}=\frac{T_S}{4L}\left[V_o+nV_{\rm in}\left(2d-1\right)\right]. \tag{12}$$

Solving for the HV switching instant current based on the current slope during the interval $dT_S/2$ gives

$$I_P=\frac{T_S}{4L}\left[nV_{\rm in}+V_o\left(2d-1\right)\right]. \tag{13}$$

To evaluate the average ultracapacitor current, an expression is required for interval t_B: the time taken for i_L to fall to zero following the LV switching instant. Since the i_0 current waveform is piecewise linear, this can be calculated from the following:

$$\frac{I_P+I_{L1}}{dT_S/2}=\frac{I_{L1}}{t_B}=\tan\theta \tag{14}$$

where θ is the angle marked on the i_0 current waveform shown in Fig. 3. The total current change during interval $dT_S/2$, where the current is decreased from $+I_{L1}$ to $-I_P$, can be written as

TABLE II
AVERAGE CURRENT MODEL OF DEVICES IN DAB CONVERTER FOR BUCK MODE (POWER TRANSFER FROM THE HV SIDE TO THE LV SIDE)

Device	Average current expression
HV side Transistor	$I_{avg}=\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)}{\frac{T_S}{2}-t_B}$
HV side Diode	$I_{avg}=\frac{\frac{1}{2}\times I_P\times t_B}{t_B}$
LV side Transistor	$I_{avg}=\frac{\frac{1}{2}\times I_{L1}\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
LV side Diode	$I_{avg}=\frac{\frac{1}{2}\times(I_{L1}+I_P)\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)+\frac{1}{2}\times I_P\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$

$$I_{\rm rms}=\sqrt{\frac{2}{T_S}\left[\int_0^{(dT_S/2)-t_B}\left(\frac{I_{L1}}{(dT_S/2)-t_B}\right)^2 t^2dt+\int_0^{(T_S/2)-(dT_S/2)}\left(I_{L1}^2+\left(\frac{I_r}{(T_S/2)-(dT_S/2)}\right)^2 t^2+\frac{2I_{L1}I_r t}{(T_S/2)-(dT_S/2)}\right)dt + \int_0^{t_B}\left(I_P^2+\left(\frac{I_P}{t_B}\right)^2 t^2-\frac{2I_P^2 t}{t_B}\right)dt\right].}$$

$$I_{\rm rms}=\sqrt{\frac{2}{T_S}\left[\frac{I_{L1}^2}{3}\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_{L1}^2+\frac{I_r^2}{3}+I_{L1}I_r\right)+\frac{I_P^2 t_B}{3}\right]}. \tag{11}$$

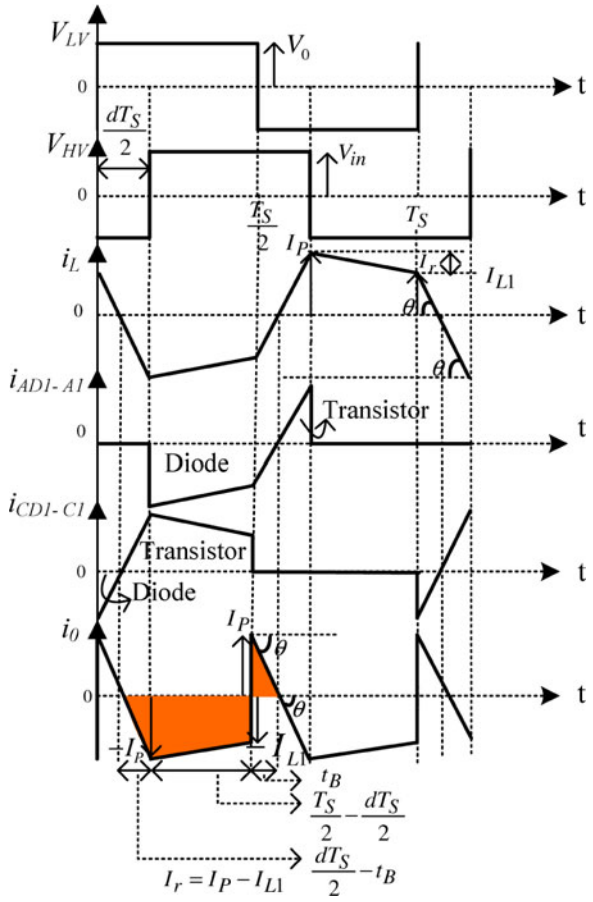

Fig. 3. Operating waveforms of the DAB converter under boost mode.

follows:

$$I_P + I_{L1} = \left(\frac{nV_{\text{in}} + V_0}{L}\right)\frac{dT_S}{2}. \tag{15}$$

Substituting (12) and (15) in (14), then solving for t_B gives

$$t_B = \frac{T_S\left[V_o + nV_{\text{in}}\left(2d-1\right)\right]}{4\left(nV_{\text{in}} + V_o\right)}. \tag{16}$$

Using the above equations, the area under the i_0 current waveform, shown as shaded regions in Fig. 3, is obtained. Since the waveform is periodic over half a cycle, dividing the area by duration, which is $T_S/2$, gives the average output current of the DAB converter as follows:

$$I_o = \frac{nV_{\text{in}}T_S}{2L}\left(d^2 - d\right). \tag{17}$$

Normalizing the average output current by the base value $nV_{\text{in}}T_S/2L$ gives

$$I_o' = d^2 - d. \tag{18}$$

Similar to (7), for the full control range of the DAB dc–dc converter, from (18) the maximum power transfer is found to occur at a duty ratio of 0.5.

A similar procedure is followed to that of the buck mode in deriving the rms current model. The rms value of inductor current and output current i_0 can be derived using HV and LV switching instant current expressions and their respective time intervals, which result in (19) as shown at the bottom of next page.

TABLE III
RMS CURRENT MODEL OF DEVICES IN DAB CONVERTER FOR BOOST MODE (POWER TRANSFER FROM THE LV SIDE TO THE HV SIDE)

Device	RMS current equation
HV side Transistor	$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{(I_P)^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)\right]}$
HV side Diode	$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_P{}^2+\frac{I_r{}^2}{3}-I_PI_r\right)+\frac{(I_{L1})^2\times t_B}{3}\right]}$
LV side Transistor	$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{(I_P)^2}{3}\times\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_P{}^2+\frac{I_r{}^2}{3}-I_PI_r\right)\right]}$
LV side Diode	$I_{RMS} = \sqrt{\frac{1}{T_S}\left[\frac{I_{L1}{}^2}{3}\times(t_B)\right]}$

TABLE IV
AVERAGE CURRENT MODEL OF DEVICES IN DAB CONVERTER FOR BOOST MODE (POWER TRANSFER FROM THE LV SIDE TO THE HV SIDE)

Device	Average current expression
HV side Transistor	$I_{avg} = \frac{\frac{1}{2}\times I_P\times\left(\frac{dT_S}{2}-t_B\right)}{\left(\frac{dT_S}{2}-t_B\right)}$
HV side Diode	$I_{avg} = \frac{\frac{1}{2}\times(I_P+I_{L1})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)+\frac{1}{2}\times I_{L1}\times t_B}{\left(\frac{T_S}{2}-\frac{dT_S}{2}+t_B\right)}$
LV side Transistor	$I_{avg} = \frac{\frac{1}{2}\times I_P\times\left(\frac{dT_S}{2}-t_B\right)+\frac{1}{2}\times(I_P+I_{L1})\times\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)}{\left(\frac{T_S}{2}-t_B\right)}$
LV side Diode	$I_{avg} = \frac{\frac{1}{2}\times I_{L1}\times t_B}{t_B}$

The rms and average current model for devices on HV and LV sides of the DAB converter are derived from the waveforms shown in Fig. 3 and are given in Tables III and IV, respectively.

From the boost mode analysis, it can be observed that the corresponding expressions for the currents at the HV and LV switching instants, I_P and I_{L1}, respectively, in (1) and (2), are unchanged. However, in the expressions for i_0, the LV-side terminal current, given by (6) and (7), the $(d-d^2)$ term is replaced by (d^2-d). Also, the expressions for the transistor and diode currents will be interchanged in Tables I and II. For example, the expression for the HV-side transistor current becomes the expression for the LV-side transistor with I_P, I_{L1} replaced by I_{L1}, I_P, respectively, and so forth.

C. ZVS Limits

During transistor turn-OFF, resonance will naturally occur between device output capacitance and coupling inductance. The

energy stored in the coupling inductance is sufficient to ensure charge/discharge of device output capacitances at the switching instants. The converter operating conditions to achieve virtually loss-less ZVS conditions are:

1) at turn-ON of any device, its antiparallel diode is conducting;
2) at turn-OFF of any device, the minimum current flow through the device is positive.

In practice, the ZVS limits will be slightly different due to the requirement for inductor current to be sufficient to ensure charge/discharge of the device output capacitances at the switching instants.

By applying the ZVS conditions to the device current waveforms, shown in Fig. 2, the current at the LV switching instant must be greater than zero to achieve ZVS in the LV-side bridge. Therefore, based on (2), the following condition must be satisfied for achieving ZVS in the LV side:

$$I_{L1} = \frac{T_S}{4L}\left[nV_{\rm in}\left(2d-1\right)+V_0\right] \geq 0. \tag{20}$$

Solving for the inequality given in (20), the duty ratio at which ZVS occurs is obtained as follows:

$$d \geq 0.5 - \frac{V_0'}{2} \tag{21}$$

where $V_0' = V_0/nV_{\rm in}$ is the normalized voltage conversion ratio. To achieve ZVS in the HV bridge, the current at the HV switching instant given in (1) must be positive. However, this condition is normally achieved and the limiting condition for ZVS is that given by (21).

For power transfer from the HV side to the LV side, (21) is applicable when $V_0{}' < 1$. If $V_0{}' > 1$, the shape of the inductor current in Fig. 2 will change, as shown in Fig. 3, and the effect of this is to interchange the expressions for the currents at the LV and HV switching instants. Therefore, with $V_0' > 1$, the expression for the LV switching instant current is given by (1) and the expression for the HV switching instant current is given by (2). The ZVS limit still occurs in the LV bridge, but is now specified by requiring the current level in (1) to be greater than zero, which leads to the following condition:

$$d \geq 0.5 - \frac{1}{2V_0'}. \tag{22}$$

When the power transfers from the LV side to the HV side, the ZVS limit is again found to occur in the LV bridge and may be expressed by (20)–(22).

Although turn-ON of transistors in the DAB converter is achieved at minimum (near-zero) positive diode current, the instantaneous transistor currents that occur during the turn-OFF process are significant. Normally, the device output capacitance is too low to produce a low *dv*/*dt*. Hence, minimal transistor currents during the turn-OFF switching time instant are mandatory in order to achieve low switching losses. To limit switching transients, reduce current/voltage spikes, and to minimize electromagnetic compatibility (EMC) problems associated with high *dv*/*dt*, snubber capacitors can be placed across the switching devices. These capacitors slow down the rate of voltage rise across the devices so that a lower voltage appears during the current decay time. Although snubber capacitors suppress voltage transients during switching, inclusion of a snubber across the switching transistors requires more energy to be stored in the coupling inductance to achieve soft switching [3].

The analysis was performed by assuming that the input (HV) and output (LV) voltages are constant during the transistor turn-OFF instants to estimate the minimum current necessary during turn-OFF to achieve ZVS. To achieve ZVS, energy stored in the inductor must equal the energy delivered to charge and discharge the snubber and device output capacitances. Kheraluwala *et al*. [3] and Naayagi [31] performed analysis to obtain an expression for the minimum inductor current during turn-OFF as follows:

$$I_L = 2\sqrt{\frac{v_0' V_{\rm in}}{L'/C_S}} \tag{23}$$

where L' is the primary referred coupling inductance and v_0' is the primary referred LV bridge voltage source. It has been assumed in the analysis that the insulated gate bipolar transistor (IGBT) tail current does not change when the snubber capacitor is added. The snubber creates oscillations due to the resonance induced between parasitic inductance of the IGBT module and the snubber capacitance during turn-OFF transient. In practice, the IGBT tail current may be reduced with the addition of an appropriate value of snubber capacitor. However, the tail time increases due to reduced *dv*/*dt*. Therefore, to simplify the analysis, the assumption that the IGBT tail current does not change with the inclusion of the snubber capacitor is made.

The inductor current should be greater than or equal to the value of I_L in (23) during transistor turn-OFF to achieve ZVS. This paper extends the analysis further to obtain the equations of duty ratio for HV and LV device ZVS limits for a specified value of snubber capacitor.

Without the snubber, the condition to be satisfied for achieving ZVS during buck mode is given by (20). From (20) and (23), the ZVS boundary condition for $V_0' < 1$ while considering the inclusion of snubber is given by

$$I_{L1} = \frac{T_S}{4L}\left[V_0 + nV_{\rm in}\left(2d-1\right)\right] \geq 2\sqrt{\frac{v_0' V_{\rm in}}{L'/C_S}}. \tag{24}$$

Solving for the above inequality, the duty ratio at which ZVS occurs for $V_0' < 1$ is given as follows:

$$d \geq 0.5 - \frac{V_0'}{2} + \frac{4}{T_S}\sqrt{\frac{v_0' L' C_S}{V_{\rm in}}}. \tag{25}$$

$$I_{\rm rms} = \sqrt{\frac{2}{T_S}\left[\frac{I_P^2}{3}\left(\frac{dT_S}{2}-t_B\right)+\left(\frac{T_S}{2}-\frac{dT_S}{2}\right)\left(I_P^2+\frac{I_r^2}{3}-I_P I_r\right)+\frac{I_{L1}^2\, t_B}{3}\right]}. \tag{19}$$

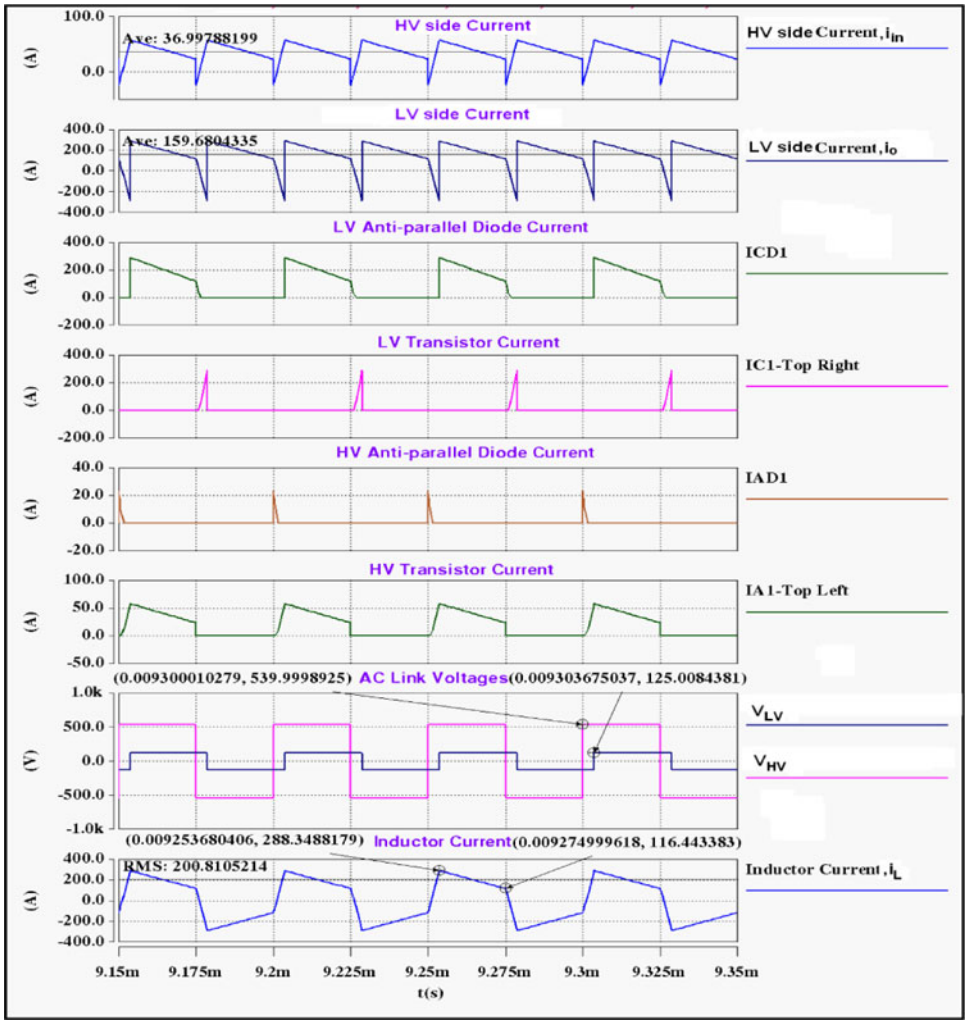

Fig. 4. Simulation results of the converter under buck mode. $V_{\rm HV} = 540$ V, $n = 1{:}\ 0.2$, $V_{\rm LV} = 125$ V, $d = 0.146$, $P_0 = 20$ kW, $I_0 = 160$ A, $f_s = 20$ kHz, and $L = 2.11$ μH.

Similarly, for $V_0' > 1$, from (22) and (23), with the snubber, the duty ratio at which ZVS occurs is given as follows:

$$d \geq 0.5 - \frac{1}{2V_0'} + \frac{4}{T_S}\sqrt{\frac{V_{\rm in}L'C_S}{v_0'}}. \tag{26}$$

Equations (25) and (26) are unique and determine the ZVS boundary of the DAB converter for any value of snubber capacitor under buck and boost modes.

III. Simulation Results

To validate the model presented in Section II, extensive simulations were carried out using SABER. Figs. 4 and 5 show SABER simulations for buck and boost modes. These figures depict the voltages generated by the two full bridges, $V_{\rm HV}$ on the HV side and $V_{\rm LV}$ on the LV side, the current flowing through the coupling inductance i_L, the device currents on the HV side i_{A1},$i_{\rm AD1}$ and the device currents on the LV side $i_{C1,}$ i_{CD1}, the HV-side terminal current $i_{\rm in}$, and the LV-side terminal current i_0. For $V_{\rm HV} = 540$ V, $n = 1{:}0.2$, $V_{\rm LV} = 125$ V, the voltage conversion ratio is 1.16. For a voltage conversion ratio greater than one ($V_0' > 1$), during power flow from the HV side to the LV side, the shape of the inductor current in Fig. 2 will change, as shown in Fig. 4, and the effect of this is to interchange the expressions for the currents at the LV and HV switching instants. Therefore, with $V_0' > 1$, the expression for the LV switching instant current is given by (1) and the expression for the HV switching instant current is given by (2).

The values used in SABER simulations are typical of likely future aerospace systems [30], [32] at the HV side, and the capacities of commercial ultracapacitor modules at the LV side. According to the theoretical model, for the buck mode, i.e., when power flows from the HV side to the LV side, the expected steady-state values are $I_P = 288.1$ A, $I_0 = 160$ A, $I_{L1} = 116.2$ A, and $I_{\rm rms} = 196.5$ A, and for the boost mode, when power transfers from the LV side to the HV side, the expected values are $I_P = 640$ A, $I_0 = 320$ A, $I_{L1} = 370.4$ A, and $I_{\rm rms} = 426.9$ A. These correlate well with the SABER simulation results.

Fig. 6 depicts the simulation waveforms of the DAB converter on the ZVS boundary, with a 47 nF snubber capacitor across the HV-side devices and a 100 nF snubber capacitor across the

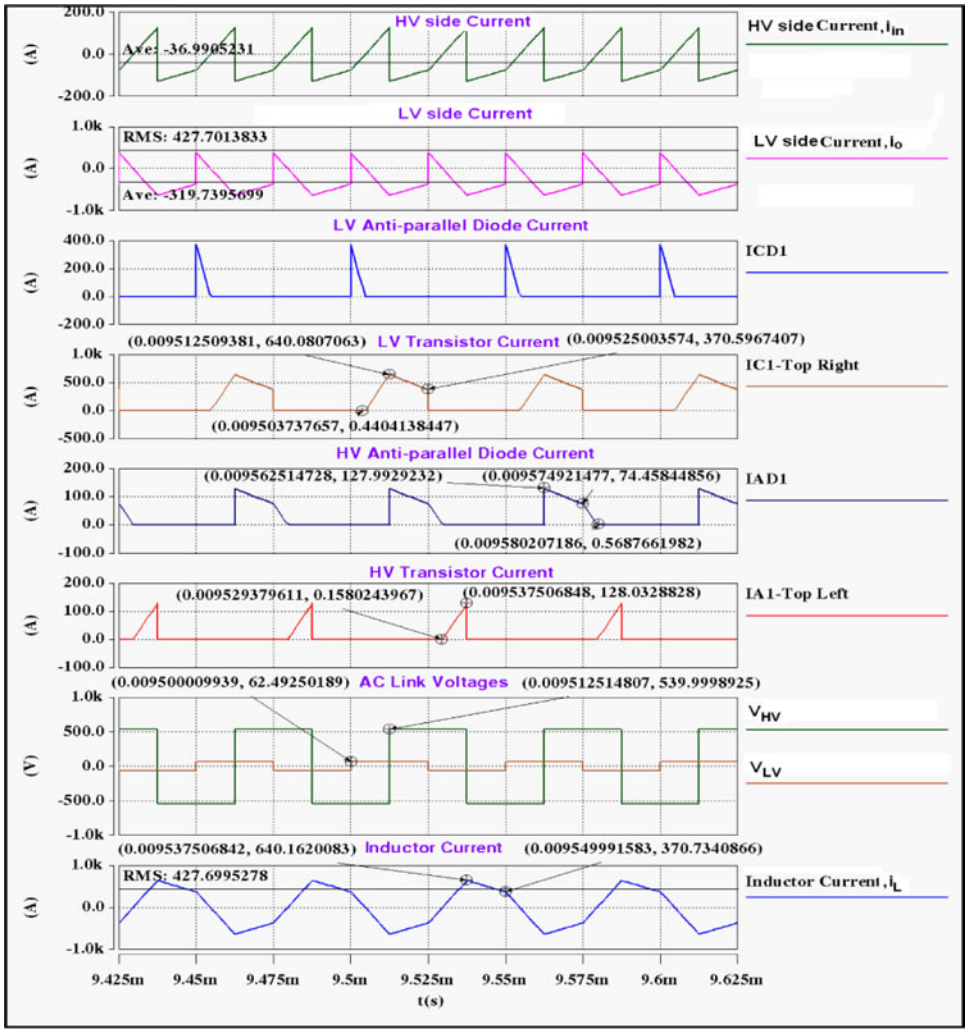

Fig. 5. Simulation results of the converter for boost mode. $V_{\mathrm{HV}} = 540\,\mathrm{V}$, $n = 1{:}\,0.2$, $V_{\mathrm{LV}} = 62.5\,\mathrm{V}$, $d = 0.5$, $P_0 = 20$ kW, $I_0 = 320\,\mathrm{A}$, $f_s = 20\,\mathrm{kHz}$, and $L = 2.11\ \mu\mathrm{H}$.

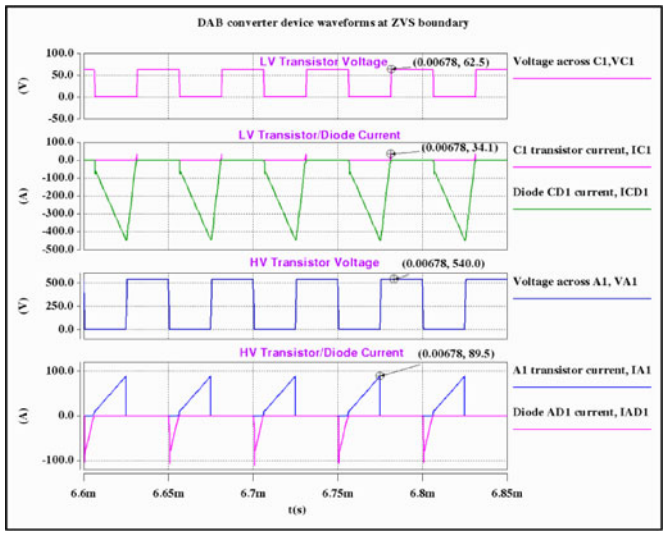

Fig. 6. Simulation results of the converter showing device waveforms at the ZVS boundary. $V_{\mathrm{HV}} = 540\,\mathrm{V}$, $n = 1{:}\,0.2$, $V_{\mathrm{LV}} = 62.5\,\mathrm{V}$, $d = 0.2386$, $P_0 = 14.5\,\mathrm{kW}$, $I_0 = 232\,\mathrm{A}$, $f_s = 20\,\mathrm{kHz}$, and $L = 2.11\ \mu\mathrm{H}$.

TABLE V
SIMULATION SETUP PARAMETERS

Simulation set-up parameter	Rating
Maximum power output	20kW
Nominal input (HV) voltage	540V
Output (LV) voltage	62.5V – 125V
Switching frequency	20kHz
Transformer turns ratio	1:0.2
Leakage Inductance	2.11μH

LV-side devices. The ZVS boundary occurs when the duty ratio between the bridges reaches a value of $d = 0.24$. The parameters for the simulation setup are given in Table V.

In the absence of snubber capacitors, the ZVS boundary was found to be $d = 0.21$ from the steady-state analysis. From Fig. 6, the instantaneous value of inductor current during the device turn-OFF is found to be 35.78 A, which is also the minimum current requirement necessary to achieve ZVS with a 100 nF snubber capacitor, as estimated from the model described in Section II, thus, confirming the accuracy of the model.

IV. Experimental Validation

A. DAB Converter Prototype Design

A DAB converter prototype was designed and constructed based on the proposed model to transfer 20 kW of power with a switching frequency of 20 kHz for an input (HV) voltage of 540 V and a nominal output (LV) voltage of 125 V. These figures are typical of likely future aerospace systems [32] at the HV side and the capabilities of ultracapacitor modules at the LV side. The converter is designed to meet the peak power demands of aircraft electric loads such as actuators and is based on data from the Intelligent Electrical Power Networks Evaluation Facility of Rolls-Royce University Technology Centre, University of Manchester. Assuming a 2:1 working range for the ultracapacitor voltage, the worst-case operating condition of the converter is: $V_{\rm HV} = 540$ V, $V_{\rm LV} = 62.5$ V, $I_{\rm rms} = 427$ A, $I_0 = 320$ A, $P_0 = 20$ kW, and $I_P = 640$ A, where $d = 0.5$.

The converter design is based on the new model presented in Section II. Key component values of the converter are determined by applying the worst case operating condition to the equations derived from the steady-state model. From (6), the coupling inductance is calculated as 2.11 μH for the worst case scenario of maximum power and minimum ultracapacitor voltage. At this operating condition, d was assumed to be 0.5. Using the average and rms current values on the HV and LV sides, the rms currents flowing through the HV- and LV-side filter capacitors were estimated as 77 and 283 A, respectively. For the worst case, to maintain 1% ripple voltage, capacitors of 123 μF and 2.91 mF, are required for the HV and LV sides, respectively. Low ESR filters were used on both the HV- and LV-side bridges. Based on the model, the conduction loss of devices can be calculated using the average current equations given in Tables II and IV. The switching loss calculation was made using the energy loss curves from the device datasheet for the operating frequency of 20 kHz. Ultrafast 1200 V, 300 A phase leg IGBT modules (SKM300GB125D) from Semikron have been selected for the HV-side bridge and fourth generation high temperature 600 V, 760 A phase leg IGBT modules (SKM600GB066D) from Semikron have been chosen for the LV-side bridge. Simple lossless snubber capacitors were selected to reduce the turn-OFF switching loss of the IGBTs. The peak current flowing through snubbers at the time of turn-OFF, determined from the model, and the corresponding *dv/dt* were estimated for the worst-case operating condition. 47 nF and 100 nF polypropylene pulse capacitors have been chosen for the HV and LV sides, respectively. Considering the snubber capacitor charging time, a dead time of 2.2 μs between the top and bottom IGBTs of a phase leg was chosen. The switching time of the LV-side IGBT as per the manufacturer's datasheet is about 1 μs. The dead time needs to be longer than the transistor switching time. Although inclusion of snubber capacitor across the IGBT reduces the initial current fall time, it significantly increases the tail current suppression time due to reduced *dv/dt*. In addition, the dead time generated by *RC* networks of the IGBT driver was incorporated into the design. To minimize circuit parasitics, the circuit connections were configured using planar busbars. The entire converter is forced air-cooled. The devices on the HV and LV sides of the DAB converter were individually tested with an inductive load to their full voltages and maximum currents, and the corresponding results were presented in [30].

TABLE VI
Design Specifications of the DAB Converter Prototype

Performance parameter	Rating
Maximum power output	20kW
Nominal input (HV) voltage	540V
Output (LV) voltage	62.5V – 125V
Switching frequency	20kHz
Maximum input ripple voltage	<2%
Maximum output ripple voltage	<5%

TABLE VII
Experimental Setup Parameters for Testing

Experimental set-up parameter	Rating
Power output	7kW
Nominal input (HV) voltage	390V
HV side IGBT	1200V, 300A, SKM300GB125D
Output (LV) voltage	181V
LV side IGBT	600V, 760A, SKM600GB066D
Input Filter Capacitor	100μF
Output Filter Capacitor	360μF
Load Resistance	5Ω
Switching frequency	20kHz
Transformer turns ratio	1:1
Coupling Inductance	61.2μH

B. Experimental Results

To practically validate the new steady-state model presented in Section II, experimental results were obtained for a power transfer of 7 kW at 20 kHz for $d = 0.5$, $V_{\rm HV} = 390$ V, and $V_{\rm LV} = 180.77$ V with a resistive load of R = 5 Ω connected on the LV-side bridge. Experimental testing of the converter was performed with the two active bridges interfaced through a transformer of 1:1 turns ratio with an air core coupling inductor $L = 61.2$ μH. A dc blocking capacitor was connected in series with transformer windings to prevent transformer saturation. A common-mode choke was connected to both supply rails and a damping filter was introduced to improve the EMC of the converter. The experimental results are presented mainly to demonstrate the effectiveness of the steady-state model, and therefore results for the DAB converter operating under buck mode alone are presented in this section as results for operation under boost mode can be obtained in a similar manner. Fig. 7 shows a photograph of the prototype and Table VI highlights its main features. Table VII gives the parameters for experimental testing of the DAB converter.

Figs. 8–12 show measured waveforms of the DAB converter for maximum power transfer ($d = 0.5$) and for the ZVS boundary

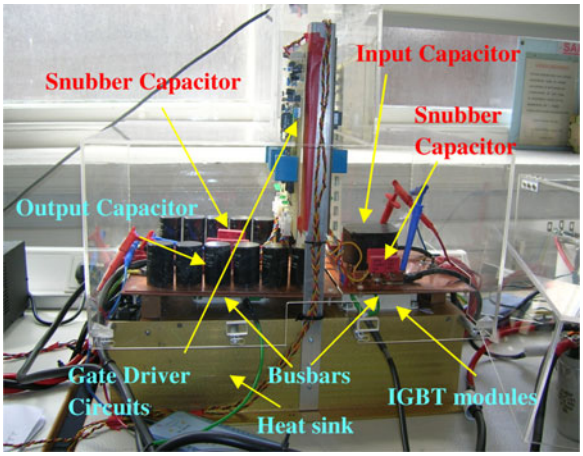

Fig. 7. Photograph of the DAB dc–dc converter prototype.

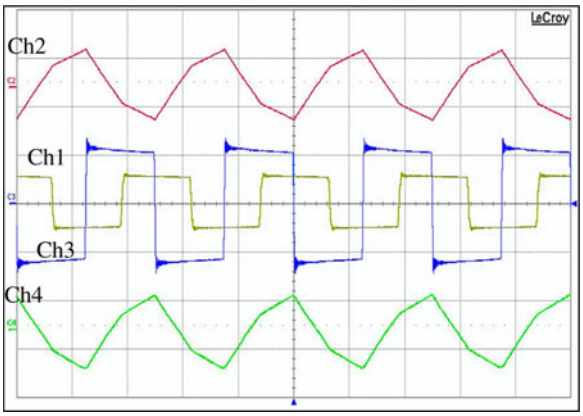

Fig. 8. Experimental results of the DAB converter at 7 kW during buck mode. Voltages generated by the full bridges V_{HV} and V_{LV} (Ch3 and Ch1: 350 V/div) and the currents through the transformer windings (Ch2 and Ch4: 100 A/div). Timescale: 20 μs/div.

($d = 0.33$). The voltages generated by the full bridges and the transformer currents are displayed in Fig. 8. The HV-side device current and voltage waveforms, the inductor current, and the output voltage waveforms are shown in Fig. 9. Fig. 10 shows the LV-side device current and voltage waveforms, and the output current waveform. The oscillations observed on the device voltages, currents, and transformer voltages are due to resonances induced between the stray inductance and snubber capacitance during device switching. The converter operates with an efficiency of 90% at 7 kW. The predicted steady-state values from the model are $I_P = 79.7$ A, $I_0 = 39.8$ A, $I_{L1} = 36.6$ A, and $I_{\mathrm{rms}} = 50.2$ A and the measured results are $I_P = 73$ A, $I_0 = 35$ A, $I_{L1} = 31$ A, and $I_{\mathrm{rms}} = 47$ A. The differences between measured and calculated currents are likely due to the effect of resistive load on the converter waveforms and parameter uncertainties in component values, winding resistances, dead-time generation of drivers, etc. Overall, there is a close agreement among the experimental results, simulations, and mathematical analysis.

The experimental results presented in Figs. 11 and 12 confirm the operation of the converter prototype over the ZVS

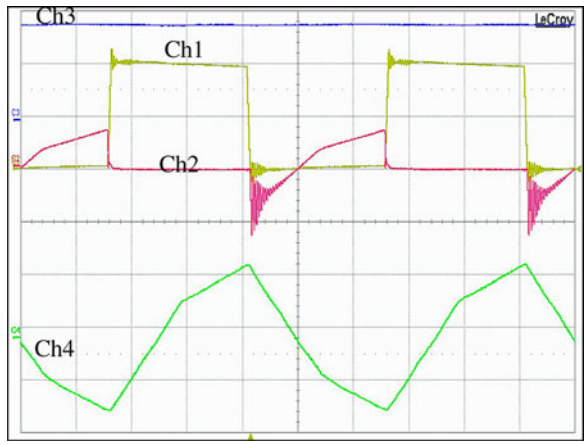

Fig. 9. Experimental results of the DAB converter at 7 kW during buck mode. HV-side device voltage and current (Ch1: 200 V/div; Ch2: 100 A/div), output voltage (Ch3: 100 V/div), and inductor current (Ch4: 50 A/div). Timescale: 10 μs/div.

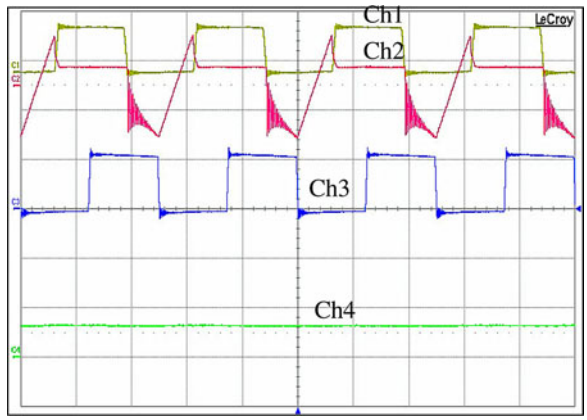

Fig. 10. Experimental results of the DAB converter at 7 kW during buck mode. LV-side device voltage and current (Ch1: 200 V/div, Ch2: 50 A/div), output current (Ch4: 50 A/div), and transformer primary voltage (Ch3: 350 V/div). Timescale: 20 μs/div.

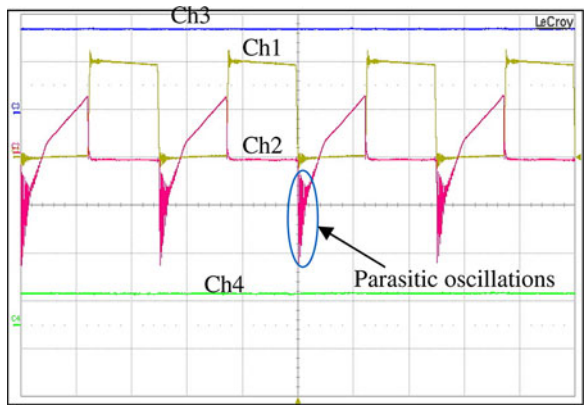

Fig. 11. Experimental results of the DAB converter under ZVS boundary operation at 6.4 kW during buck mode. HV-side device voltage and current (Ch1: 200 V/div, Ch2: 50 A/div), output voltage (Ch3: 100 V/div), and output current (Ch4: 50 A/div). Timescale: 20 μs/div.

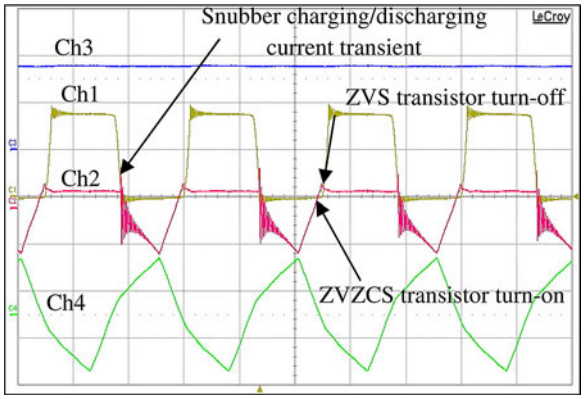

Fig. 12. Experimental results of the DAB converter for ZVS boundary operation at 6.4 kW during buck mode. LV-side device voltage and current (Ch1: 100 V/div, Ch2: 50 A/div), inductor current (Ch4: 50 A/div), and output voltage (Ch3: 100 V/div). Timescale: 20 μs/div.

boundary and validate the DAB converter model presented in Section II. It can be seen in Fig. 12 that positive current oscillations are present in the LV-side device current waveform at turn-ON of the antiparallel diode. However, the oscillations are small in magnitude and occur since there is insufficient stored energy in the inductor to be able to fully charge/discharge the snubber capacitor. This is because the converter is operating slightly outside the ZVS boundary due to parameter uncertainties in components and resistances, slight variation in duty ratios, and delays in control signals between the practical system and simulation model.

Figs. 13 and 14 show the respective turn-ON and turn-OFF transients of HV-and LV-side devices of the DAB converter for 7 kW power transfer. From Figs. 13(a) and 14(a), it can be seen that diode conduction occurs before the transistor conducts. This ensures ZVS/ZCS turn-ON of IGBTs. Moreover, the diode turns OFF at zero current thus eliminating reverse-recovery loss. The effect of snubber capacitor in limiting voltage rising slope during the device turn-OFF process can also be seen in the figures.

In Fig. 14(a), it can be observed that the duration of diode conduction interval is longer than that in Fig. 13(a). This is due to the rectification function performed by the LV-side diode of the DAB converter. From Figs. 13(b) and 14(b), the time taken for the tail current to reduce to zero is noted as 0.65 μs for the HV-side ultrafast IGBT; for the LV-side trench IGBT, it takes a significantly longer time (1.25 μs) for the tail current to reduce to zero. This is owing to the effect of snubber capacitor on the IGBT tail current and the characteristics of semiconductor device technologies.

Fig. 15 captures the power loss breakdown of the DAB converter prototype at the maximum power transfer operating point, namely, $d = 0.5$ and the ZVS boundary point $d = 0.33$, with snubber capacitors present. The measured results confirm that the converter operates with an efficiency of 90.13% at $d = 0.5$, and at 90.82% under the ZVS boundary $d = 0.33$. Although snubber capacitors were used across all the IGBTs, the switching losses of HV-side IGBTs are high when compared to other converter losses as highlighted in Fig. 15. The total loss at the maximum duty ratio was found to be 693 W, which is

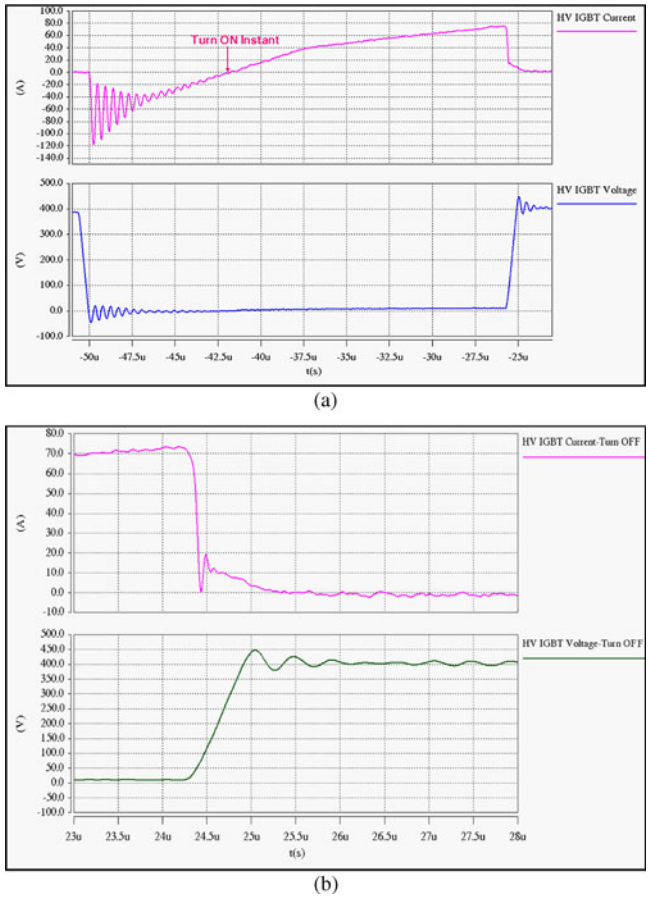

Fig. 13. Experimental results. (a) Turn-ON and (b) turn-OFF transient waveforms of HV IGBT. $V_{\rm in} = 390$ V, $V_0 = 180.77$ V, $I_{\rm OFF} = 73$ A, $L = 61.2$ μH, $P_{\rm in} = 7020$ W, $P_0 = 6327$ W, $f_s = 20$ kHz, $C_s = 47$ nF, and $R = 5$ Ω.

18.1% higher than the losses occurring at the ZVS operating boundary of the DAB converter when snubber capacitors were introduced. This is mainly because of an increase in the IGBT conduction and turn-OFF switching losses on the HV and LV sides. The diode conduction losses remain approximately constant and there is no reverse-recovery loss due to ZVS operation. Copper losses incurred in the air core inductor increase as the phase shift increases due to an increase in rms current. The losses in the filters remain approximately constant and are of low value due to the small equivalent series resistance (ESR) of the filter capacitors.

A comparison of theoretical device conduction losses and passive component losses estimated from the steady-state model with the experimental loss per device at 7 kW throughput is shown in Fig. 16. Device losses were estimated from the model given in Table II for the operating condition specified in Fig. 16. The conduction losses of power devices were calculated from their average current model given in Table II. For example, HV-side transistor conduction losses are calculated as follows:

$$P_{\rm HVT,Cond} = V_{\rm CE(ON)} \times I_{\rm avg(HVT)} \times \left(\frac{(T_S/2) - t_B}{T_S} \right) \tag{27}$$

where $I_{\rm avg(HVT)}$ as shown at the bottom of this page. $V_{\rm CE(ON)}$ is obtained from the typical output characteristics of the device

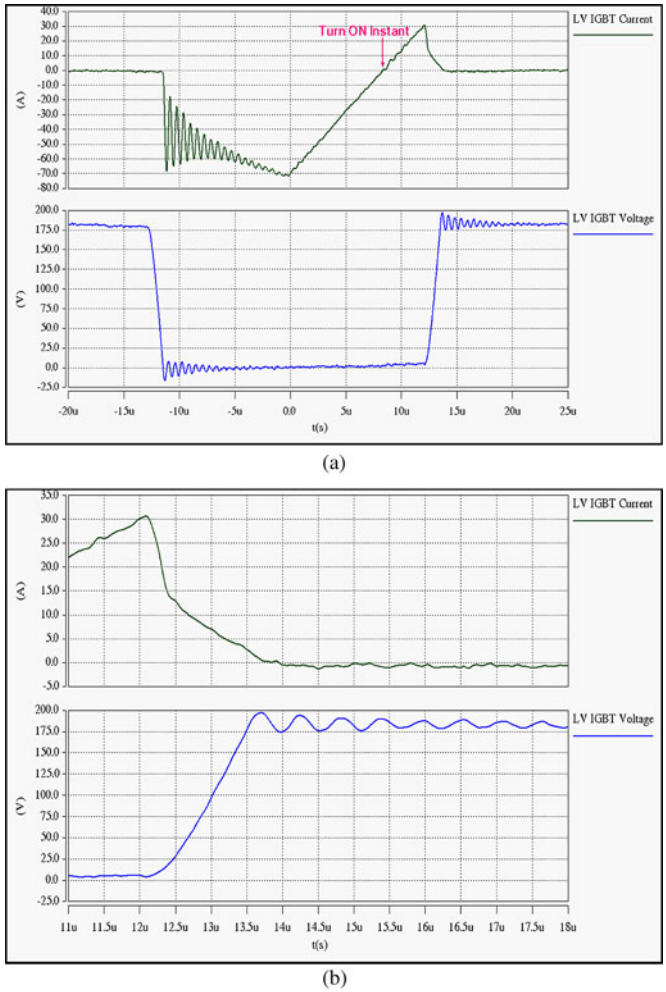

Fig. 14. Experimental results. (a) Turn-ON and (b) turn-OFF transient waveforms of LV IGBT. $V_{\rm in} = 390$ V, $V_0 = 180.77$ V, $I_{\rm OFF} = 31$ A, $L = 61.2$ μH, $P_{\rm in} = 7020$ W, $P_0 = 6327$ W, $f_s = 20$ kHz, $C_s = 100$ nF, and $R = 5$ Ω.

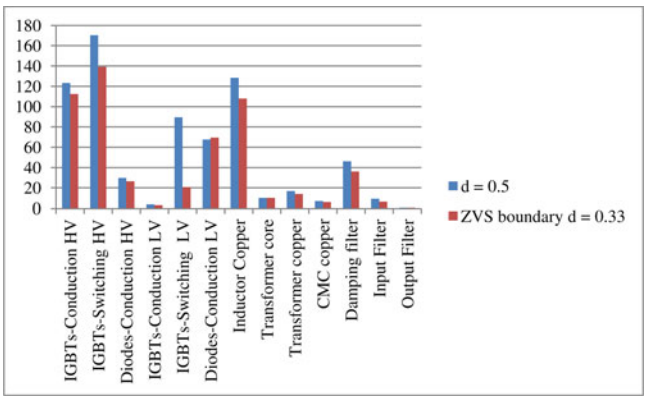

Fig. 15. Experimental power loss distribution of the DAB converter. $V_{\rm in} = 390$ V, $f_s = 20$ kHz, $R = 5\Omega$, $L = 61.2$ μH, $C_{S-\rm HV} = 47$ nF, $C_{S-\rm LV} = 100$ nF, $V_0 = 180.77$ V at $d = 0.5$ and $V_0 = 174.91$ V at $d = 0.33$.

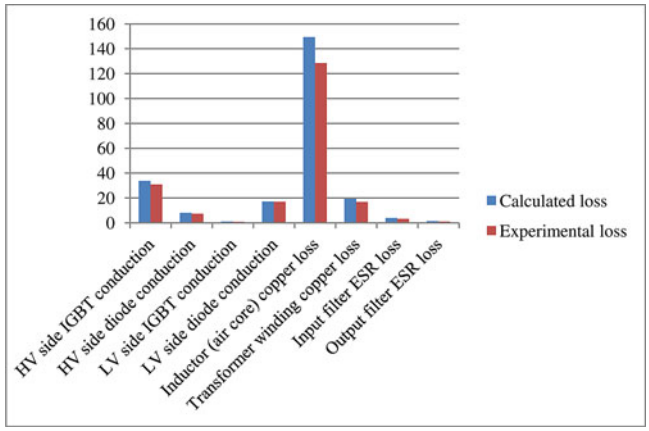

Fig. 16. Comparison of predicted and experimental losses. $V_{\rm in} = 390$ V, $V_0 = 180.77$ V, $L = 61.2$ μH, $P_{\rm in} = 7020$ W, $P_0 = 6327$ W, $f_s = 20$ kHz, and $R = 5\Omega$.

datasheet and $(T_S/2) - t_B$ is the conduction interval of the HV-side transistor.

Similarly, HV-side diode conduction losses are calculated as follows:

$$P_{\rm HVD,Cond} = V_f \times I_{\rm avg(HVD)} \times \left(\frac{t_B}{T_S}\right) \tag{28}$$

where $I_{\rm avg(HVD)} = ((1/2) \times I_P \times t_B/t_B)$, V_f is the diode forward voltage drop obtained from the diode forward characteristics given in the datasheet, and t_B is the conduction interval of the HV-side diode. A similar procedure was followed to calculate the LV-side transistor and diode conduction losses. The converter is designed to operate within the ZVS range; hence, turn-ON losses of transistor and reverse-recovery losses of diodes are zero. Although the transistor turn-OFF occurs under ZVS, switching current during turn-OFF instant is significant; hence, turn-OFF losses of transistors are calculated from the typical turn-OFF energy loss curves given in the datasheet for the corresponding turn-OFF current and operating voltage

$$P_{\rm HVT,Sw} = E_{\rm OFF(Sw)} \times f_S \times \frac{V_{\rm CE(SW)}}{V_{\rm CC}} \tag{29}$$

where $E_{\rm OFF(Sw)}$ is energy loss for the corresponding turn-OFF current, f_S is the switching frequency, $V_{\rm CE(Sw)}$ is the operating voltage of the transistor, and $\rm V_{CC}$ is the maximum voltage for which the energy loss curves are defined.

Using (11) and the winding resistance of transformer, inductor, and ESR of capacitors, the passive component losses, as shown in Fig. 16, were predicted. For the air core inductor, the copper losses are calculated using the rms current given in (11) and the inductor copper resistance $R_L\,(f_s) = 58.13$ mΩ; hence, $P_L = I_{\rm rms}^2 \times R_L\,(f_s)$.

The dc copper losses in the transformer winding can be calculated using the total dc resistance of 8 mΩ and is given by $P_{Tr} = I_{\rm rms}^2 \times R_{\rm dc}$.

$$I_{\rm avg(HVT)} = \frac{(1/2) \times I_{L1} \times ((dT_S/2) - t_B) + (1/2) \times (I_{L1} + I_P) \times ((T_S/2) - (dT_S/2))}{(T_S/2) - t_B}.$$

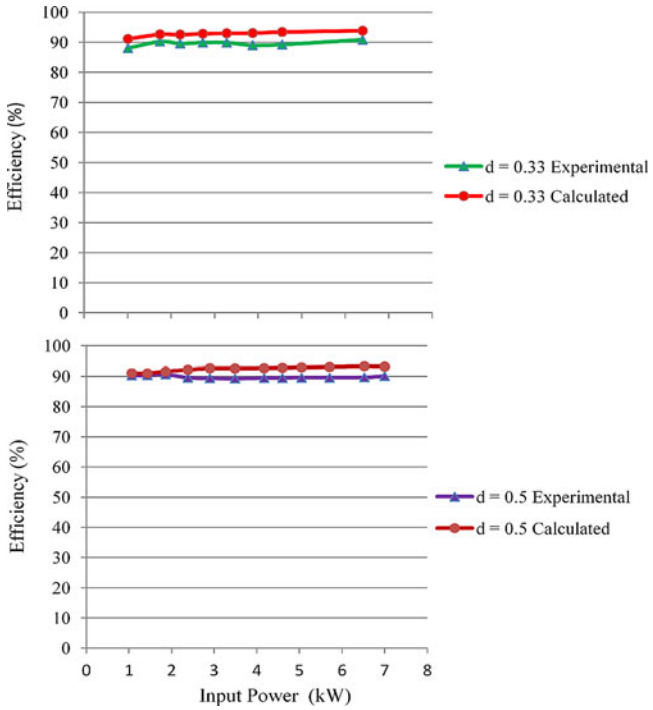

Fig. 17. Efficiency versus DAB converter input power for operating points: $d = 0.33$ (ZVS) and $d = 0.5$ (maximum power transfer). (▲): experimental and (●): calculated.

Input filter ESR is 1.5 mΩ and its loss is calculated as $P_{\mathrm{InputFilter}} = I_{\mathrm{rms}}^2 \times \mathrm{ESR}_{\mathrm{IF}}$.

For the output filter, 12 metalized polypropylene capacitors connected in parallel each having 6 mΩ ESR result in a total ESR of 500 $\mu\Omega$. Hence, the output filter loss due to ESR is calculated as $P_{\mathrm{OutputFilter}} = I_{\mathrm{rms}}^2 \times \mathrm{ESR}_{\mathrm{OF}}$.

A close agreement between theoretical and experimental losses can be observed in Fig. 16, which once again confirms the accuracy of the proposed model.

The DAB converter is designed to operate within the ZVS range. Fig. 17 shows the experimentally measured efficiency and calculated efficiency (from the proposed model) versus the converter input power for two different operating points: $d = 0.33$ (ZVS) and $d = 0.5$ (maximum power transfer). It can be concluded that the calculated efficiency is in very close agreement with the measured efficiency. The difference between the calculated and measured efficiencies are likely due to the effect of snubber capacitor on device switching losses and parameter uncertainties. However, the variation is within 2% of the overall operating range, which demonstrates the effectiveness of the proposed model.

V. Conclusion

This paper has presented a new steady-state model for the DAB converter. The square-wave operating mode of DAB is the best mode for high-power transfer. The proposed model produced key design equations for the square-wave mode of the DAB dc–dc converter. Expressions for average and rms device currents, along with peak and rms currents of the coupling inductor were obtained from the model. These equations are useful in predicting losses that occur in the devices and passive components and enable a study of the converter characteristics, in addition to aiding in the practical design of converter prototypes. The influence of the snubber capacitor was analyzed in detail and the minimum current required to operate the converter in the soft-switching region, and its corresponding duty ratio for buck and boost modes, has been determined. The operation of the DAB dc–dc converter has been verified through extensive simulations which, in turn, confirm the accuracy of the model. The experimental results confirm that provision of snubber capacitors across the IGBTs reduces switching losses and device stresses and improves the converter performance. The experimental testing validated the steady-state model, the prototype design, and the theoretical predictions, as discussed in this paper. The experimental results are presented for 7 kW, 390/180 V, 20 kHz operation as well as for ZVS boundary working conditions of the prototype with a measured efficiency of 90%. The simulation and experimental results are in good agreement demonstrating the effectiveness of the steady-state model. Therefore, the proposed model can serve as an important teaching-cum-research tool for DAB hardware design (devices and passive components selection), soft-switching-operating range estimation, and performance prediction at the design stage.

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R. T. Naayagi (M'12) received the B.E degree (University first rank and gold medal) from Bharathidasan University, Tiruchirapalli, India, in 2000, the M.Sc. (IT) degree from Alagappa University, Karaikudi, India, in 2003, the M.E degree (University second rank and gold medal) from Anna University, Chennai, India, in 2005, and the Ph.D. degree in electrical and electronic engineering from the University of Manchester, Manchester, U.K., in 2010.

She is currently a Professor at S. A. Engineering College (affiliated to Anna University). From 2000 to 2006 and 2010 to 2011, she was also a Lecturer/Senior Lecturer in various institutions in India and the U.K. Her research interests include power electronics for aerospace, electric vehicle applications, and power electronic solutions to sustainability.

Dr. Naayagi is a reviewer for the IEEE, the Institution of Engineering and Technology, and other international journals. She received the Best Outgoing Female Graduate award during her Bachelor's and the Outstanding Master's Student award. She is the first recipient of the Engineering and Physical Sciences Research Council's Rolls Royce Dorothy Hodgkin Postgraduate Award for her Ph.D. studies in the School of Electrical and Electronic Engineering at the University of Manchester.

Andrew J. Forsyth (M'98) received the B.Sc. (Eng.) degree from Imperial College, London, U.K., in 1981, and the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 1987.

From 1981 to 1983, he was a Design Engineer with GEC Electrical Projects Ltd. From 1986 to 1990, he was a Lecturer at the University of Bath. From 1991 to 2004, he was a Lecturer/Senior Lecturer at Birmingham University. Since 2004, he has been a Professor of Power Electronics at the University of Manchester, Manchester, U.K. His research interests include HF converters, high-power-factor rectifiers, modeling and control of autonomous power systems, aerospace, and electric vehicle applications.

R. Shuttleworth (M'98) received the B.Sc. and Ph.D. degrees from the University of Manchester, Manchester, U.K., in 1972 and 1976, respectively.

He was with GEC Traction for one year. He later became a Lecturer in the power systems research group at the University of Manchester, where he has been a Lecturer in the power conversion group of the School of Electrical and Electronic Engineering since 2004. He has been involved in research on a number of areas related to power systems and power electronics. He is the author or coauthor of more than 70 papers and holds 8 patents. His current research interests include LED street lighting, charger circuits for electric vehicles, energy harvesting, and energy recovery from waste heat.