# High Step-Up DC-DC Converters Using Zero-Voltage Switching Boost Integration Technique and Light-Load Frequency Modulation Control

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***Abstract*—This paper describes nonisolated high step-up DC-DC converters using zero voltage switching (ZVS) boost integration technique (BIT) and their light-load frequency modulation (LLFM) control. The proposed ZVS BIT integrates a bidirectional boost converter with a series output module as a parallel-input and series-output (PISO) configuration. It provides many advantages such as high device utilization, high step-up capability, power and thermal stress distribution, switch voltage stress clamping, and soft switching capability. As an example of ZVS BIT, a flyback converter with a voltage-doubler rectifier (VDR) as a series output module is presented and analyzed in detail. In addition, to overcome the efficiency degradation at a light load due to the load-dependent soft switching capability of the proposed ZVS BIT, a control method using a frequency modulation (FM) proportional to the load current is proposed. By means of ZVS BIT and LLFM control, the overall conversion efficiency is significantly improved. The experimental results are presented to clarify the proposed schemes.**

***Index Terms*—Boost integration technique (BIT), frequency modulation (FM), step-up ratio, zero-voltage switching (ZVS).**

## I. Introduction

NONISOLATED DC-DC conversion applications such as electric vehicles (EV), photovoltaic (PV) grid-connected power systems, fuel cells, uninterruptible power supplies (UPS), and high-intensity-discharge (HID) lamps for automobile headlamps call for high-performance step-up techniques [1], [5], [13]. The general approach to these applications is a classical boost converter having simple structure, continuous input current, and clamped switch voltage stress to the output voltage. However, the limited step-up capability due to the parasitic resistances, the reverse recovery problem caused by a high voltage rating diode, and the large switching losses due to the hard switching are major obstacles not allowing the high step-up ratio and efficiency.

To handle these concerns, several converter topologies adopting the voltage conversion ability, i.e., a voltage-multiplier, a coupled-inductor, a transformer, and a stacked output capacitor, have been proposed [1]–[23].

In [2]–[6], it has been demonstrated that a voltage-multiplier using additional diodes and capacitors on the output stage in a classical boost converter contributes to extending a step-up ratio without the penalty of an extreme duty ratio. However, as the output voltage is increased, the number of stages is increased, demanding more capacitors and diodes. Moreover, the snubber circuits across the switches and diodes increase the cost, losses, and design complexity. Also, no soft switching capability still confines the efficiency to be low.

A coupled-inductor employed in a boost converter is also a favorable step-up technique for its simple structure [1], [7]–[12]. Although it can achieve a high efficiency and protect the switch from the high peak voltage, an auxiliary circuit is required to suppress the switch voltage stress. The active-clamp cell in the coupled-inductor scheme can alleviate this problem [10]–[12]. Also, it can achieve the soft switching performance. However, the active-clamp cell in [10] and [11] is quite complex, requiring a pair of switches and diodes. Although the cell presented in [12] can reduce the number of active devices, the additional resonant inductor to guarantee the ZVS should be adopted. Besides, as the auxiliary turns of a coupled-inductor are increased to raise a step-up ratio further, an input current ripple becomes larger in return. Thus, more input filter is needed.

Another easy approach for a high step-up ratio is the current-fed type converters using a transformer [14]–[21]. A transformer leakage inductance causes a voltage spike across the switches so that a snubber circuit is required, resulting in an additional loss. The active-clamp approach similar to that applied on the coupled-inductor scheme releases these problems and reduces switching losses by using its soft switching capability [17]–[21].

Unfortunately, in view of the clamp capacitors in [10]–[12] and [17]–[21], they are connected to the input side so that it has no function of extending a step-up ratio.

Focused on the step-up ratio extension with the concept of the stacked output capacitors, the high step-up boost-flyback converter is proposed in [22] and improved with a secondary voltage-doubler rectifier in [23]. Despite their high step-up capability, the switch suffers from the hard switching losses.

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This paper includes previously presented literatures titled as

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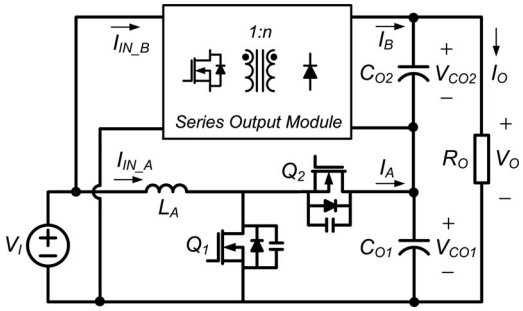



Fig. 1. Conceptual diagram of ZVS BIT.

As a desirable solution to the abovementioned drawbacks, this paper proposes nonisolated high step-up DC-DC converters using a zero-voltage switching (ZVS) boost integration technique (BIT). It integrates a bidirectional boost converter into several isolated current-fed type converters as a parallel-input and series-output (PISO) configuration. This connection makes the bidirectional boost converter an active-clamp circuit which is not connected to the input side but the output side. Therefore, it can use a high step-up capability of the stacked output capacitors while maintaining the soft switching capability of the active-clamp circuit. Furthermore, several advantages such as high device utilization, power and thermal stress distribution, and switch voltage stress clamping can be achieved. Since a leakage inductor alleviates *di*/*dt* of the secondary rectifier current, reverse recovery problems too can be reduced.

However, the proposed ZVS BIT has the load-dependent ZVS condition, which is an inherent characteristic of the active-clamp circuit. It causes a hard switching at a light load and degrades the conversion efficiency. To recover the ZVS at a light load, a control method using a frequency modulation (FM) is also proposed, which can be applied to other active-clamp schemes to improve light-load efficiency.

The general concept and features of the proposed ZVS BIT are introduced first. Then, a flyback converter with a voltage-doubler rectifier (VDR) as a series output module is proposed and analyzed in detail as an example of ZVS BIT. Next, the light-load frequency modulation (LLFM) control is presented. Also, other converters derived from the ZVS BIT are proposed and summarized. The experimental results are presented to verify the proposed schemes.

## II. Zero-Voltage Switching Boost Integration Technique

Fig. 1 shows the conceptual diagram of ZVS BIT. A series output module is connected to a bidirectional boost converter as a PISO configuration. This series output module can be any isolated current-fed type converter. Also, it can adopt any kind of secondary rectifiers such as the full-bridge, center-tapped, voltage-doubler, and so on. For an easy understanding of the proposed ZVS BIT, an example using a flyback converter as a series output module is introduced as shown in Fig. 2.

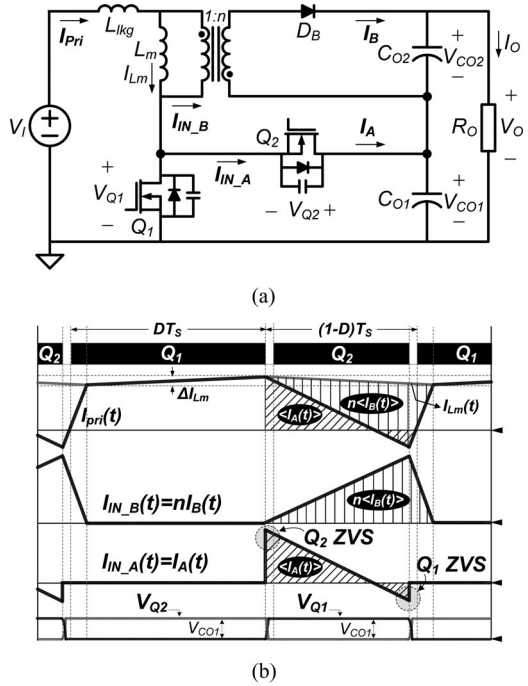



Fig. 2. Derived ZVS flyback-boost converter: (a) Flyback converter as a series output module. (b) Key waveforms.

### A. High Device Utilization

To increase the device utilization and simplify the circuit, the common parts integration between a series output module and a bidirectional boost converter is recommended. Fig. 2 shows an example of the common parts integration. As shown in Fig. 2(a), a bidirectional boost converter and a flyback converter can be integrated easily since the boost inductor $L_A$ and switch $Q_1$ in Fig. 1 become the flyback converter counterparts.

### B. High Step-up Capability

Due to the stacked output capacitors, each output capacitor voltage is added and the overall output voltage can be extended as

$$V_O = V_{CO1} + V_{CO2}. \tag{1}$$

That is, the output voltage of the converters employing the proposed ZVS BIT is a sum of the output voltages of the boost converter and the series output module, which is suitable for high step-up applications.

### C. Power and Thermal Stress Distribution

By imposing the node equations on the output capacitor $C_{O2}$, the steady-state output current equation can be derived as

$$I_O = \langle I_A(t) \rangle = \langle I_B(t) \rangle \tag{2}$$

where $\langle \bullet \rangle$ denotes the average value of $\bullet$. Equation (2) implies the power distribution between the bidirectional boost converter and the series output module is proportional to each output voltage. Therefore, the thermal stress can be decentralized.

Since the same average current flows through each output capacitor, the current distribution at the primary side is also predictable and can be expressed as follows:

$$n\langle I_{\mathrm{IN\_}A}(t)\rangle = \langle I_{\mathrm{IN\_}B}(t)\rangle. \tag{3}$$

That is, the current distribution ratio at the powering phase only depends on the transformer turns ratio $n$, which decides the slope of the primary current $I_{\mathrm{pri}}(t)$ while $Q_1$ is turned off. It is noted from Fig. 2(b) that the powering current distribution depicted by the diagonal-lined and vertical-lined areas satisfies (2) and (3).

### D. Switch Voltage Stress Clamping

The switch voltage stresses $V_{Q1}$ and $V_{Q2}$ can be clamped to the partial output voltage $V_{CO1}$. Thus, additional protection circuit for the high voltage spike caused by a leakage inductor $L_{\mathrm{lkg}}$ is not required.

### E. Soft Switching Capability

The proposed ZVS BIT seems to be an active-clamp network, which is not connected to the input side but the output side. The previous works regarding the active-clamp circuit concentrate on the soft switching capability and switch voltage stress clamping [10]–[12], [17]–[21]. However, the proposed ZVS BIT provides these abilities as well as the step-up ratio extension because of the series output connection of the clamp capacitor $C_{O1}$.

The soft switching characteristics are similar to the active-clamp circuit. A main switch $Q_1$ has a load-dependent ZVS condition relying on the value of the leakage inductor $L_{\mathrm{lkg}}$, whereas an auxiliary switch $Q_2$ has a wide ZVS load range resulting from a large boost inductor $L_m$. Thus, all switches can be turned on under ZVS condition if the energy stored in $L_{\mathrm{lkg}}$ is sufficient.

However, since ZVS condition of $Q_1$ is load-dependent and lost at a light load due to the insufficient leakage energy, the efficiency degradation caused by switching loss is inevitable. To improve the efficiency even at a light load, the magnetizing current ripple, $\Delta I_{Lm}$ in Fig. 2(b), extension by the frequency modulation control can recover the ZVS of $Q_1$. The detailed principle of this control method will be presented in Section IV.

## III. Flyback Converter With VDR as a Series Output Module

To analyze the converter adopting the ZVS BIT in detail, a ZVS flyback-boost converter with voltage-doubler rectifier (VDR) is proposed and introduced, as shown in Fig. 3.

Based on the circuit shown in Fig. 2, a VDR is adopted at the secondary side to clamp the output rectifier voltage stress. Also, this VDR contributes the increase in a step-up ratio further. Thus, the proposed converter has the high step-up capability by the help of both ZVS BIT and VDR. With the features of ZVS BIT, the proposed converter can ensure the high operating frequency, high step-up ratio, low voltage stresses across the switches and output rectifiers, soft switching of all switches, and so on.

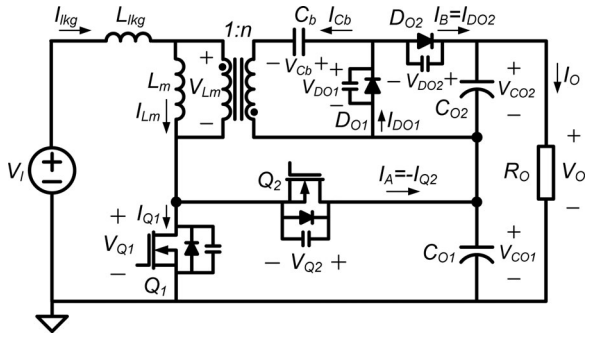



Fig. 3. Circuit diagram of ZVS flyback-boost converter with VDR.

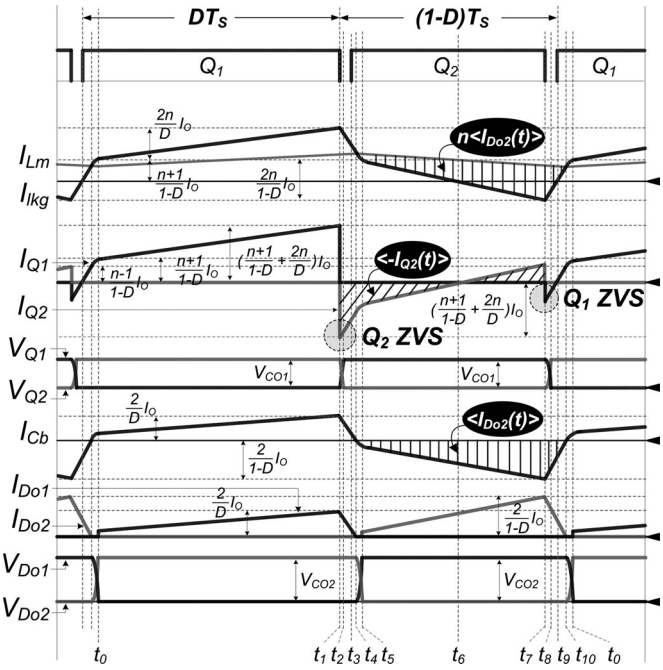



Fig. 4. Steady-state waveforms of ZVS flyback-boost converter with VDR.

### A. Circuit Operation

Figs. 4 and 5 illustrate the steady-state waveforms and topological states of the proposed converter, respectively. Due to the VDR, the circuit acts as a conventional forward converter when the main switch $Q_1$ is turned ON and a flyback-boost converter when $Q_1$ is turned OFF. At the boosting phase, when $Q_1$ is turned ON, the transferred current through a transformer charges a link capacitor $C_b$. At the powering phase, when $Q_1$ is turned OFF, $C_b$ is discharged. It is noted that the vertical-lined and diagonal-lined areas, which represent each average value of two powering currents, should agree with (2) as follows:

$$I_O = \langle -I_{Q2}(t)\rangle = \langle I_{DO2}(t)\rangle. \tag{4}$$

After considering (4) and the transformer turns ratio $n$, the current distribution ratio at the primary side follows (3), since $I_{\mathrm{IN\_}A}(t) = -I_{Q2}(t)$ and $I_{\mathrm{IN\_}B}(t) = nI_{DO2}(t)$ at the powering phase.

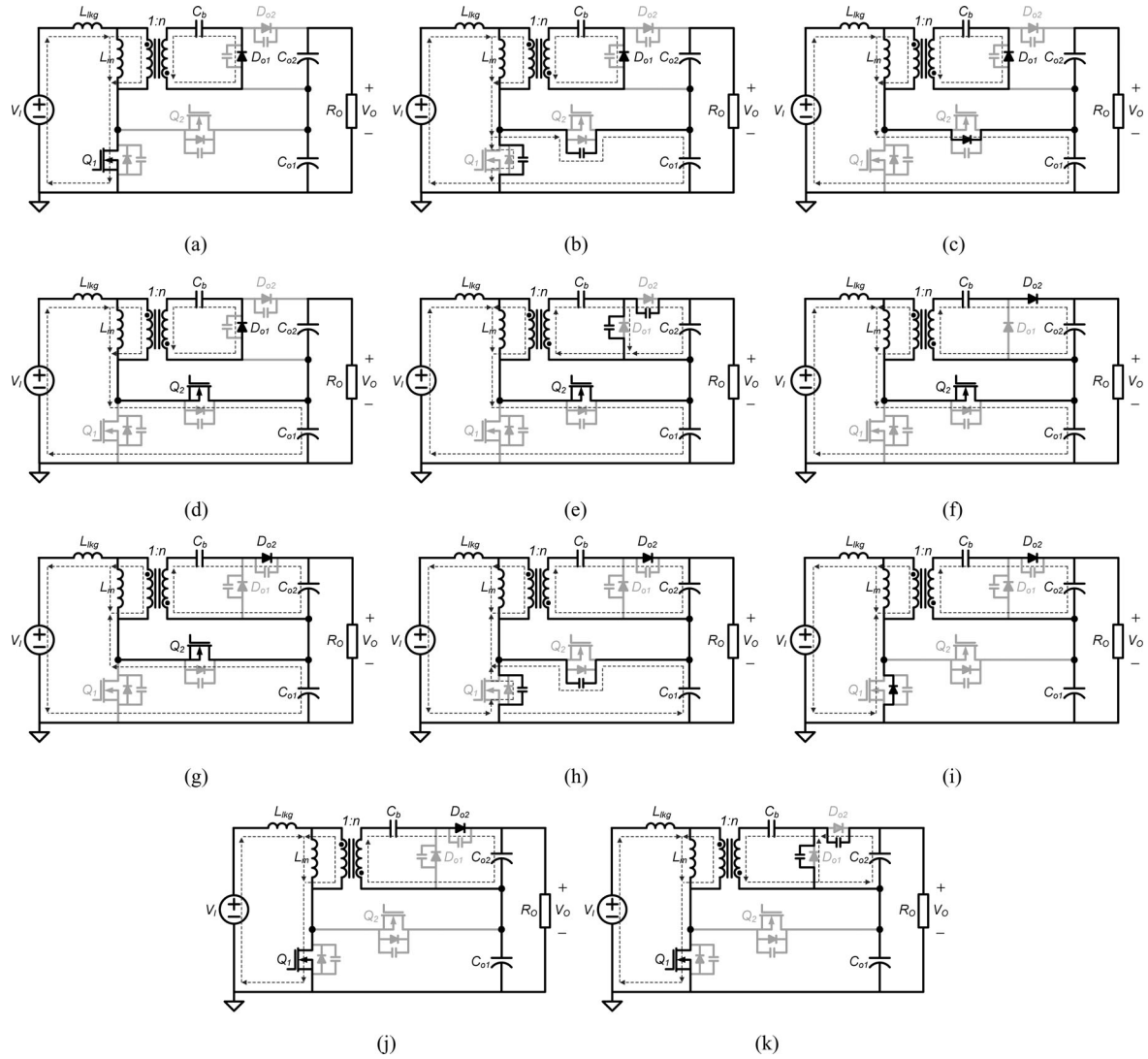



Fig. 5. Topological states of ZVS flyback-boost converter with VDR: (a) Mode 1 ($t_0$–$t_1$), (b) Mode 2 ($t_1$–$t_2$), (c) Mode 3 ($t_2$–$t_3$), (d) Mode 4 ($t_3$–$t_4$), (e) Mode 5 ($t_4$–$t_5$), (f) Mode 6 ($t_5$–$t_6$), (g) Mode 7 ($t_6$–$t_7$), (h) Mode 8 ($t_7$–$t_8$), (i) Mode 9 ($t_8$–$t_9$), (j) Mode 10 ($t_9$–$t_{10}$), and (k) Mode 11 ($t_{10}$–$t_0$).

To present the operation of each mode sequentially, it is assumed that the voltage transition between the secondary rectifiers $D_{O1}$ and $D_{O2}$ has been finished at $t = t_0$.

*Mode 1 ($t_0$–$t_1$):* At $t = t_0$, the transferred current via the transformer flows through the output rectifier $D_{O1}$ to charge the link capacitor $C_b$, which is similar to the operation of the conventional forward converter. Because the applied voltage across $L_m$ is $V_{Cb}/n$, the current $I_{\rm lkg}(t)$ is linearly increased as follows:

$$I_{\rm lkg}(t) = \frac{V_I - V_{Cb}/n}{L_{\rm lkg}}(t - t_0) + I_{\rm lkg}(t_0). \tag{5}$$

*Mode 2 ($t_1$–$t_2$):* At $t = t_1$, the switch $Q_1$ is turned OFF. The current $I_{\rm lkg}(t)$ charges the junction capacitor of $Q_1$ to $V_{CO1}$ and discharges that of $Q_2$ to 0 V in a short time.

*Mode 3 ($t_2$–$t_3$):* After the junction capacitor of $Q_1$ is charged to $V_{CO1}$ at $t = t_2$, the antiparallel diode of $Q_2$ is conducted. Thus, no protection circuit is required, and the primary conduction loss can be reduced by using lower voltage-rated power switches. The conducting antiparallel diode provides the zero voltage across $Q_2$ until the next mode. The current $I_{\rm lkg}(t)$ is linearly decreased as follows:

$$I_{\rm lkg}(t) = \frac{V_I - V_{CO1} - V_{Cb}/n}{L_{\rm lkg}}(t - t_2) + I_{\rm lkg}(t_2). \tag{6}$$

This decreasing current during $t_1$–$t_4$ is also reflected to $I_{DO1}(t)$. Thereby, $L_{\rm lkg}$ alleviates $di/dt$ of $I_{DO1}(t)$ and this current snubbing effect can reduce the reverse recovery problem.

*Mode 4 ($t_3$–$t_4$):* At $t = t_3$, the switch $Q_2$ is turned on under ZVS conditions. The current $I_{\rm lkg}(t)$ continuously decreases until it reaches the magnetizing current $I_{Lm}(t)$ at $t_4$.

*Mode 5 ($t_4$–$t_5$):* At $t = t_4$, the diode $D_{O1}$ is reverse-biased. The transferred current via the transformer charges the junction capacitor of $D_{O1}$ to $V_{CO2}$ and discharges that of $D_{O2}$ to 0 V for a short time, respectively. During this period, the abrupt build-up current occurs both at the primary and secondary sides due to the resonance between $L_{\rm lkg}$ and the junction capacitors of secondary rectifiers, which is well presented in [24]. This

resonant current can be expressed as

$$I_{\mathrm{lkg}}(t) = -\frac{n(V_{CO1} - V_I) + V_{Cb}}{\sqrt{L_{\mathrm{lkg}}/(C_{j1} + C_{j2})}} \sin(\omega_r(t - t_4)) + I_{\mathrm{lkg}}(t_4) \tag{7}$$

where

$$\omega_r = \frac{1}{n\sqrt{L_{\mathrm{lkg}}(C_{j1} + C_{j2})}}. \tag{8}$$

$C_{j1}$ and $C_{j2}$ denote the junction capacitor of $D_{O1}$ and $D_{O2}$, respectively.

*Mode 6 ($t_5$–$t_6$):* After completing the voltage transition from $D_{O2}$ to $D_{O1}$ at $t_5$, $D_{O2}$ is conducted and $C_b$ is discharged. The current $I_{\mathrm{lkg}}(t)$ is linearly decreased until it reaches zero as follows:

$$I_{\mathrm{lkg}}(t) = \frac{V_I - V_{CO1} + (V_{CO2} - V_{Cb})/n}{L_{\mathrm{lkg}}}(t - t_5) + I_{\mathrm{lkg}}(t_5). \tag{9}$$

*Mode 7 ($t_6$–$t_7$):* At $t = t_6$, the current $I_{\mathrm{lkg}}(t)$ changes its direction from positive to negative and keeps the negative slope as (9) until the switch $Q_2$ is turned OFF at $t_7$. The current $I_{\mathrm{lkg}}(t)$ flows back to the input source.

*Mode 8 ($t_7$–$t_8$):* At $t = t_7$, the switch $Q_2$ is turned OFF. The primary leakage current $I_{\mathrm{lkg}}(t)$ charges the junction capacitor of $Q_2$ to $V_{CO1}$ and discharges that of $Q_1$ to 0 V, respectively.

*Mode 9 ($t_8$–$t_9$):* After the junction capacitor of $Q_2$ is charged to $V_{CO1}$ at $t = t_8$, the anti-parallel diode of $Q_1$ is conducted. The current $I_{\mathrm{lkg}}(t)$ is linearly increased as follows:

$$I_{\mathrm{lkg}}(t) = \frac{V_I + (V_{CO2} - V_{Cb})/n}{L_{\mathrm{lkg}}}(t - t_8) + I_{\mathrm{lkg}}(t_8). \tag{10}$$

This increasing current also provides the current snubbing effect of $I_{DO2}(t)$.

*Mode 10 ($t_9$–$t_{10}$):* At $t = t_9$, the switch $Q_1$ is turned ON under ZVS conditions. The current $I_{\mathrm{lkg}}(t)$ increases until it reaches the magnetizing current $I_{Lm}(t)$ at $t = t_{10}$.

*Mode 11 ($t_{10}$–$t_0$):* At $t = t_{10}$, the transferred current via the transformer charges the junction capacitor of $D_{O2}$ to $V_{CO2}$ and discharges that of $D_{O1}$ to 0 V for a short time, respectively. Similar to Mode 5, the resonant current is built up for a quarter of a resonant period $\omega_r$ noted in (8), and is expressed as follows:

$$I_{\mathrm{lkg}}(t) = \frac{nV_I + V_{CO2} - V_{Cb}}{\sqrt{L_{\mathrm{lkg}}/(C_{j1} + C_{j2})}} \sin(\omega_r(t - t_{10})) + I_{\mathrm{lkg}}(t_{10}). \tag{11}$$

### B. Step-up Ratio

As a matter of convenience to derive the step-up ratio, the relatively narrow intervals, $t_1$–$t_5$ and $t_7$–$t_0$, are assumed to be zero and the ripple-free current $I_{Lm}(t)$ is assumed. The values on the current waveform in Fig. 4 are derived under these assumptions. By applying the volt-second balance rules on $L_{\mathrm{lkg}}$ and $L_m$ and the current-second balance rule on $C_b$ while considering (1) and (4), the step-up ratio of the proposed converter can be found as

$$M = \frac{V_O}{V_I} = \frac{n + 1}{1 - D + (2n^2/D^2)Q} \tag{12}$$

$$M_1 = \frac{V_{CO1}}{V_I} = \frac{1}{1 - D} \tag{13}$$

where the dimensionless parameter $Q$ is defined as $(L_{\mathrm{lkg}} f_S)/R_O$ and $f_S$ denotes the switching frequency. Provided that $Q$ is small enough, the step-up ratio of overall system can be approximated to

$$M = \frac{V_O}{V_I} \approx \frac{n + 1}{1 - D} \tag{14}$$

$$M_2 = \frac{V_{CO2}}{V_I} \approx \frac{n}{1 - D} \tag{15}$$

$$\frac{V_{Cb}}{V_I} \approx n. \tag{16}$$

Equations (13)–(15) show that the integrated boost converter contributes the overall step-up ratio $M$ by adding its step-up ratio $M_1$. The step-up ratio of the proposed converter is higher than those of the flyback, $nD/(1\text{-}D)$, and ZVS flyback-boost converter, $(nD+1)/(1\text{-}D)$, as shown in Fig. 6(a). Fig. 6(b) shows the step-up ratio $M$ according to the variation of $Q$, which mainly depends on $L_{\mathrm{lkg}}$. As shown in this figure, since the overall step-up ratio $M$ falls as $Q$ increases, the turns ratio $n$ and the nominal duty ratio $D$ should be selected by considering the damping effect of $Q$. Since $Q$ depends on the load resistance $R_O$ and $L_{\mathrm{lkg}}$ while $f_S$ is constant, the value of the leakage inductor is a dominant factor affecting $Q$ at the worst case, i.e., a full load condition. Thus, a smaller leakage inductor is preferable to a higher step-up ratio.

### C. Output Capacitors $C_{O1}$ and $C_{O2}$

By calculating the quantity of electric charge or discharge on $C_{O1}$ and $C_{O2}$, the voltage ripple of each output capacitor can be derived as follows:

$$\frac{\Delta V_{CO1}}{V_O} = \frac{n}{4DR_O C_{O1} f_S} \tag{17}$$

$$\frac{\Delta V_{CO2}}{V_O} = \frac{(1 + D)^2}{4R_O C_{O2} f_S}. \tag{18}$$

### D. Link Capacitor $C_b$

In a similar way, the necessary value of the link capacitor can be determined from the voltage ripple equation as follows:

$$C_b = \frac{V_O}{R_O f_S \Delta V_{Cb}}. \tag{19}$$

### E. ZVS Conditions

To achieve the ZVS of the switch $Q_1$, the energy stored in the leakage inductor at $t_7$ must be large enough to fully charge and discharge the junction capacitors of $Q_2$ and $Q_1$, respectively, before the switch $Q_1$ is turned ON. The ZVS conditions of the switch $Q_1$ by neglecting the transformer parasitic capacitor can be expressed as

$$0.5 L_{\mathrm{lkg}} I_{\mathrm{lkg}}^2(t_7) \geq 0.5(C_{OSS1} + C_{OSS2}) V_{CO1}^2 \tag{20}$$

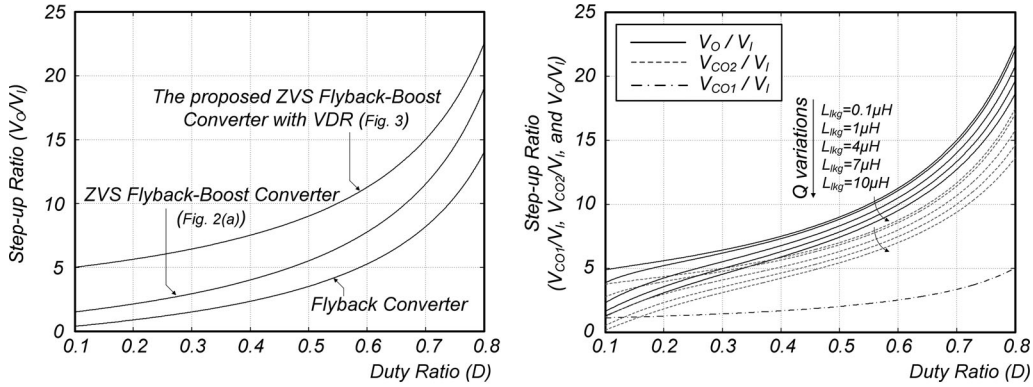



Fig. 6. Step-up ratio when $n = 3.5$: (a) Comparison of step-up ratios $V_O/V_I$ when $Q = 0$, (b) $V_{CO1}/V_I$, $V_{CO2}/V_I$, and $V_O/V_I$ according to leakage inductor variations ($f_s = 70$ kHz).

$$I_{\rm lkg}(t_7) = \left(M - \frac{2n}{1-D}\right)\frac{V_O}{R_O}. \tag{21}$$

$C_{OSS1}$ and $C_{OSS2}$ denote the junction capacitors of $Q_1$ and $Q_2$, respectively. Similarly, the ZVS conditions of the auxiliary switch $Q_2$ can be found as

$$0.5L_m I_{Lm}^2(t_1) + 0.5L_{\rm lkg} I_{\rm lkg}^2(t_1) \geq 0.5(C_{OSS1} + C_{OSS2})V_{CO1}^2 \tag{22}$$

$$I_{Lm}(t_1) = M\frac{V_O}{R_O} \tag{23}$$

$$I_{\rm lkg}(t_1) = \left(M + \frac{2n}{D}\right)\frac{V_O}{R_O}. \tag{24}$$

Regardless of the leakage inductor, $Q_2$ can easily achieve ZVS through the energy stored in the magnetizing inductor $L_m$.

In summary, the main switch $Q_1$ has a load-dependent ZVS condition relying on $L_{\rm lkg}$, whereas the auxiliary switch $Q_2$ has a wide ZVS load range due to a large magnetizing inductor $L_m$. Thus, to assure the ZVS of all switches, (20) should be satisfied. From (20), the desired leakage inductor, which decides a ZVS load range, can be selected as shown in Fig. 7. A boundary between ZVS and non-ZVS range in Fig. 7, $I_{O\min\_ZVS\_Lkg}$, can be derived from (20) and (21) as follows:

$$I_{O\min\_ZVS\_Lkg} = \sqrt{\frac{C_{OSS1} + C_{OSS2}}{L_{\rm lkg}}} \cdot \frac{V_{CO1}}{(2n/(1-D) - M)}. \tag{25}$$

The curve and point on Fig. 7 are originated from the parameters used in the experiment. In this case, the ZVS load boundary $I_{O\min\_ZVS\_Lkg}$ is 0.155 A. That is, the ZVS of all switches can be guaranteed from a 25% load to a full load. On the other hand, the ZVS of $Q_1$ is lost below a 25% load condition due to the insufficient energy stored in $L_{\rm lkg}$. Thus, a large leakage inductor, i.e., small $I_{O\min\_ZVS\_Lkg}$, is preferable to a wide ZVS range.

Increasing an external leakage inductor is an easy approach to extend a ZVS range. A large leakage inductor can lower the ZVS load boundary $I_{O\min\_ZVS\_Lkg}$ as noted in (25) and Fig. 7. However, as a leakage inductor increases, an increasing rate of

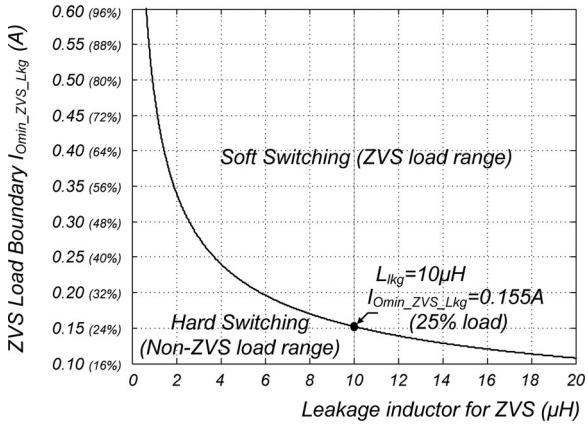



Fig. 7. ZVS load boundary according to leakage inductor.

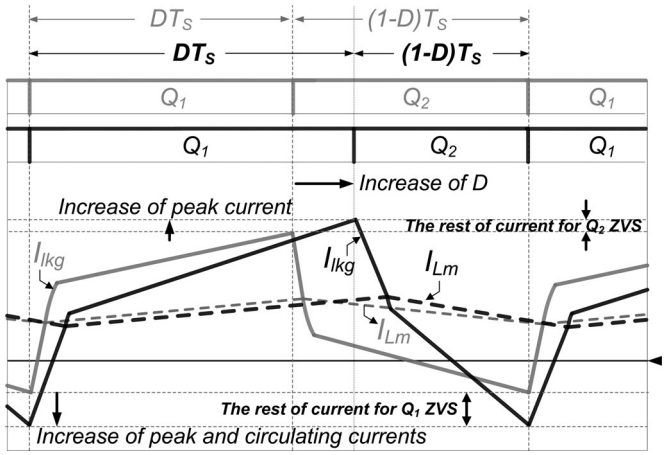



Fig. 8. Effect of increasing leakage inductor at heavy load condition (gray-line, in case of small leakage inductor; black-line, in case of large leakage inductor).

the ZVS range decreases because $I_{O\min\_ZVS\_Lkg}$ is inversely proportional to the square root of a leakage inductor. For example, with Fig. 7, the increase from 2 $\mu$H to 10 $\mu$H contributes to the ZVS range extension from 53% to 25% load condition. On the other hand, the increase from 12 $\mu$H to 20 $\mu$H extends

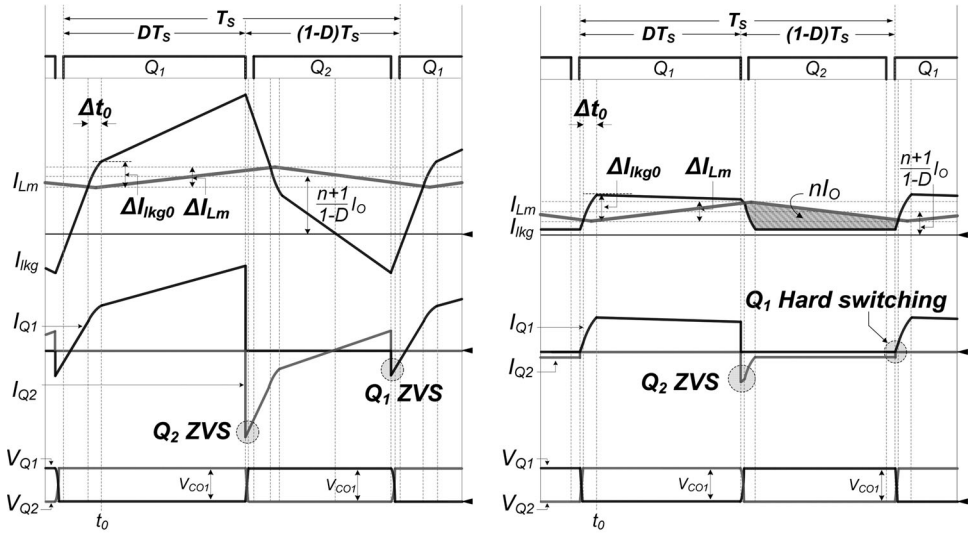



Fig. 9. Key Waveforms of ZVS flyback-boost converter with VDR according to load condition: (a) at heavy load (ZVS load range), and (b) at light load (non-ZVS load range).

the ZVS range at most from 22% to 17% load condition. That is, increasing a leakage inductor cannot facilitate the ZVS range extension effectively at a light load.

Furthermore, if a large leakage inductor is used to maintain the ZVS even at a light load despite the poor effectiveness, the efficiency degradation occurs at a heavy load condition adversely. As the leakage inductor increases, the voltage step-up capability decays as noted in Fig. 6(b) so that the duty ratio $D$ should be increased for the compensation. It causes the increase in the peak and RMS values of the primary leakage current. Accordingly, extra conduction losses can be generated by the rest of the currents satisfying the ZVS. Fig. 8 summarizes this effect. In addition, the conduction loss from the additional leakage inductor windings can also deteriorate the efficiency at a heavy load.

Consequently, increasing $L_{\mathrm{lkg}}$ excessively to extend a ZVS range is not effective at a light load. Also, it can cause extra conduction losses at a heavy load. Therefore, the leakage inductor should be limited to the reasonable value.

## IV. Light-Load Frequency Modulation Control

In order to extend a ZVS load range without increasing the leakage inductor, a light-load frequency modulation (LLFM) control is proposed.

### A. Circuit Operation at Light Load

Fig. 9 illustrates the key waveforms of ZVS flyback-boost converter with VDR according to the load condition. Compared with Fig. 9(a), it is noted in Fig. 9(b) that ZVS of a main switch $Q_1$ is lost since the decreased load current is lower than $I_{O\min\_\mathrm{ZVS\_Lkg}}$.

As the load current decreases, the primary leakage current $I_{\mathrm{lkg}}(t)$ is distorted as shown in Fig. 9(b). This results from the effect of both the magnetizing current ripple $\Delta I_{Lm}$ and the

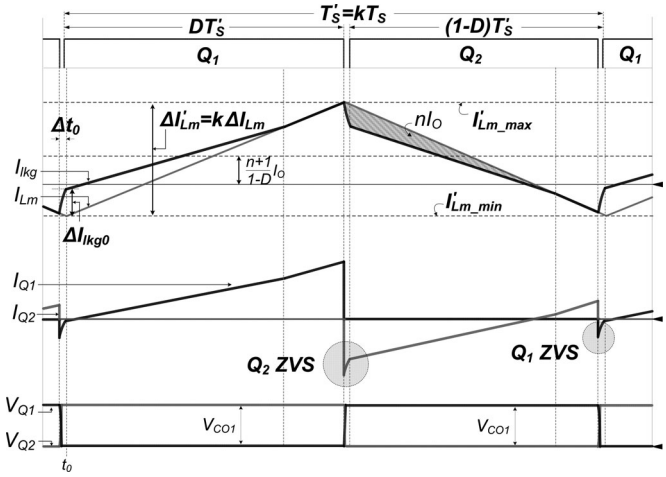



Fig. 10. Effect of decreasing frequency at light load.

abrupt current build-up of $I_{\mathrm{lkg}}(t)$ during $\Delta t_0$, i.e., $\Delta I_{\mathrm{lkg0}}$. Since these two quantities are constant values at any load condition, the magnitudes of $\Delta I_{Lm}$ and $\Delta I_{\mathrm{lkg0}}$ in both Fig. 9(a) and (b) are the same. Thus, these two quantities affect the shape of $I_{\mathrm{lkg}}(t)$ dominantly as the load current decreases, as shown in Fig. 9(b).

Since the imposed voltage on $L_m$ is $V_{Cb}/n$ for $DT_S$, the magnitude of $\Delta I_{Lm}$ is easily calculated and approximated by using (16) as follows:

$$\Delta I_{Lm} = \frac{V_{Cb}}{nL_m} DT_S \approx \frac{V_I}{L_m} DT_S. \tag{26}$$

The abrupt current build-up of $I_{\mathrm{lkg}}(t)$ during $\Delta t_0$ is caused by the resonance between a leakage inductor and junction capacitors of secondary rectifiers during the secondary rectifier voltage transition interval, which was presented as Mode 11 in Section III-A. Since this resonant current derived in (11) flows for a quarter of

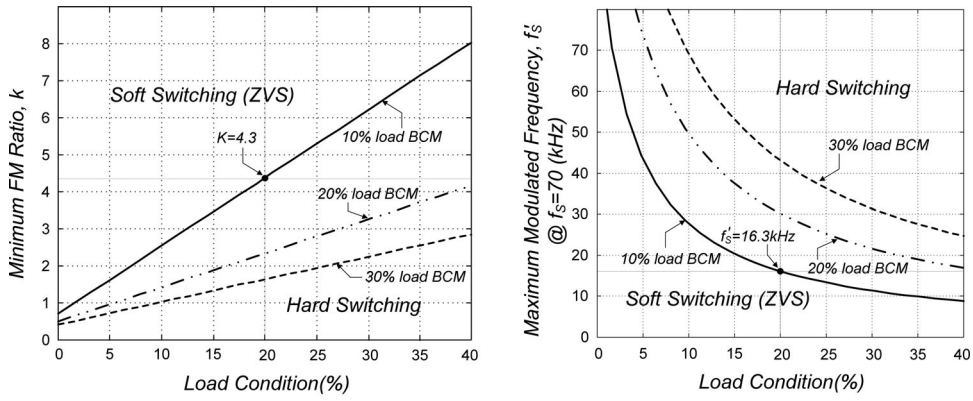



Fig. 11. Minimum FM ratio and maximum modulated frequency for ZVS of $Q_1$ at light load: (a) Minimum FM ratio $k$. (b) Maximum modulated frequency $f'_S$.

a resonant period $\omega_r$, the time interval $\Delta t_0$ can be derived as

$$\Delta t_0 = \frac{\pi}{2} n \sqrt{L_{\mathrm{lkg}}(C_{j1} + C_{j2})}. \tag{27}$$

Thus, the magnitude of $\Delta I_{\mathrm{lkg0}}$ can be expressed by using (11) and (27) as follows:

$$\Delta I_{\mathrm{lkg0}} = \frac{nV_I + V_{CO2} - V_{Cb}}{\sqrt{L_{\mathrm{lkg}}/(C_{j1} + C_{j2})}}. \tag{28}$$

It is pointed out that the load current information is nowhere in (26)–(28). That is, each value is constant regardless of the load level. Therefore, the current waveforms are distorted due to the reduced powering current compared with these constant values at a light load.

### *B. Effect of Decreasing Switching Frequency at Light Load*

By decreasing a switching frequency for the load range below $I_{O\min\_\mathrm{ZVS\_Lkg}}$, $Q_1$ can recover ZVS by the energy stored in a magnetizing inductor $L_m$.

Fig. 10 shows the effect of decreasing a switching frequency at a light load. Compared with the waveforms before the frequency modulation (FM) shown in Fig. 9(b), $\Delta I_{\mathrm{lkg0}}$ and $\Delta t_0$ are not changed and the switching period and the magnetizing current ripple are extended to $T'_S$ and $\Delta I'_{Lm}$, respectively, until the minimum value of $I'_{Lm}$, $I'_{Lm\_\min}$, becomes negative. This negative magnetizing current can provide ZVS of $Q_1$ even at a light load. Meanwhile, since the increased value of the maximum magnetizing current $I'_{Lm\_\max}$ still provides ZVS of $Q_2$, ZVS of all switches is obtained by decreasing a switching frequency. It is also noted that the shaded areas in both Figs. 9(b) and 10 are the same and this value is identical to $nI_O$.

To obtain a general condition satisfying ZVS of $Q_1$ below the load condition of $I_{O\min\_\mathrm{ZVS\_Lkg}}$, a FM ratio $k$ can be defined as

$$k = \frac{f_S}{f'_S} = \frac{T'_S}{T_S} = \frac{\Delta I'_{Lm}}{\Delta I_{Lm}} > 1 \tag{29}$$

where the prime mark implies the parameters after FM. Since the negative value of $I'_{Lm\_\min}$ discharges a junction capacitor of $Q_1$ and charges that of $Q_2$ in a short time during $\Delta t_0$, the ZVS conditions of $Q_1$ by FM can be obtained as follows:

$$I'_{Lm\_\min} = I_{\mathrm{in}} - \frac{1}{2}\Delta I'_{Lm} = MI_O - \frac{1}{2}\Delta I'_{Lm} < 0 \tag{30}$$

$$\frac{1}{2} L_m I'^2_{Lm\_\min} \geq \frac{1}{2}(C_{OSS1} + C_{OSS2}) V^2_{CO1}. \tag{31}$$

By substituting (30) into (31), a minimum FM ratio according to the load current can be derived as

$$k \geq \frac{2M}{\Delta I_{Lm}} I_O + 2\sqrt{\frac{C_{OSS1} + C_{OSS2}}{L_m}} \cdot \frac{V_{CO1}}{\Delta I_{Lm}}. \tag{32}$$

Equation (32) can also be expressed in terms of the frequency relation as

$$f'_S \leq \frac{f_S}{(2M/\Delta I_{Lm})I_O + 2\sqrt{(C_{OSS1} + C_{OSS2})/L_m} \cdot (V_{CO1}/\Delta I_{Lm})}. \tag{33}$$

Fig. 11 depicts a minimum FM ratio and a maximum modulated frequency for achieving ZVS of $Q_1$ according to the load condition. A solid-line in Fig. 11(a) shows the critical value of $k$ to achieve the soft switching of $Q_1$ assuming that $L_m$ is designed to satisfy the boundary conduction mode (BCM) at a 10% load. Under this assumption, to achieve ZVS below a 20% load condition, $k$ should be higher than $k = 4.3$. In addition, since the value of $L_m$ influences both the magnitude of $\Delta I_{Lm}$ and the value of the load current satisfying BCM, the FM ratio can be adjusted by $L_m$ as depicted by dotted lines in Fig. 11(a). These phenomena also appear with respect to the frequency relation as shown in Fig. 11(b) when $f_S$ is 70 kHz. It is noted that a frequency less than 70/4.3 $\approx$ 16.3 kHz can guarantee ZVS below a 20% load condition when $L_m$ is designed to satisfy BCM at a 10% load.

### *C. Control Strategy*

Prior to confirming a frequency modulation ratio $k$ according to the load condition, ZVS load boundary $I_{O\min\_\mathrm{ZVS\_Lkg}}$ should be selected first by using (25). At the load range above $I_{O\min\_\mathrm{ZVS\_Lkg}}$, since all switches can be turned on under ZVS

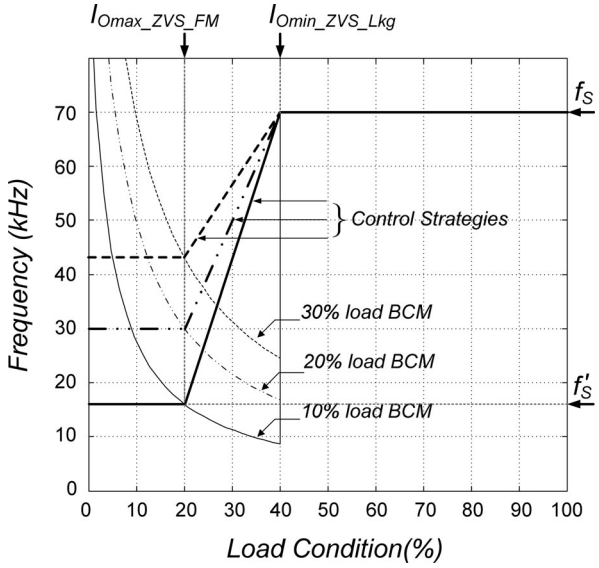



Fig. 12. FM control strategies according to load condition when $f_S = 70$ kHz.

conditions due to the sufficient energy stored in the leakage inductor, the FM control is unnecessary. Nevertheless, if the FM control is applied to the system, larger conduction losses caused by the increased $\Delta I_{Lm}$ occur. Thus, a fixed high-frequency control is recommended in this load range.

At the load range below $I_{O\min\_ZVS\_Lkg}$, the FM control can be effective to improve the conversion efficiency through the recovered ZVS. From Fig. 11(b), since the region at below the curves allows ZVS of $Q_1$, a constant modulated-frequency $f'_S$ is eligible below the desired load current. This desired load current is defined as a ZVS load boundary by FM, $I_{O\max\_ZVS\_FM}$. It can be derived from (32) as follows:

$$I_{O\max\_ZVS\_FM} = \frac{1}{M}\left(\frac{\Delta I_{Lm}}{2}\cdot k - \sqrt{\frac{C_{OSS1}+C_{OSS2}}{L_m}}\cdot V_{CO1}\right). \tag{34}$$

If $I_{O\max\_ZVS\_FM}$ is located at a 20% load, a constant frequency less than 16.3 kHz can ensure ZVS of all switches at the load range below $I_{O\max\_ZVS\_FM}$ from Fig. 11(b).

In summary, Fig. 12 shows control strategies according to the load condition when $f_S = 70$ kHz. It is assumed that the ZVS load boundary by $L_{\rm lkg}$, $I_{O\min\_ZVS\_Lkg}$, is set at a 40% load and the ZVS load boundary by FM, $I_{O\max\_ZVS\_FM}$, is set at a 20% load, respectively. Between these two boundaries, there is a frequency modulating region to avoid the abrupt frequency transition from $f_S$ to $f'_S$.

For an easy implementation, the slope of this region is assumed to be linear. If an FM ratio is increased until $I_{O\max\_ZVS\_FM}$ reaches $I_{O\min\_ZVS\_Lkg}$, i.e., $I_{O\max\_ZVS\_FM} = I_{O\min\_ZVS\_Lkg}$, the abrupt frequency transition as well as high conduction losses caused by the excessive FM ratio near $I_{O\max\_ZVS\_FM}$ can occur even though it provides the ZVS at an entire load range. Thus, a comparison between reduced switching losses and increased conduction losses due to FM should be considered when selecting $I_{O\max\_ZVS\_FM}$.

### *D. Comparison With Other Methods Extending ZVS Range*

To improve the efficiency, focused on reducing the switching losses, several methods are proposed [31]–[39]. These techniques can be classified into two categories: the quasiresonant technique [31], [32] and the active-clamp technique [33]–[39].

In the quasiresonant technique, the constant off-time control method at boundary conduction mode (BCM) can reduce the switching losses by using a resonant valley [31]. Theoretically, since the switching frequency approaches infinity as the load current approaches zero, this converter suffers from an extremely wide frequency range and excessive switching losses at a light load. To handle this problem, adaptive off-time control has been proposed, which increases the off-time adaptively while maintaining the soft switching at a light load [32]. However, the quasiresonant technique usually operates the converter in BCM and discontinuous conduction mode (DCM) at an entire load range. It causes high conduction losses at a heavy load. This is the main limitation of the quasiresonant technique.

The active-clamp technique can not only reduce the conduction losses by operating in continuous conduction mode (CCM) but also achieve the soft switching for both switches by utilizing the energy stored in a leakage inductor. Based on the active-clamp circuit presented in [33], several modified circuits have been proposed [34]–[38]. Although they have good performance in efficiency at heavy load condition, the load-dependent ZVS condition of the main switch and constant frequency control result in poor efficiency at light load condition due to the high switching losses.

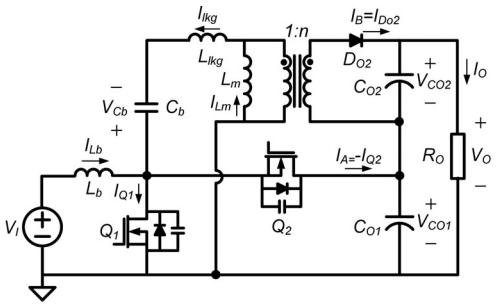
To achieve the ZVS of the main switch at any load conditions, a variable frequency control by adjusting the off-time with noncomplementary gate signals has been proposed [39]. Since an auxiliary switch is turned ON for a short time before the main switch is turned ON, the recycled leakage energy can be used to achieve the ZVS of the main switch, which reduces the circulating energy effectively compared to the conventional complementary switching techniques. However, the ZVS of an auxiliary switch is lost at an entire load range due to the noncomplementary gate signals. Furthermore, there is a narrow current pulse in the secondary side when the auxiliary switch turns ON, which can degrade the EMI performance.

The proposed LLFM technique uses a variable frequency control with complementary gate signals. The main difference from the previously introduced scheme is that there are two constant frequency ranges according to the load level. Also, there is a frequency transition range between two constant frequency ranges as noted in Fig. 12. Especially, the lower constant frequency can determine the ZVS recovering load range. Therefore, compared with [33]–[38], the proposed method can achieve ZVS even at a light load while maintaining the same soft switching performance and the same device stresses at heavy load condition. Compared with [39], the auxiliary switch can also achieve ZVS without any narrow current pulse in the secondary side. However, the circulating current is higher.

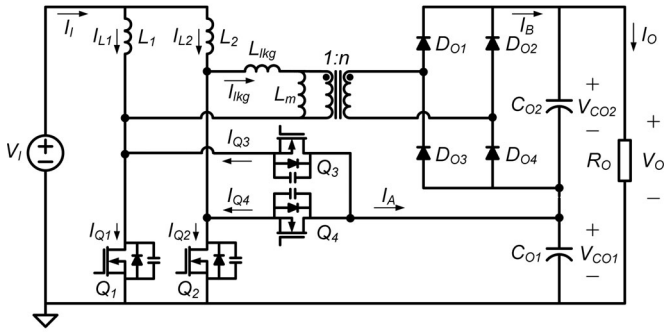
Table I summarizes the comparison of the several techniques to extend the ZVS load range. $Q_1$ and $Q_2$ in Table I indicate a main switch and an auxiliary switch, respectively.

TABLE I
COMPARISON OF SEVERAL ZVS RANGE EXTENSION TECHNIQUES

| Classifications | | No. of switches | Switching frequency | Conduction loss | | Switching loss | |
|---|---|---|---|---|---|---|---|
| | | | | Light load | Heavy load | Light load | Heavy load |
| Quasi-resonant technique | [31] | 1 | Variable | Low | High | High | Low |
| | [32] | 1 | Variable | High | High | Low | Low |
| Active-clamp technique | [33]-[38] | 2 | Constant | Low | Low | High ($Q_1$: Hard Sw.) ($Q_2$: ZVS) | Low ($Q_1$: ZVS) ($Q_2$: ZVS) |
| | [39] | 2 | Variable | Low | Low | Medium ($Q_1$: ZVS) ($Q_2$: Hard Sw.) | Medium ($Q_1$: ZVS) ($Q_2$: Hard Sw.) |
| | Proposed control | 2 | Variable | High | Low | Low ($Q_1$: ZVS) ($Q_2$: ZVS) | Low ($Q_1$: ZVS) ($Q_2$: ZVS) |




(a)




(b)

Fig. 13. Topology variations: (a) Isolated sepic converter as a series output module. (b) Current-fed half-bridge (CFHB) converter as a series output module.

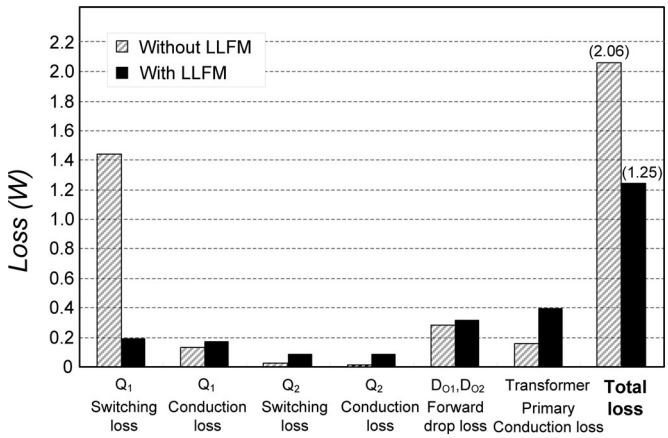



Fig. 14. Estimated loss comparison at 20% load condition.

## V. TOPOLOGY VARIATIONS

With the proposed ZVS BIT, other types of current-fed converter as a series output module are presented briefly. The proposed ZVS BIT concept can be applied to any current-fed type converters. However, to increase the device utilization and minimize the number of active and passive components, the common parts integration presented in Section II-A should be considered. Under this rule, an isolated sepic converter and a current-fed half-bridge (CFHB) converter as a series output module are proposed, as shown in Fig. 13. These converters are also suitable candidates for the high step-up applications.

The pulsating input current of the ZVS flyback-boost converter with VDR is relatively high, which can cause a high conduction loss on the switches. It is one of the main limitations, which results from the inherent characteristics of both a flyback converter and a VDR. Therefore, the use in low-to-medium power applications is recommended. If the high pulsating input current is troublesome, the isolated sepic converter shown in Fig. 13(a) can be an alternative because a boost inductor $L_b$ relieves it. The reduced current stresses on the switches can also reduce the conduction losses.

To diminish the pulsating input current further, the CFHB converter shown in Fig. 13(b) is more attractive. Its interleaving gate signals with two boost inductors, $L_1$ and $L_2$, provide the ripple cancellation between two phases. Also, the half-reduced inductor currents can reduce the conduction losses in the boost

TABLE II
CHARACTERISTICS OF THE PROPOSED CONVERTERS

| Classifications | | | Series Output Module | | |
|---|---|---|---|---|---|
| | | | Flyback Converter with VDR | Sepic Converter | CFHB Converter |
| Common Parts | | | $L_m$ and $Q_1$ | $L_b$ and $Q_1$ | $L_1$, $L_2$, $Q_1$, and $Q_2$ |
| Step-up Ratio $M(Q=\frac{L_{lkg}f_S}{R_O})$ | | | $\frac{n+1}{1-D+\frac{2n^2}{D^2}Q}$ | $\frac{nD+1}{1-D+\frac{2n^2D}{1-D}Q}$ | $\frac{n+1}{1-D}\cdot\{1-\frac{Qn^2}{(1-D)^2}\}$ |
| Approximated $M(Q=0)$ | | | $\frac{n+1}{1-D}$ | $\frac{nD+1}{1-D}$ | $\frac{n+1}{1-D}$ |
| Device Stresses | Main Switch | Voltage | $V_{CO1}=\frac{1}{1+n}V_O$ | $V_{CO1}=\frac{1}{1+nD}V_O$ | $V_{CO1}=\frac{1}{1+n}V_O$ |
| | | Current | $(\frac{n+1}{1-D}+\frac{2n}{D})I_O$ | $\frac{n+1}{1-D}I_O$ | $\frac{3n+1}{2(1-D)}I_O$ |
| | Auxiliary Switch | Voltage | $V_{CO1}=\frac{1}{1+n}V_O$ | $V_{CO1}=\frac{1}{1+nD}V_O$ | $V_{CO1}=\frac{1}{1+n}V_O$ |
| | | Current | $(\frac{n+1}{1-D}+\frac{2n}{D})I_O$ | $\frac{n+1}{1-D}I_O$ | $\frac{n+1}{2(1-D)}I_O$ |
| | Secondary Rectifier | Voltage | $V_{CO2}=\frac{n}{1+n}V_O$ | $V_{CO2}=\frac{nD}{1+nD}V_O$ | $V_{CO2}=\frac{n}{1+n}V_O$ |
| | | Current | $D_{O1}:\frac{2}{D}I_O$<br>$D_{O2}:\frac{2}{1-D}I_O$ | $\frac{2}{1-D}I_O$ | $\frac{1}{1-D}I_O$ |
| Output Voltage Ripples | $\frac{\Delta V_{CO1}}{V_O}$ | | $\frac{n}{4DR_OC_{O1}f_S}$ | $\frac{(n+D-1)(n+D)}{4nR_OC_{O1}f_S}$ | $\frac{(n-nD-2D^2+3D-1)}{8n(1-D)R_OC_{O1}f_S}$<br>$\times(n+2D-1)$ |
| | $\frac{\Delta V_{CO2}}{V_O}$ | | $\frac{(1+D)^2}{4R_OC_{O2}f_S}$ | $\frac{D(1+D)}{4R_OC_{O2}f_S}$ | $\frac{D^2}{2R_OC_{O2}f_S}$ |
| Input Current Ripple | | | $\frac{2n}{D(1-D)}I_O$ | $\frac{D(1-D)}{(1+nD)L_bf_S}V_O$ | $\frac{(D-0.5)(1-D)L_1L_2}{(1+n)(L_1+L_2)f_S}V_O$ |
| ZVS Characteristics | Main switch | | Load-dependent ZVS range (by $L_{lkg}$) | | |
| | Auxiliary switch | | Wide ZVS range | | |
| | | | (by $L_m$) | (by $L_b$) | (by $L_1$ and $L_2$) |

TABLE III
DESIGN SPECIFICATIONS AND CIRCUIT PARAMETERS

| | | |
|---|---|---|
| Input Voltage, $V_I$ | | 42V |
| Output Voltage, $V_O$ | | 400V |
| Maximum Output Current and Power, $I_{Omax}$ and $P_{Omax.}$ | | 0.625A and 250W |
| Switching Frequency, $f_S$ | | 70kHz |
| Transformer (PQ 3535) | Turns ratio $N_P : N_S$ | 18 : 63 ($n$=3.5) |
| | Magnetizing Inductor, $L_m$ | 280μH (10% load BCM condition) |
| | Leakage Inductor, $L_{lkg}$ | 10μH |
| Link Capacitor, $C_b$ | | 8.8μF/630V |
| Output Capacitors, $C_{O1}$ and $C_{O2}$ | | 100μF/400V |
| Power Switches, $Q_1$ and $Q_2$ | | FQA38N30 (38.4A/300V) $R_{DS(on)}$=65mΩ and $C_{OSS}$=670pF |
| Rectifiers, $D_{O1}$ and $D_{O2}$ | | FFPF20U40S (20A/400V) $C_j$=100pF |

inductor windings. Therefore, it can be adapted to high power applications.

A series output module can be properly selected for the desired applications by considering the input current ripple, rated power level, device stresses, number of components, step-up ratio, and so on. To increase a step-up ratio further, secondary rectifiers can be modified to a voltage-doubler rectifier as adopted in the ZVS flyback-boost converter with a VDR.

All of these converters have the common features of ZVS BIT. The output voltage is stacked as (1). Each average value of two powering currents satisfies (2) and (3). The switch voltage stresses are clamped to $V_{CO1}$. The leakage inductor alleviates the reverse recovery problem of the secondary rectifiers. A main switch has a load-dependent ZVS condition, whereas an auxiliary switch has a wide ZVS load range. Thus, the LLFM control method can be also applied to these converters.

Despite the many advantages, the integrated boost converter limits the use of the proposed converters only to applications where no isolation is required.

Table II summarizes the characteristics of these proposed converters.

## VI. EXPERIMENTAL VERIFICATION

### A. Design Example

To verify the validity of the proposed converters employing the ZVS BIT and LLFM control, a prototype of 250 W ZVS flyback-boost converter with VDR is implemented. The design specifications and circuit parameters are given in Table III.

From the input and output voltage specifications, $M$ can be calculated as $M = 9.52$. By using (14), a nominal duty ratio $D$ and a transformer turns ratio $n$ can be selected by considering the conversion efficiency, i.e., $D$ is about 0.6 and $n = 3.5$. Then, select $L_m$ that satisfies the boundary conduction mode (BCM) at a desired load condition and measure the leakage inductor, i.e., $L_m = 280\ \mu$H for a 10% load BCM and the intrinsic $L_{\rm lkg} = 1.5\ \mu$H. To extend a ZVS load range by a leakage inductor, an external inductor is added by using (20) and Fig. 7, i.e., total $L_{\rm lkg} = 10\ \mu$H to ensure ZVS above a 25% load condition. Since the increased $L_{\rm lkg}$ decreases the step-up ratio due to the damping effect of $Q$ in (12), the nominal duty ratio $D$ should be confirmed by using (12) and Fig. 6(b), i.e., $D = 0.63$. With the selected $n$ and $D$, $V_{CO1}$ and $V_{CO2}$ are designed to be about 110 V and 290 V, respectively. Thus, the switches and diodes can be selected by considering the voltage and current stresses shown in Table III. The capacitors $C_b$, $C_{O1}$, and $C_{O2}$, which satisfy the desired voltage ripple conditions, can also be selected by using (17)–(19).

To apply the LLFM control to this converter, the ZVS load boundary by a leakage inductor, $I_{O\min\_ZVS\_Lkg}$, should be defined. With the value of $L_{\rm lkg}$, $I_{O\min\_ZVS\_Lkg}$ is located around a 25% load condition derived from (25) and Fig. 7. However, since (25) does not consider the effect of parasitic capacitors of a transformer, the actual ZVS load boundary by $L_{\rm lkg}$ is higher than the theoretical value. Therefore, $I_{O\min\_ZVS\_Lkg}$ is set at a 40% load condition, which can be confirmed clearly by the experiments. Next, to define the ZVS load boundary by FM, $I_{O\max\_ZVS\_FM}$, a loss comparison between without and with the LLFM is preceded. Fig. 14 shows the results at a 20% load condition. Although the proposed LLFM control has higher conduction losses due to increased currents, much less switching losses due to ZVS turn-on can contribute the efficiency improvement. Thus, $I_{O\max\_ZVS\_FM}$ is set at a 22% load condition, resulting in $k = 4.67$ and $f_S' = 15$ kHz from (34) and

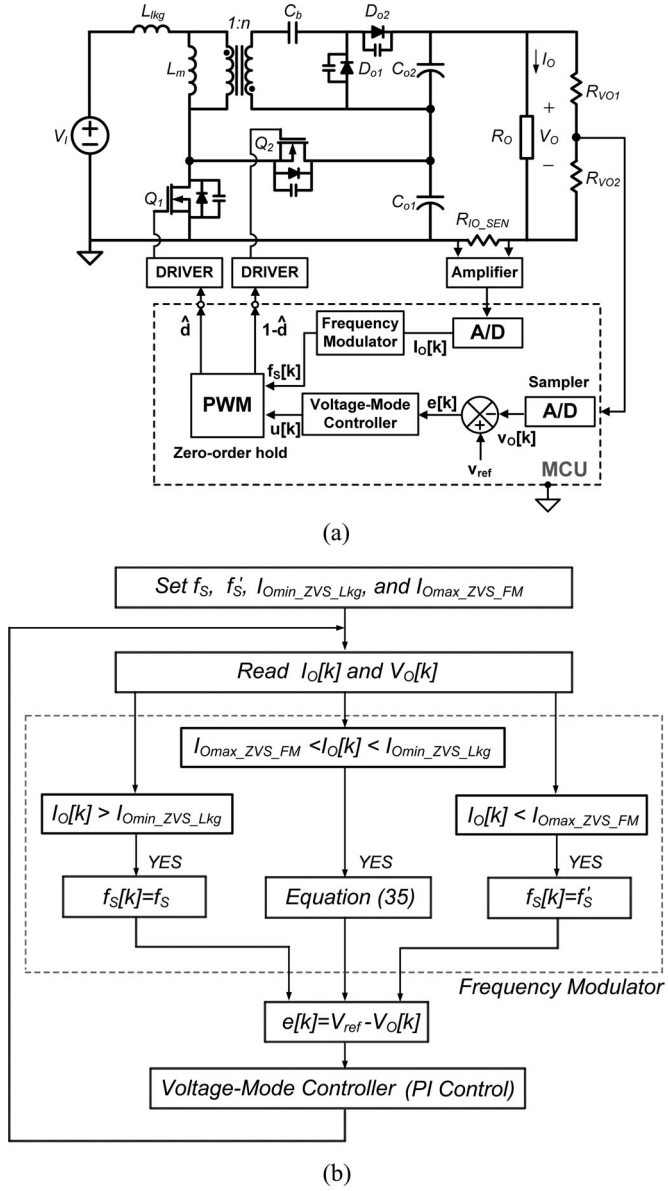



Fig. 15. Digital implementation of LLFM control: (a) Schematic. (b) Control algorism.

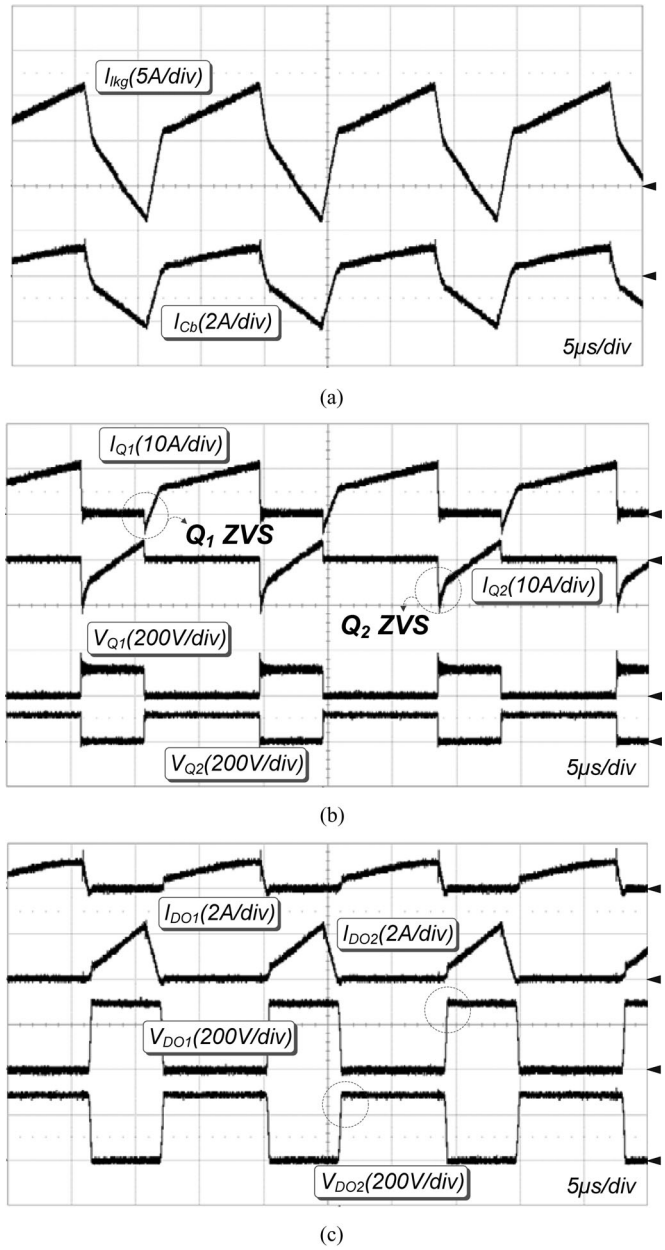



Fig. 16. Key experimental waveforms at a full load: (a) Primary leakage current and secondary link capacitor current. (b) Current and voltage waveforms of the switches. (c) Current and voltage waveforms of the output rectifiers.

Fig. 11. To accommodate an easy implementation, the linear frequency modulating region exists between 22% and 40% load conditions.

In summary, $I_{O\min\_ZVS\_Lkg} = 0.4I_{O\max}$, $I_{O\max\_ZVS\_FM} = 0.22I_{O\max}$, $k = 4.67$, and $f_S' = 15\,\text{kHz}$. Thus, all switches employed in the converter can achieve ZVS both above 40% load condition by a leakage inductor and below 22% load condition through the LLFM control. This design example mainly focuses on the verification of the ZVS recovering capability through the LLFM control. The ZVS of an entire load range can be realized by increasing either a leakage inductor or a FM ratio slightly.

### *B. Digital Implementation of LLFM Control*

The overall system has been implemented fully in software using a microcontroller unit (MCU), Texas Instrument *TMS320F28027*, as shown in Fig. 15(a). The voltage and current sensing signals, $V_O[k]$ and $I_O[k]$, have been measured with the 12-bit A/D converter. The switching frequency can be modulated with a counter unit in the MCU so that the updated frequency $f_S[k]$ is generated from the current sensing signal $I_O[k]$. This control algorism for FM is shown in Fig. 15(b). When $I_O[k]$ is higher than $I_{O\min\_ZVS\_Lkg}$, the switching frequency $f_S[k]$ becomes $f_S$. On the other hand, when $I_O[k]$ is lower than $I_{O\max\_ZVS\_FM}$, the switching frequency $f_S[k]$ becomes $f_S'$. Between these two load boundaries, the frequency modulation is performed linearly according to $I_O[k]$ as

$$f_S[k] = \frac{f_S - f_S'}{I_{O\max\_ZVS\_lkg} - I_{O\min\_ZVS\_FM}} I_O[k] + f_S'. \quad (35)$$

After finishing the FM control, the voltage-mode controller utilizing a PI-control law executes the output voltage to regulate

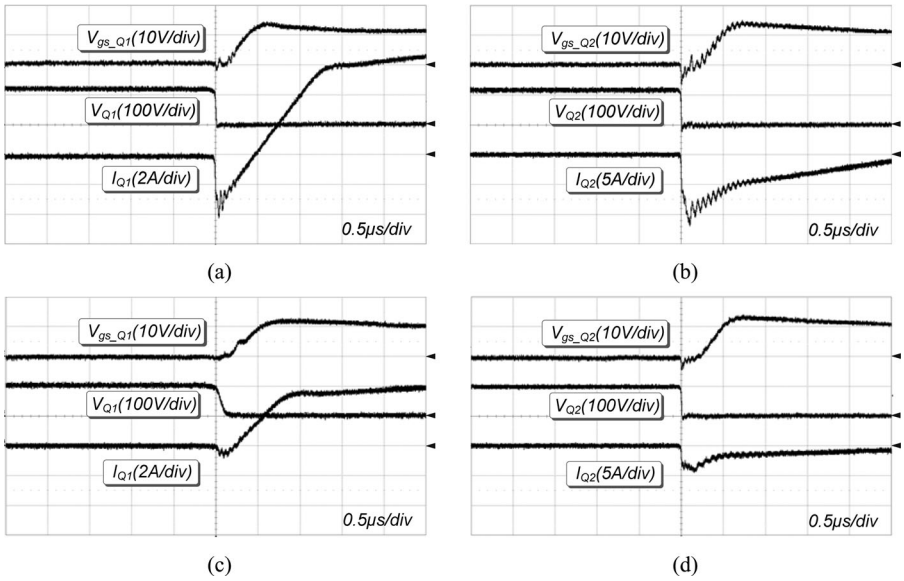



Fig. 17. ZVS waveforms of switches: (a) $Q_1$ at full load. (b) $Q_2$ at full load. (c) $Q_1$ at half load. (d) $Q_2$ at half load.

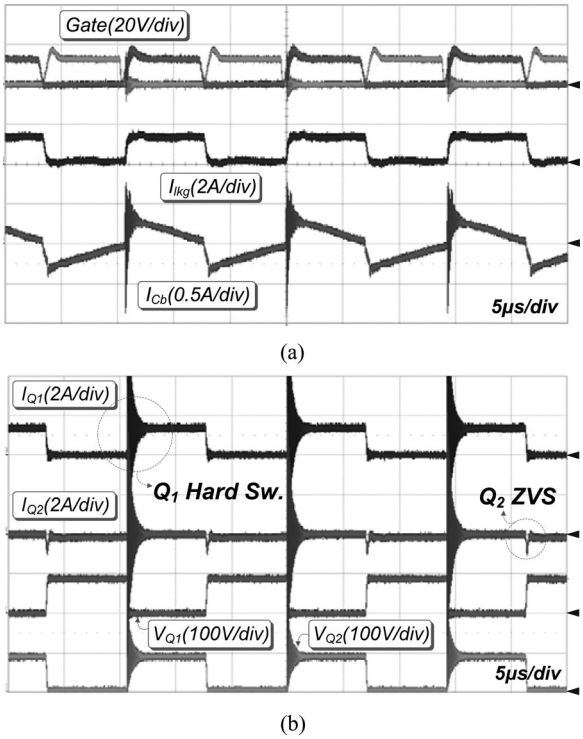



Fig. 18. Key experimental waveforms without LLFM control at a 15% load: (a) Primary leakage current and secondary link capacitor current. (b) Current and voltage waveforms of the switches.

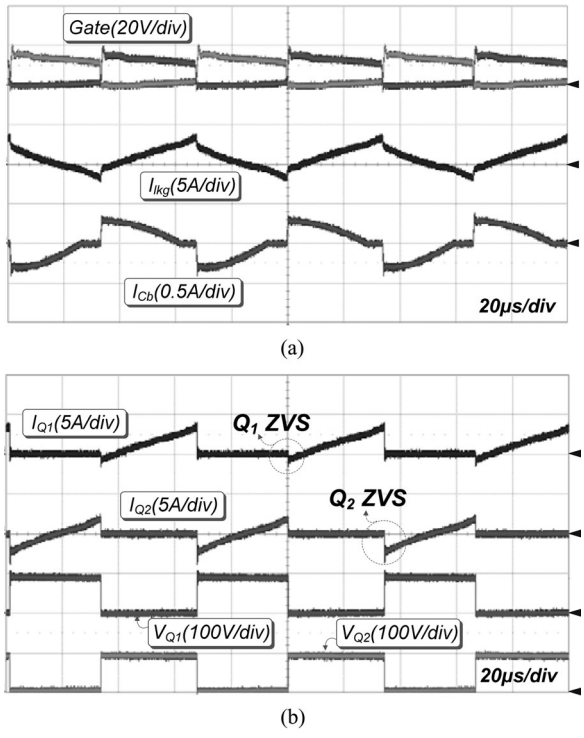



Fig. 19. Key experimental waveforms with LLFM control at a 15% load: (a) Primary leakage current and secondary link capacitor current. (b) Current and voltage waveforms of the switches.

cycle by cycle, since the sampling frequency is synchronized with the updated frequency.

### C. Experimental Results

Fig. 16 indicates the key experimental waveforms of the prototype converter at the full load condition, which are well coincided with aforementioned theoretical analysis. Fig. 16(a) shows the primary leakage current and secondary link capacitor current. Fig. 16(b) shows current and voltage waveforms of the switches. The negative currents of the switches by the aid of ZVS BIT offer ZVS of all switches. Fig. 16(c) shows the current and voltage waveforms of the output rectifiers. The alleviated $di/dt$ of $I_{DO1}(t)$ and $I_{DO2}(t)$ offers the current snubbing effect and reduces the reverse recovery problem. From Fig. 16(b) and (c), the voltages across the switches and output rectifiers are well clamped to $V_{CO1}$ and $V_{CO2}$, respectively.

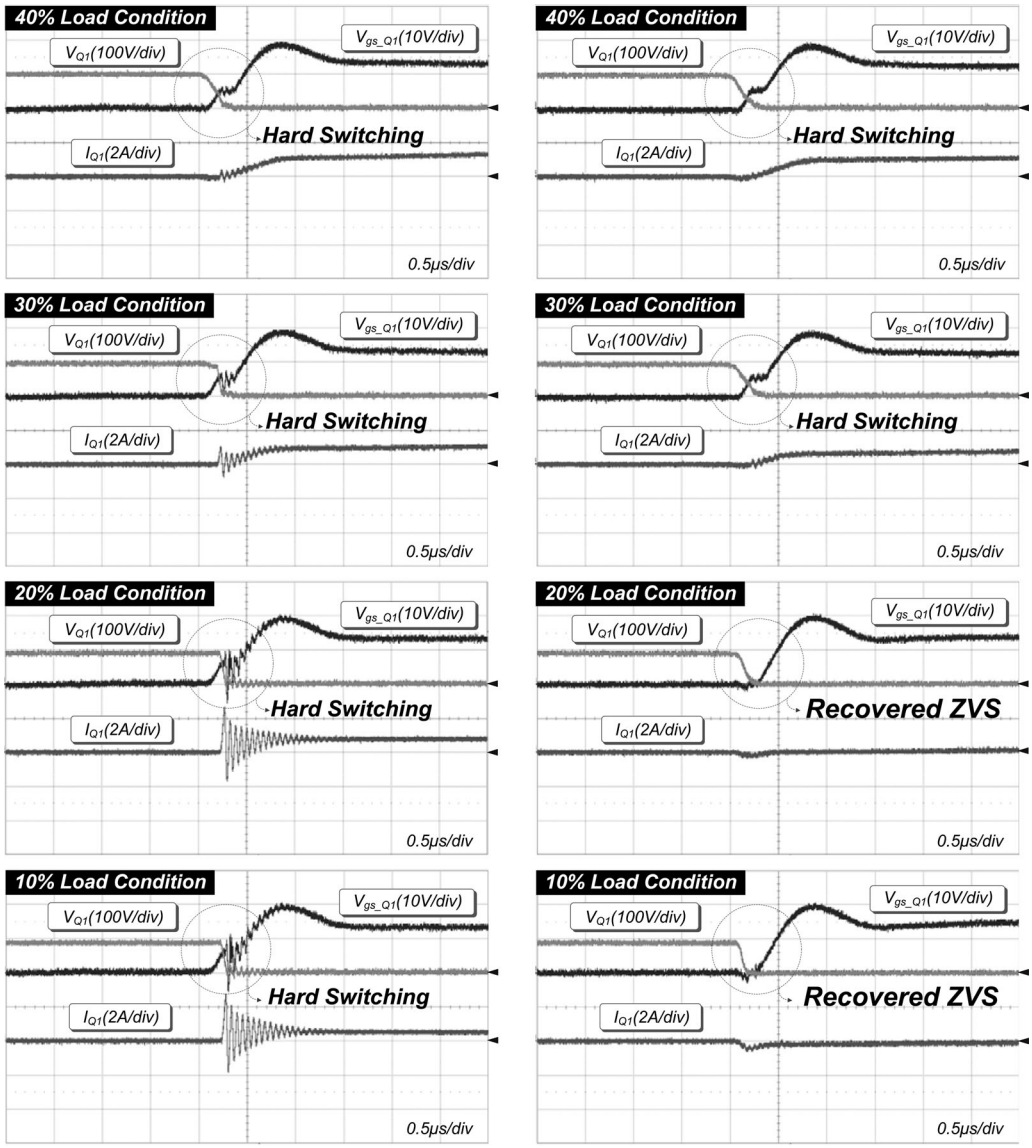



Fig. 20. ZVS waveforms of main switch $Q_1$ according to load conditions: (a) without LLFM control and (b) with LLFM control.

Fig. 17 shows that the switches $Q_1$ and $Q_2$ are turned on after $V_{Q1}$ and $V_{Q2}$ drop to 0 V, i.e., ZVS of all switches is achieved. Theoretically, with the values of the leakage inductor and junction capacitors of the switches used in the experiment, ZVS of all switches should be guaranteed approximately from 25% to 100% load conditions as noted in Fig. 7. However, in real systems, parasitic capacitors of a transformer make the ZVS range narrow so that it is guaranteed approximately from 40% to 100% load conditions.

Fig. 18 shows the key experimental waveforms of the proposed converter without LLFM control at a 15% load condition. It agrees well with Fig. 9(b) except for the distortion of the current waveforms due to the hard switching noise. It is noted that the magnitude of the abrupt build-up current $\Delta I_{\mathrm{lkg}0}$ is about 1.2 A, which is well matched with the estimated value, i.e., 1.3 A, from (28). This build-up current affects the shape of $I_{\mathrm{lkg}}(t)$ dominantly at light load condition. Furthermore, the main switch $Q_1$ suffers from the hard switching so that the considerable high-frequency switching noises are observed when it turns ON. On the contrary, the auxiliary switch $Q_2$ still maintains ZVS due to the sufficient energy stored in $L_m$.

In case of applying the LLFM control, the current waveforms are changed, as shown in Fig. 19, which are well coincided with Fig. 10. Since the modulated frequency below a 22% load condition is 15 kHz, the magnetizing current ripple $\Delta I_{Lm}$ is extended accordingly. It is worth noticing that the negative value of $I_{\mathrm{lkg}}(t)$ due to the extended $\Delta I_{Lm}$ offers ZVS of the main switch $Q_1$. Therefore, no switching noise occurs unlike Fig. 18. Furthermore, the auxiliary switch $Q_2$ also achieves ZVS.

Fig. 20 shows the ZVS waveforms at light load conditions with and without the LLFM control. Without LLFM control, ZVS of $Q_1$ is lost from a 40% load condition due to the

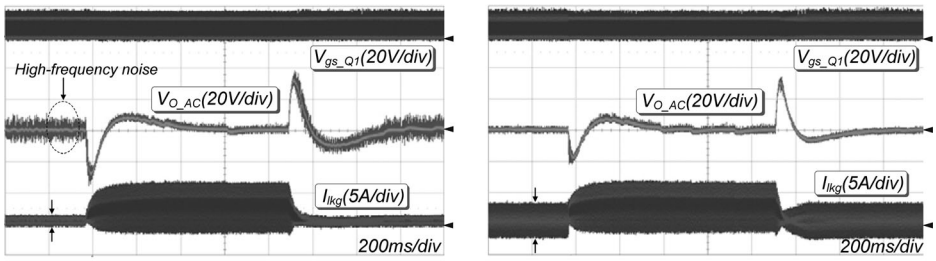



Fig. 21. Load transient response: (a) without LLFM control and (b) with LLFM control.

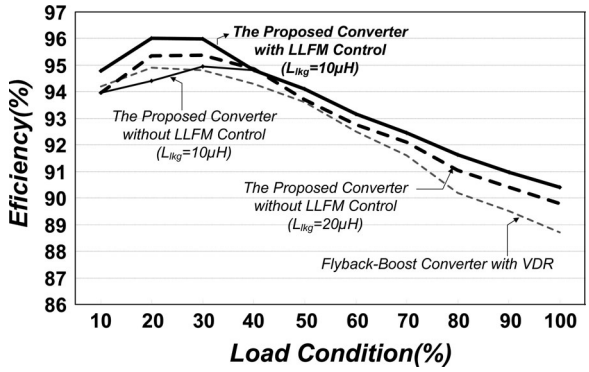



Fig. 22. Measured efficiency.

insufficient leakage energy, as shown in Fig. 20(a). However, with the LLFM control, since the ZVS load boundary by FM, $I_{O\max\_ZVS\_FM}$, is set at $0.22I_{O\max}$, the missed ZVS of $Q_1$ is recovered below a 20% load condition as shown in Fig. 20(b).

Fig. 21 shows the load transient response with and without the LLFM control. The step is changed from a 10% load to a 60% load and vice versa. Without LLFM control, only the voltage-mode control is performed while the frequency is fixed to 70 kHz regardless of the load condition. On the other hand, with the LLFM control, the frequency is modulated according to the load condition from 15 kHz to 70 kHz. From Fig. 21(a), the high-frequency noise due to the hard switching is applied to the output voltage at a 10% load condition, which can cause an EMI problem. However, the LLFM control eliminates this noise due to ZVS of all switches, as shown in Fig. 21(b). It is also noted that the LLFM control increases the magnitude of $I_{\rm lkg}(t)$ at a light load. It causes the increase in the conduction loss, but much reduced switching loss can contribute to the overall efficiency improvement as noted in Fig. 14. Moreover, provided that the crossover frequency of the voltage-mode controller is designed much less than the modulated frequency $f_S'$, the LLFM control does not affect the dynamics of the voltage-mode controller.

Fig. 22 shows the measured efficiency of the proposed converter with and without the LLFM control compared to the flyback-boost converter with a VDR. This compared converter has the same configuration as the proposed converter except that an auxiliary switch $Q_2$ is replaced by a diode. Thus, the main switch operates under hard switching condition.

The efficiency of the compared converter shows the degradation as the load current increases. It is the inherent and common characteristic of the step-up topology mainly resulting from the increased current stresses on all components. The switching losses also instigate this degradation. By eliminating the turn-on switching losses, the efficiency of the proposed converter is improved by 0.5%–1.7% above a 40% load condition, which is the ZVS load range by 10 $\mu$H of $L_{\rm lkg}$. However, the proposed converter gives no improvement at light load condition. Actually, the light-load efficiency is degraded due to the hard switching of $Q_1$ as well as larger conduction losses than the compared converter.

By increasing a leakage inductor to 20 $\mu$H to extend a ZVS range, the light-load efficiency is improved somewhat. However, the degradation at heavy load condition occurs as presented in Section III-E. By applying the LLFM control to the proposed converter with a smaller leakage inductor, i.e., 10 $\mu$H, the light-load efficiency is improved by 0.7%–1.6% without any degradation at heavy load condition. The maximum efficiency reaches above 96% at a 20% load condition. The elimination of the turn-on switching loss below a load condition of $I_{O\max\_ZVS\_FM}$ and reduction of the turn-off switching loss below a load condition of $I_{O\min\_ZVS\_Lkg}$ contribute to this improvement at light load condition.

## VII. Conclusion

Nonisolated high step-up DC-DC converters using ZVS BIT and their LLFM control are presented in this paper. The proposed ZVS BIT integrates the common parts between a bidirectional boost converter and a series output module. The simple but effective ZVS BIT gives many desirable features for high efficiency and high step-up applications. With the concept of ZVS BIT, a ZVS flyback-boost converter with VDR is derived and investigated in detail as an example. In addition, focused on the soft switching characteristics of the ZVS BIT, the LLFM control method is analyzed to extend a ZVS load range. Then a series of ZVS BIT converters employing an isolated sepic and a current-fed half-bridge converter are summarized. All these works are verified experimentally with a digitally controlled prototype converter. Although the efficiency improvement by ZVS BIT is prominent in a ZVS load range, it does not appear at light load condition. The LLFM control can compensate this degraded efficiency greatly by recovering ZVS of all switches. Therefore, the proposed ZVS BIT and LLFM control can be a promising solution for high step-up applications.

In summary, this paper summarizes the general law and structure of the ZVS BIT. Also, the LLFM control method is expected to be well suited for ZVS BIT as well as various active-clamp circuit employed converters.

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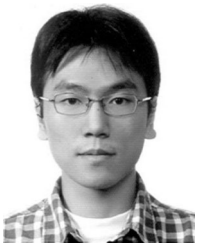

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