Improved Natural Balancing With Modified Phase-Shifted PWM for Single-Leg Five-Level Flying-Capacitor Converters

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***Abstract*—Flying-capacitor converters (FCCs), like most multilevel converter topologies, require a balancing mechanism of the capacitor voltages. FCCs feature natural voltage balancing when a special modulation technique is used. The classic methods, such as phase-shifted pulse width modulation (PS-PWM), result in very slow balancing for some duty-ratio ranges. Previous work has shown that for a single-leg five-level FCC, one time constant is infinite for a zero desired output voltage. In this paper, a modified PS-PWM scheme for a single-leg five-level FCC is presented, which results in faster balancing over the total duty-ratio range. The modified PS-PWM scheme is studied, resulting in an averaged voltage-balancing model. This model is verified using simulations and experiments. The modified PS-PWM scheme solves the slow-balancing problems of the normal PS-PWM method for odd-level FCCs, while maintaining the passive control property, and it provides a self-precharge capability.**

***Index Terms*—Capacitor voltage balancing, multilevel converters, power converters, pulse width modulation (PWM).**

I. Introduction

MULTILEVEL converters offer advantages over two-level converters. A higher voltage handling is possible due to a series connection of switch components. These topologies also allow intermediate voltage levels to be applied, which results in a better approximation of the desired output voltage with lower harmonic distortion [1]. Specifically, flying-capacitor converters (FCCs) have several advantages over other multilevel topologies, such as neutral-point-clamped (NPC) and cascaded converters [1], [2].

Most multilevel topologies require some kind of balancing of capacitor voltages in order to construct the required output voltage levels. With FCCs many redundant states are possible for the same output voltage. Thus, the capacitor voltages can be balanced directly on a small term, such as a PWM period. Other topologies, such as NPC, need a total fundamental period to balance the capacitors due to the lack of redundant switch states.

Two major types of balancing mechanisms for FCCs exist. The first mechanism is active balancing. Here, measurements are required to define the unbalance state and algorithms can determine the appropriate switch state, which creates the required output voltage and at the same time balances the capacitors [3]–[6]. Besides the measurements and additional control effort, the uneven switching loss distribution over the switches is a disadvantage. The second mechanism utilizes the natural-balancing property of FCCs. Using special pulse width modulation (PWM), i.e., phase-shifted PWM (PS-PWM), or a derivative of PS-PWM, a natural balancing of the capacitor voltages is obtained. Without any measurements or special control algorithms, the capacitor voltages balance to the required values. This natural-balancing mechanism has been analyzed in numerous papers [7]–[13], mostly using frequency-domain analysis.

Recent time-domain analysis of the dynamics of PS-PWM natural balancing [14], [15] results in time constant equations, which reveal large time constants, which means poor voltage-balancing dynamics, for some duty-ratio (D) regions. It turns out that PS-PWM does not use the redundant switch states optimally in some duty-ratio regions. The small stability margin of the voltage balancing, which is caused by the poor dynamics, results in an increased sensitivity to nonidealities (semiconductor switch voltage drops, deadtime, delays, etc.). In a practical setup, divergence of the capacitor voltage due to the nonidealities can occur for small duty ratios, as observed in [4]. To make FCCs with natural voltage balancing suitable for practical applications, the challenge is to design switching patterns (and corresponding modulation strategies) that assure convergence and fast natural voltage-balancing dynamics. As an additional requirement, the benefits of PS-PWM, the optimal voltage quality, the minimal switching losses, and the uniform loss distribution over the switches, have to be sustained.

In this paper, a new PWM scheme, which results in better balancing properties than the normal PS-PWM, will be proposed and analyzed. A five-level FCC will be used, because this is the converter with the lowest level-count and suffering infinite time constants when applying the PS-PWM. Simulations and experiments will verify the theoretical results from the time-domain analysis.

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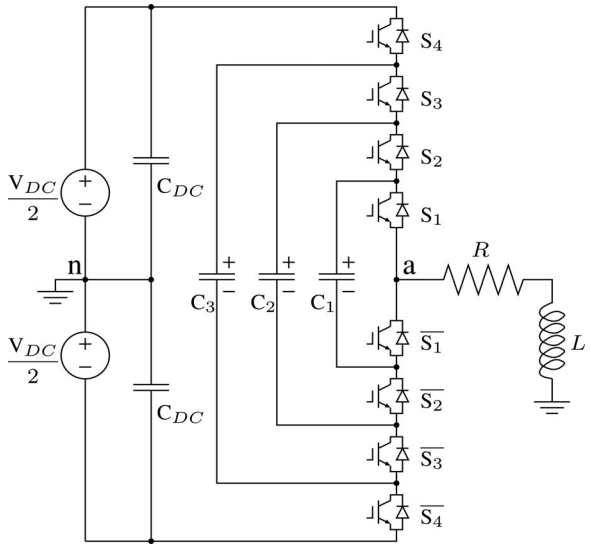

Fig. 1. Topology of a five-level single-leg FCC.

II. Five-Level Single-Leg FCC Topology and Switch States

A. Five-Level Single-Leg FCC Topology

The topology of a five-level single-leg FCC is depicted in Fig. 1. The converter has four pairs of complementary controlled switches $(S_1, \overline{S_1})$, $(S_2, \overline{S_2})$, $(S_3, \overline{S_3})$, and $(S_4, \overline{S_4})$. These switches make it possible to connect the flying capacitors in series with the load. The load is represented here as an RL series connection, to simulate a simple inductive load. The flying capacitors C_1, C_2 and C_3 should be charged to their nominal voltages $V_{\rm dc}/4$, $V_{\rm dc}/2$, and $3V_{\rm dc}/4$, respectively, to be able to construct the desired output voltages. To ensure that the voltage stress over the switches is limited and the output voltage quality is acceptable, the capacitor voltages need to remain nominal.

The switch states can be represented by four digits corresponding with the switch pairs. A normal digit means the upper switch of the switch pair is closed, while an overlined digit means the bottom switch is closed. An overview of the possible switch states and their resulting output voltage V_{an} is given in Table I.

B. Switch States and Their Circuit Topologies

Applying a certain switch state results in a temporary circuit topology. The capacitors connected in series with the load in these circuits define, together with the dc-bus voltage, the voltage over the load. At the same time, the voltages of these capacitors are altered by the load current, which flows through these capacitors for a certain time.

The six circuit topologies of a five-level FCC, which result in a zero voltage over the load, are depicted in Fig. 2. Switch states 1 ($\overline{1}2\overline{3}4$) and 2 ($12\overline{3}\overline{4}$) can be considered as the inverse of each other, as are switch states 3 and 4 and switch states 5 and 6. The same current direction in these inverse circuits has an opposite effect on the capacitor voltages.

TABLE I
Switch States and the Corresponding Output Voltages of a Five-Level Single-Leg FCC (When $V_{C1} = V_{\rm dc}/4$, $V_{C2} = V_{\rm dc}/2$ and $V_{C3} = 3V_{\rm dc}/4$)

#	switch state	V_{an}
1	$\overline{1}2\overline{3}4$	0
2	$12\overline{3}\overline{4}$	0
3	$1\overline{2}\overline{3}4$	0
4	$\overline{1}23\overline{4}$	0
5	$\overline{1}2\overline{3}4$	0
6	$1\overline{2}3\overline{4}$	0
7	$\overline{1}234$	$V_{\rm DC}/4$
8	$1\overline{2}34$	$V_{\rm DC}/4$
9	$12\overline{3}4$	$V_{\rm DC}/4$
10	$123\overline{4}$	$V_{\rm DC}/4$
11	$1\overline{2}3\overline{4}$	$-V_{\rm DC}/4$
12	$\overline{1}2\overline{3}4$	$-V_{\rm DC}/4$
13	$\overline{1}23\overline{4}$	$-V_{\rm DC}/4$
14	$\overline{1}2\overline{3}4$	$-V_{\rm DC}/4$
15	1234	$V_{\rm DC}/2$
16	$\overline{1}\overline{2}\overline{3}\overline{4}$	$-V_{\rm DC}/2$

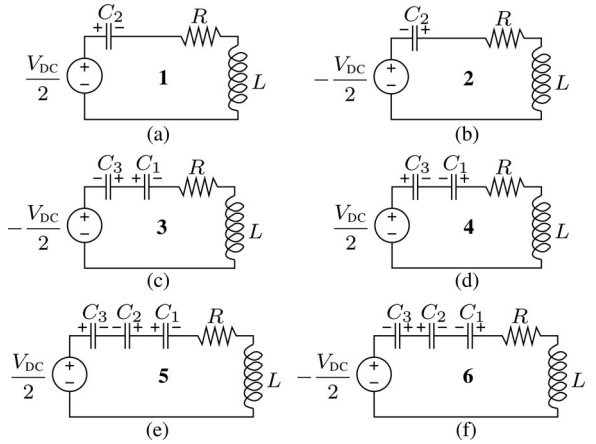

Fig. 2. Circuit topologies of a five-level single-leg FCC resulting in zero load voltage. (a) Topology 1: $\overline{1}2\overline{3}4$. (b) Topology 2: $12\overline{3}\overline{4}$. (c) Topology 3: $1\overline{2}\overline{3}4$. (d) Topology 4: $\overline{1}23\overline{4}$. (e) Topology 5: $\overline{1}2\overline{3}4$. (f) Topology 6: $1\overline{2}3\overline{4}$.

The four circuit topologies of a five-level FCC resulting in a load voltage of $V_{\rm dc}/4$ are depicted in Fig. 3. The inverse of these switch states results in a load voltage of $-V_{\rm dc}/4$ and corresponds with switch states 11–14. The two remaining possible switch states 15 and 16, which result in an output voltage of $V_{\rm dc}/2$ and $-V_{\rm dc}/2$, respectively, are created by closing all upper or bottom switches (1234 and $\overline{1}\overline{2}\overline{3}\overline{4}$). As no flying capacitors are connected in switch states 15 and 16, their voltages are not altered and they do not have any influence on the load voltage.

III. Natural Balancing With PS-PWM

The most convenient way to control the capacitor voltages of an FCC is by using a modulation strategy, which results in natural balancing. This passive control method does not need measurements and the control effort is low. To achieve natural balancing, all the switch pairs in a phase leg must be controlled

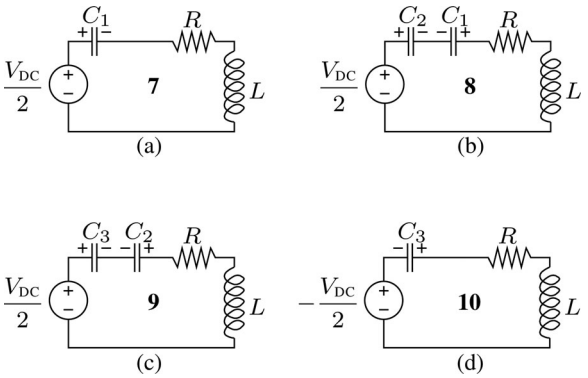

Fig. 3. Circuit topologies of a single-leg five-level FCC resulting in a load voltage of $V_{\rm dc}/4$. (a) Topology 7: $\bar{1}234$. (b) Topology 8: $1\bar{2}34$. (c) Topology 9: $12\bar{3}4$. (d) Topology 10: $123\bar{4}$.

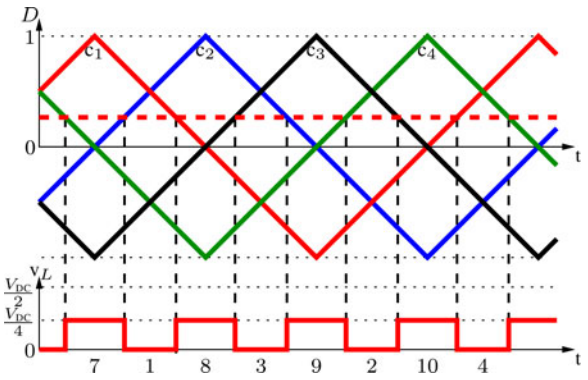

Fig. 4. Carriers of PS-PWM for a five-level FCC.

using the same duty cycle. Typically, this is implemented using the PS-PWM, depicted in Fig. 4, for a five-level converter. Each switch pair has its own triangular carrier. The carriers are phase shifted over $2\pi/(N-1)$ for an N-level converter. The normalized voltage command D (from -1 to 1), with $V_{\rm dc}/2$ as reference, is used to compare the carriers. This results in the switch state for each switch pair. When D is above the carrier, the upper switch is closed and when below the carrier, the bottom switch is closed. The order of the carriers (here c_1, c_2, c_3, c_4, lead order) can be reversed to the lag order (c_4, c_3, c_2, c_1), without influencing the balancing time constants [16].

The PS-PWM for five-level single-leg FCCs has been heavily analyzed mostly in the frequency domain [7]–[9], [11]. The time-domain analysis [14]–[16] clarified that the voltage balancing is driven by the losses caused by current harmonics, which are generated by the unbalance of the capacitors. All loss mechanisms influence the dynamics of the voltage balancing. In this study, only the ohmic loss mechanism in the load is considered, but every additional loss mechanism speeds up the balancing dynamics [17]. The time-domain analysis of the voltage balancing of the flying capacitors results in closed-form solutions of the time constants of the balancing dynamics. The obtained equations show the dependence on the system parameters (including load parameters) and D.

From the obtained time-constant equations, it is possible to characterize some problematic aspects of natural balancing. The

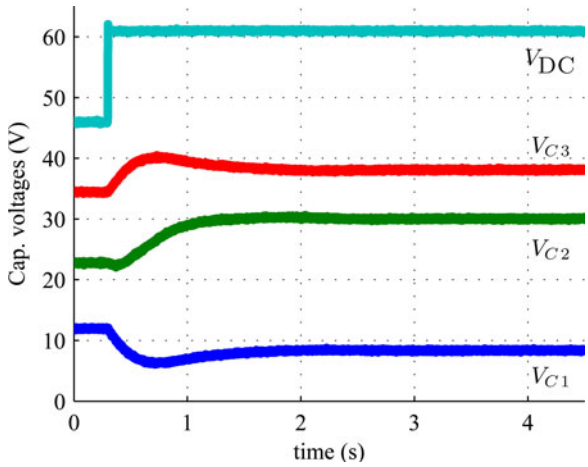

Fig. 5. Balancing with the PS-PWM for a five-level FCC at $D = 0$ (experimental measurement).

largest (and most significant) time constant, i.e., the aperiodic time constant, tends to infinity for some ranges of D. For a five-level converter, this is not only the case for ranges, where the flying capacitors are not used (D close to 1 and -1), but also for D close to zero. As an example, the balancing after a dc-bus voltage step for the PS-PWM with $D = 0$ is depicted in Fig. 5, using the experimental setup. As predicted by the theory, while capacitor C_2 balances immediately, the voltages of capacitors C_1 and C_3 do not balance to their nominal values as the common-mode time constant of both capacitors is infinite.

When the balancing time constants increase (or approach infinity), the stability margin of the system becomes very small. In simulation, this still results in (slow) balancing. In practice, the slow balancing is unable to overcome the unbalancing influences of parasitic effects, nonlinearities, and nonidealities (power switch voltage drops, deadtimes, finite rise and fall times, etc.). To overcome these effects, the balancing has to be fast enough.

The switch state sequence for $D = 0$ is 1–3–2–4 (see Fig. 4). In [16], it is shown that the cause of this infinite time constant for $D = 0$ is found in the circuit topologies 1, 2, 3, and 4. It is clear from these topologies, see Fig. 2, that capacitors C_1 and C_3 are, for $D = 0$, always used as a pair and are always connected in an antiseries way. If capacitors C_1 and C_3 both have the same voltage deviation, it is impossible to balance it out, as this unbalance has no influence on the output voltage.

Besides this practical explanation, this can also be confirmed by theoretical reasoning. The balancing dynamics can be mathematically simplified by assuming $V_{\rm dc} = 0$, ideal switches (no diodes), and charged flying capacitors. For a voltage balancing with noninfinite time constant, the charged capacitors have to balance to 0 V. This zero solution should be the single steady-state solution of the homogeneous system of linear equations, created by topologies in the sequence $1, 2, 3$, and 4. The rank of this system (the number of independent equations in the base of the system) is only 2. Because there are three variables, the three flying-capacitor voltages, the system is underdetermined and there is more than one solution. The rank of the system

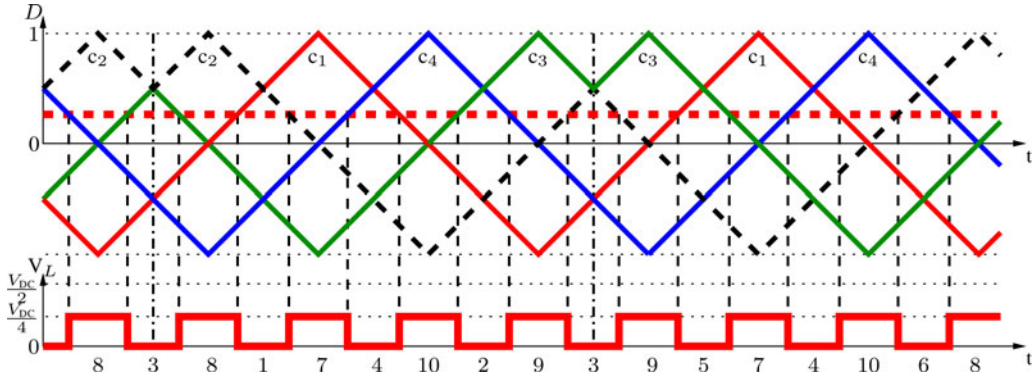

Fig. 6. Modified PS-PWM for a five-level FCC for $0 < D < 0.5$.

of linear equations created by adding topologies 5 and 6 to the original system is 3, i.e., equal to the number of variables. When all zero-voltage-generating topologies are used in the sequence, there is only one unique solution, which is the zero solution and, thus, a completely balanced system.

IV. Natural Balancing With Modified PS-PWM

After a thorough analysis of the balancing aspects of a five-level single-leg FCC, it was found that all switch states resulting in zero output voltage are necessary to guarantee a fast balancing. Other aspects that should be met are as follows.

1) Switch to the nearest levels to obtain the optimal voltage quality.
2) Consecutive switch states should differ only in the state of one switch (limit the switching losses).
3) Uniform distribution of the switching losses over the switch pairs.
4) Inverse states should be applied during equal time period.

These elements will be implemented in a new modulation scheme with improved natural-balancing dynamics.

A. Modified PS-PWM Strategy

As concluded in the previous section, the order of equations requires all six switch states to be used for $D = 0$. It seems impossible to create a sequence of six states using these six switch states with a uniform distribution of the switching losses, although this requirement can be met when using eight states in a sequence. An appropriate sequence can be constructed starting from the following scheme:

$$z - * - \overline{z} - * - z - * - \overline{z} - *.$$

In this sequence, scheme $(z, \overline{z})$ is the base pair that can be one of the zero-voltage-generating complementary switch pairs (1,2), (3,4), or (5,6). Once one base pair is chosen, the other zero-voltage-generating switch states have to be spread over the four $*$'s. The exact placement of these states influences the balancing dynamics. There are 24 (=4!) ways to place these switch states for every chosen base pair. With three possible base pairs, this results in 72 possible sequences.

A good sequence is, e.g., (for $D = 0$, with (3,4) as a base pair): 3–1–4–2–3–5–4–6. The switch-state sequences for $D \neq 0$, which include states creating the other intermediate voltages ($V_{\rm dc}/4$ and $-V_{\rm dc}/4$), must be chosen to have only one switching for every switch-state transition. The sequence for $0 < D < 0.5$, corresponding with the previously presented zero sequence, is: 3–8–1–7–4–10–2–9–3–9–5–7–4–10–6–8. For $-0.5 < D < 0$, the sequence is 3–14–1–13–4–12–2–11–3–14–5–12–4–13–6–11.

The proposed switch-state sequence can be obtained using carriers. The carrier representation of the proposed sequence example is depicted in Fig. 6 for $0 < D < 0.5$. The carrier waveforms are constructed by alternating two carrier signals after half of the PWM period. It should be noted that the PWM period is now, unlike the PS-PWM case in Fig. 4, double that of the normal triangular carrier signal. In this example, the carriers c_2 and c_3 alternate places at every dash-dotted line; this is when they meet each other on the positive D side. In the first part (states 3–8–1–7–4–10–2–9), carrier c_2 is leading carrier c_3, and at the second switch state 3, the carriers switch places, and from there on, (states 3–9–5–7–4–10–6–8) carrier c_3 leads carrier c_2.

B. Related Sequences

As stated earlier, the proposed method of creating the modified PS-PWM sequences results in 72 possible sequences. These sequences are not all unrelated, in fact, most of them are related. This means some sequences can be created by a transformation of another sequence. These related switch-state sequences can not only be constructed from each other, but their balancing dynamics are also related. Using these properties, the number of sequences that have to be investigated to find the optimum sequence can be significantly reduced.

There are three ways to relate the sequences with each other. All three ways cause the number of sequences to be divided by 2. In the end, only three sequences for every base pair remain unrelated. The three ways to relate the sequences are discussed as follows.

1) Reversing the sequences: The sequences, which have the reversed order, result in the same dynamic parameters (the same time constants and oscillation frequencies). The only difference is a sign change of the sinusoidal term in the solution, similar

to the PS-PWM [16]. Examples are 3–1–4–2–3–5–4–6 and 6–4–5–3–2–4–1–3.

2) Swap first and last part: Swapping the first four and last four states, 3–1–4–2–3–5–4–6 results in the same sequence as 3–5–4–6–3–1–4–2.

3) Mirror equivalent sequences: As can be derived from the carrier representation of Fig. 6, the sequence for $D > 0$ is significantly different from the one for $D < 0$. This means that the balancing dynamics are also different for the two cases and not symmetrical around $D = 0$, which is the case for the PS-PWM. When the carriers of Fig. 6 are mirrored over the time axis, the resulting sequence can be found by taking for every switch state the inverse of the original switch state. For the zero switch states, this means replacing state 1 by 2, 3 by 4, 5 by 6, and the other way around. The balancing dynamics of the resulting sequence is mirror equivalent with the original. The dynamics for $D > 0$ of the new sequence are equal to the dynamics for $D < 0$ of the original sequence. For the example of 3–1–4–2–3–5–4–6, the mirror equivalent sequence is 4–2–3–1–4–6–3–5. In Fig. 6, the faster balancing for $D > 0$ is caused by the identical adjacent switch states when approaching $D = 0.5$. This creates a higher current ripple and stronger damping due to the PWM copper loss.

These three ways to relate the switch-state sequences reduce the total number of possible switch-state sequences to three per base pair, making a total of nine sequences. These sequences each have their own balancing dynamics. These dynamics can be analyzed to find an optimal sequence with the fastest balancing.

C. Self-Precharge

The precharging of an FCC is an important factor. In [18], it is shown that using a ramp-controlled dc-bus voltage, while maintaining a zero average load voltage ($D = 0$) and a fast enough balancing, it is possible to apply self-precharge. This self-precharge is only applicable when the load is known, so the dc-bus voltage ramp can be adapted to the largest time constant of the balancing dynamics. For a five-level single-leg FCC, however, the normal PS-PWM is not appropriate as the time constant is infinite at the desired output voltage ($D = 0$). The modified PS-PWM scheme allows fast balancing at $D = 0$.

The model that will be developed for the capacitor voltage balancing depends on the fact that $v_{C1} < v_{C2} < v_{C3}$. If this is not the case, the clamping diodes of the switches are activated, introducing nonlinearities in the system. In the self-precharge process, the capacitor voltages all start from 0 V, meaning that due to the balancing dynamics, the clamping diodes will interact with the balancing. It can be shown, however, that the effect of the clamping diodes reduces the balancing duration [18]. In Section VI, an experimental example of self-precharge will be presented.

V. Balance Dynamics Analysis and Simulation

The voltage-balancing dynamics of a five-level single-leg FCC using PS-PWM was previously carried out in the time domain in [16]. The method for analyzing the balancing dynamics uses an averaged state-space model that is obtained by applying some assumptions. These assumptions are large enough capacitor values (to be able to neglect capacitor voltage changes during a PWM period) and an inductive load, which means that load time constant L/R is significantly larger than the PWM period. In practical terms, this means that the current ripple is low and can be considered as piecewise linear. The analysis of this averaged state-space model, where high-order terms are neglected, results in a general solution with time constants and oscillation frequencies [14]. This method is directly applicable to the proposed sequences of the modified PS-PWM. For the analysis, the deviations of the capacitor voltages from their nominal (balanced) values are used. These are defined as

$$\begin{aligned} v_{d1} &= v_{C1} - \frac{V_{\rm dc}}{4} \\ v_{d2} &= v_{C2} - \frac{V_{\rm dc}}{2} \\ v_{d3} &= v_{C3} - \frac{3V_{\rm dc}}{4} \end{aligned} \tag{1}$$

where v_{C1}, v_{C2}, and v_{C3} are the voltages of the flying capacitors C_1, C_2, and C_3, respectively. The flying capacitors are supposed to be equal in the following analysis.

All the potential candidate sequences were analyzed and only the two most promising were selected to be presented here based on balancing speed. For all sequences, the time constant equations were obtained. The maximum time constant over the total D-range was used as criterion for the selection, keeping in mind that the time constants increase to infinity for D going to 1 or -1.

A. Analysis of Two Promising Sequences

The first promising sequence is the one already introduced and has a zero-voltage-generating sequence of 3–1–4–2–3–5–4–6. The general solution for this sequence is

$$\begin{aligned} v_{d1}(t) &= \exp\left(-\frac{t}{T_P}\right)[v_{d1}(0)\cos\omega t + v_{d3}(0)\sin\omega t] \\ v_{d2}(t) &= \exp\left(-\frac{t}{T_A}\right)v_{d2}(0) \\ v_{d3}(t) &= \exp\left(-\frac{t}{T_P}\right)[v_{d3}(0)\cos\omega t - v_{d1}(0)\sin\omega t] \end{aligned} \tag{2}$$

with $v_{C1}(0)$, $v_{C2}(0)$, and $v_{C3}(0)$ being the initial capacitor voltages. It can be noted that voltage v_{d2} has no oscillating term. The time constants and the oscillation frequencies for this sequence for the whole range of D are tabulated in Table II, with the constant K_T

$$K_T = \frac{192L^2C}{RT_{\rm pwm}^2}. \tag{3}$$

The second example of a zero-voltage-generating sequence which results in fast balancing is 5–1–6–3–5–4–6–2. Also, for this sequence, it is possible to find a carrier representation as Fig. 6 but now carriers c_2 and c_4 are alternating places. The

TABLE II
PARAMETERS OF THE BALANCING DYNAMICS FOR THE SEQUENCE 3–1–4–2–3–5–4–6

D	$-1 < D < -0.5$	$-0.5 < D < 0$	$0 < D < 0.5$	$0.5 < D < 1$
$\frac{T_A}{K_T}$	$\frac{1}{(1+D)^2(1-2D)}$	$\frac{4}{5+6D}$	$\frac{4}{5+6D}$	$\frac{1}{(7+2D)(1-D)^2}$
$\frac{T_P}{K_T}$	$\frac{16}{(1+D)^2(13-32D)}$	$\frac{16}{15+6D-27D^2-16D^3}$	$\frac{16}{15+6D-27D^2+16D^3}$	$\frac{16}{(37+32D)(1-D)^2}$
Ω	$\frac{(1+D)^2 T_{\text{PWM}}}{16LC}$	$\frac{(1-2D^2) T_{\text{PWM}}}{32LC}$	$\frac{(1-2D^2) T_{\text{PWM}}}{32LC}$	$\frac{(1-D)^2 T_{\text{PWM}}}{16LC}$

general solution for this sequence is

$$
\begin{aligned}
v_{d1}(t) &= \exp\left(-\frac{t}{T_P}\right) \\
&\quad \times \left[\frac{v_{d1}(0)-v_{d2}(0)}{2}\cos\omega t - \frac{v_{d3}(0)}{2}\sin\omega t\right] \\
&\quad + \exp\left(-\frac{t}{T_A}\right)\frac{v_{d1}(0)+v_{d2}(0)}{2} \\
v_{d2}(t) &= \exp\left(-\frac{t}{T_P}\right)\left[\frac{v_{d2}(0)-v_{d1}(0)}{2}\cos\omega t + \frac{v_{d3}(0)}{2}\sin\omega t\right] \\
&\quad + \exp\left(-\frac{t}{T_A}\right)\frac{v_{d1}(0)+v_{d2}(0)}{2} \\
v_{d3}(t) &= \exp\left(-\frac{t}{T_P}\right)\left[v_{d3}(0)\cos\omega t + \frac{v_{d1}(0)-v_{d2}(0)}{2}\sin\omega t\right].
\end{aligned}
\tag{4}
$$

It can be noted that voltage v_{d3} has no overdamped (aperiodic) term. The parameters of both presented modified PS-PWM sequences and the regular PS-PWM are depicted in Fig. 7 as a function of D. In Fig. 7(a) and (b), the normalized time constants τ_A and τ_P are depicted, with as reference the minimum aperiodic time constant of PS-PWM. Fig. 7(c) shows the normalized oscillation frequency. The most significant difference between the PS-PWM and the modified PS-PWM sequences is noticeable in the aperiodic time constant. The infinite time constant for $D = 0$ has disappeared and the aperiodic balancing is faster over the full D-range. The aperiodic time constant of the first example (sequence 1) is half the one of the second example (sequence 2). The periodic time constants [see Fig. 7(b)] of the modified PS-PWM sequences are slightly asymmetric and smaller than the periodic time constant of the normal PS-PWM. In general, the periodic time constant is smaller than the aperiodic time constant. The oscillation frequencies, see Fig. 7(c), are equal for the PS-PWM and the first example of the modified PS-PWM. The oscillation frequency of the second example is larger (factor $\sqrt{2}$). These oscillation frequencies are of smaller interest in this study. They are a parameter of the step response, but have no real influence on the stability or the speed of the balancing.

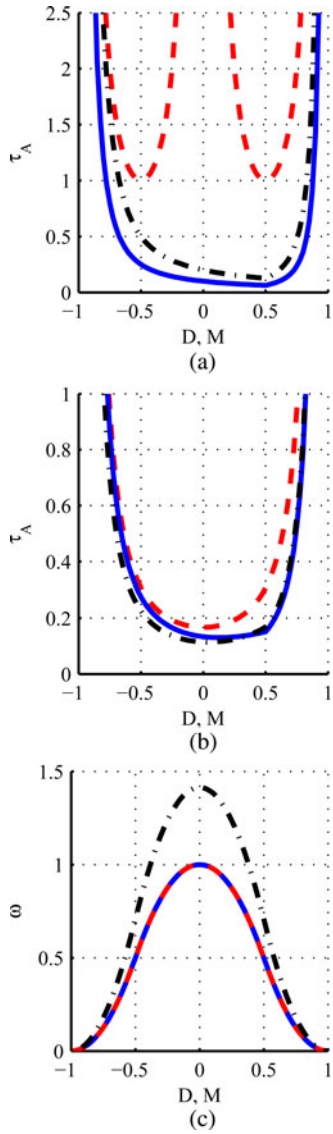

Fig. 7. Voltage-balancing dynamics parameters for PS-PWM (dashed line) and the two proposed examples of the modified PS-PWM, sequence 1 (full line) and sequence 2 (dash-dotted line). (a) Normalized aperiodic time constant. (b) Normalized periodic time constant. (c) Normalized oscillation frequency.

A sequence of the improved PS-PWM is not equally beneficial over the total D-range, especially because of the asymmetry. This can be overcome by using, in the example of sequence 1, for $D < 0$, the mirror equivalent sequence, while keeping the original sequence 1 for $D > 0$. This results in symmetric behavior. A detailed analysis of this possibility is out of the scope of this paper.

The dc parameters of Table II can be used to obtain ac parameters. Substituting $D = M\sin(\omega t)$ (M is the modulation index and ω is the fundamental frequency) in the equations and

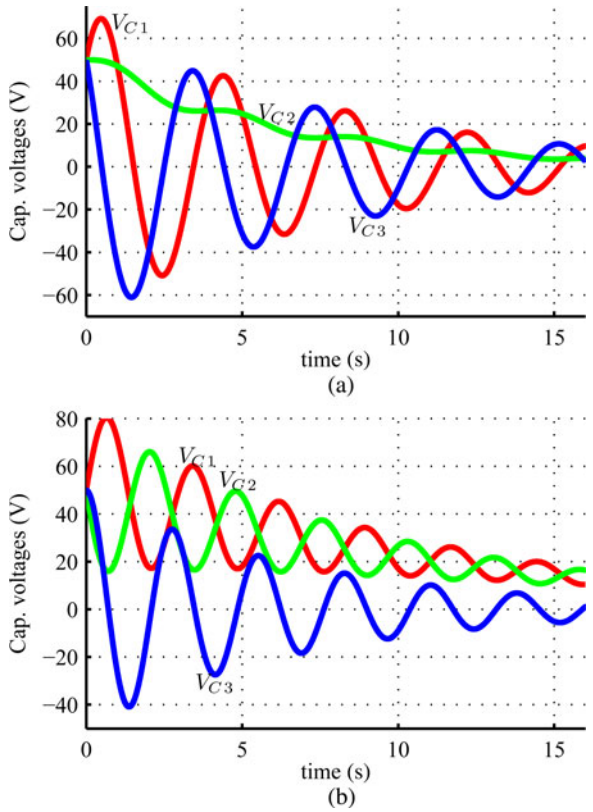

Fig. 8. Simulation of voltage balancing with initially charged capacitors, $D = 0$, and zero dc-bus voltage (ideal switches). (a) First example of modified PS-PWM, sequence 3–1–4–2–3–5–4–6, sequence 1. (b) Second example of modified PS-PWM, sequence 5–1–6–3–5–4–6–2, sequence 2.

averaging over a fundamental period results in the ac parameters, as presented in [16].

B. Simulations

To visualize the balancing terms in (2) and (4), the results of switched simulations are presented in Fig. 8. The system parameters, which are used in this simulation, are the same as those of the practical setup and will be discussed later. The capacitors are equally charged to a voltage of 50 V. With a zero dc-bus voltage, the capacitors start to balance to 0 V. This is only possible with ideal switches, without clamping diodes. The behavior in Fig. 8(a) for sequence 1 corresponds with (2) except for a small oscillating term in the capacitor voltage v_{C2}, which is not included in (2). This small periodic term is not included in the model because it is caused by higher order terms and by the nonzero R/L load parameter. The lower the value, the smaller the oscillating term in voltage v_{C2}. The simulation using sequence 2, see Fig. 8(b), corresponds perfectly with (4).

In Fig. 9, simulation results are presented of a step response in the capacitor voltages for a step in $V_{\rm dc}$ from 90 to 120 V for the classic PS-PWM (gray lines) together with the modified PS-PWM (sequence 1, black lines). For small D, capacitors C_1 and C_3 take a long time to balance for the classic PS-PWM. After the oscillations damped out, the overdamped part of the solutions takes a long time due to the large aperiodic time constant. The

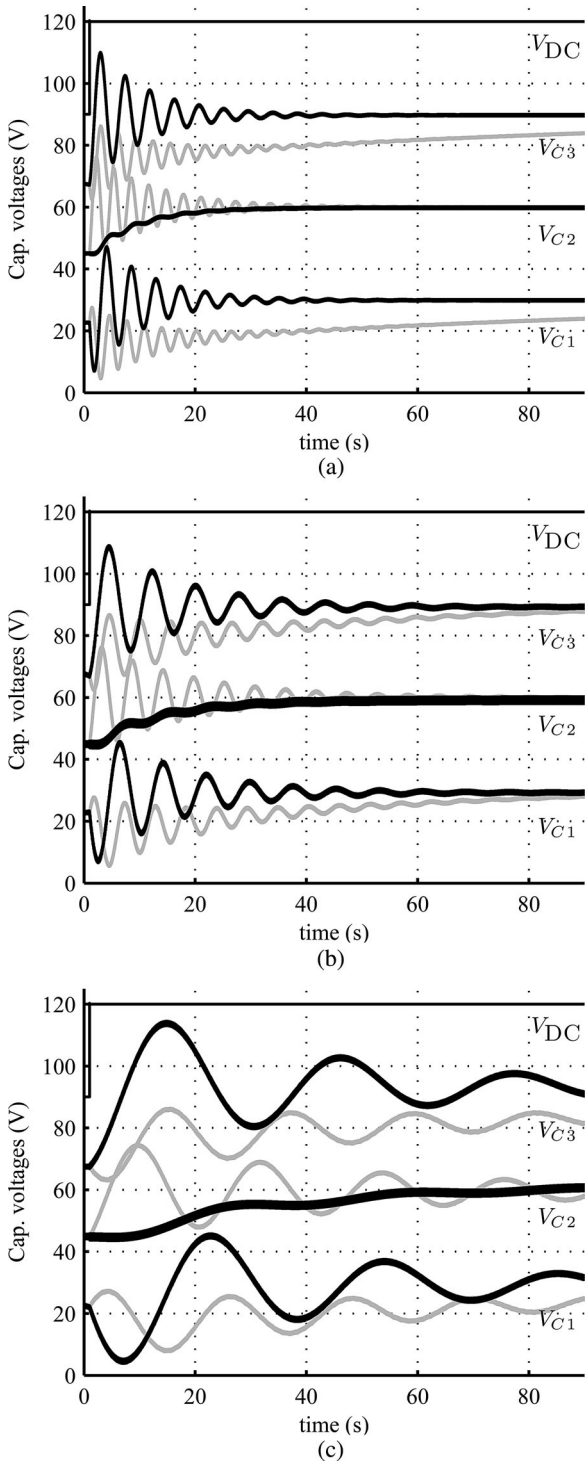

Fig. 9. Simulation of voltage balancing after a step in $V_{\rm dc}$ from 90 to 120 V. Classic PS-PWM (gray line). Modified PS-PWM (black line). (a) $D = 0.25$. (b) $D = 0.5$. (c) $D = 0.75$.

absence of an important overdamped part in the solution for the modified PS-PWM of those capacitors lets the voltages oscillate around the steady-state solution and the oscillations are damped in a short time. Using the modified PS-PWM, capacitor C_2 only has an overdamped part as expected. For high D, balancing is

TABLE III
SYSTEM PARAMETERS

Converter parameters		Load parameters	
C_1, C_2, C_3	$= 880\ \mu$F	L	$= 30$ mH
T_{PWM}	$= 1/750$ ms	R	$= 11\ \Omega$

slower for both methods, but even there the modified PS-PWM is a significant improvement.

VI. EXPERIMENTAL VERIFICATION

A. Experimental Setup

The experimental setup is a five-level flying-capacitor converter constructed from in-house, half-bridge power electronic building blocks. The system parameters of the setup are the same as those used in the simulation study and are given in Table III. The converter is controlled with an Xilinx VirtexII-Pro FPGA (XUPV2P-30), clocked at 100 MHz.

An ironless choke is used as load, connected between the output and the mid-point of the voltage supply (see Fig. 1). A simple series connection of a resistance R and an inductance L is used as a model for the load. Because of the absence of an iron core, the parameters do not depend very much on the frequency. The inductance, as well as the resistance, is only slightly influenced by the frequency and taken constant. The load parameters are found using an *LCR* meter.

B. Experimental Results

Measurements of the balancing after a step in the dc-bus voltage are depicted in Fig. 10. These measurements are carried out using the sequence 3–1–4–2–3–5–4–6 (sequence 1 in Fig. 7). In each subfigure, the graphs represent, from top to bottom: the dc-bus voltage V_{dc}, followed by the capacitor voltages v_{C3}, v_{C2}, and v_{C1}. The black lines in the graphs are calculated using the model (2).

The oscillation frequency of the balancing corresponds well with the theoretical values. Except for $D = 0$, the damping of the oscillation in the experiments is only slightly faster than in theory. This is caused by the losses in the converter, whereas in the model only load losses are included. As stated earlier, these additional losses speed up the voltage balancing. The small oscillating term in voltage v_{C2}, as found in the simulations of Fig. 8, is also noticeable in the measurements.

In the measurements, the voltage-balancing damping is significantly higher around $D = 0$ than that of the model. The reason for this was studied using simulations and measurements and is explained here. When D is small enough, the current ripple amplitude is larger than the average load current. This results in a sign change of the load current during a voltage pulse. The actual voltage pulse depends on the applied switch state and the capacitor voltages. Let us assume as an example a positive voltage pulse. This pulse will start with a negative current. The forward voltage drop over the four IGBTs or diodes in the current path is about 0.7 V, resulting in an extra voltage rise of 2.8 V for negative current. When the current changes to a positive sign, the voltage over the IGBTs or diodes results in

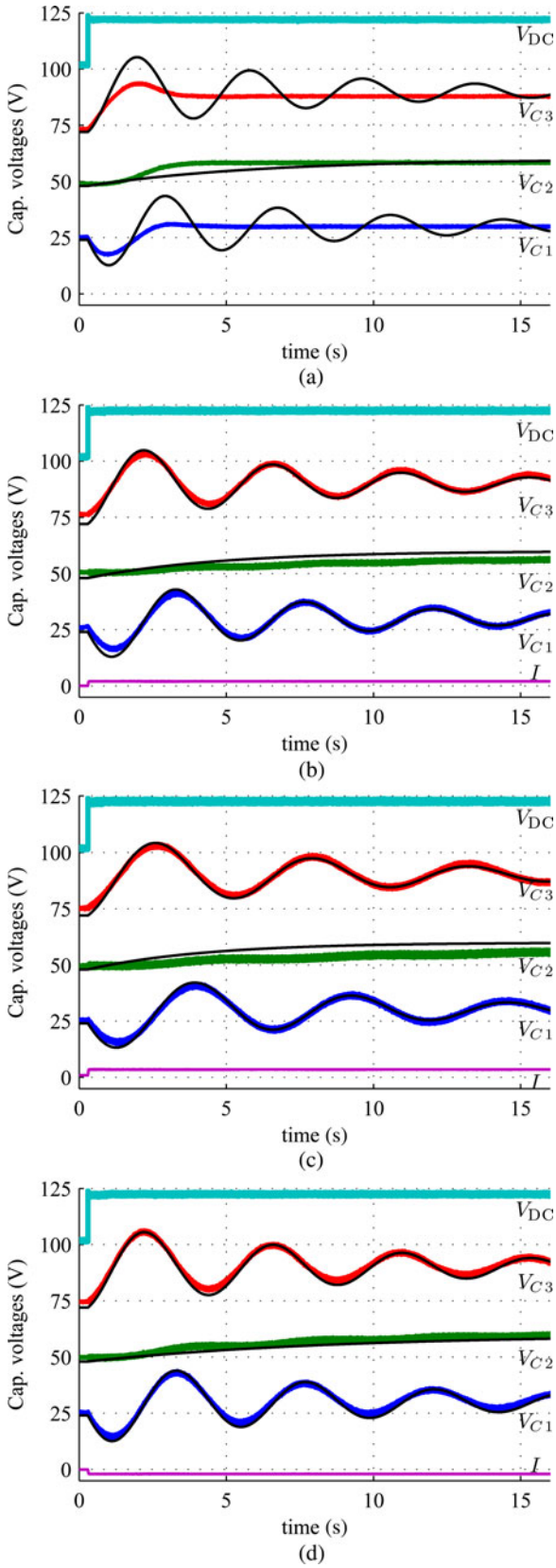

Fig. 10. Experiment of voltage balancing after step in V_{dc} from 45 to 60 V at $t = 0.3$ s for modified PS-PWM sequence, compared with the derived model (black lines). (a) $D = 0$. (b) $D = 0.25$. (c) $D = 0.375$. (d) $D = -0.25$.

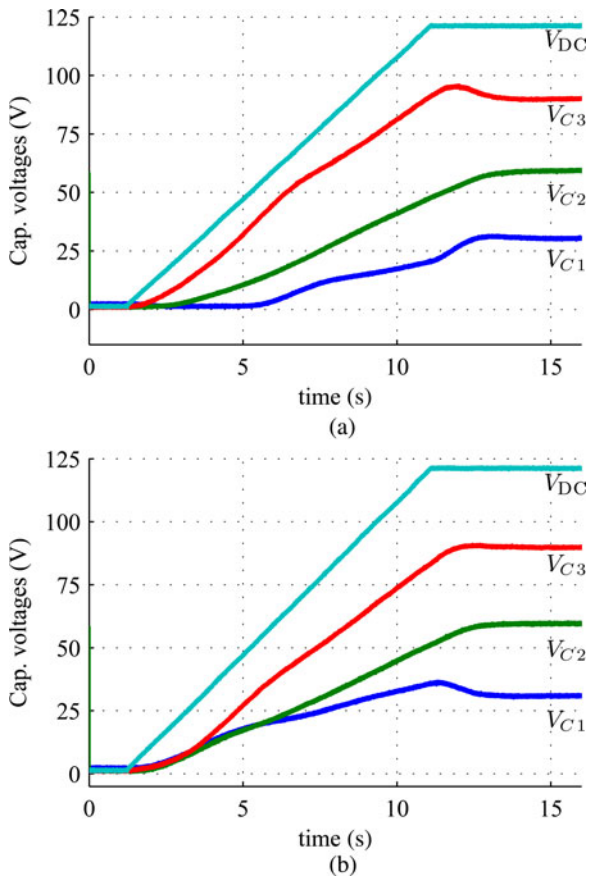

Fig. 11. Self-precharge example with a controlled dc-bus voltage rise. (a) Sequence 3–1–4–2–3–5–4–6. (b) Reversed sequence 6–4–5–3–2–4–1–3.

an extra voltage drop of 2.8 V (after a short transient). In total, an extra voltage variation of 5.6 V is created by the voltage drops over the IGBTs because of the current sign change. This extra voltage variation results in extra losses, which makes the balancing faster. The influence of this effect depends on the relative voltage variation to the total voltage. For a higher dc-bus voltage, the relative voltage variation due to the voltage drops decreases and the balancing is less influenced by the forward voltage drops of the switch components. This effect can be reproduced in simulation (using nonideal switches and diodes), but it is out of the scope of this paper to be presented in detail. The effect of the extra introduced losses is an even faster balancing around $D = 0$ than expected from our model. This means that the model is on the safe side and results in a maximum time constant.

The fast balancing of the modified PS-PWM at $D = 0$ is an important improvement over the normal PS-PWM. This property can be used for self-precharge, when the dc-bus voltage rise is controlled. When using $D = 0$ during the self-precharge process, a zero average current flows through the load. Fig. 11 shows a self-precharge example. During self-precharge, the most important factor is the voltage stress over the switches. The voltage stresses over the different switch pairs is equal to the voltage difference between the consecutive flying capacitors. This means that the distance between the lines in Fig. 11 should not exceed the voltage rating of the switches.

An example of self-precharge is depicted in Fig. 11(a), where the previously discussed sequence (i.e., 3–1–4–2–3–5–4–6) is used. Due to the nonlinearities introduced by the clamping diodes, the capacitor voltage v_{C1} stays at 0 V for some time because according to the linear model, the voltage first goes negative. By using the reversed sequence (i.e., 6–4–5–3–2–4–1–3), see Fig. 11(b), the capacitor voltages rise immediately, but stay the same for some time due to the clamping diodes. This effect change is caused by the changing sign of the sine terms in (2) when the switch state sequence is reversed. The reversed sequence results in slightly faster balancing and lower voltage stress. By slowing down the dc-bus voltage rise even more, the maximum voltage stress over the switches during self-precharge can be further reduced.

VII. Conclusion

Natural balancing of FCCs can be achieved by using the normal PS-PWM scheme. It was observed that the balancing is not guaranteed at certain regions of the duty ratio. For five-level single-leg converters, there is no balancing for $D = 0$. A new PWM scheme should enhance the voltage balancing, while maintaining the optimal voltage quality of nearest voltage level switching and an equal distribution of the switching losses over the switches.

The presented modified PS-PWM scheme results in faster balancing dynamics, with balancing over the total range of D, unlike the normal PS-PWM scheme. The modified PS-PWM scheme creates 72 possible sequences, which are all related to nine original sequences, with their own balancing dynamics. A carrier representation of the modified PS-PWM scheme is presented. The balancing dynamics of the two most promising sequences were analyzed.

The models for the two promising sequences were developed using an averaged state-space model approach. The balancing time constants are small, even for $D = 0$, but are asymmetric around $D = 0$. The experimental results show improved balancing dynamics compared with the normal PS-PWM and they also confirmed the accuracy of the obtained model parameters. A good characterization of the load is necessary to obtain correct theoretical values. The modified PS-PWM scheme allows self-precharge for a five-level converter as for $D = 0$, the time constants are not infinite.

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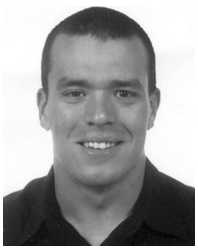

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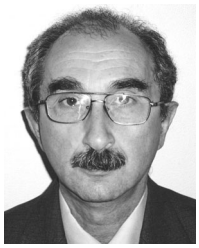

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