Improved Transformerless Inverter With Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System

Bo Yang, Wuhua Li, *Member, IEEE*, Yunjie Gu, Wenfeng Cui, and Xiangning He, *Fellow, IEEE*

***Abstract*—To eliminate the common-mode leakage current in the transformerless photovoltaic grid-connected system, an improved single-phase inverter topology is presented. The improved transformerless inverter can sustain the same low input voltage as the full-bridge inverter and guarantee to completely meet the condition of eliminating common-mode leakage current. Both the unipolar sinusoidal pulsewidth modulation (SPWM) as well as the double-frequency SPWM control strategy can be applied to implement the three-level output in the presented inverter. The high efficiency and convenient thermal design are achieved thanks to the decoupling of two additional switches connected to the dc side. Moreover, the higher frequency and lower current ripples are obtained by adopting the double-frequency SPWM, and thus the total harmonic distortion of the grid-connected current are reduced greatly. Furthermore, the influence of the phase shift between the output voltage and current, and the influence of the junction capacitances of the power switches are analyzed in detail. Finally, a 1-kW prototype has been simulated and tested to verify the theoretical analysis of this paper.**

***Index Terms*—Common-mode leakage current, junction capacitance, phase shift, photovoltaic (PV) system, sinusoidal pulsewidth modulation (SPWM) strategy, transformerless inverter.**

I. Introduction

NOWADAYS, the gird-connected photovoltaic (PV) systems, especially the low-power single-phase systems, call for high efficiency, small size, light weight, and low-cost grid-connected inverters. Most of the commercial PV inverters employ either line-frequency or high-frequency isolation transformers. However, line-frequency transformers are large and heavy, making the whole system bulky and hard to install. Topologies with high-frequency transformers commonly include several power stages, which increases the system complexity and reduces the system efficiency [1]–[6]. Consequently, the transformerless configuration for PV systems is developed to offer the advantages of high efficiency, high power density, and low cost. Unfortunately, there are some safety issues because a galvanic connection between the grid and the PV array exists in the transformerless systems. A common-mode leakage current flows through the parasitic capacitor between the PV array and the ground once a variable common-mode voltage is generated in transformerless grid-connected inverters [7]–[12]. The common-mode leakage current increases the system losses, reduces the grid-connected current quality, induces the severe conducted and radiated electromagnetic interference, and causes personal safety problems [7], [13].

To avoid the common-mode leakage current, the conventional solution employs the half-bridge inverter or the full-bridge inverter with bipolar sinusoidal pulsewidth modulation (SPWM), because no variable common-mode voltage is generated. However, the half-bridge inverter requires a high input voltage which is greater than, approximately, 700 V for 220-V_{ac} applications. As a result, either large numbers of PV modules in series are involved or a boost dc/dc converter with extremely high-voltage conversion ratio is required as the first power processing stage. The full-bridge inverter just needs half of the input voltage demanded by the half-bridge topology, which is about 350 V for 220-V_{ac} applications. But the main drawback is that the full-bridge inverter can only employ the bipolar SPWM strategy with two levels, which induces high current ripple, large filter inductor, and low system efficiency. Furthermore, the half-bridge neutral point clamp (NPC) inverter is applied to achieve three or more level output. However, NPC inverter also demands the high input voltage the half-bridge inverter does [8], [14]. Therefore, many advanced inverter topologies for transformerless PV applications were developed such as H5 inverter, HERIC inverter, etc. [17]–[25], as shown in Fig. 1. These topologies need the same low input voltage as the full-bridge inverter and can adopt the unipolar SPWM strategy with three levels. The conclusion drawn from [17]–[25] is that various solutions are being researched and employed in transformerless inverters to minimize the common-mode leakage current and improve the efficiency, weight, and size of the whole PV grid-connected power system.

In this paper, an improved grid-connected inverter topology for transformerless PV systems is presented, which can sustain the same low input voltage as the full-bridge inverter and guarantee not to generate the common-mode leakage current. Furthermore, both the unipolar SPWM and the double-frequency SPWM with three-level output can be applied in the presented inverter. The high efficiency and convenient thermal design are achieved by adopting the unipolar SPWM. Moreover, the higher

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The authors are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: yangbo@zju.edu.cn; woohualee@yahoo.com.cn; dmonkey@zju.edu.cn; cuiwenfeng@zju.edu.cn; hxn@zju.edu.cn).

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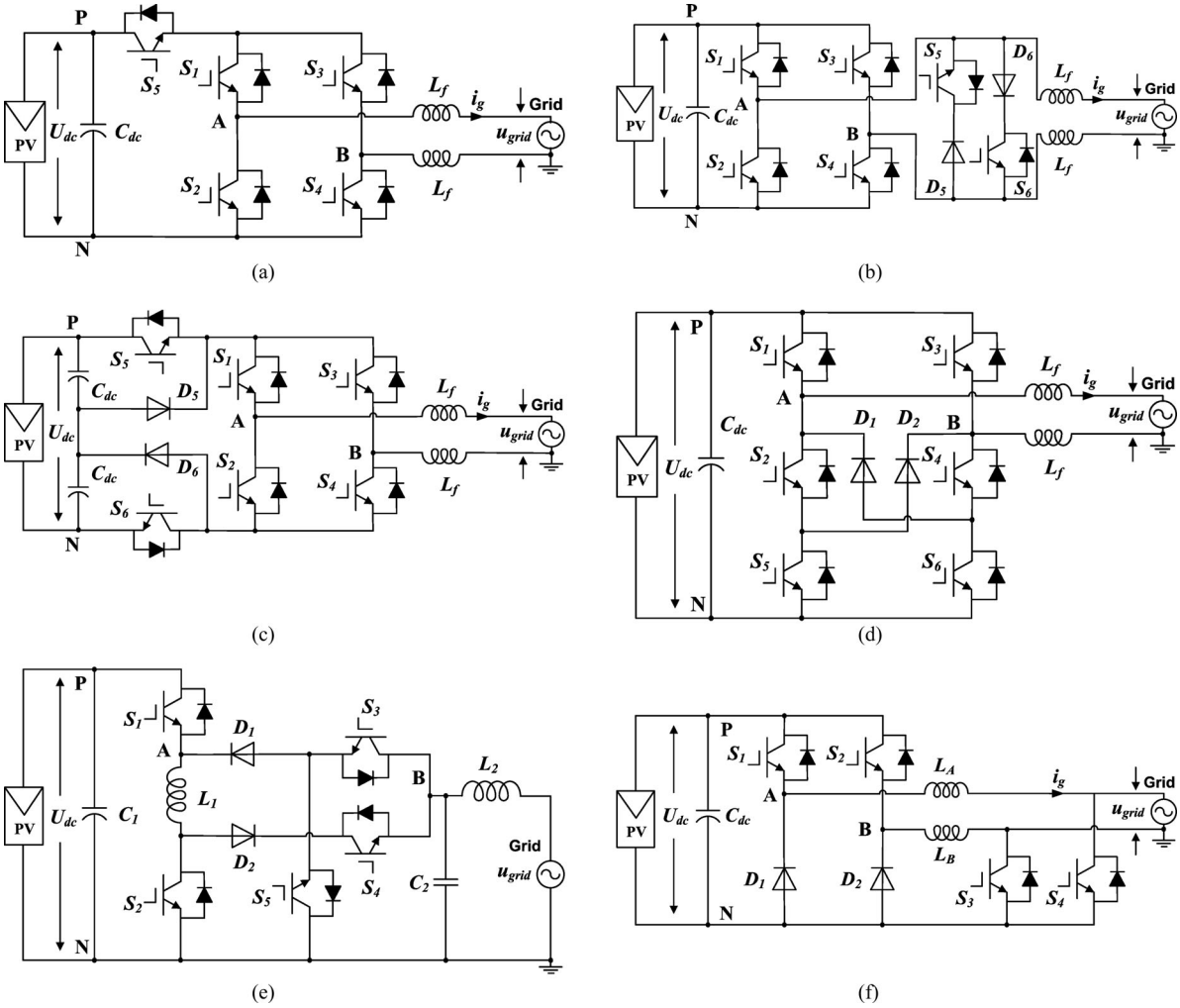

Fig. 1. Advanced inverter topologies for transformerless PV applications. (a) H5 inverter. (b) HERIC inverter. (c) Full-bridge inverter with dc bypass. (d) High-efficiency inverter with H6-type configuration. (e) Karschny inverter. (f) Inverter with two paralleled buck converters.

equivalent frequency and lower current ripples are obtained by using the double-frequency SPWM. Therefore, a smaller filter inductor can be employed and the harmonic contents and total harmonic distortion (THD) of the output current are reduced greatly, and the grid-connected power quality is improved accordingly.

This paper is organized as follows. The condition of eliminating common-mode leakage current is analyzed in Section II. The improved inverter topology and correlative operation modes under two SPWM control strategies are introduced in Section III. The influence of the power switches' junction capacitances is illustrated in Section IV. The simulated and experimental results are shown in Section V to explore the performance of the presented inverter. Section VI summarizes the conclusions drawn from the investigation.

II. Condition of Eliminating Common-Mode Leakage Current

Without an isolated transformer in the PV grid-connected power systems, there is a galvanic connection between the grid and the PV array, which may form a common-mode resonant circuit and induce the common-mode leakage current. The simplified equivalent model of the common-mode resonant circuit has been derived in [7]–[16] as shown in Fig. 2, where $C_{\rm PV}$ is the parasitic capacitor, L_A and L_B are the filter inductors, $i_{\rm cm}$ is the common-mode leakage current. And, an equivalent common-mode voltage $u_{\rm ecm}$ is defined by

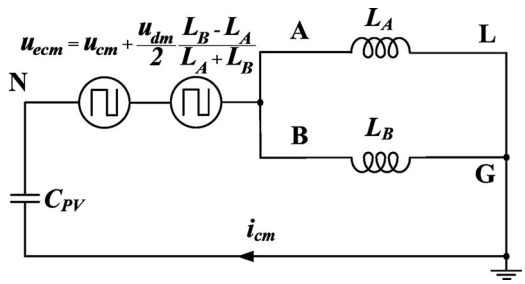

Fig. 2. Simplified equivalent model of common-mode resonant circuit.

$$u_{\rm ecm} = u_{\rm cm} + \frac{u_{\rm dm}}{2}\frac{L_B - L_A}{L_A + L_B} \tag{1}$$

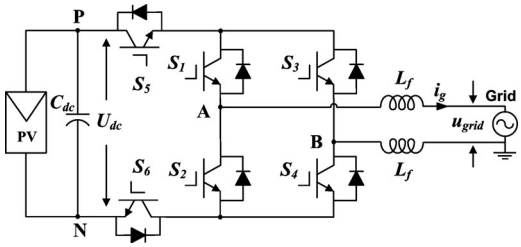

Fig. 3. Improved inverter topology.

where $u_{\rm cm}$ is the common-mode voltage, $u_{\rm dm}$ is the differential-mode voltage, $u_{\rm AN}$ and $u_{\rm BN}$ are the output voltages of the inverter relative to the negative terminal N of the dc bus as the common reference

$$u_{\rm cm} = \frac{u_{\rm AN} + u_{\rm BN}}{2} \tag{2}$$

$$u_{\rm dm} = u_{\rm AB} = u_{\rm AN} - u_{\rm BN}. \tag{3}$$

It is clear that the common-mode leakage current $i_{\rm cm}$ is excited by the defined equivalent common-mode voltage $u_{\rm ecm}$. Therefore, the condition of eliminating common-mode leakage current is drawn that the equivalent common-mode voltage $u_{\rm ecm}$ must be kept a constant as follows:

$$u_{\rm ecm} = u_{\rm cm} + \frac{u_{\rm dm}}{2}\frac{L_B - L_A}{L_A + L_B} = \frac{u_{\rm AN} + u_{\rm BN}}{2} + \frac{u_{\rm AN} - u_{\rm BN}}{2}\frac{L_B - L_A}{L_A + L_B} = \text{Constant}. \tag{4}$$

In the half-bridge inverter family, including NPC inverter, Karschny inverter, and the inverter with two paralleled buck converters as shown in Fig. 1, one of the filter inductors L_A and L_B is commonly zero. Therefore, the condition of eliminating common-mode leakage current is accordingly met that

$$u_{\rm ecm} = \frac{u_{\rm AN} + u_{\rm BN}}{2} + \frac{u_{\rm AN} - u_{\rm BN}}{2} = u_{\rm AN} = \text{Constant} \quad (L_A = 0) \tag{5}$$

$$u_{\rm ecm} = \frac{u_{\rm AN} + u_{\rm BN}}{2} - \frac{u_{\rm AN} - u_{\rm BN}}{2} = u_{\rm BN} = \text{Constant} \quad (L_B = 0). \tag{6}$$

Similarly, in the full-bridge inverter family including H5 inverter, HERIC inverter, the full-bridge inverter with dc bypass, and the high-efficiency inverter with H6-type configuration as shown in Fig. 1, the filter inductors L_A and L_B are commonly selected with the same value. As a result, the condition of eliminating common-mode leakage current is met that

$$u_{\rm ecm} = u_{\rm cm} = \frac{u_{\rm AN} + u_{\rm BN}}{2} = \text{Constant} \quad (L_A = L_B). \tag{7}$$

III. Improved Inverter Topology and Operation Modes

Fig. 3 shows the improved grid-connected inverter topology, which can meet the condition of eliminating common-mode leakage current. In this topology, two additional switches S_5 and S_6 are symmetrically added to the conventional full-bridge inverter, and the unipolar SPWM and double-frequency SPWM strategies with three-level output can be achieved.

A. Unipolar SPWM Strategy

Like the full-bridge inverter with unipolar SPWM, the improved inverter has one phase leg including S_1 and S_2 operating at the grid frequency, and another phase leg including S_3 and S_4 commutating at the switching frequency. Two additional switches S_5 and S_6 commutate alternately at the grid frequency and the switching frequency to achieve the dc-decoupling states. Accordingly, four operation modes that generate the voltage states of $+U_{\rm dc}$, 0, $-U_{\rm dc}$ are shown in Fig. 4.

Fig. 5 shows the ideal waveforms of the improved inverter with unipolar SPWM. In the positive half cycle, S_1 and S_6 are always ON. S_4 and S_5 commutate at the switching frequency with the same commutation orders. S_2 and S_3, respectively, commutate complementarily to S_1 and S_4. Accordingly, *Mode 1* and *Mode 2* continuously rotate to generate $+U_{\rm dc}$ and zero states and modulate the output voltage. Likewise, in the negative half cycle, *Mode 3* and *Mode 4* continuously rotate to generate $-U_{\rm dc}$ and zero states as a result of the symmetrical modulation.

Mode 1: when S_4 and S_5 are ON, $u_{\rm AB} = +U_{\rm dc}$ and the inductor current increases through the switches S_5, S_1, S_4, and S_6. The common-mode voltage is

$$u_{\rm cm} = \frac{1}{2}(u_{\rm AN} + u_{\rm BN}) = \frac{1}{2}(U_{\rm dc} + 0) = \frac{U_{\rm dc}}{2}. \tag{8}$$

Mode 2: when S_4 and S_5 are turned OFF, the voltage $u_{\rm AN}$ falls and $u_{\rm BN}$ rises until their values are equal, and the antiparallel diode of S_3 conducts. Therefore, $u_{\rm AB} = 0$ V and the inductor current decreases through the switch S_1 and the antiparallel diode of S_3. The common-mode voltage changes into

$$u_{\rm cm} = \frac{1}{2}(u_{\rm AN} + u_{\rm BN}) = \frac{1}{2}\left(\frac{U_{\rm dc}}{2} + \frac{U_{\rm dc}}{2}\right) = \frac{U_{\rm dc}}{2}. \tag{9}$$

Mode 3: when S_3 and S_6 are ON, $u_{\rm AB} = -U_{\rm dc}$ and the inductor current increases reversely through the switches S_5, S_3, S_2, and S_6. The common-mode voltage becomes

$$u_{\rm cm} = \frac{1}{2}(u_{\rm AN} + u_{\rm BN}) = \frac{1}{2}(0 + U_{\rm dc}) = \frac{U_{\rm dc}}{2}. \tag{10}$$

Mode 4: when S_3 and S_6 are turned OFF, the voltage $u_{\rm AN}$ rises and $u_{\rm BN}$ falls until their values are equal, and the antiparallel diode of S_4 conducts. Similar as to *Mode 2*, $u_{\rm AB} = 0$ V and the inductor current decreases through the switch S_2 and the antiparallel diode of S_4. The common-mode voltage $u_{\rm cm}$ also keeps $U_{\rm dc}/2$ referring to (9).

From (8) to (10), the common-mode voltage can remain a constant $U_{\rm dc}/2$ during the four commutation modes in the improved inverter with unipolar SPWM. The switching voltages of all commutating switches are half of the input voltage $U_{\rm dc}/2$, and thus, the switching losses are reduced compared with the full-bridge inverter. Furthermore, in a grid period, the energies of the switching losses are distributed averagely to the four switches S_3, S_4, S_5, and S_6 with high-frequency commutations, and it benefits the thermal design of printed circuit board and the life of the switching components compared with H5 inverter.

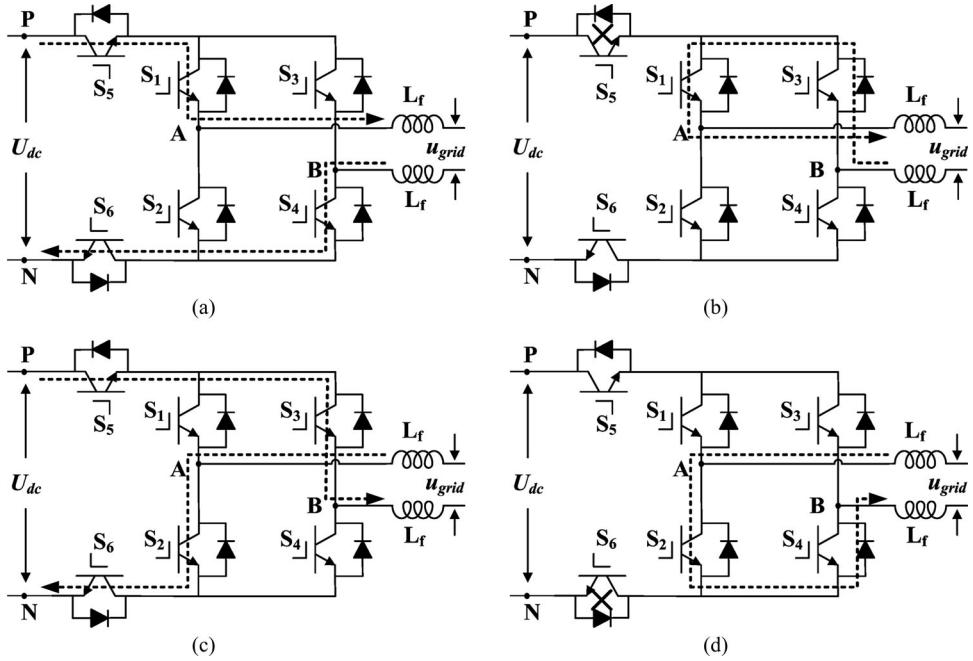

Fig. 4. Four operation modes of the improved inverter with unipolar SPWM. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

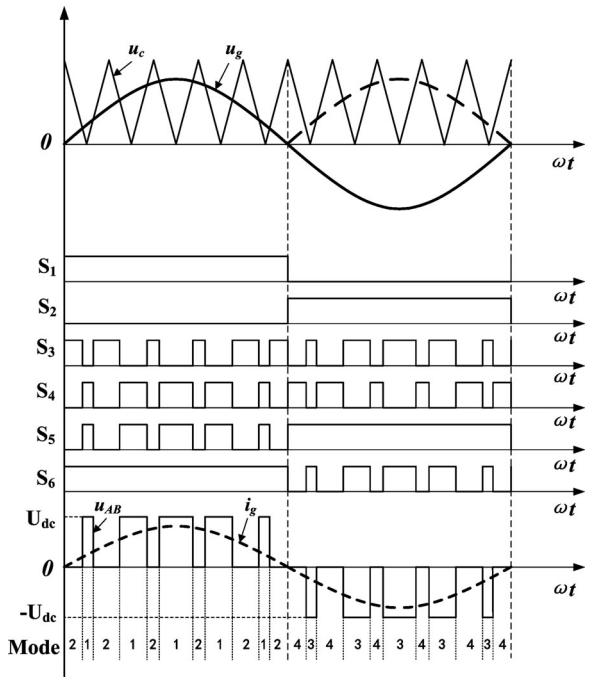

Fig. 5. Ideal waveforms of the improved inverter with unipolar SPWM.

B. Double-Frequency SPWM Strategy

The improved inverter can also operate with the double-frequency SPWM strategy to achieve a lower ripple and higher frequency of the output current. In this situation, both phase legs of the inverter are, respectively, modulated with 180° opposed reference waveforms and the switches S_1–S_4 all acting at the switching frequency. Two additional switches S_5 and S_6 also commutate at the switching frequency cooperating with the commutation orders of two phase legs. Accordingly, there are six operation modes to continuously rotate with double frequency and generate $+U_{\rm dc}$ and zero states or $-U_{\rm dc}$ and zero states, as shown in Figs. 4 and 6.

Fig. 7 shows the ideal waveforms of the improved inverter with double-frequency SPWM. In the positive half cycle, S_6 and S_1 have the same commutation orders, and S_5 and S_4 have the same orders. S_2 and S_3, respectively, commutate complementarily to S_1 and S_4. Accordingly, *Mode 1*, *Mode 2*, and *Mode 5* continuously rotate to generate $+U_{\rm dc}$ and zero states and modulate the output voltage with double frequency. In the negative half cycle, *Mode 3*, *Mode 4* and *Mode 6* continuously rotate to generate $-U_{\rm dc}$ and zero states with double frequency due to the completely symmetrical modulation.

Mode 5: when S_1 and S_6 are turned OFF, the voltage $u_{\rm AN}$ falls and $u_{\rm BN}$ rises until their values are equal, and the antiparallel diode of S_2 conducts. Therefore, $u_{\rm AB} = 0\,{\rm V}$ and the inductor current decreases through the switch S_4 and the antiparallel diode of S_2. The common-mode voltage $u_{\rm cm}$ keeps a constant $U_{\rm dc}/2$ referring to (9).

Mode 6: similarly, when S_2 and S_5 are turned OFF, the voltage $u_{\rm AN}$ rises and $u_{\rm BN}$ falls until their values are equal, and the antiparallel diode of S_1 conducts. Therefore $u_{\rm AB} = 0\,{\rm V}$ and the inductor current decreases through the switch S_3 and the antiparallel diode of S_1. The common-mode voltage $u_{\rm cm}$ still is a constant $U_{\rm dc}/2$ referring to (9).

Under the double-frequency SPWM strategy, the common-mode voltage can keep a constant $U_{\rm dc}/2$ in the whole switching process of six operation modes. Furthermore, the higher frequency and lower current ripples are achieved, and thus, the higher quality and lower THD of the grid-connected current are obtained, or a smaller filter inductor can be employed and the copper losses and core losses are reduced.

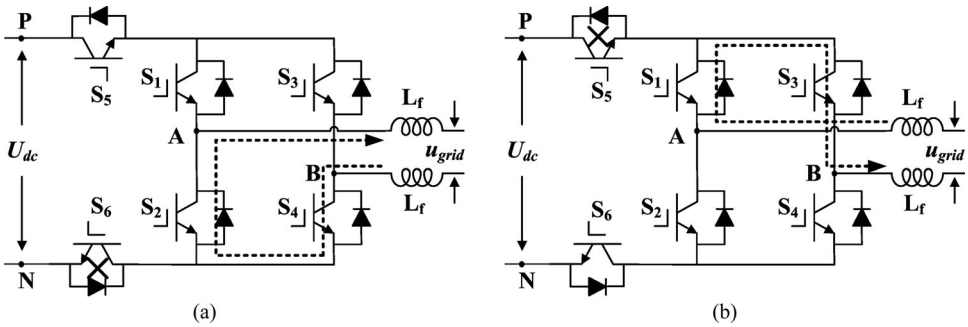

Fig. 6. Remaining two of six operation modes under double-frequency SPWM. (a) Mode 5. (b) Mode 6.

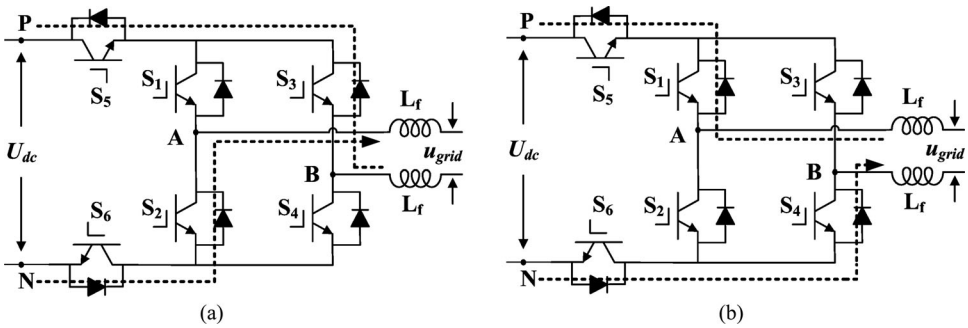

Fig. 8. Two additional operation modes when voltage and current are in different directions. (a) Mode 7. (b) Mode 8.

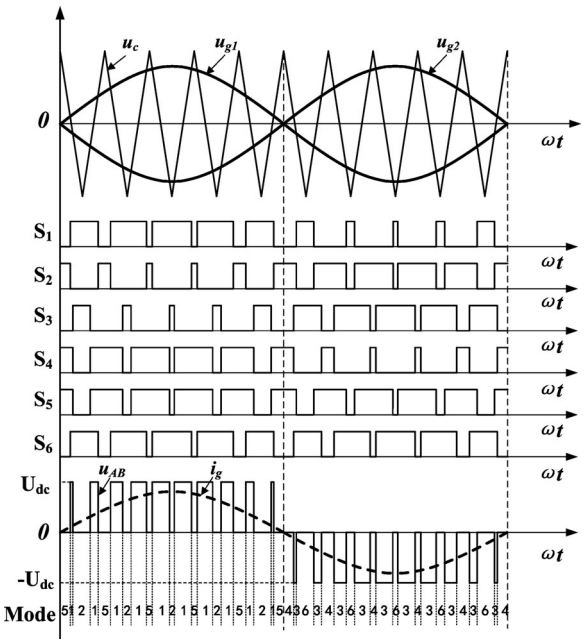

Fig. 7. Ideal waveforms of the improved inverter with double-frequency SPWM.

C. Phase Shift Between Output Voltage and Current

There is actually a phase shift between the output voltage $u_{\rm AB}$ and output current i_g in the grid-connected inverter due to the existence of the filter inductance. Two additional operation modes occur in the small regions where the output voltage and current are in different directions, as shown in Fig. 8.

Fig. 9 shows the practical waveforms of the improved inverter when considering the phase shift, where $u_{\rm AB1}$ is the fundamental component of the output voltage $u_{\rm AB}$. In *Region I* and *Region II*, the detailed operation principle and modes of the unipolar SPWM and double-frequency SPWM have been analyzed earlier, under the condition that the output voltage and current are in the same direction.

In *Region III*, the output current is positive. Meanwhile, the output voltage is negative and modulated according to the operation principle in the negative half cycle. Therefore, if the unipolar SPWM strategy is adopted, accordingly *Mode 7* and *Mode 5* continuously rotate to generate $-U_{\rm dc}$ and zero states. If the double-frequency SPWM strategy is used, *Mode 7*, *Mode 2*, and *Mode 5* continuously rotate to generate $-U_{\rm dc}$ and zero states with double frequency.

Symmetrically in *Region IV*, the output current becomes negative, and the output voltage is modulated according to the operation principle in the positive half cycle. Hereby, *Mode 8* and *Mode 6* continuously rotate to generate $+U_{\rm dc}$ and zero states when the unipolar SPWM strategy is used. *Mode 8*, *Mode 4*, and *Mode 6* continuously rotate to generate $+U_{\rm dc}$ and zero states with double frequency when the double-frequency SPWM is adopted.

With *Mode 7*, although the switches S_2, S_5, S_3, and S_6 are ON, and S_1 and S_4 are OFF, the positive inductor current only freewheels through the antiparallel diodes S_3, S_5, S_6, and S_2, and decreases rapidly for enduring the reverse voltage. The common-mode voltage $u_{\rm cm}$ keeps $U_{\rm dc}/2$ referring to (10).

With *Mode 8*, similarly, the negative inductor current only freewheels through the antiparallel diodes of S_1, S_5, S_6, and S_4, and decreases rapidly for enduring the reverse voltage.

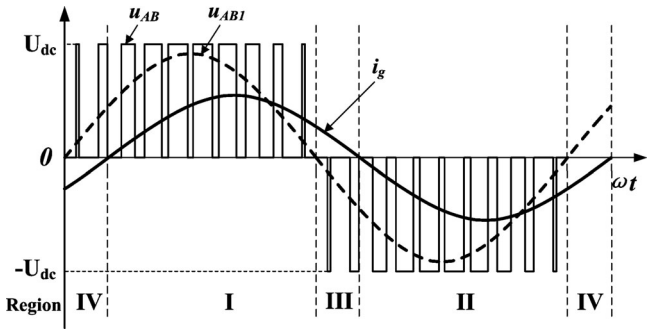

Fig. 9. Practical waveforms of the improved inverter considering phase shift.

TABLE I
SEMICONDUCTOR LOSSES ANALYSIS IN THE IMPROVED INVERTER

Conduction Losses		
MODE	**DEVICE**	**TIME**
Mode 1, Mode 3	4 Switches	DT_s
Mode 2, Mode 4 *Mode 5, Mode 6*	1 Switch 1 Anti-parallel Diode	$(1\text{-}D)T_s$
Mode 7, Mode 8	4 Anti-parallel Diodes	DT_s
Switching Losses		
REGION	**DEVICE**	**SWITCHING VOLTAGE**
Region I, Region II	2 Switches	$U_{dc}/2$
	1 Anti-parallel Diode	U_{dc}
Region III, Region IV	1 Switch	U_{dc}
	2 Anti-parallel Diodes	$U_{dc}/2$

The common-mode voltage $u_{\rm cm}$ still keeps $U_{\rm dc}/2$ referring to (8).

Therefore, it is summarized that the condition of eliminating common-mode leakage current is met completely in the whole switching process including all eight operation modes

Furthermore, in regard to the inverter losses, compared with H5 inverter and HERIC inverter, the improved inverter produces similar low switching losses and relatively high conduction losses. In *Mode 1*, *Mode 3*, *Mode 7*, and *Mode 8*, the conduction losses increase due to more devices conducting. However, this inverter achieves the double-frequency SPWM strategy, which has significant harmonic advantages and makes the current ripple further decrease to half of one with unipolar SPWM strategy. Therefore, much lower current ripple of the filter inductor conduces to the great reduction of the core losses and copper losses of the filter inductor. Table I shows the detail of the semiconductor losses analysis in the improved inverter, where $U_{\rm dc}$ is the input dc voltage, T_s is the switching period, and D is the duty ratio in a switching period.

IV. INFLUENCE OF SWITCHES' JUNCTION CAPACITANCES

The aforementioned eight operation modes can be classified into two categories based on whether the dc and ac sides of the improved inverter are decoupled.

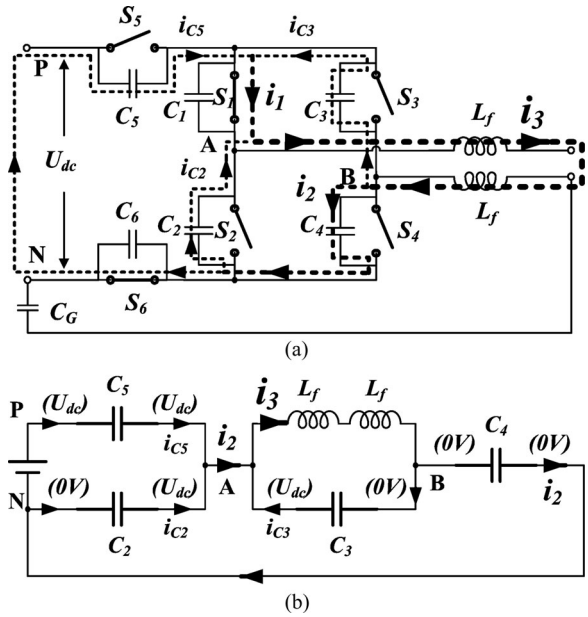

Fig. 10. Transient circuit of commutation from *Mode 1* to *Mode 2*. (a) Transient circuit. (b) Equivalent circuit.

In the nondecoupling states, *Mode 1*, *Mode 3*, *Mode 7*, and *Mode 8*, the dc and ac sides of the inverter are directly connected by the filter inductors, and the operation states and the common-mode voltage are not affected by the junction capacitances of any switches.

However, in the dc-decoupling states, *Mode 2*, *Mode 4*, *Mode 5*, and *Mode 6*, the dc and ac sides are decoupled by turning OFF the additional switch S_5 or S_6. It becomes more complicated to achieve the condition of eliminating common-mode leakage current if considering the junction capacitances of the switches. Actually, when the improved inverter commutates from one of the nondecoupling modes to one of the dc-decoupling modes, the slopes of voltage $u_{\rm AN}$ and $u_{\rm BN}$ are determined by the junction capacitances of the switches, and accordingly, the common-mode voltage $u_{\rm cm}$ is affected.

Taking the commutation from *Mode 1* to *Mode 2* as an example, there are always two stages whether the unipolar SPWM or the double-frequency SPWM strategy is adopted. Other commutations are similar due to the symmetry of the operation modes.

Stage I: Fig. 10 shows the transient circuit of the commutation from *Mode 1* to *Mode 2*, where C_1–C_6 represent the junction capacitors of the switches S_1–S_6. As shown in Fig. 10(a), when S_4 and S_5 are turned OFF and the antiparalleled diode of S_3 has not conducted to freewheel, three charging or discharging circuits are composed of the junction capacitors C_2, C_3, C_4, and C_5. According to Kirchhoff's current law, the following current equations can be given

$$i_1 = i_{C3} + i_{C5} \tag{11}$$

$$i_2 = i_{C4} = i_{C2} + i_{C5} \tag{12}$$

$$i_3 = i_{C2} + i_{C3} + i_{C5} \tag{13}$$

where i_1, i_2, and i_3 represent the currents of three charging or

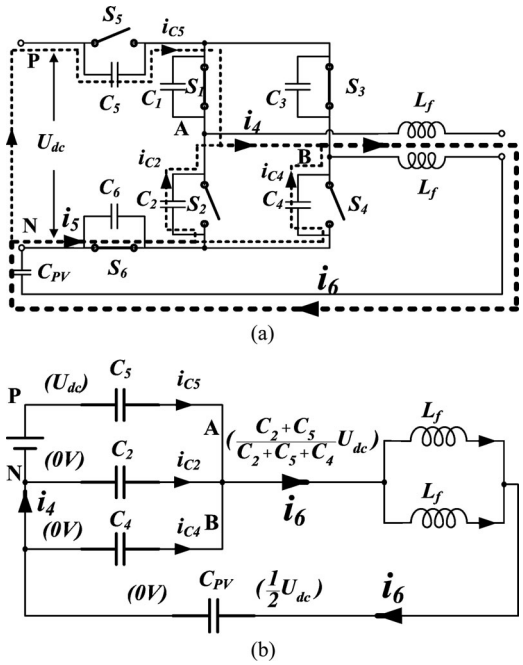

Fig. 11. Potential resonant circuit in *Mode 2*. (a) Resonant circuit. (b) Equivalent circuit.

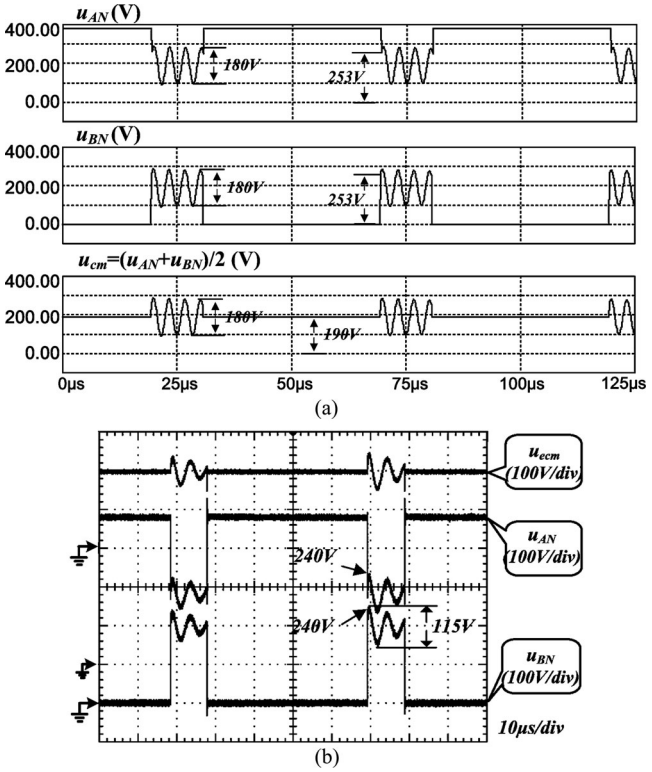

Fig. 12. Simulated and experimental results by employing the unipolar SPWM when junction capacitances of six switches are equal. (a) Simulated waveforms of $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$. (b) Experimental waveforms of $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$.

discharging circuits; i_{C2}, i_{C3}, i_{C4}, and i_{C5} are, respectively, the currents of C_2, C_3, C_4, and C_5.

From (11)–(13), the equivalent circuit model is demonstrated in Fig. 10(b), where the initial voltages in *Stage I* are indicated in the brackets. It is obvious that the junction capacitor C_4 is charged by C_2 and C_5 in parallel through the filter inductor L_f; thus, the voltage $u_{\rm AN}$ falls and $u_{\rm BN}$ rises until their values are equal. Meanwhile, the antiparalleled diode of S_3 conducts and the transient process in *Stage I* end. Based on the charge conservation, it can be found that

$$u_{\rm AN} = u_{\rm BN} = \frac{C_2 + C_5}{C_2 + C_5 + C_4} U_{\rm dc}. \tag{14}$$

Stage II: Fig. 11 shows the potential resonant circuit in *Mode 2* according to (14). If $C_4 = C_2 + C_5$, the voltages $u_{\rm AN}$ and $u_{\rm BN}$ become $U_{\rm dc}/2$ synchronously when *Stage I* ends, thus the common-mode voltage $u_{\rm cm}$ can still keep $U_{\rm dc}/2$. Therefore, the improved inverter works normally in *Mode 2*, and the condition of eliminating common-mode leakage current is met as analyzed earlier.

If $C_4 \neq C_2 + C_5$, the voltages $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$ are not equal to $U_{\rm dc}/2$ when *Stage I* ends. As shown in Fig. 11(a), on entering *Stage II*, a high-frequency common-mode current is excited in the resonant circuit that consists of the junction capacitors C_2, C_4, and C_5, the parasitic capacitor $C_{\rm PV}$ between the PV array and the ground, and the filter inductor L_f. Therefore, the voltage oscillations of $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$ are induced, and the condition of eliminating common-mode leakage current in *Mode 2* may be broken. The equivalent circuit model is demonstrated in Fig. 11(b).

In conclusion, there are four commutations from one of the nondecoupling modes to one of the dc-decoupling modes, and the following equations can be analyzed and summarized similarly to reach $u_{\rm AN} = u_{\rm BN} = U_{\rm dc}/2$ at the end of the transient process in *Stage I*, when the unipolar SPWM is adopted.

1) Commutation from Mode 1 to Mode 2: $C_4 = C_2 + C_5$.
2) Commutation from Mode 3 to Mode 4: $C_3 = C_1 + C_6$.
3) Commutation from Mode 7 to Mode 5: $C_3 = C_1 + C_6$.
4) Commutating from Mode 8 to Mode 6: $C_4 = C_2 + C_5$.

Therefore, to meet the condition of eliminating common-mode leakage current, the value principle of the junction capacitors under the unipolar SPWM is concluded that

$$C_4 = C_2 + C_5 \quad \text{and} \quad C_3 = C_1 + C_6. \tag{15}$$

Furthermore, when the double-frequency SPWM is adopted, four additional equations must be added to balance the junction capacitances of the switches.

1) Commutation from Mode 1 to Mode 2: $C_1 = C_3 + C_6$.
2) Commutation from Mode 3 to Mode 4: $C_2 = C_4 + C_5$.
3) Commutation from Mode 7 to Mode 5: $C_2 = C_4 + C_5$.
4) Commutating from Mode 8 to Mode 6: $C_1 = C_3 + C_6$.

Similarly, the value principle of the junction capacitors under the double frequnecy SPWM is concluded that $C_5 = C_6 = 0$, $C_2 = C_4$, and $C_1 = C_3$. Considering that the junction capacitance of the switch cannot be zero, the theoretic value principle is modified as next for practical applications

$$C_5 \ll C_2 = C_4 \text{ and } C_6 \ll C_1 = C_3 \tag{16}$$

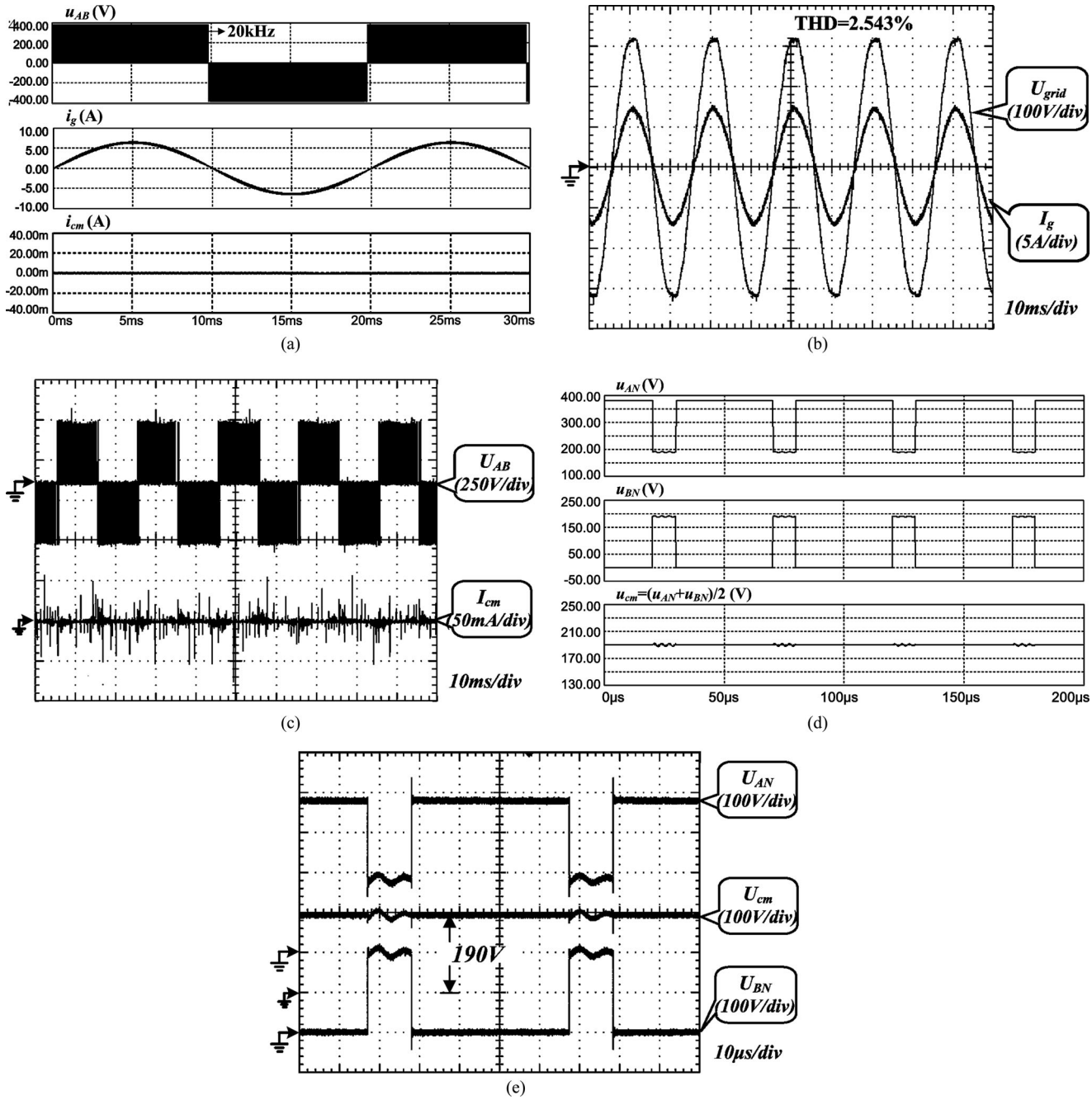

Fig. 13. Simulated and experimental results by employing the unipolar SPWM when two additional capacitors with values of 29 pF are, respectively, paralleled to S_3 and S_4. (a) Simulated waveforms of $u_{\rm AB}$, i_g, and $i_{\rm cm}$. (b) Experimental waveforms of $u_{\rm grid}$ and i_g. (c) Experimental waveforms of $u_{\rm AB}$ and $i_{\rm cm}$. (d) Simulated waveforms of $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$. (e) Experimental waveforms of $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$.

V. Simulated and Experimental Results

In order to verify the theoretical analysis in previous sections, a 1-kWp PV array is simulated, having the frame of the panels connected to ground with the parasitic capacitance of 75 nF. A 1-kW inverter prototype is also built. The detailed components and parameters used are as follows: output power, $P_{\rm out} = 1\,{\rm kW}$; input voltage, $U_{\rm dc} = 380\,{\rm V}$; input capacitor, $C_{\rm dc}$: 940 μF; grid voltage, $U_g = 220\,{\rm V_{ac}}$; grid frequency, $f_g = 50\,{\rm Hz}$; switch frequency, $f_s = 20\,{\rm kHz}$; filter inductor, $L_f = 4$ mH; parasitic capacitor, $C_{\rm PV} = 75$ nF; power switches, S_1–S_6 = IRGB4056DPbF; junction capacitors of the switches, C_1–C_6: 29 pF.

Fig. 12 shows the simulated and experimental results by employing the unipolar SPWM when the junction capacitances of six switches are equal. Since the value principle of the junction capacitors described in (15) is not reached, the relatively large oscillations of the voltages $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$ are induced. As shown in Fig. 12(a), the simulated waveforms indicate that $u_{\rm AN} = u_{\rm BN} = 253\,{\rm V}$ at the end point of the transient process from *Mode 1* to *Mode 2*, according to the theoretical analysis in (14). Subsequently $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$ begin to resonate

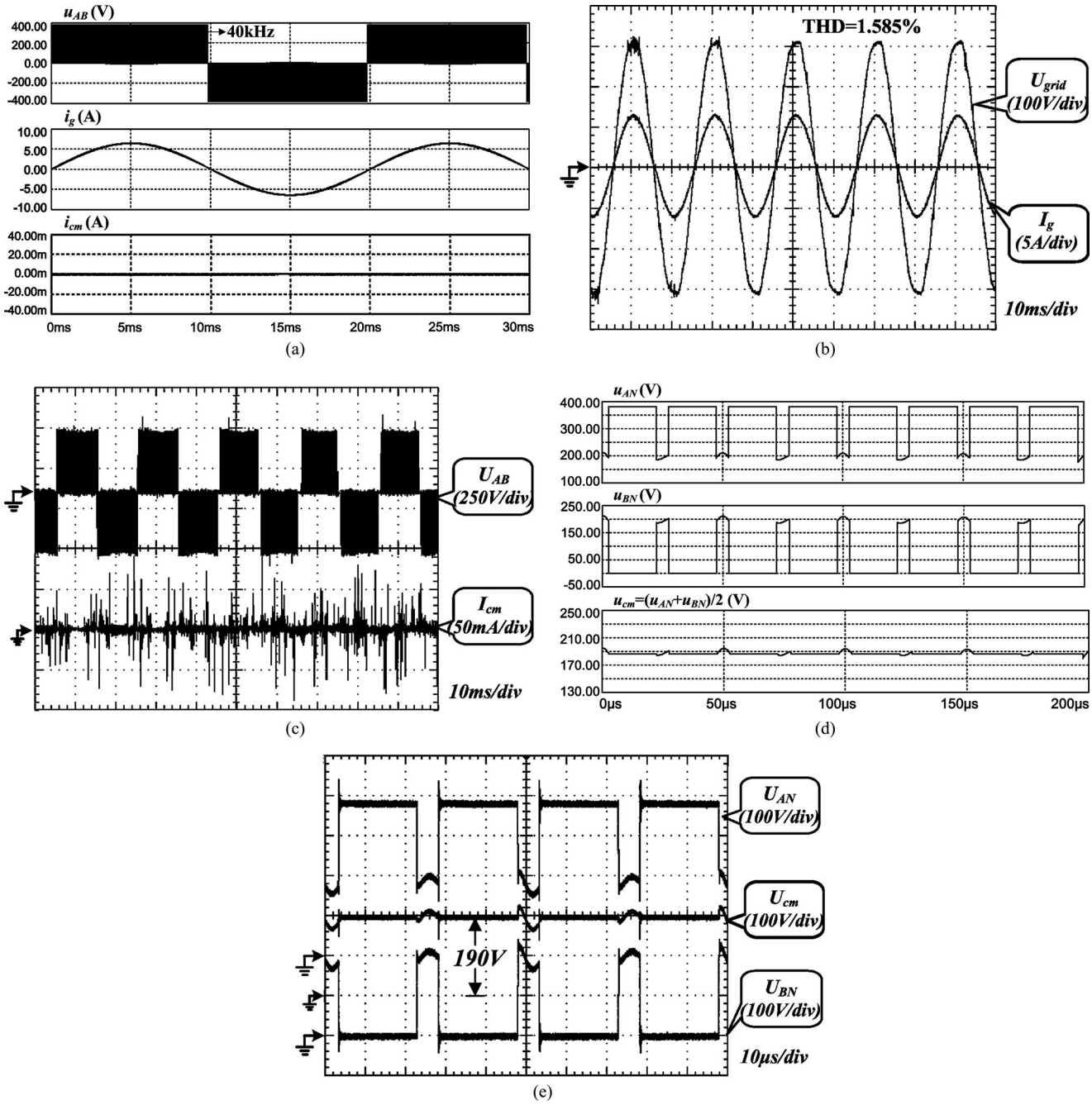

Fig. 14. Simulated and experimental results by employing double-frequency SPWM when four additional capacitors with values of 470 pF are, respectively, paralleled to S_1–S_4. (a) Simulated waveforms of $u_{\rm AB}$, i_g, and $i_{\rm cm}$. (b) Experimental waveforms of $u_{\rm grid}$ and i_g. (c) Experimental waveforms of $u_{\rm AB}$ and $i_{\rm cm}$. (d) Simulated waveforms of $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$. (e) Experimental waveforms of $u_{\rm AN}$, $u_{\rm BN}$, and $u_{\rm cm}$.

with the amplitude up to 180 V. The experimental waveforms are shown in Fig. 12(b), which is similar to the simulation, but the resonant amplitude is slightly damped due to the internal resistance of the practical inverter prototype.

Therefore, to accord with the value principle of the junction capacitors under the unipolar SPWM, two additional capacitors with the values of 29 pF are, respectively, paralleled to S_3 and S_4. Fig. 13 shows the simulated and experimental results. The simulated and experimental waveforms of the grid-connected current i_g are shown in Fig. 13(a) and (b). It is clear that the grid-connected current is highly sinusoidal synchronized with the grid voltage by achieving the three-level output. The experimental THD counted to 50th of the grid-connected current is 2.543%. Furthermore, the simulated waveforms shown in Fig. 13(a) and (d) indicate that when the common-mode voltage $u_{\rm cm}$ keeps 190 V constantly, the common-mode leakage current $i_{\rm cm}$ is almost zero since $u_{\rm AN}$ and $u_{\rm BN}$ are fully complementary in the switching periods. Accordingly, as shown in Fig. 13(c) and (e), in the experimental waveforms, even though the junction capacitances of practical switches are nonlinear and hard to

TABLE II
MEASURED EFFICIENCY OF THE IMPROVED INVERTER

Output Power		5.0% 50W	10.0% 100W	20.0% 200W	30.0% 300W	50.0% 500W	100% 1000W	Max	Euro
Unipolar SPWM	Efficiency (%)	90.6	93.1	95.1	95.9	96.5	96.5	97.1	95.9
Doubled Frequency SPWM		90.5	91.9	94.6	95.5	96.1	96.2	96.6	95.5

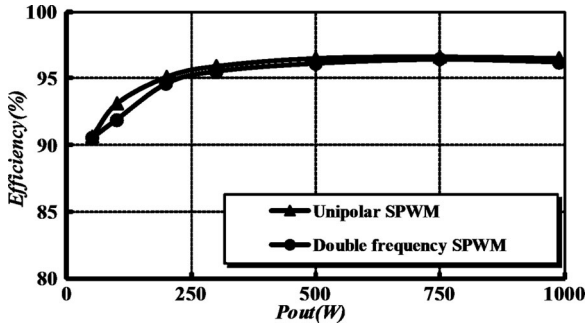

Fig. 15. Measured efficiency of the improved inverter.

be matched accurately, the common-mode leakage current $i_{\rm cm}$ is successfully limited within a very small value that is less than 50 mA for the peak value and less than 10 mA for the rms value, which complies with DIN V VDE V 0126-1-1 standard [26].

Similarly, to accord with the value principle of the junction capacitors under the double-frequency SPWM, four additional capacitors are respectively paralleled to S_1–S_4, whose values are much larger than the junction capacitances of S_5 and S_6. However, considering the increased switching losses induced by the paralleled capacitors, the value of the paralleled capacitor is decided as 470 pF as a tradeoff. Therefore, from (14), $u_{\rm AN} = u_{\rm BN} = 0.514U_{\rm dc}$ is obtained at the end point of the transient process from *Mode 1* to *Mode 2*, and thus, $u_{\rm cm}$ is maintained at $U_{\rm dc}/2$ approximately. Fig. 14 shows the simulated and experimental results. It is distinct that the equivalent frequency of the output voltage $u_{\rm AB}$ is duplicated to 40 kHz and the ripples of the grid-connected current i_g are reduced greatly thanks to the double-frequency SPWM strategy; thus, the experimental THD of the grid-connected current drops to 1.585%. Meanwhile, the common-mode leakage current $i_{\rm cm}$ is effectively limited within a safety range, although the common-mode resonance between the junction capacitors of the switches cannot be thoroughly eliminated. The peak value of the common-mode leakage current is measured less than 100 mA, and the rms value is less than 25 mA.

Fig. 15 and Table II show the detailed efficiency data of the improved inverter including the maximum efficiency and European efficiency, which are measured by the power analyzer PZ4000 from Yokogawa, respectively, when the unipolar SPWM and the double-frequency SPWM are adopted. The maximum efficiency of 97.1% and European efficiency of 95.9% are achieved under the unipolar SPWM. And the maximum efficiency and European efficiency are 96.6% and 95.5% under the double-frequency SPWM due to the slight increase of the switching losses.

VI. CONCLUSION

This paper presented an improved grid-connected inverter topology for transformerless PV systems. The unipolar SPWM and double-frequency SPWM control strategies are both implemented with three-level output in the presented inverter, which can guarantee not to generate the common-mode leakage current because the condition of eliminating common-mode leakage current is met completely. Furthermore, the switching voltages of all commutating switches are half of the input dc voltage and the switching losses are reduced greatly. The high efficiency and convenient thermal design are achieved thanks to the decoupling of two additional switches S_5 and S_6. Moreover, by adopting the double-frequency SPWM, the higher frequency and lower current ripples are achieved. Consequently, the higher quality and lower THD of the grid-connected current are obtained, or the smaller filter inductors are employed and the copper losses and core losses are reduced accordingly. Finally, a 1-kW prototype was built, and the validity and applicability of the improved inverter were confirmed by the simulated and experimental results.

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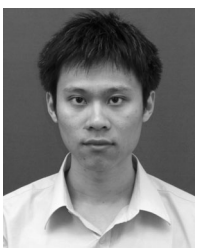

Bo Yang was born in Sichuan, China, in 1981. He received the B.Sc. and Ph.D. degrees in applied power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 2004 and 2010, respectively.

In October 2010, he joined the College of Electrical Engineering, Zhejiang University, where he is currently a Postdoctoral Fellow. His research interests include renewable power system, power converter modeling, and digital control techniques.

Wuhua Li (M'09) received the B.Sc. and Ph.D. degrees in applied power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively.

From September 2004 to March 2005, he was an Intern, and from January 2007 to June 2008, a Research Assistant in GE Global Research Center, Shanghai, China. From July 2008 to April 2010, he was a Postdoctoral Fellow at the College of Electrical Engineering, Zhejiang University. In May 2010, he became a Faculty Member at Zhejiang University as a Lecturer. In December 2010, he was promoted to Associate Professor. Since July 2010, he has been a Ryerson University Postdoctoral Fellow in the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. His research interests include high-efficiency power converters and renewable energy power conversion system.

Yunjie Gu was born in Hebei, China, in 1987. He received the B.Sc. degree in electronic engineering from Zhejiang University, Hangzhou, China, in 2010, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include photovoltaic power system, power converter modeling, and digital control techniques.

Wenfeng Cui was born in Zhejiang, China, in 1987. He received the B.Sc. degree in applied power electronics from Zhejiang University, Hangzhou, China, in 2009, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include photovoltaic power system and modeling and control of power converter.

Xiangning He (M'95–SM'96–F'10) received the B.Sc. and M.Sc. degrees from the Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 1989.

From 1985 to 1986, he was an Assistant Engineer at the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer at Zhejiang University. In 1991, he obtained a Fellowship from the Royal Society, U.K. He conducted research in the Department of Computing and Electrical Engineering, Heriot-Watt University, Edinburgh, U.K., as a Postdoctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor, where he has been a Full Professor at the College of Electrical Engineering, since 1996. He was the Director of the Power Electronics Research Institute and the Head of the Department of Applied Electronics. He is currently the Vice Dean of the College of Electrical Engineering, Zhejiang University. He is the author or coauthor of more than 200 papers and a book entitled, *Theory and Applications of Multi-level Converters*. He holds 12 patents. His research interests include power electronics and their industrial applications.

Dr. He received the 1989 Excellent Ph.D. Graduate Award, the 1995 Elite Prize Excellence Award, the 1996 Outstanding Young Staff Member Award, and the 2006 Excellent Staff Award from Zhejiang University for his teaching and research contributions. He received five Scientific and Technological Progress Awards from Zhejiang Provincial Government and the State Educational Ministry of China in 1998, 2002, and 2009, respectively, and five Excellent Paper Awards. He is a Fellow of the Institution of Engineering and Technology (formerly IEE), U.K.