Interleaved High Step-Up Converter With Winding-Cross-Coupled Inductors and Voltage Multiplier Cells

Wuhua Li, *Member, IEEE*, Yi Zhao, Jiande Wu, and Xiangning He, *Fellow, IEEE*

***Abstract*—The concept of winding-cross-coupled inductors (WCCIs) and voltage multiplier cells is integrated to derive a novel interleaved high step-up converter in this paper. The voltage gain is extended and the switch voltage stress is reduced by the WCCIs and the voltage multiplier cells in the presented circuit, which minimizes the peak current ripple of the power devices and makes low-voltage MOSFETs with high performance available in high step-up and high output voltage applications. Moreover, the output diode reverse-recovery problem is alleviated by the leakage inductance of the WCCIs, which reduces the reverse-recovery losses. Zero current switching (ZCS) turn-on is realized for the power switches to reduce the switching losses. Furthermore, the voltage spikes on the MOSFETs are clamped and the leakage energy is recycled by the voltage multiplier cells, when the switch turns off. A 1 kW prototype with 35–45 V input and 380 V output operating at 50 kHz switching frequency is built and tested to verify the significant improvements of the proposed converter.**

***Index Terms*—High step-up, interleaved boost converter, voltage multiplier cell, winding-cross-coupled inductor.**

I. Introduction

THE MASSIVE usage of the fossil fuels, such as the oil, the coal and the gas, result in global surface temperature increase and serious CO_2 gas emission, which worsens the human being's environment. On the other hand, the world's proved reserves of the oil, the coal and the natural gas could not satisfy the growing of the global energy demand. Along with the declining production of the fossil fuels, more and more researchers concentrate on exploring the renewable energy sources, such as the photovoltaic (PV) sources, the fuel cells, the wind energy and so on. Among them, PV sources are predicted to become the biggest energy candidates by year 2040 due to the clean, efficient, and environmentally friendly performance [1], [2].

The diagram of a single-phase PV grid-connected power system is shown in Fig. 1. About 380 V bus voltage is required for the 220 V ac grid by employing the full bridge inverter. A high step-up and high-efficiency dc–dc converter is necessary due to the relatively low output voltage of the PV arrays. The battery

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The authors are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: woohualee@zju.edu.cn; diabloturen@zju.edu.cn; w94@hzcnc.com; hxn@zju.edu.cn).

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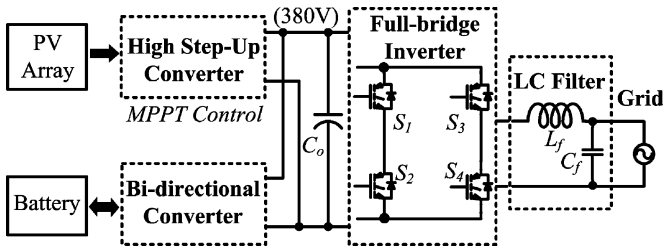

Fig. 1. Diagram of single-phase PV grid-connected power system.

sources in Fig. 1 are adopted to provide a continuous energy to the grid and to avoid the possible instability caused by the weather and temperature variation. The 48 V battery is a suitable candidate for the distributed power system due to the safety and universality concern. There are two operation modes for the converter between the battery sources and the bus voltage, which includes the charging mode and the discharging mode. During the discharging operation, high step-up and high-efficiency performance are required to improve the power density. How to extend the voltage gain, how to reduce the switch voltage stress and how to minimize the power device current ripple are the major considerations in high step-up applications.

Commonly, the conventional boost converter cannot realize such a high voltage gain even with an extreme duty cycle due to the parasitic parameters limitation [3]. The high voltage gain can be achieved by the cascade boost converter [4], but the circuit is complex and the cost is high due to the cascade structure.

A lot of single-stage high step-up and high-efficiency converters are explored by employing the coupled inductor recently [5]–[10]. The voltage gain is extended and the switch voltage stress is reduced by the transformer function of the coupled inductor. The leakage energy is recycled by the clamp circuit and the output diode reverse-recovery problem is alleviated by the leakage inductance. Unfortunately, the power level is limited and the input current ripple is large due to the single-phase operation.

The interleaved boost converters with switched-capacitors are presented in [11] and [12] for high step-up and high power applications. However, more switched-capacitor cells are required to realize an extreme high voltage gain. A family of interleaved high step-up boost converters with winding-cross-coupled inductors (WCCIs) is proposed in [13]–[15]. The second and the third windings of the WCCIs serve as the dc voltage sources and are in series to the circuit to achieve a high step-up conversion and to reduce the switch voltage stress. The active clamp scheme

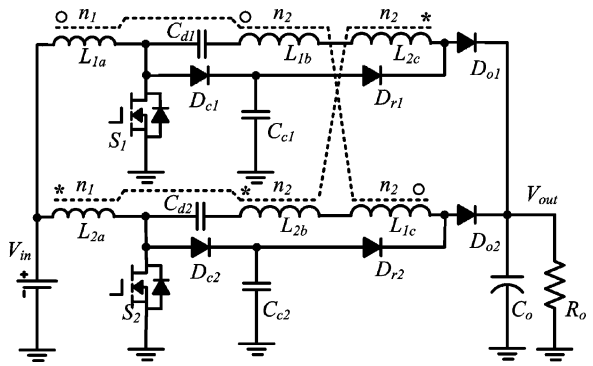

Fig. 2. Proposed interleaved high step-up converter.

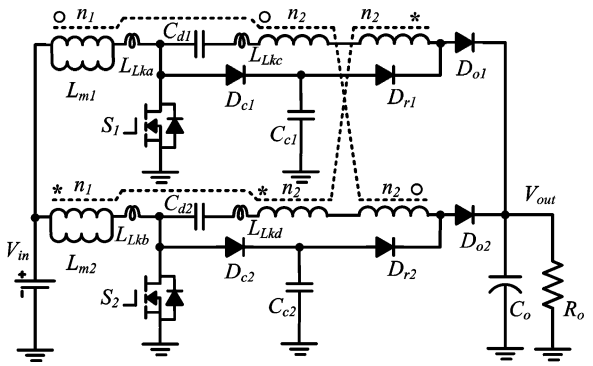

Fig. 3. Equivalent circuit of the proposed converter.

is applied to recycle the leakage energy and to suppress the voltage spikes in [14]. However, one set of active clamp circuit and an additional gate driver are necessary for each phase, which increases the circuit complexity. With some topology variations, the passive lossless clamp scheme can be derived to recycle the leakage energy and to suppress the turn-off voltage ringing on the MOSFETs [15].

A novel interleaved high step-up converter integrated with WCCIs and voltage multiplier cells is proposed in this paper. The voltage gain is extended and the switch voltage stress is reduced by the WCCIs and the voltage multiplier cells. ZCS turn-on soft switching performance is realized and the output diode reverse-recovery problem is alleviated by the leakage inductance of the WCCIs. The leakage energy is recovered and the turn-off voltage spikes are absorbed by the voltage multiplier cells. Furthermore, the voltage multiplier cells are inserted into the power branch to reduce the conduction losses and to extend the voltage gain compared with the circuit introduced in [15]. Experimental results of a 1 kW 35–45 V input and 380 V output prototype operating at 50 kHz switching frequency verify the significant improvements of the proposed converter.

II. Proposed Converter and Operational Principle

The proposed interleaved high step-up converter is shown in Fig. 2. There are two coupled inductors in the circuit. Each coupled inductor has three windings and the third winding of the coupled inductor is inserted into another phase, which is named as WCCIs [13]. The second winding with n_2 turns couples to the inductor in its phase with n_1 turns (L_{1b} versus L_{1a} and L_{2b} versus L_{2a}) and the third winding with n_2 turns couples to the inductors in another phase (L_{1c} versus L_{1a} and L_{1b}, L_{2c} versus L_{2a} and L_{2b}). The coupling reference of the WCCIs are marked by "$\circ$" and "$*$" as shown in Fig. 2. Each phase has one set of voltage multiplier cell [12], which is composed of a clamp diode D_{c1} (D_{c2}), a clamp capacitor C_{c1} (C_{c2}), a regenerative diode D_{r1} (D_{r2}) and a series capacitor C_{d1} (C_{d2}).

The WCCI can be modeled as the combination of a magnetizing inductor, an ideal transformer with corresponding turns ratio and the leakage inductances in each winding. The equivalent circuit of the proposed converter is shown in Fig. 3, where L_{m1}, L_{m2} are the magnetizing inductors; $L_{\mathrm{Lk}a}$, $L_{\mathrm{Lk}b}$ are the leakage inductances in the primary winding of each WCCI; $L_{\mathrm{Lk}c}$ is the summation leakage inductances of the second winding of WCCI 1 and the third winding of WCCI 2; $L_{\mathrm{Lk}d}$ is the summation leakage inductances of the second winding of WCCI 2 and the third winding of WCCI 1; D_{c1} and D_{c2} are the clamp diodes; C_{c1} and C_{c2} are the clamp capacitors; D_{r1} and D_{r2} are the regenerative diodes; C_{d1} and C_{d2} are the series capacitors; S_1 and S_2 are the power switches; D_{o1} and D_{o2} are the output diodes; C_o is the output capacitor. V_{in} and V_{out} are the input and output voltages. N is defined as the turns ratio n_2/n_1.

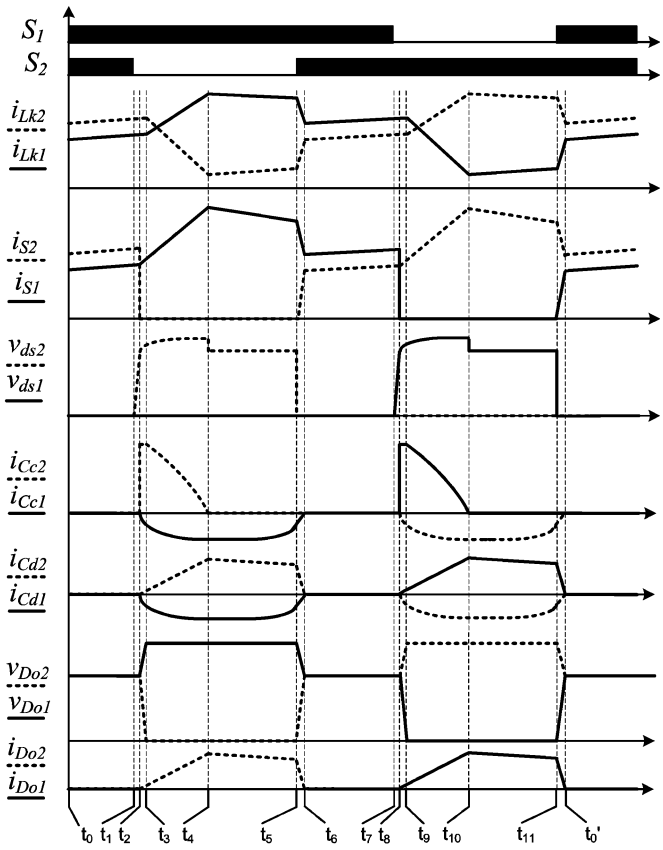

Fig. 4. Key waveforms of the proposed converter.

The key steady-state waveforms of the proposed converter are shown in Fig. 4. There are 12 stages in one switching period. Due to the symmetry of the circuit, only six stages are analyzed here

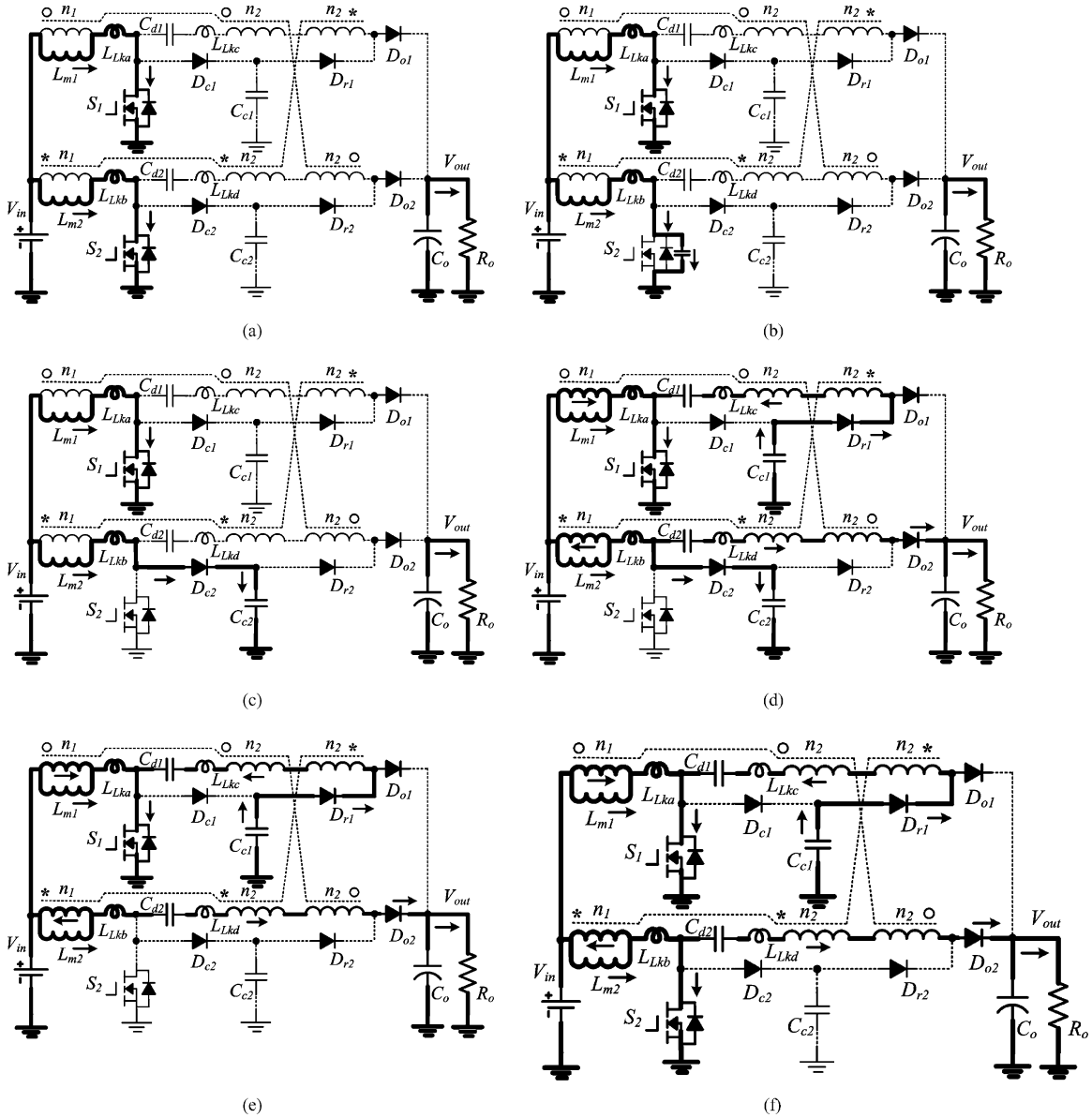

Fig. 5. Operation stages of the proposed converter. (a) Stage 1 [t_0–t_1]; (b) Stage 2 [t_1–t_2]; (c) Stage 3 [t_2–t_3]; (d) Stage 4 [t_3–t_4]; (e) Stage 5 [t_4–t_5]; (f) Stage 6 [t_5–t_6].

and the corresponding equivalent circuits for each operational stage are shown in Fig. 5.

Stage 1 [t_0, t_1]: The switches S_1 and S_2 are both in turn-on state before t_1. The output diodes D_{o1} and D_{o2} are both reverse-biased. The diodes D_{c1}, D_{c2}, D_{r1} and D_{r2} are all in turn-off state. The magnetizing inductors L_{m1}, L_{m2} and the primary leakage inductances $L_{\mathrm{Lk}a}, L_{\mathrm{Lk}b}$ are charged linearly by the input voltage

$$i_{Lm1}(t) = I_{Lm1}(t_0) + \frac{V_{\mathrm{in}}}{L_{m1} + L_{\mathrm{Lk}a}} t \tag{1}$$

$$i_{Lm2}(t) = I_{Lm2}(t_0) + \frac{V_{\mathrm{in}}}{L_{m2} + L_{\mathrm{Lk}b}} t. \tag{2}$$

Stage 2 [t_1, t_2]: At t_1, the switch S_2 turns off. The parasitic drain-source capacitor C_{S2} of S_2 is charged by the current of the magnetizing inductor L_{m2} in an approximately linear way. The voltage of the clamp diode D_{c2} decreases as the drain-source voltage of S_2 increases. This stage is very short due to the small capacitance of C_{S2}

$$v_{\mathrm{ds}2}(t) = \frac{I_{Lm2}(t_1)}{C_{S2}} t. \tag{3}$$

Stage 3 [t_2, t_3]: At t_2, the voltage of the clamp diode D_{c2} decreases to zero and it begins to conduct. The clamp capacitor C_{c2} is charged by the current of the magnetizing inductor L_{m2} linearly. The switch S_2 turns off and its drain-source voltage v_{ds2} is clamped by the capacitor C_{c2}. The energy stored in the leakage inductance $L_{\mathrm{Lk}b}$ starts to transfer to the clamp capacitor C_{c2}

$$v_{\mathrm{ds}2}(t) = V_{\mathrm{ds}2}(t_2) + \frac{I_{Lm2}(t_2)}{C_{c2}} t. \tag{4}$$

Stage 4 [t_3, t_4]: At t_3, the voltage of the output diode D_{o2} decreases to zero and it begins to turn on. The current increasing rate through D_{o2} is determined by the leakage inductance $L_{\mathrm{Lk}d}$. As the current through D_{o2} increases, the current through the clamp capacitor C_{c2} decreases. The series capacitor C_{d2}, the second winding of WCCI 2 and the third winding of WCCI 1 operate as voltage sources, which is in series to extend the voltage gain. Meanwhile, due to the transformer function of the coupled inductor, the regenerative diode D_{r1} begins to conduct. The energy stored in the clamp capacitor C_{c1} starts to transfer to the series capacitor C_{d1} through the regenerative diode D_{r1}, the second winding of WCCI 1 and the third winding of WCCI 2 and the switch S_1. The current through C_{c1} and C_{d1} is controlled by the leakage inductance $L_{\mathrm{Lk}c}$. The current expression can be derived by

$$i_{S1}(t) = i_{Lm1}(t) + (N+1)i_{Dr1}(t) + Ni_{Do2}(t) \quad (5)$$

$$i_{Cc2}(t) = i_{Lm2}(t) - Ni_{Dr1}(t) - (N+1)i_{Do2}(t) \quad (6)$$

$$i_{\mathrm{Lk}b}(t) = i_{Cc2}(t) + i_{Do2}(t). \quad (7)$$

Stage 5 [t_4, t_5]: At t_4, the current through the clamp capacitor C_{c2} decreases to zero and the clamp diode D_{c2} turns off naturally. There is no reverse-recovery problem for the clamp diodes. The energy stored in the series capacitor C_{d2} continues to transfer to the load. The current through D_{o2} is determined by the leakage inductances $L_{\mathrm{Lk}b}$ and $L_{\mathrm{Lk}d}$.

Stage 6 [t_5, t_6]: At t_5, the switch S_2 turns on. Due to the leakage inductance $L_{\mathrm{Lk}b}$, S_2 turns on with ZCS soft switching condition. The leakage inductance $L_{\mathrm{Lk}b}$ is quickly charged by the summation of the input voltage, the voltage on the series capacitor C_{d2}, the reflected voltages of the second winding of WCCI 2 and the third winding of WCCI 1. The current falling rate through the output diode D_{o2} is controlled by the leakage inductance $L_{\mathrm{Lk}d}$, which alleviates the output diode reverse-recovery problem. This stage ends when the output diode D_{o2} turns off

$$i_{Do2}(t) \approx I_{Do2}(t_5) - \frac{V_{\mathrm{out}} - V_{Cd2}}{L_{\mathrm{Lk}d}} t. \quad (8)$$

A similar operation works in the rest stages of the switching period.

III. Converter Performance Analysis

Due to the circuit symmetry of the proposed converter, it is reasonable to consider $L_{m1} = L_{m2} = L_m$, $C_{c1} = C_{c2} = C_c$, $C_{d1} = C_{d2} = C_d$. In order to simplify the analysis, the leakage inductance is assumed to be zero and the voltages on the clamp capacitor C_c and the series capacitor C_d are considered to be constant during the whole switching transition. The detailed performance of the presented converter is analyzed as follows.

A. Voltage Gain Expression

From the steady analysis in the above section, the charging voltage of the magnetizing inductor L_m is the input voltage V_{in} during the switch turn-on stage and the discharging voltage during the switch turn-off stage is given by

$$v_{Lm\_\mathrm{dis}} = \frac{V_{\mathrm{out}} - 2(N+1)V_{\mathrm{in}}}{2(N+1)}. \quad (9)$$

By applying the voltage-second balance to the magnetizing inductor, the output voltage gain is given by

$$M = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{2(N+1)}{1-D} \quad (10)$$

where *M* is the voltage gain, *N* is the turns ratio of the WCCIs and *D* is duty cycle of the switch.

From (10), it is clear that the proposed converter can achieve a high voltage gain because another two parameters appear in the numerator compared with the conventional boost converter. The detailed curve of the voltage gain *M* related to the turns ratio *N* and the duty cycle *D* is given in Fig. 6. As the duty cycle and the turns ratio increase, the voltage gain increases greatly, which makes the proposed converter able to avoid the extreme duty cycle and the large peak current existed in the conventional boost converter in high step-up applications.

The voltage multiplier cells are in series to the power branch to double the voltage gain under the same turns ratio and duty cycle condition compared with the interleaved high step-up converters published in [13]–[15] with only WCCIs.

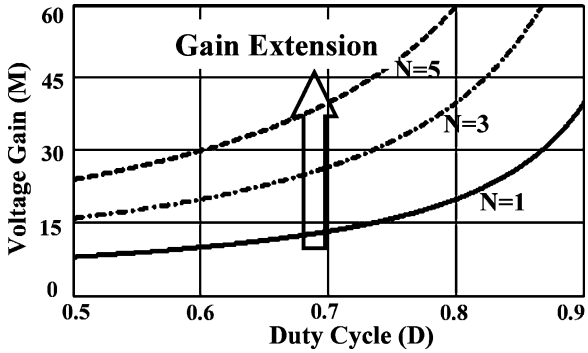

Fig. 6. Voltage gain curve versus turns ratio and duty cycle.

B. Voltage Stress Analysis

The voltage ripple on the clamp capacitors and the series capacitors are ignored to simplify the voltage stress analysis on the components of the proposed converter. The voltage stress of the clamp capacitors C_{c1} and C_{c2} is given by

$$V_{Cc} = \frac{V_{\mathrm{in}}}{1-D} = \frac{V_{\mathrm{out}}}{2(N+1)}. \quad (11)$$

The voltage stresses of the switches S_1, S_2 and the clamp diodes D_{c1}, D_{c2} are equal to that of the clamp capacitors, which are given by

$$V_S = V_{Dc} = V_{Cc} = \frac{V_{\mathrm{in}}}{1-D} = \frac{V_{\mathrm{out}}}{2(N+1)}. \quad (12)$$

The switch voltage stress is determined by the turns ratio of the WCCIs. The curve of the normalized switch voltage stress as a function of the turns ratio of the WCCIs is plotted in Fig. 7. It is shown that the maximum switch voltage stress is half of

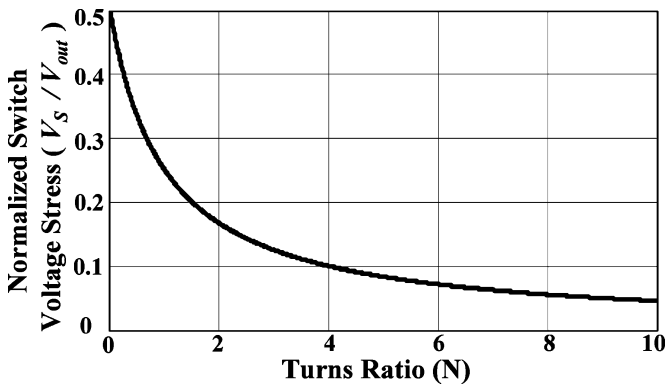

Fig. 7. Plot of normalized switch voltage stress versus turns ratio.

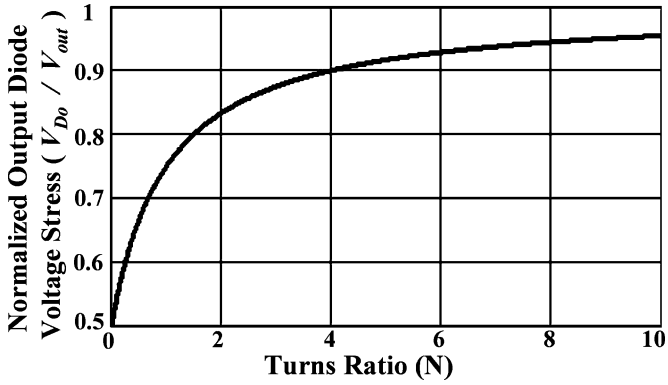

Fig. 8. Plot of normalized output diode voltage stress versus turns ratio.

the output voltage. As the turns ratio increases, the switch voltage stress decreases, which makes it possible that low-voltage power MOSFETs with low $R_{\mathrm{DS\_ON}}$ can be employed in high step-up and high output voltage applications. As a result, the conduction losses are reduced compared with the conventional boost converter.

The voltage stress of the series capacitors C_{d1} and C_{d2} is given by

$$V_{Cd} = V_{\mathrm{out}} - (N+1)V_{\mathrm{in}} = \frac{(N+1)(1+D)}{(1-D)}V_{\mathrm{in}} = \frac{1+D}{2}V_{\mathrm{out}}. \quad (13)$$

The voltage stress of the output diodes D_{o1} and D_{o2} can be derived by

$$V_{Do} = V_{\mathrm{out}} - V_{Cc} = \frac{2N+1}{1-D}V_{\mathrm{in}} = \frac{2N+1}{2(N+1)}V_{\mathrm{out}}. \quad (14)$$

The plot of the normalized output diode voltage stress with the turns ratio of the WCCIs is shown in Fig. 8. It can be seen that the output diode voltage stress increases as the turns ratio increases, but it is always lower than the output voltage. The minimum voltage stress of the output diode is half of the output voltage.

The voltage stress of the regenerative diodes D_{r1} and D_{r2} can be derived by

$$V_{Dr} = V_{\mathrm{out}} - V_{Cc} = \frac{2N+1}{1-D}V_{\mathrm{in}} = \frac{2N+1}{2(N+1)}V_{\mathrm{out}}. \quad (15)$$

It can be seen that the voltage stress of the regenerative diodes is the same as that of the output diodes.

C. Soft Switching Performance

Due to the leakage inductance of the WCCIs, ZCS turn-on is realized for the switch S_1 and S_2, which reduces the switching losses. When the switch turns off, the leakage energy is transferred to the clamp capacitor through the clamp diode, which absorbs the voltage spikes on the MOSFETs and recycles the leakage energy. Furthermore, the output diode current falling rate is controlled by the leakage inductance existed in the second and the third windings of the WCCIs, which alleviates the output diode reverse-recovery problem and reduces the reverse-recovery losses. The clamp diode turns off naturally, so there is no reverse-recovery problem for the clamp diode.

D. C_c and C_d Design Consideration

The voltage ripple on the capacitors C_c and C_d is the main consideration for the capacitor design. From the steady operational analysis, it can be derived that the variation of the electric charge on the capacitors C_c and C_d is the electric charge transferred to the load in each switching period. The relationship between the voltage ripple and the output power can be derived by

$$C = \frac{P_{\mathrm{out}}}{2f_s V_{\mathrm{out}} \Delta V_c} \quad (16)$$

where P_{out} is the output power, f_s is the switching frequency, V_{out} is the output voltage and ΔV_c is the voltage ripple on the capacitor C_c or C_d. It can be seen that the voltage ripple can be reduced when a large capacitor is employed. However, the large capacitor is bulky and costly. The design of the capacitors C_c and C_d should make a compromise between the voltage ripple cancellation and the cost.

E. Current Sharing Performance With Asymmetrical Duty Cycle and Leakage Inductance

The third winding of the WCCI in the proposed converter is inserted into another interleaved phase, which can improve the current sharing performance under asymmetrical duty cycle or leakage inductance condition. The simulation current difference with asymmetrical duty cycle is given in Fig. 9. The switch duty cycle of phase 2 keeps 0.75 and the switch duty cycle of phase 1 varies from 0.7 to 0.8 to show the current sharing performance under 1 kW load condition. The current difference $(I_{\mathrm{in1}}–I_{\mathrm{in2}})/I_{\mathrm{in2}}$ is 0.73, when the duty cycle of phase 1 is 0.8 with $N = 2$. However, the current difference is only 0.27 when the turns ratio is increased to $N = 4$. From the simulation results, the conclusion can be drawn that as the turns ratio of the WCCIs increases, the current sharing performance improves.

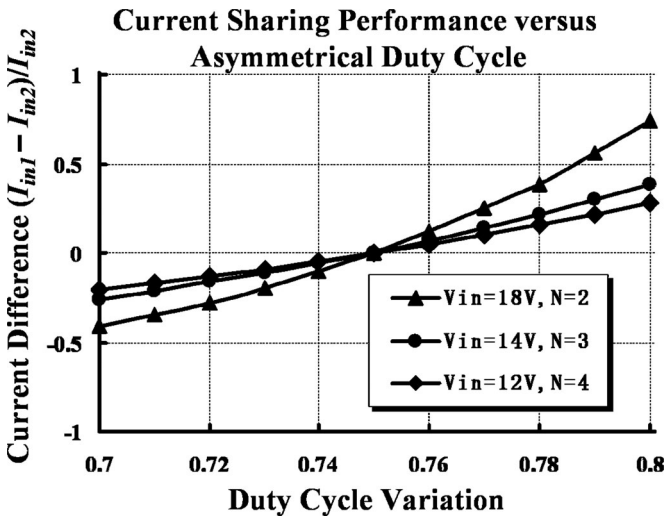

Fig. 9. Current sharing performance with asymmetrical duty cycle.

TABLE I
CURRENT SHARING PERFORMANCE WITH ASYMMETRICAL LEAKAGE INDUCTANCE ($V_{\rm in} = 16$ V, $N = 3$, $D = 0.75$, $P_{\rm out} = 1$ kW, $f_s = 50$ kHz)

L_{Lka}(μH)	0.5	0.5	0.5	0.5	0.5
L_{Lkc}(μH)	9	9	9	9	9
L_{Lkb}	L_{Lka}/4	L_{Lka}/2	L_{Lka}	$2L_{Lka}$	$4L_{Lka}$
L_{Lkd}	L_{Lkc}/4	L_{Lkc}/2	L_{Lkc}	$2L_{Lkc}$	$4L_{Lkc}$
(I_{in1} - I_{in2})/I_{in2}	0.43%	0.29%	0	-0.79%	-1.1%

The simulation results of the current sharing performance with asymmetrical leakage inductance are given in Table I. It can be seen that the current difference is very small even the leakage inductance has a wide range variation. The leakage inductance has small effect on the current sharing performance.

F. Limitation of the Turns Ratio

From the steady operational analysis, it can be concluded that the duty cycle of the proposed converter should be exceeded 0.5. So the limitation of the turns ratio can be derived by

$$N \le \frac{V_{\rm out}}{4V_{\rm in}} - 1. \tag{17}$$

G. Performance Comparison

Most of the high step-up converters presented in previous work [5]–[10] with coupled inductor concept are single-phase circuits. Although the extreme duty cycle existed in the conventional boost converter is avoided, the input current ripple is still large due to their single-phase operation and the pulsed current waveforms, which limits these converters in high power and high current applications.

Due to the interleaved structure, the current ripple is reduced, the passive component size is reduced and the power level is increased. The circuit performance comparison of the conventional interleaved boost converter, the interleaved boost converter introduced in [15] and the proposed interleaved high step-up converter is shown in Table II.

TABLE II
CONVERTER PERFORMANCE COMPARISON

	Conventional interleaved boost converter	Converter introduced in [15]	Proposed converter
Voltage gain	$\frac{1}{1-D}$	$\frac{N+1}{1-D}$	$\frac{2\cdot(N+1)}{1-D}$
Switch voltage stress	V_{out}	$\frac{V_{out}}{N+1}$	$\frac{V_{out}}{2\cdot(N+1)}$
Output diode voltage stress	V_{out}	$\frac{2\cdot N}{N+1}\cdot V_{out}$	$\frac{2\cdot N+1}{2\cdot(N+1)}\cdot V_{out}$
Current ripple	Large	Small	Small
Switching losses	Large	Small	Small
Reverse-recovery losses	Large	Small	Small
Conduction losses	Large	Medium	Small

Compared with the conventional interleaved boost converter, the extreme duty cycle is avoided to reduce the current stress on the power devices. The large current ripple is minimized to reduce the conduction losses. The switch voltage stress is reduced to make low voltage MOSFETs with low $R_{\rm DS\_ON}$ available in high step-up and high output voltage application. Furthermore, ZCS turn-on is achieved for the switches and the output diode reverse-recovery problem is alleviated by the leakage inductance of the WCCIs, which improves the efficiency and reduces the electromagnetic interference (EMI) noise.

The voltage gain of the proposed converter is twice of that of the converter introduced in [15] because the voltage multiplier cells are inserted into the power branch to extend the voltage gain. The switch voltage stress is half of that of the converter in [15] due to the voltage multiplier cells under the same turns ratio condition. The maximum output diode voltage stress of the proposed converter is the output voltage, but the maximum output diode voltage stress of the converter in [15] is twice of the output voltage stress as the turns ratio increases. These factors make the proposed converter more suitable in high step-up and high power applications to improve the efficiency and power density.

IV. START-UP OPERATION

From the above-mentioned analysis, it can be seen that the limitation of the proposed converter is that the duty cycle of the circuit should be larger than 0.5. During the start-up operation, the duty cycle of the two switches is in the synchronization mode instead of the interleaved mode. Both the two phases work in the same mode in the whole switching transition to adjust the duty cycle from 0 to 0.5 during the start-up stage. The key waveforms are shown in Fig. 10 and the corresponding equivalent circuits for each stage are given in Fig. 11 during the start-up operation.

Stage 1 [t_0, t_1]: During this stage, the switches S_1 and S_2 are both in turn-on state. The output diodes D_{o1} and D_{o2} are both reverse-biased. The energy stored in the clamp capacitors C_{c1} and C_{c2} is transferred to the series capacitors C_{d1} and C_{d2}

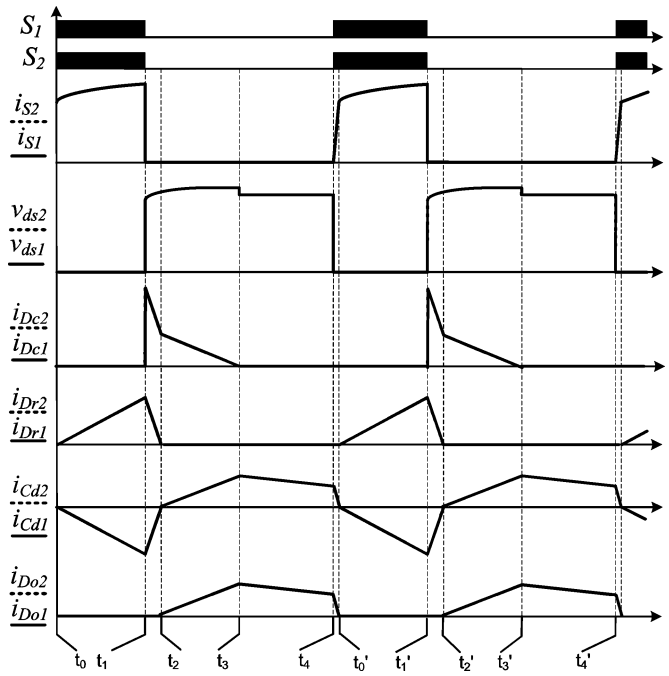

Fig. 10. Key waveforms with duty cycle less than 0.5.

through the regenerative diodes D_{r1} and D_{r2}. Due to the symmetry of the circuit, the voltage stress of the clamp capacitors C_{c1} and C_{c2} is the same as that of the series capacitors C_{d1} and C_{d2}.

Stage 2 [t_1, t_2]: The turn-off gate signals of the switches S_1 and S_2 are given synchronously at t_1. The clamp diodes D_{c1} and D_{c2} turn on to transfer the leakage energy to the clamp capacitors C_{c1} and C_{c2}. The current falling rate of the regenerative diodes D_{r1} and D_{r2} is controlled by the leakage inductance $L_{\mathrm{Lk}c}$ and $L_{\mathrm{Lk}d}$, respectively.

Stage 3 [t_2, t_3]: The current through the regenerative diodes D_{r1} and D_{r2} is decreased to zero and D_{r1}, D_{r2} turn off at t_2. Part of the energy stored in the magnetizing inductors L_{m1} and L_{m2} is still transferred to the clamp capacitors C_{c1} and C_{c2}. And part of the energy stored in L_{m1} and L_{m2} begins to transfer to the load through the output diodes D_{o1} and D_{o2}.

Stage 4 [t_3, t_4]: At t_3, the current through the clamp diodes D_{c1} and D_{c2} is decreased to zero and turn-off naturally. The output diodes D_{o1} and D_{o2} are still in turn-on state to transfer the energy to the load.

Stage 5 [t_4, t_5]: At t_4, the switches S_1 and S_2 turn on with ZCS soft switching performance due to the leakage inductance. The current falling rate of the output diodes D_{o1} and D_{o2} is controlled by the leakage inductance. This stage ends when D_{o1} and D_{o2} turn-off.

During the start-up operation with synchronization mode, the charging voltage on the magnetizing inductor is the input voltage and the discharging voltage is $((V_{\mathrm{out}}/2) - V_{\mathrm{in}})$ assuming the leakage inductance to be zero. The voltage gain of the converter with $D < 0.5$ condition can be derived by

$$M_{\text{start-up}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{2}{1-D}. \tag{18}$$

The voltage stresses of the switches, the clamp diodes, the regenerative diodes and the output diodes are the same and given by

$$V_{\mathrm{ds}} = V_{Dc} = V_{Dr} = V_{Do} = \frac{V_{\mathrm{in}}}{1-D}. \tag{19}$$

It can be seen that the maximum voltage stress of the power devices is twice of the input voltage during the start-up operation.

V. Simulated and Experimental Verifications

In order to verify the effectiveness of the proposed converter, a 1 kW prototype is built. The specifications of the tested converter are given as follows:

V_{in}: 35 V–45 V; V_{out}: 380 V; P_{out}: 1 kW; f_s: 50 kHz;

n_2/n_1: 22/22; L_m: 95 μH; C_o: 470 μF; C_{c1} and C_{c2}: 2.2 μF;

C_{d1} and C_{d2}: 4.7 μF;

D_{c1} and D_{c2}: RURG1540; D_{r1} and D_{r2}: MUR1560;

S_1 and S_2: Two pieces of IRF250N; D_{o1} and D_{o2}: MUR1560.

Two toroidal sendust cores in parallel are employed for each WCCIs. The primary winding, the second winding and the third winding are all 22 turns. Two pieces of MOSFETs IRF250N are selected as each switch. MUR1560 is used as the output diode. The switching frequency is 50 kHz to reduce the magnetic component size. RURG1540 is adopted as the clamp diode due to the ultrafast soft recovery performance and the clamp capacitor is 2.2 μF. The series capacitor is 4.7 μF and MUR1560 is selected as the regenerative diode.

The simulated and the experimental results of the proposed converter are given from Figs. 12–17 under 1 kW full load condition with 40 V input voltage.

The simulated and experimental results of the switch gate signals and drain-source voltages are shown in Fig. 12. It can be seen that the gate signals are interleaved to reduce the current ripple and to increase the power level. The extreme duty cycle existed in the conventional interleaved boost converter is avoided because the voltage gain of the proposed converter is extended. The switch voltage stress is about 100 V, which is far lower than the output diode. So, low-voltage MOSFETs are available for the proposed converter to reduce the conduction losses in high step-up and high-output voltage applications.

The simulated and experimental results of the gate signal, the switching voltage of S_1 and the voltage on the clamp capacitor C_{c1} are demonstrated in Fig. 13. It is shown that the switching voltage of S_1 is clamped effectively and the voltage ripple on the clamp capacitor is small. The leakage energy is recovered and the voltage spikes on the MOSFETs are absorbed by the clamp circuits.

The simulated and experimental results of the current of the primary leakage inductance $L_{\mathrm{Lk}a}$, the current and switching voltage of switch S_1 are given in Fig. 14. The current reflected effect shown in the dashed block is caused by the transformer function of the WCCIs, which increases the switch conduction losses a little.

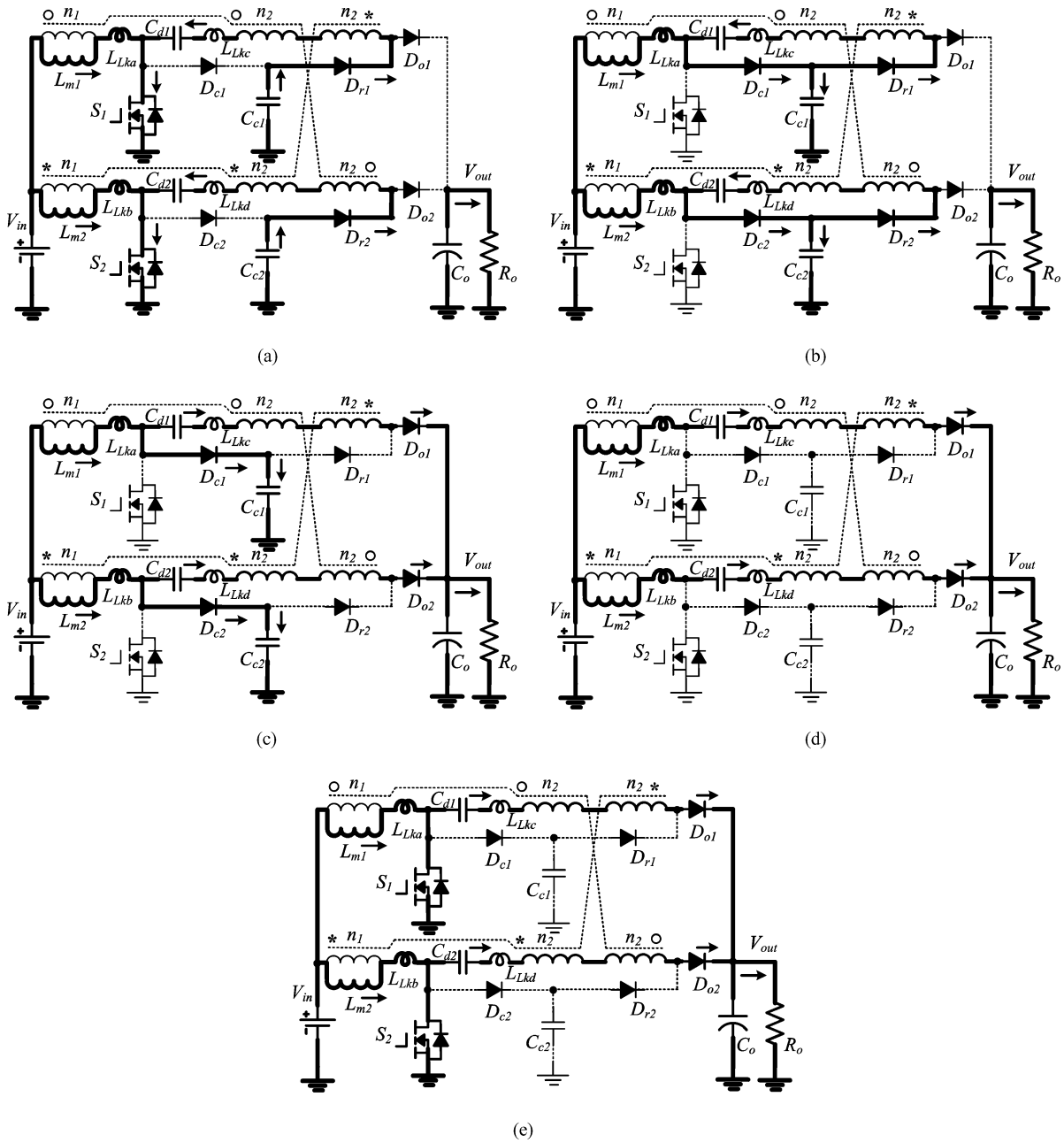

Fig. 11. Operation stages with duty cycle less than 0.5. (a) Stage 1 [t_0–t_1]; (b) Stage 2 [t_1–t_2]; (c) Stage 3 [t_2–t_3]; (d) Stage 4 [t_3–t_4]; (e) Stage 5 [t_4–t_5].

The simulated and experimental results of the current and voltage of the series capacitor C_{d1} is demonstrated in Fig. 15. The voltage ripple on the series capacitor is small and it can be taken as a constant voltage source to extend the voltage gain and to reduce the switch voltage stress further.

The simulated and experimental results of the voltages of the clamp diode D_{c1} and the regenerative diode D_{r1} are given in Fig. 16. The voltage stress of the clamp diodes is the same as that of the switches. The voltage stress of the regenerative diodes is higher than that of the clamp diodes, but is still lower than the output voltage.

The simulated and experimental results of the current and voltage of the output diode D_{o1} are shown in Fig. 17. The voltage stress of the output diodes is lower than the output voltage. The high peak current is reduced because the voltage gain is extended and the extreme duty cycle is avoided compared with the conventional interleaved boost converter in high step-up applications.

In order to examine the dynamic response performance of the proposed converter, the experimental results of the output voltage $V_{\rm out}$ and the output current $I_{\rm out}$ under the step load variation between 200 W and 1 kW are depicted in Fig. 18. It can be seen that the output voltage of the presented converter is insensitive to the load condition with a close loop control. In theory, a reduction of the duty cycle is caused by the leakage inductance of the WCCIs, which introduces an additional damping to the

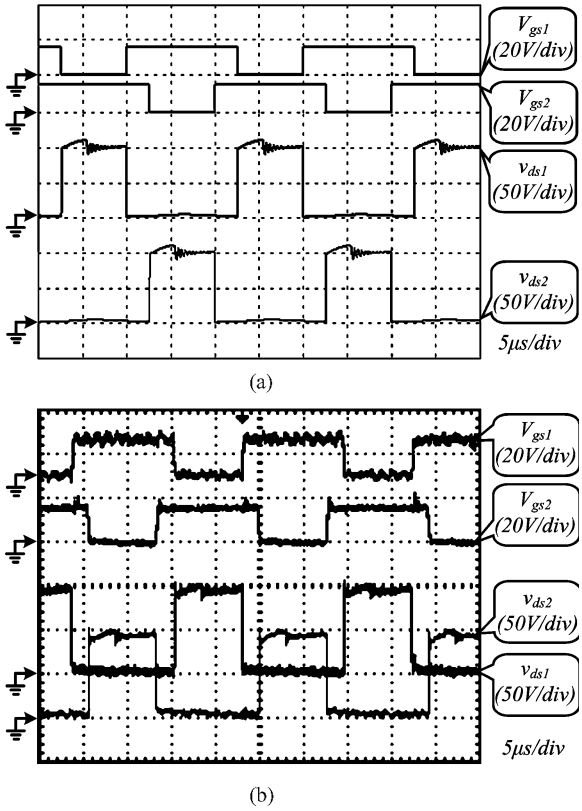

Fig. 12. Simulated and experimental results of $v_{\rm gs1}, v_{\rm gs2}, v_{\rm ds1}$, and $v_{\rm ds2}$. (a) Simulated results. (b) Experimental results.

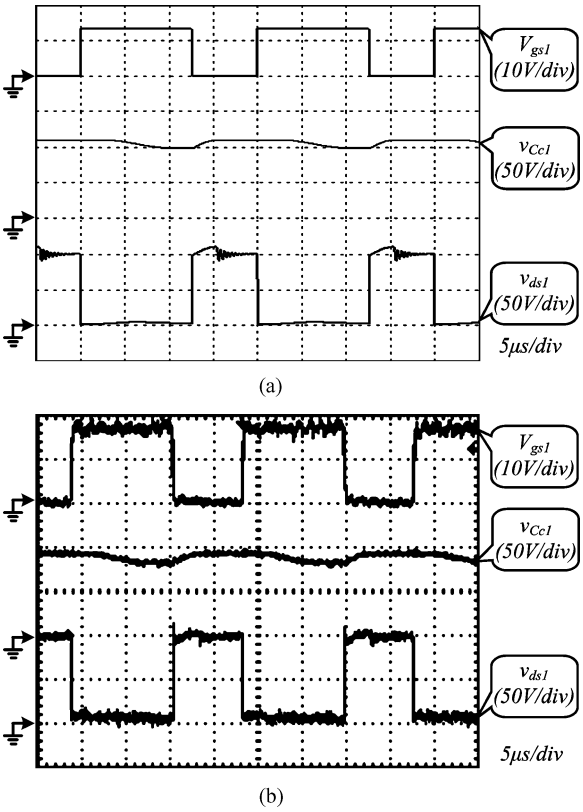

Fig. 13. Simulated and experimental results of $v_{\rm gs1}, v_{\rm ds1}$, and v_{Cc1}. (a) Simulated results. (b) Experimental results.

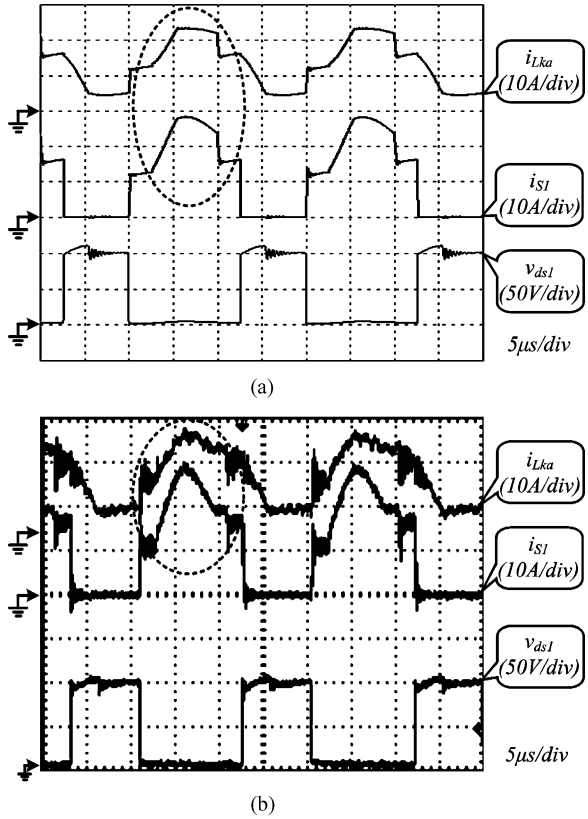

Fig. 14. Simulated and experimental results of $i_{\rm Lka}, i_{S1}$, and $v_{\rm ds1}$. (a) Simulated results. (b) Experimental results.

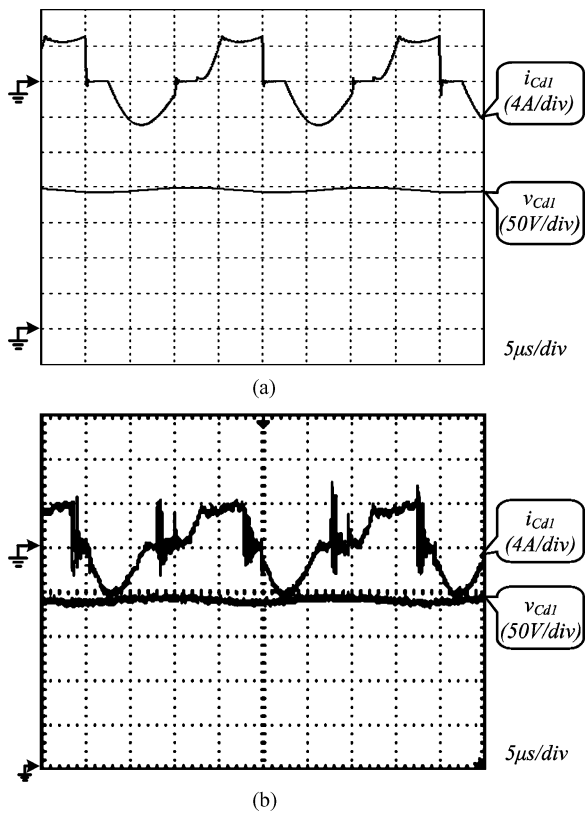

Fig. 15. Simulated and experimental results of current and voltage of C_{d1}. (a) Simulated results. (b) Experimental results.

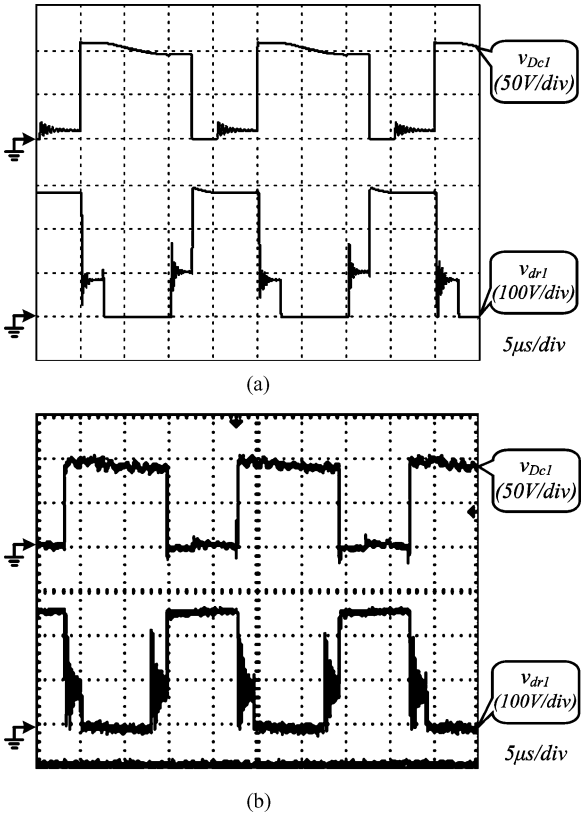

Fig. 16. Simulated and experimental results of voltage on D_{c1} and D_{r1}. (a) Simulated results. (b) Experimental results.

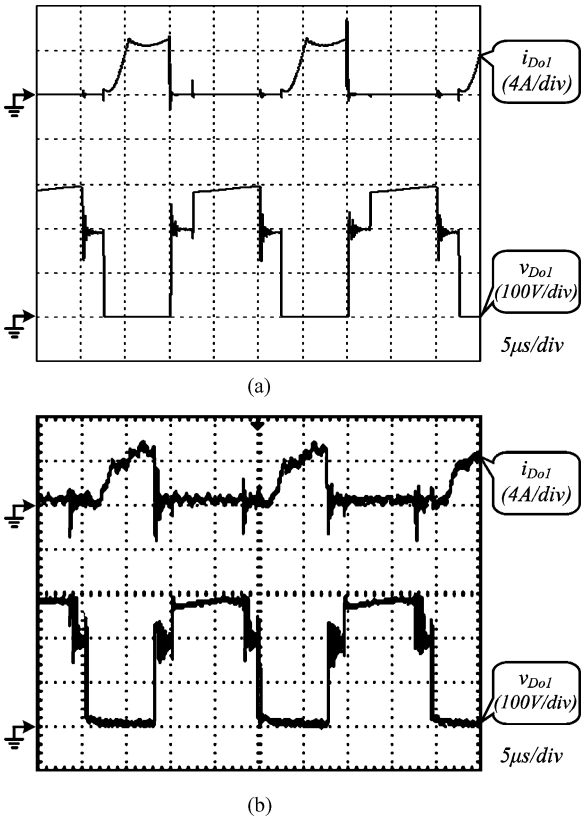

Fig. 17. Simulated and experimental results of current and voltage of D_{o1}. (a) Simulated results. (b) Experimental results.

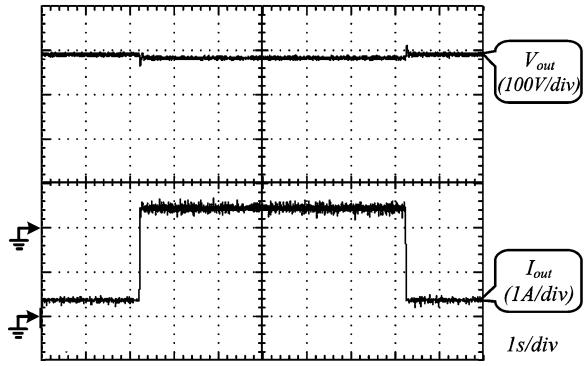

Fig. 18. Experimental results with step load variation between 200 W and 1 kW.

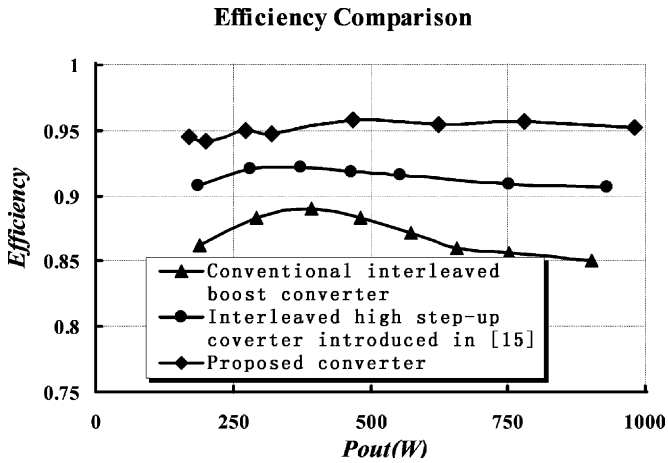

Fig. 19. Measured efficiency comparison with different converters at different loads.

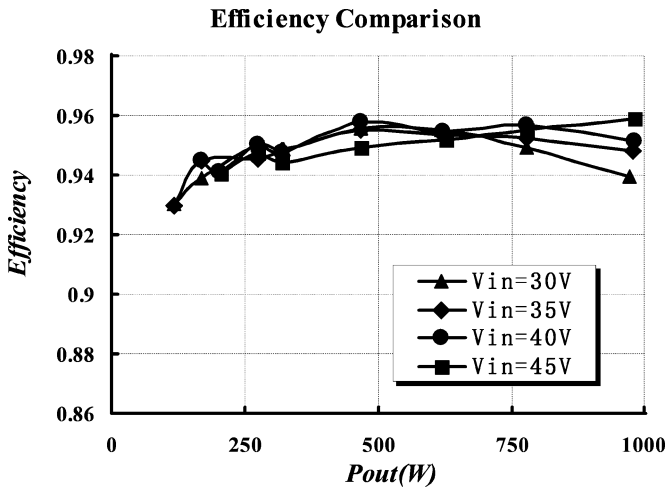

Fig. 20. Measured efficiency comparison with different input voltages.

circuit performance [16]. The influence of the clamp capacitors C_c and the series capacitors C_d in the proposed converter is similar to that of the capacitors in the converter introduced in [12].

The measured efficiency at different loads is given in Fig. 19. The efficiency at 1 kW full load is 95.1% and the maximum efficiency is 95.8% for the proposed converter with 40–380 V conversion. There is about 10% efficiency improvement compared with the conventional interleaved boost converter. More

than 4% efficiency improvement compared with the converter introduced in [15] under the similar test condition.

The measured efficiency with different input voltage of the proposed converter is shown in Fig. 20. It can be seen that the efficiency of the proposed converter at full load is higher than 94% even the input voltage is reduced to 30 V. The efficiency at full load with 45 V input voltage is nearly 96%.

VI. Conclusion

An interleaved boost converter integrated with WCCIs and voltage multiplier cells was introduced in this paper. The voltage gain is extended and the extreme duty cycle is avoided by the WCCIs and the voltage multiplier cells compared with the conventional interleaved boost converter, which can reduce the peak current and voltage stress on the switches to reduce the conduction losses. Moreover, ZCS turn-on for the switch is achieved and the output diode reverse-recovery problem is alleviated by the leakage inductance to reduce the switching losses and EMI noises. Furthermore, the leakage energy is recycled and the voltage spikes on the power MOSFETs are absorbed by the voltage multiplier cells. The simulated and experimental results showed that the proposed converter is a suitable topology candidate for high step-up, high power PV grid-connected power system.

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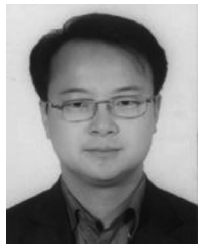
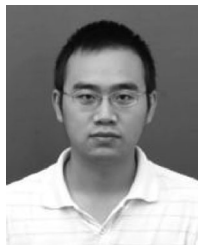


Wuhua Li (M'09) received the B.Sc. and Ph.D. degrees in applied power electronics and electrical engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively.

From September 2004 to March 2005, he was an Intern, and from January 2007 to June 2008, a Research Assistant with GE Global Research Center, Shanghai, China. From July 2008 to April 2010, he was with the College of Electrical Engineering, Zhejiang University, Hangzhou, China, as a Postdoctoral Fellow. In May 2010, he became a Faculty Member at Zhejiang University as a Lecturer. In December 2010, he was promoted as an Associate Professor. From July 2010 to September 2011, he was a Ryerson University Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. His research interests include high efficiency power converters and renewable energy power conversion system. He has published more than 70 technical papers and holds more than 20 issued/pending patents.



Yi Zhao was born in Liaoning, China, in 1983. He received the B.Sc. degree in electrical and electronic engineering from Huazhong University of Science and Technology, Wuhan, China, in 2006. He is currently working toward the Ph.D. degree at the College of Electrical Engineering, Zhejiang University, Hangzhou, China.

His current research interests include dc–dc converters and photovoltaic power systems.

Jiande Wu was born in Zhejiang, China, in 1973. He received the B.Sc. and M.Sc. degrees from Zhejiang University, Hangzhou, China, in 1994, and 1997, respectively.

Since 1997, he has been a Lecturer at the College of Electrical Engineering, Zhejiang University. His current research interests include power electronics modeling, advanced digital control, and advanced communication techniques for power electronics.

Xiangning He (M'95–SM'96–F'10) received the B.Sc. and M.Sc. degrees from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989.

From 1985 to 1986, he was an Assistant Engineer at the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer at Zhejiang University. In 1991, he obtained a Fellowship from the Royal Society of U.K., and conducted research in the Department of Computing and Electrical Engineering, Heriot-Watt University, Edinburgh, U.K., as a Postdoctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor. Since 1996, he has been a Full Professor in the College of Electrical Engineering, Zhejiang University, Hangzhou, China. He was the Director of the Power Electronics Research Institute and the Head of the Department of Applied Electronics; he is currently the Vice Dean of the College of Electrical Engineering, Zhejiang University, Hangzhou, China. His research interests are power electronics and their industrial applications. He is the author or coauthor of more than 200 papers and one book titled *Theory and Applications of Multi-level Converters*. He holds 12 patents.

Dr. He received the 1989 Excellent Ph.D. Graduate Award, the 1995 Elite Prize Excellence Award, the 1996 Outstanding Young Staff Member Award, and 2006 Excellent Staff Award from Zhejiang University for his teaching and research contributions. He received five Scientific and Technological Progress Awards from Zhejiang Provincial Government and the State Educational Ministry of China in 1998, 2002, and 2009, respectively, and five Excellent Paper Awards. He is a Fellow of the Institution of Engineering and Technology (formerly IEE), U.K.