Multilevel Current Waveform Generation Using Inductor Cells and H-Bridge Current-Source Inverter

Suroso and Toshihiko Noguchi, *Senior Member, IEEE*

***Abstract*—This paper presents a new circuit configuration of single-phase multilevel current-source inverter (CSI). In this new topology, a basic H-bridge CSI working as a main inverter generates a multilevel current waveform in cooperation with inductor cells connected in parallel as auxiliary circuits. Each inductor cell is composed by four unidirectional power switches with an inductor across the cell circuit. The inductor cells work by generating the intermediate level of the multilevel current waveform with no additional external dc-power sources. A simple proportional-integral controller is applied to control the intermediate-level currents of the multilevel output waveform. A five-level and a nine-level pulsewidth-modulation inverter configuration, with chopper-based dc-current sources, are verified through computer simulations. Furthermore, an experimental prototype of a five-level CSI is set up and is tested. The results show that the test circuit works properly to generate the multilevel output-current waveform with low output harmonics by using small size of inductors without any additional external dc-power sources, which proves feasibility of the proposed strategy.**

***Index Terms*—Current-source inverter (CSI), H-bridge, inductor cell, multilevel.**

I. Introduction

RECENT development of high-performance semiconductor power switches such as MOSFETs and insulated-gate bipolar transistors (IGBTs) increases the research interest in high-power converters, such as multilevel voltage-source inverters (VSIs) and its dual, multilevel current-source inverters (CSIs). Multilevel inverters have the capability to deliver higher output power with lower dv/dt or lower di/dt and with less-distorted output waveforms, resulting in reduction of electromagnetic interference (EMI) noise and size of an output filter [1]–[3]. In distributed-power-generation application, as most renewable energy sources, such as photovoltaic systems, deliver dc power; the generated power must be converted to ac power and is fed into the grid through grid-connected inverters [6]–[8]. Various international standards, like IEEE-1547, IEEE-929, and EN-61000-3-2, impose requirements on the inverter's output-power quality, i.e., harmonic currents and total harmonics distortion (THD) of the output current. Multilevel CSI is one of the effective solutions to tackle such problems. Control of the grid-connected CSI is comparatively simpler than its counterpart, VSI. A grid-connected CSI can buffer the output current from the grid-voltage fluctuation, generates a predetermined current to the power grid without ac-current-feedback loops, and can achieve a high-power-factor operation. Its output current is less affected by a grid voltage, and the CSI has inherent short-circuit protection abilities [7], [8]. Moreover, the discrete diodes connected in series with the power switches to obtain unidirectional power switches in the CSI will be unnecessary because new IGBTs with reverse-blocking capability (reverse-blocking IGBTs) are emerging [4], [5].

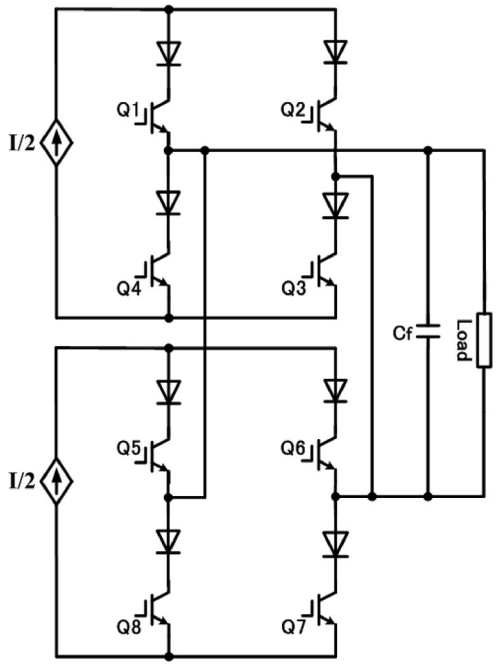

Fig. 1. Parallel H-bridge five-level CSI.

Few topologies of the multilevel CSIs have been proposed by researchers and engineers. A conventional method to generate the multilevel current waveform is by paralleling some three-level H-bridge CSIs, as shown in Fig. 1 [9]–[11]. This topology is a dual circuit of a cascade multilevel VSI [9]. However, the requirement of many isolated dc-current sources with their complex, bulky, and costly isolation transformers and inductors is a problem introduced by this configuration. Another topology of the multilevel CSI is obtained by applying a multicell topology of the CSI (or multirating inductor multilevel CSI [9]), which is a dual converter of a flying-capacitor-based full-bridge multilevel VSI [12]–[14]. However, this topology has a

Manuscript received January 25, 2010; revised April 22, 2010, accepted June 17, 2010. Date of current version February 7, 2012. Recommended for publication by Associate Editor P. Barbosa.

Suroso is with the Department of Electrical Engineering, University of Jenderal Soedirman, Purwokerto 53122, Indonesia, and also with the Department of Energy and Environment Engineering, Nagaoka University of Technology, Nagaoka, Japan (e-mail: suroso.te.unsoed@gmail.com).

T. Noguchi is with the Department of Electrical and Electronic Engineering, Shizuoka University, Shizuoka 432-8561, Japan (e-mail: ttnogut@ipc.shizuoka.ac.jp).

Digital Object Identifier 10.1109/TPEL.2010.2056933

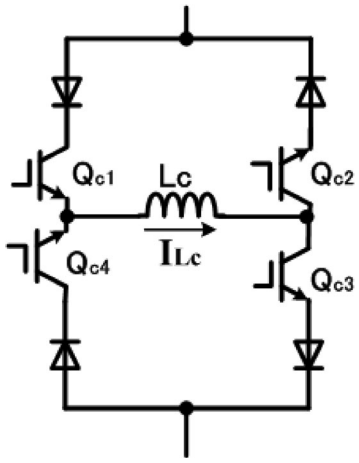

Fig. 2. Proposed inductor cell circuit.

drawback with its bulky intermediate inductors and complexity for balancing control of the intermediate-level currents. Some control methods have been proposed for balancing control of the intermediate-level currents in [13] and [14], but very large in size of the intermediate inductors (100 mH) are still used. These cumbersome inductors will be costly and limit the application of the inverter. Bai and Zhang [9] presented the configuration of a single-rating inductor multilevel CSI that is the dual structure of an improved diode-clamped multilevel VSI. Noguchi and Suroso [15], [16] presented a common-emitter configuration of the multilevel CSI obtained by connecting two-level CSI modules in parallel with the three-level common-emitter CSI. This configuration has a great advantage over conventional approaches because all of the power switches are connected at a common-emitter point or an identical potential line. This topology needs only a single isolated gate-drive circuit to drive all power switches of the inverter; hence, the complexity of the gate-drive circuits can be moderated. Unfortunately, the requirement of many split dc-current sources is an apparent disadvantage of this topology.

This paper proposes a new circuit configuration of the multilevel CSI. In this new topology, a basic H-bridge CSI, working as a main inverter circuit, is connected in parallel with inductor cells working as auxiliary circuits. The inductor cells generate the intermediate levels of the multilevel output-current waveform, with no additional external dc-power sources. The operating performance of the proposed multilevel CSI is examined and is tested through some computer simulations. Furthermore, a laboratory experimental prototype of a five-level CSI circuit was set up to verify the proposed multilevel CSI topology.

II. Circuit Configuration and Operation Principle

A. Operation Principle of Proposed Multilevel CSI

Fig. 2 shows a configuration of the proposed inductor cell circuit composed by four unidirectional power switches Q_{C1}, Q_{C2}, Q_{C3}, and Q_{C4}, and an inductor L_C connected across the cell circuit. The newly proposed configuration of the multilevel CSI can be obtained by connecting the H-bridge CSI in parallel with a single or more inductor cells, as shown in a schematic diagram of the proposed multilevel CSI in Fig. 3. A five-level CSI configuration is obtained by connecting a single inductor cell, a nine-level CSI configuration is achieved by connecting two inductor cells in parallel with the main three-level H-bridge CSI, and so forth. The relation between the level number of the output-current waveform (M) and the number of the inductor cells (N) can be formulated as follows:

$$M = 2^{(N+1)} + 1. \tag{1}$$

Figs. 4 and 5 show the configurations of five-level and nine-level CSIs using the proposed strategy, respectively.

For M-level CSI, if the dc-current source of the main H-bridge CSI is assumed to have an amplitude I, the current flowing through the Nth inductor cell $I_{L_c(i)}$ is expressed as follows:

$$I_{L_c(i)} = \frac{I}{2^i}, \qquad \text{where} \qquad i = 1, 2, 3, \ldots, N. \tag{2}$$

The output-current levels of the five-level CSI are $+I$, $+I/2$, 0, $-I/2$, and $-I$. For the nine-level CSI, the output waveform has $+I$, $+3I/4$, $+I/2$, $+I/4$, 0, $-I/4$, $-I/2$, $-3I/4$, and $-I$ current levels.

The inductor cells generate intermediate-level currents of the multilevel output waveform from the basic three-level current of the H-bridge CSI. It utilizes the charging and the discharging operation modes of the inductor. Fig. 6 shows the operation modes of the inductor cell during a positive-cycle operation of the five-level CSI. The charging operation mode of the inductor L_c is conducted when the switches Q_{C1} and Q_{C3} are turned on, while the switches Q_{C2} and Q_{C4} are turned off. A current $I_{L_c} = I/2$ flows through the power switches Q_{C1} and Q_{C3} that energizes the inductor L_c. The discharging operation mode is achieved by turning on the switches Q_{C2} and Q_{C4} and by turning off Q_{C1} and Q_{C3}. The stored energy in the inductor is discharged to the load as a current $I/2$. The circulating current modes occur when the inductor cell deliver a null current to keep a constant current in the inductor cell. Similar operation modes occurred for the negative cycle of the output-current waveform.

Table I lists the switch states of the proposed five-level CSI. Power device utility and average switching frequency between Q_{C1}, Q_{C2} and Q_{C3}, Q_{C4} in the circulating modes of the inductor cell current is one of the considerations to use redundant switching states for I, 0, and $-I$ output-current generation. It is also related to the heat distribution among the power switches Q_{C1}, Q_{C2}, Q_{C3}, and Q_{C4} caused by the switching and conduction losses.

B. DC-Current Source

In the proposed multilevel CSI, the dc-current source is indispensable. In order to test the proposed multilevel CSI, the dc-current source is obtained by employing a chopper with a smoothing inductor (L_i) connected with the H-bridge CSI. The chopper consists of a controlled switch (Q_C) that regulates the dc current flowing through the smoothing inductor as the dc input current I_{L_i}. A free-wheeling diode (D_F) is used to keep continuous current flowing through the smoothing inductor. The

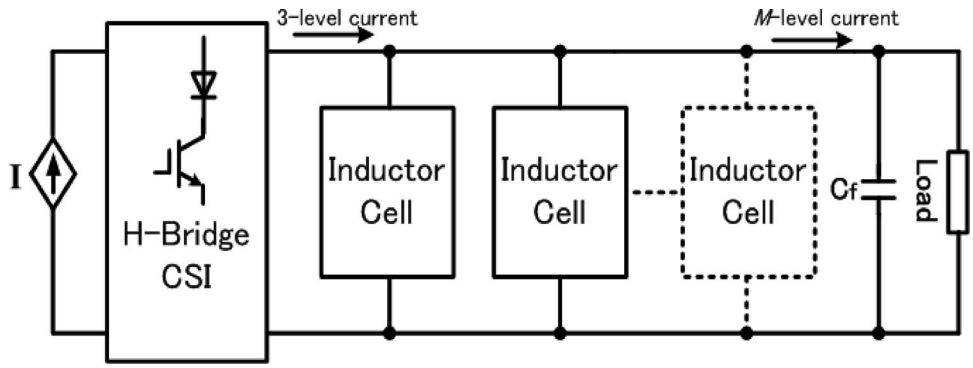

Fig. 3. Proposed configuration of multilevel CSI.

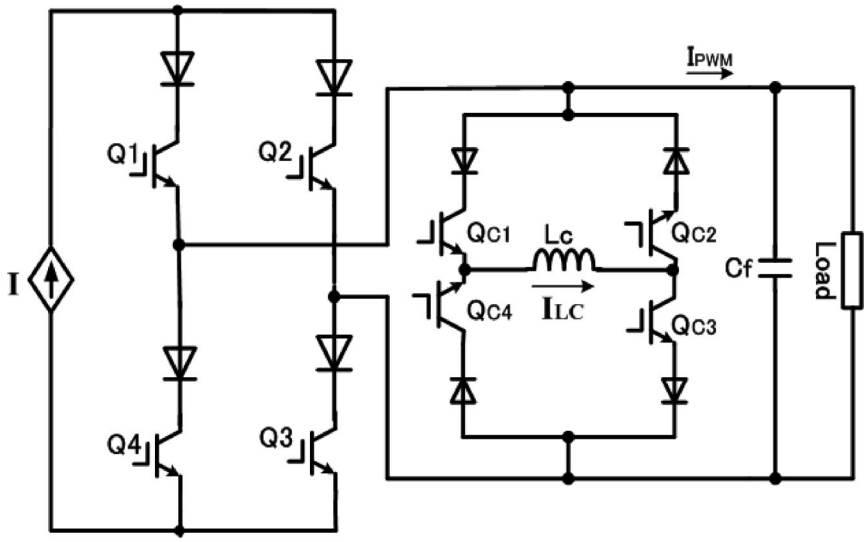

Fig. 4. Proposed five-level CSI.

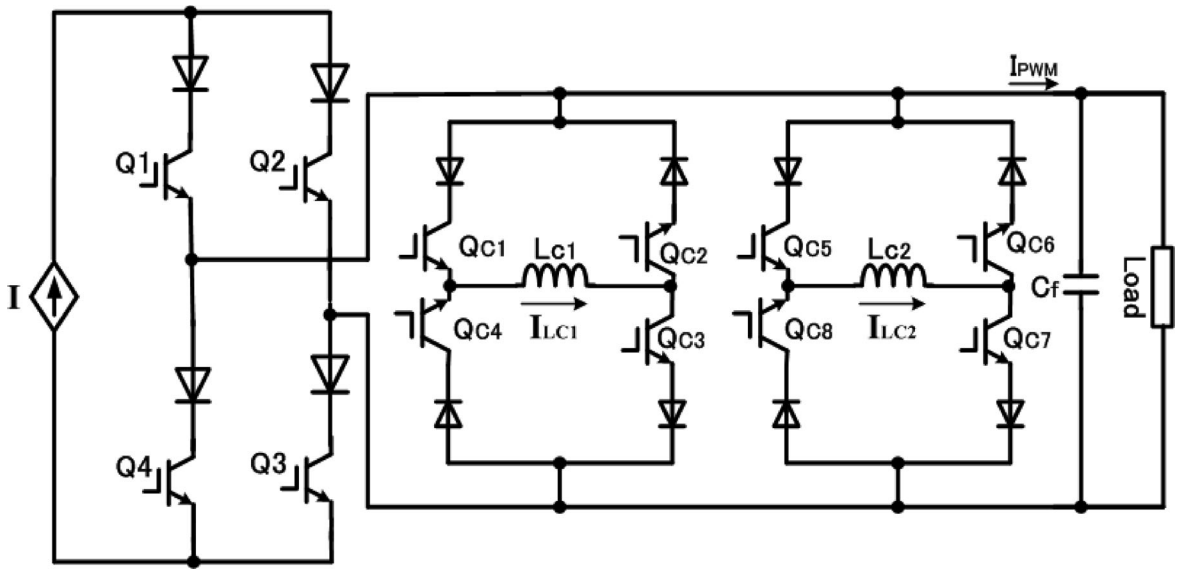

Fig. 5. Proposed nine-level CSI.

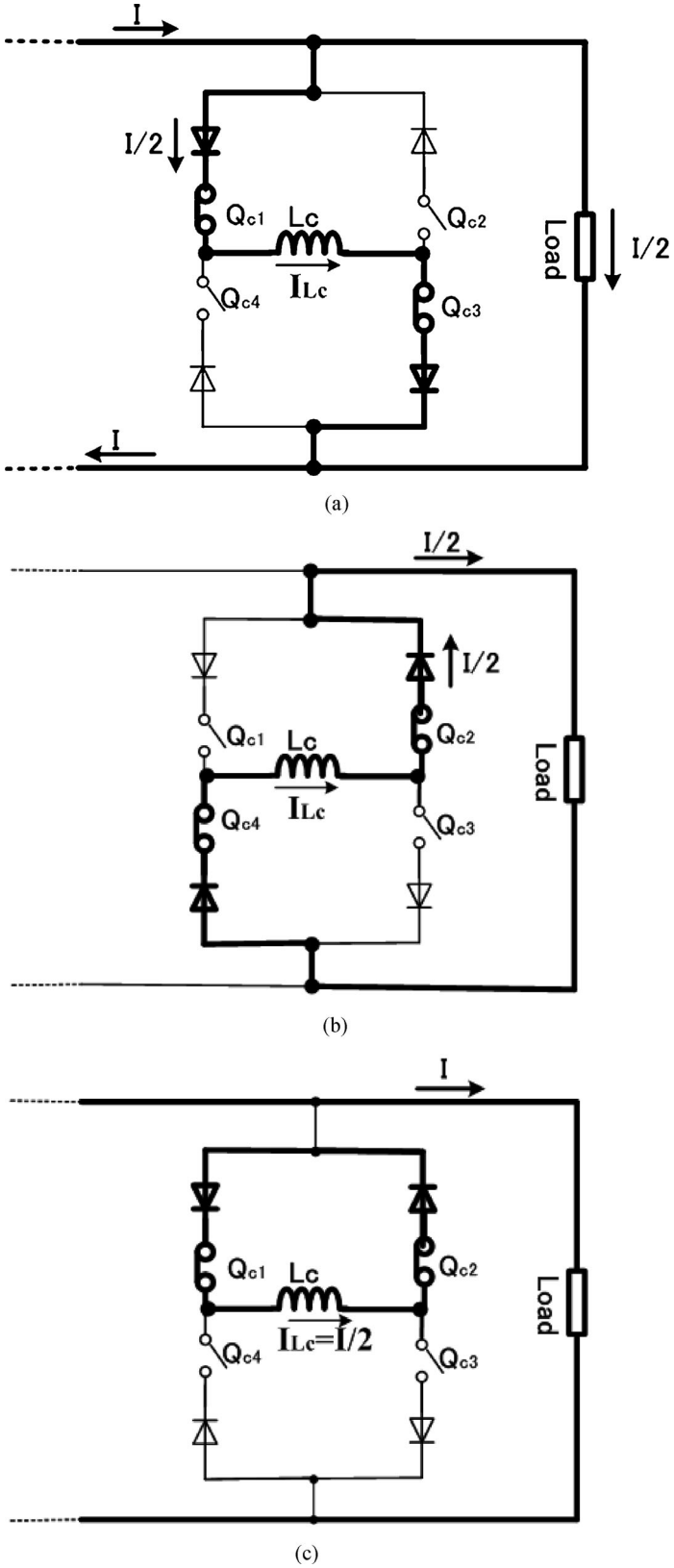

Fig. 6. Operation modes of inductor cell. (a) Charging mode of inductor cell. (b) Discharging mode of inductor cell. (c) Circulating current mode of inductor cell.

chopper works as a regulated dc-current source. Fig. 7 shows the five-level CSI configuration with the chopper-based dc-current source. The power source ($V_{\rm in}$) may be batteries system, photovoltaic (PV) modules, a fuel cell, or a rectifier.

A simple proportional-integral (PI) regulator is applied to control the dc current flowing through the smoothing inductor, which determines the amplitude of the pulsewidth modulation (PWM) output-current waveform $I_{\rm PWM}$ simultaneously. Making the smoothing inductor current follows the reference current is an objective of this current regulator. The switching gate signals of the chopper switch (Q_c) is generated by comparing the error signal of the detected inductor current in the steady state and a triangular waveform after passing through the PI regulator.

C. PWM Technique and Inductor Cell Control

In order to achieve a lower distortion of the output-current waveform, a PWM technique is applied. In this paper, a level-shifted multicarrier-based sinusoidal PWM technique is employed to generate gate signals for the CSI power switches and to obtain the PWM current waveforms [18], [19]. A schematic control diagram, including the current controller of the chopper and the inductor cell for the five-level CSI, is shown in Fig. 8.

The control circuit of the inductor cell functions to control the operation modes, i.e., the charging, the discharging, and the circulating modes, of the inductor cell L_c. The current flowing through the inductor cell I_{L_c} is kept constant. It generates the intermediate-level currents based on the output-current waveform of the H-bridge CSI. A PI regulator is applied to zero the error between the detected current flowing through the inductor cell and the reference current to obtain stable and balanced intermediate-level currents. The amplitude of the inductor cell current is half of the dc input current I_{L_i}. The output of the PI regulator is modulated by a triangular carrier to generate the control signal i[0], determining the operation mode of the inductor cell. In case of the nine-level CSI, the control circuit of the second inductor cell is similar to the first inductor cell mentioned earlier. The difference is only the reference value of the second inductor cell current $I_{L_{c2}}$, which is quarter of the dc input current. Therefore, for an M-level CSI, if the dc-current source is assumed to have amplitude I, the current flowing through the Nth inductor cell I_{L_c} is as expressed in (2).

During the maximum and zero levels of the output-current generation, there is only circulating current mode, no charging and no discharging operation modes in the inductor cell, as listed in Table I. The frequency of the triangular carrier waveform determines the switching frequency of the inductor cell's power switches, which also regulates the charging and the discharging modes of the inductor cell. The discharging mode means that the inductor cell injects power to the load, and during the charging mode, the main H-bridge inverter injects power to the load.

In case of a resistive load, the inductor cell value can be found as

$$L_c = \frac{I_{L_c} R}{f_s \Delta I_{L_c}} \tag{3}$$

where I_{L_c} is the inductor cell current (in amperes), R is a load resistance (in ohms), *fs* is a switching frequency of the inductor

TABLE I
SWITCH STATES OF FIVE-LEVEL CSI

Q_1	Q_2	Q_3	Q_4	Q_{c1}	Q_{c2}	Q_{c3}	Q_{c4}	**Output**	**Operation Mode of Inductor-Cell**
1	0	1	0	1	1	0	0	+I	circulating mode
1	0	1	0	0	0	1	1	+I	circulating mode
1	0	1	0	1	0	1	0	+I/2	charging of inductor-cell
1	0	0	1	0	1	0	1	+I/2	discharging of inductor-cell
1	0	0	1	1	1	0	0	0	circulating mode
1	0	0	1	0	0	1	1	0	circulating mode
0	1	0	1	0	1	0	1	-I/2	charging of inductor-cell
0	1	1	0	1	0	1	0	-I/2	discharging of inductor-cell
0	1	0	1	0	0	1	1	-I	circulating mode
0	1	0	1	1	1	0	0	-I	circulating mode

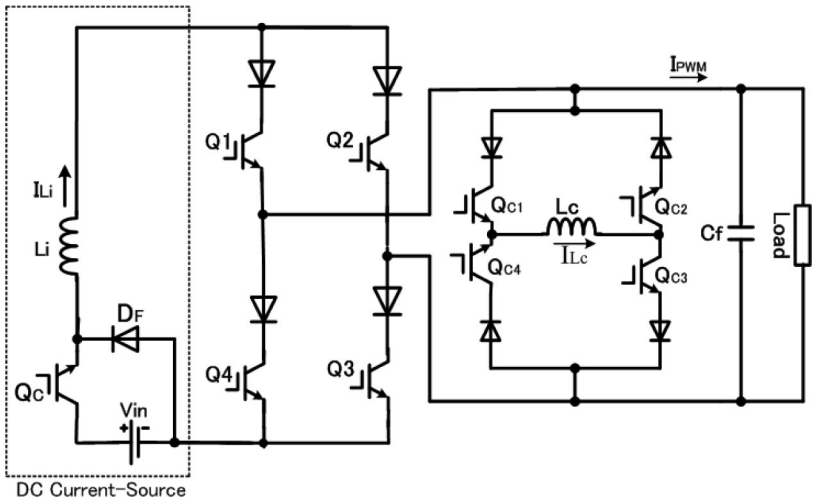

Fig. 7. Proposed five-level CSI with chopper based dc-current source.

cell circuit (in hertz), and ΔI_{L_c} is an acceptable current ripple of the inductor cell current (in amperes). The higher the switching frequency is, the higher is the frequency of the charging and discharging of the inductor cell, which results in the smaller ripple of the inductor cell current, and even a smaller size of the inductor cell can be used.

D. Filter Capacitor

It is necessary to connect a capacitor across the load, because the inverter works as a current source and the load usually has an inductive component. The capacitor also functions to filter the harmonic components, e.g., switching harmonic components, of the PWM multilevel output current [17]. The harmonic components of the PWM current will flow through the filter capacitor C_f. In general, using a higher switching frequency with its constraints, and using the higher level number of the output current, a smaller size of filter capacitor can be achieved. A proper choice of the filter capacitor is also important to minimize the heat in the filter, such as capacitors having small equivalent series resistance (ESR).

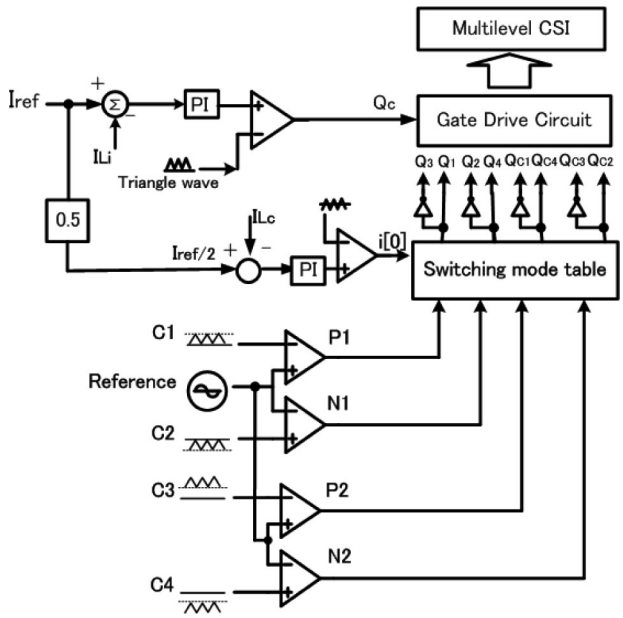

Fig. 8. Control diagram of proposed five-level CSI.

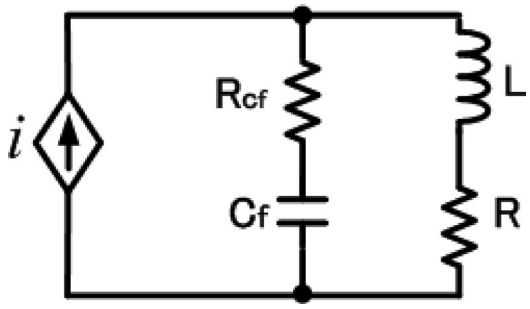

Fig. 9. Simplified model of CSI, filter capacitor, and load.

TABLE II
TEST PARAMETERS

Smoothing inductor (Li) and inductor-cell (Lc)	1 mH and 5 mH
Power source voltage (Vin)	160 V
Inverter switching frequency	22 kHz
Filter capacitor Cf	5 μF
Load	R = 8 Ω, L =1.2 mH
Output current frequency	60 Hz

Fig. 9 shows a circuit model of the CSI (i) connected with a filter capacitor (C_f) with its internal resistance (RC_f), and the load, which is a series connection of a resistor R and an inductor L. For this circuit, the resonance frequency (ω_0) is expressed as

$$\omega_0 = \frac{1}{\sqrt{LC_f}} \left[\frac{R^2 C_f - L}{R_{cf}^2 C_f - L} \right]^{1/2}. \quad (4)$$

Therefore, the capacitor value that satisfies (4) should be avoided to prevent such resonance in the circuit. In addition, as in dual property with the VSI, because the inverter behaves as a current source, a capacitive load should be connected. Hence, the total impedance connected to the CSI including the filter capacitor should be a capacitive. It is another consideration in choosing the value of the filter capacitor.

III. SIMULATION RESULTS

In order to examine the proper operation of the proposed multilevel CSI topology, a five-level and a nine-level CSI configurations, as shown in Figs. 4 and 5 with chopper-based dc-current source, were tested by using computer simulation with a PSIM software. The test parameters are listed in Table II. Fig. 10 shows a computer simulation result of the proposed five-level CSI, where the five-level current, load current, the current flowing through the filter capacitor, the dc input current, and the inductor cell current waveforms are presented. Fig. 11 shows some transient waveforms in the start-up of the proposed five-level CSI, i.e., a five-level PWM current, a load current, a dc input current, and an inductor cell current with the same circuit parameters, as defined in Table II. An excellent transient characteristic of the chopper and the inductor cell controllers can be confirmed, as shown Fig. 11. The inductor cell current has been driven to the balanced condition of 50% of the 8-A dc input current. Fig. 12 shows another computer simulation

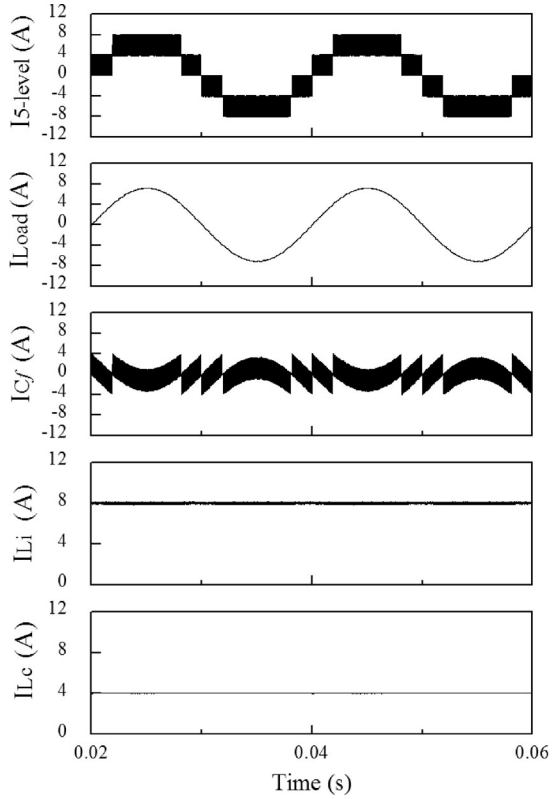

Fig. 10. Simulation result of the proposed five-level CSI representing five-level current ($I_{5\text{-level}}$), load current (I_{Load}), filter-capacitor current (I_{C_f}), dc input current (I_{L_i}), and inductor cell current (I_{L_c}) waveforms.

result of the proposed nine-level CSI representing the nine-level current, the load current, the dc input current, and the first and the second inductor cell current waveforms. The amplitudes of the first and the second inductor cell currents are 50% and 25% of the 8-A dc input current, respectively. In the proposed multilevel CSI, the voltage stress of the power switches is given by the maximum filter-capacitor voltage, which is determined by the amplitude of the multilevel current waveform and the load. It remains the same for all level number of the multilevel CSI. If we give attention to the current rating of the inductor cell's power switches, the more inductor cell are connected, the lower current rating of the power switches is required.

IV. EXPERIMENTAL TEST RESULTS

In order to verify and prove feasibility of the proposed multilevel CSI configuration experimentally, a laboratory prototype of the five-level CSI was set up with IXFK90N30 power MOSFETs in series with DSEI120-06 A fast-recovery diodes. The implemented circuit specifications are identical with the computer simulation parameters listed in Table II. The control circuits were designed with mixed-signal electronics using analog op-amps and EPROMs. The opto-isolator-based gate-drive circuits are used in the prototype. A film filter capacitor is used across the load to obtain a good filter performance.

Fig. 13 shows some experimental waveforms of the five-level CSI, i.e., an 8-A, 60-Hz five-level PWM output current, a load

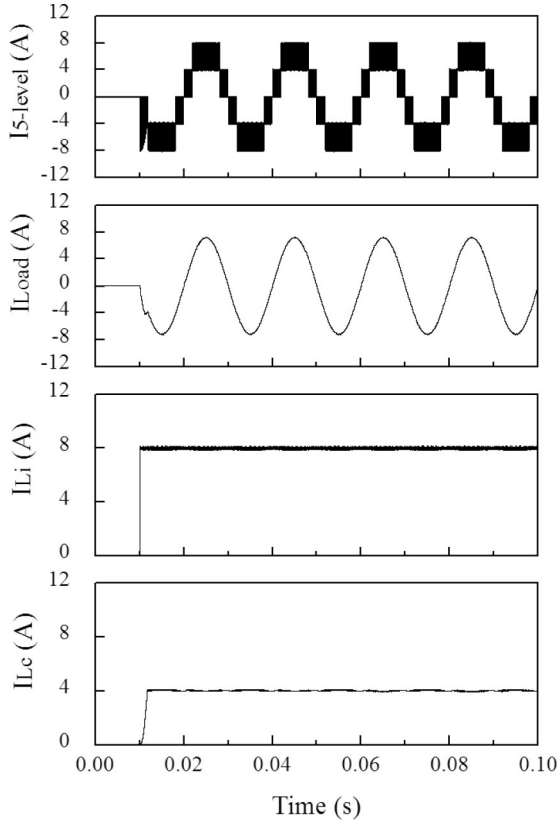

Fig. 11. Simulation result of transient waveforms in start-up of five-level CSI.

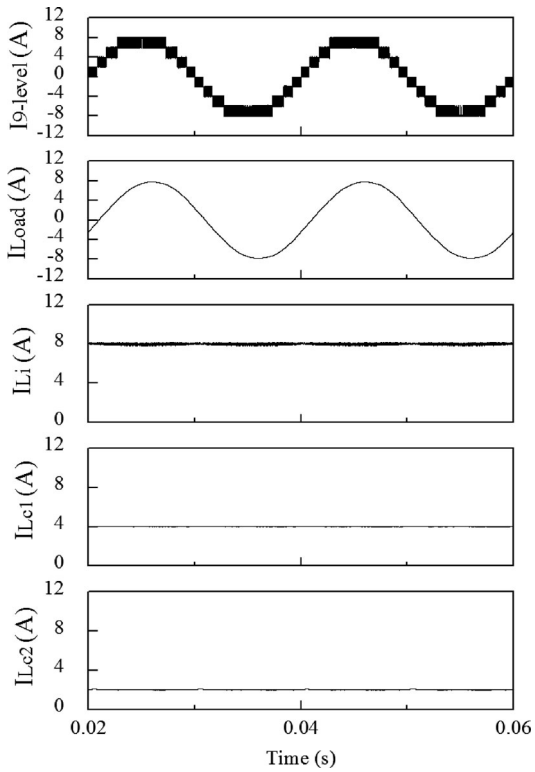

Fig. 12. Simulation result of the proposed nine-level CSI showing nine-level current ($I_{9\text{-level}}$), load current (I_{Load}), dc input current (I_{L_i}), and the first and second inductor cell current ($I_{L_{C1}}$ and $I_{L_{C2}}$) waveforms.

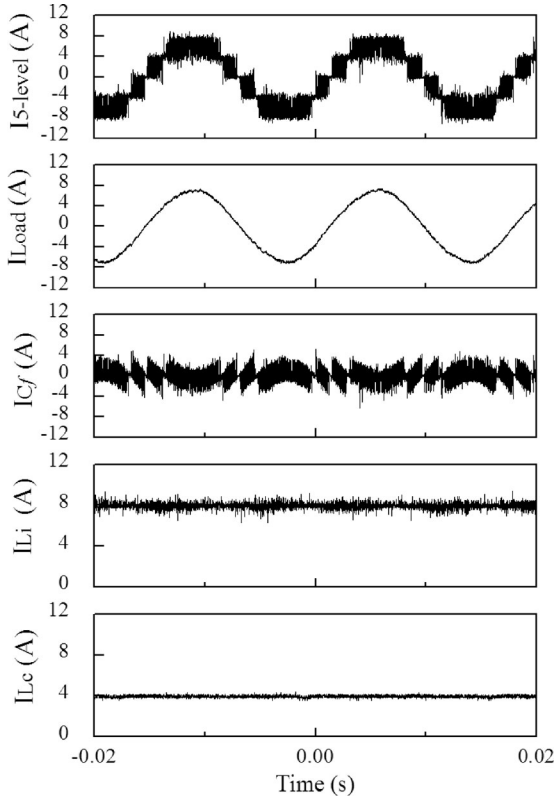

Fig. 13. Experimental test result of the five-level CSI showing five-level PWM current ($I_{5\text{-level}}$), load current (I_{Load}), filter-capacitor current (I_{C_f}), dc input current (I_{L_i}), and inductor cell current (I_{L_c}) waveforms at modulation index 0.9.

current, a filter-capacitor current, a smoothing inductor current, and an inductor cell current waveforms when the modulation index is 0.9. In addition, a sinusoidal load current waveform is obtained after filtering by a small 5-μF filter capacitor, and the inductor cell current is properly regulated at a half value of the 8-A dc input current. Fig. 14 shows a close-up of the five-level, the load current, and the filter-capacitor current waveforms, where the intermediate-level currents and the PWM patterns are clearly visible. The inverter worked properly by generating a five-level PWM output-current waveform. Fig. 15(a) shows a frequency-analysis result of the five-level PWM output-current waveform presenting the harmonics profile, including the 22-kHz switching harmonic component and its sidebands, which are normalized with respect to the fundamental component. Fig. 15(b) shows the low-frequency harmonic components up to 40th order of five-level PWM output current. The measured THD value of the five-level PWM current waveform is 2.93%. Fig. 16 shows another experimental test results of the five-level CSI at modulation index 0.8 with THD value of the five-level PWM current 2.74%. Fig. 17 shows an experimental result of the start-up transient for the five-level CSI, presenting an excellent performance of the proposed five-level CSI. All of the experimental result waveforms agree very well with those of the computer simulation results, which verify feasibility of the proposed multilevel CSI configuration.

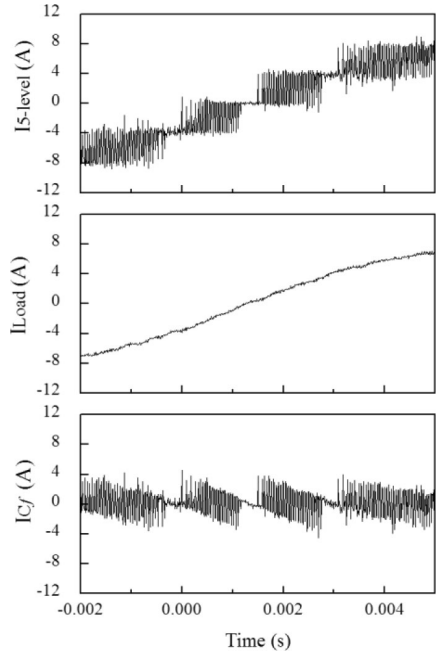

Fig. 14. Close-up of five-level PWM current, load current, and filter-capacitor current waveforms.

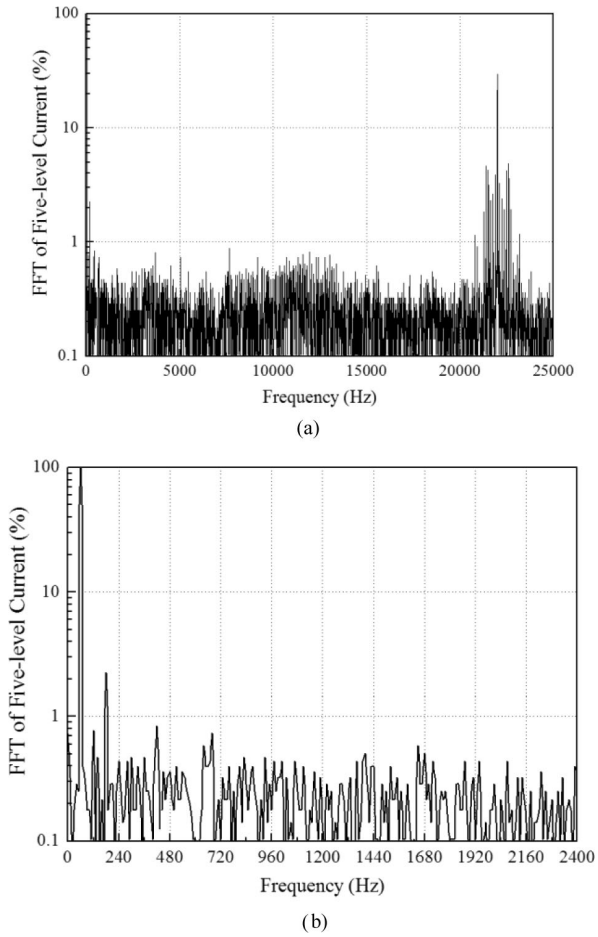

Fig. 15. Frequency spectrum of five-level PWM output current. (a) Fast Fourier transform (FFT) analysis result of five-level PWM current with frequency up to 25 kHz. (b) FFT analysis result of five-level PWM current with frequency up to 2400 Hz.

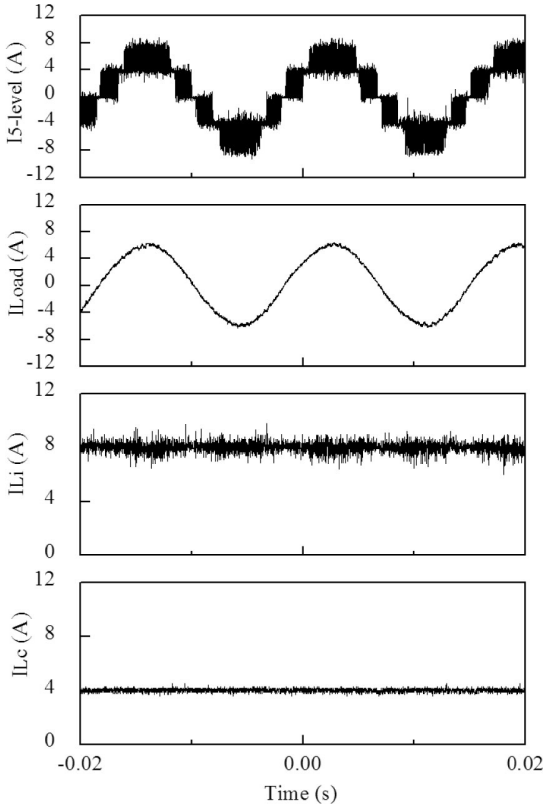

Fig. 16. Experimental test result of the five-level CSI at modulation index 0.8 representing five-level PWM current ($I_{5\text{-level}}$), load current (I_{Load}), dc input current (I_{L_i}), and inductor cell current (I_{L_c}) waveforms.

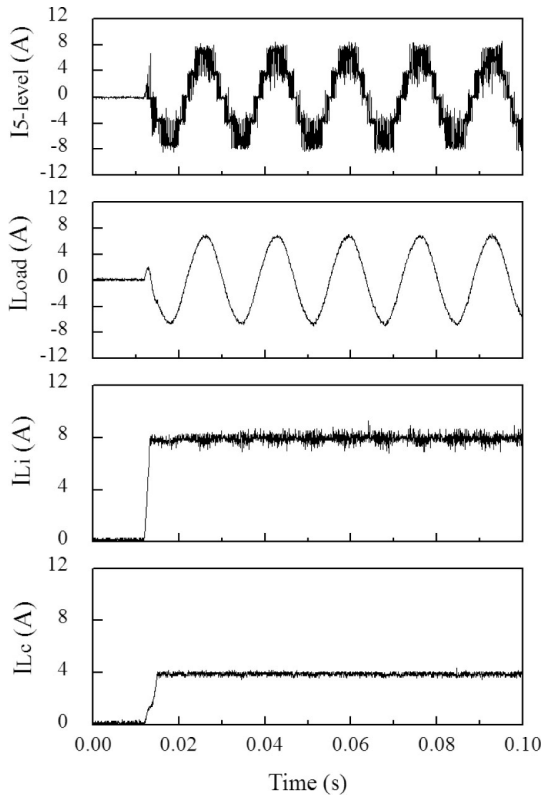

Fig. 17. Experimental result waveforms of start-up transient for five-level CSI.

V. Conclusion

In this paper, a new configuration of multilevel CSI, which employs inductor cells as auxiliary circuit, has been proposed. The inductor cells are connected in parallel with the main H-bridge CSI to generate multilevel output-current waveforms without additional external dc-power sources. The following are some advantages that can be obtained using the proposed multilevel CSI topology compared with other topologies.

1) Compared with the conventional two-level power converter, the proposed multilevel CSI can generate multilevel output-current waveform with less distortion by connecting a single or more inductor cells across the H-bridge CSI. It results in a smaller di/dt produced by the circuit. Furthermore, a smaller size of the output capacitor filter can be used to filter the harmonic components of the output current.
2) In conventional parallel multilevel CSI topology, it needs many isolated dc-current sources with its complex, bulky, and costly isolation transformers and inductors. Using the proposed multilevel CSI, multilevel output waveform can be synthesized using only a single dc-power source without any additional dc-power sources.
3) The control circuit of the intermediate-level current is simple, resulting in small size of the inductors. In conventional multilevel CSI, especially multicell multilevel CSI topology and single-rating inductor multilevel CSI, they need bulky intermediate inductors with their control complexity to generate intermediate-level currents.

The validity of the proposed topology has been verified through both computer simulations and experimental tests. Future works include an application of the proposed multilevel CSI for a grid-connected interactive system, and the development of the multiphase inverter circuit configuration.

References

[1] J. Rodiguez, J. S. Lai, and F. Z. Peng, "Multilevel inverter: A survey of topologies, controls, and application," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] S. D. Freeland, "Techniques for the practical application of duality to power circuits," *IEEE Trans. Power Electron.*, vol. 7, no. 2, pp. 374–384, Apr. 1992.

[3] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 655–664, Mar./Apr. 2005.

[4] C. Klumpner and F. Blaajerg, "Using reverse blocking IGBTs in power converters for adjustable-speed drives," *IEEE Trans. Ind. Appl.*, vol. 42, no. 3, pp. 807–816, May/Jun. 2006.

[5] C. Liu, D. Xu, and L. Jun, "Three-phase current-source buck type PFC converter with reverse-blocking IGBTs," in *Proc. Power Electron. Spec. Conf.*, 2007, pp. 1331–1335.

[6] Y. Xue, L. Chang, S. B. Kjaer, J. Bordonau, and T. Shimizu, "Topologies of single phase inverter for small distributed power generators: An overview," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1305–1314, Sep. 2004.

[7] R. T. H. Li, H. S. Chung, and T. K. M. Chan, "An active modulation technique for single-phase grid connected CSI," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1373–1380, Jul. 2007.

[8] P. G. Barbosa, H. A. C. Braga, M. C. Barbosa, and E. C. Teixeria, "Boost current multilevel inverter and its application on single phase grid connected photovoltaic system," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1116–1124, Jul. 2006.

[9] Z. H. Bai and Z. C. Zhang, "Conformation of multilevel current source converter topologies using the duality principle," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2260–2267, Sep. 2008.

[10] S. Kwak and H. A. Toliyat, "Multilevel converter topology using two types of current-source inverters," *IEEE Trans. Ind. Appl.*, vol. 42, no. 6, pp. 1558–1564, Nov./Dec. 2006.

[11] D. Xu, N. R. Zargari, B. Wu, J. Wiseman, B. Yuwen, and S. Rizzo, "A medium voltage AC drive with parallel current source inverters for high power application," in *Proc. IEEE PESC*, 2005, pp. 2277–2283.

[12] F. L. M. Antunes, A. C. Braga, and I. Barbi, "Application of a generalized current multilevel cell to current source inverters," *IEEE Trans. Power Electron.*, vol. 46, no. 1, pp. 31–38, Feb. 1999.

[13] J. Y. Bao, D. G. Holmes, Z. H. Bai, Z. C. Zhang, and D. H. Xu, "PWM control of a 5-level single-phase current-source inverter with controlled intermediate DC link current," in *Proc. IEEE PESC*, 2006, pp. 1633–1638.

[14] B. P. McGrath and D. G. Holmes, "Natural current balancing of multicell current source inverter," *IEEE Trans. Power Electron.*, vol. 23, pp. 1239–1246, May 2008.

[15] T. Noguchi and Suroso, "New topologies of multi-level power converter for use of next-generation ultra high speed switching devices," in *Proc. Energy Convers. Congr. Expo*, 2009, pp. 1968–1975.

[16] Suroso and T. Noguchi, "New generalized multilevel current-source PWM inverter with no isolated switching devices," in *Proc. IEEE PEDS*, 2009, pp. 314–319.

[17] A. Beig and V. T. Ranganathan, "A novel CSI-fed induction motor drive," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1073–1082, Jul. 2006.

[18] B. Wu, *High Power Converters and AC Drives*. Piscataway, NJ: IEEE Press, 2006, ch. 10.

[19] G. Ledwich, "Current source inverter modulation," *IEEE Trans. Power Electron.*, vol. 6, no. 4, pp. 618–623, Oct. 1991.

Suroso received the B.Eng. degree in electrical engineering from Gadjah Mada University, Jogjakarta, Indonesia, in 2001, and the M.Eng. degree in electrical and electronics engineering from Nagaoka University of Technology, Nagaoka, Japan, in 2008, where he is currently working toward the Ph.D. degree from the Department of Energy and Environment Engineering.

From 2005 to 2006, he was a Research Student in the Department of Electrical Engineering, Tokyo University, Tokyo, Japan. He is currently a Lecturer in the Department of Electrical Engineering, University of Jenderal Soedirman, Purwokerto, Indonesia. He is a Visiting Researcher in the Department of Electrical and Electronics Engineering, Shizuoka University, Shizuoka, Japan. His research interest includes static power converters, especially multilevel power converter, and its application in renewable energy and distributed power generation.

Toshihiko Noguchi (M'95–SM'02) was born in 1959. He received the B.Eng. degree in electrical engineering from Nagoya Institute of Technology, Nagoya, Japan, in 1982, and the M.Eng. and D.Eng. degrees in electrical and electronics systems engineering from Nagaoka University of Technology, Nagaoka, Japan, in 1986, 1996, respectively.

In 1982, he was at Toshiba Corporation, Tokyo, Japan. From 1991 to 1993, he was a Lecturer at Gifu National College of Technology, Gifu, Japan. From 1994 to 1995, he was a Research Associate in electrical and electronics systems engineering at Nagaoka University of Technology, where he was an Associate Professor from 1996 to 2009. Since 2009, he has been a Professor in the Department of Electrical and Electronic Engineering, Shizuoka University, Shizuoka, Japan. His current research interests include static power converters and motor drives.

Dr. Noguchi is a member of the Institute of Electrical Engineers Japan.