

New Efficient Bridgeless Cuk Rectifiers for PFC Applications

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Abstract—Three new bridgeless single-phase ac–dc power factor correction (PFC) rectifiers based on Cuk topology are proposed. The absence of an input diode bridge and the presence of only two semiconductor switches in the current flowing path during each interval of the switching cycle result in less conduction losses and an improved thermal management compared to the conventional Cuk PFC rectifier. The proposed topologies are designed to work in discontinuous conduction mode (DCM) to achieve almost a unity power factor and low total harmonic distortion of the input current. The DCM operation gives additional advantages such as zero-current turn-ON in the power switches, zero-current turn-OFF in the output diode, and simple control circuitry. Performance comparisons between the proposed and conventional Cuk PFC rectifiers are performed based on circuit simulations. Experimental results for a 150 W/48 V_{dc} at 100 V_{rms} line voltage to evaluate the performance of the proposed bridgeless PFC rectifiers are provided.

Index Terms—Bridgeless rectifier, Cuk converter, low conduction losses, power factor correction (PFC), rectifier, single-ended primary-inductance converter (SEPIC) converter, total harmonic distortion (THD).

I. INTRODUCTION

POWER supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards, such as the IEC 61000-3-2. Most of the PFC rectifiers utilize a boost converter at their front end. However, a conventional PFC scheme has lower efficiency due to significant losses in the diode bridge. A conventional PFC Cuk rectifier is shown in Fig. 1; the current flows through two rectifier bridge diodes and the power switch (Q) during the switch ON-time, and through two rectifier bridge diodes and the output diode (D_o) during the switch OFF-time. Thus, during each switching cycle, the current flows through three power semiconductor devices. As a result, a significant conduction loss, caused by the forward voltage drop across the bridge diode, would degrade the converter's efficiency, especially at a low line input voltage.

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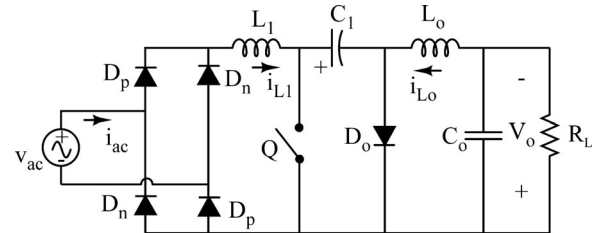


Fig. 1. Conventional Cuk PFC rectifier.

In an effort to maximize the power supply efficiency, considerable research efforts have been directed toward designing bridgeless PFC circuits, where the number of semiconductors generating losses is reduced by essentially eliminating the full-bridge input diode rectifier. A bridgeless PFC rectifier allows the current to flow through a minimum number of switching devices compared to the conventional PFC rectifier. Accordingly, the converter conduction losses can be significantly reduced and higher efficiency can be obtained, as well as cost savings. Recently, several bridgeless PFC rectifiers have been introduced to improve the rectifier power density and/or reduce noise emissions via soft-switching techniques or coupled magnetic topologies [1]–[9].

On the other hand, the bridgeless boost rectifier [10]–[17] has the same major practical drawbacks as the conventional boost converter such as the dc output voltage is higher than the peak input voltage, lack of galvanic isolation, and high start-up inrush currents. Therefore, for low-output voltage applications, such as telecommunication or computer industry, an additional converter or an isolation transformer is required to step-down the voltage.

To overcome these drawbacks, several bridgeless topologies, which are suitable for step-up/step-down applications have been recently introduced in [18]–[21]. However, the proposed topology in [18] still suffers from having three semiconductors in the current conduction path during each switching cycle. In [19]–[22], a bridgeless PFC rectifier based on the single-ended primary-inductance converter (SEPIC) topology is presented. Similar to the boost converter, the SEPIC converter has the disadvantage of discontinuous output current resulting in a relatively high output ripple. A bridgeless buck PFC rectifier was recently proposed in [23], [24] for step-down applications. However, the input line current cannot follow the input voltage around the zero crossings of the input line voltage; besides, the output to input voltage ratio is limited to half. Also, buck PFC converter results in an increased total harmonic distortion (THD) and a reduced power factor [25].

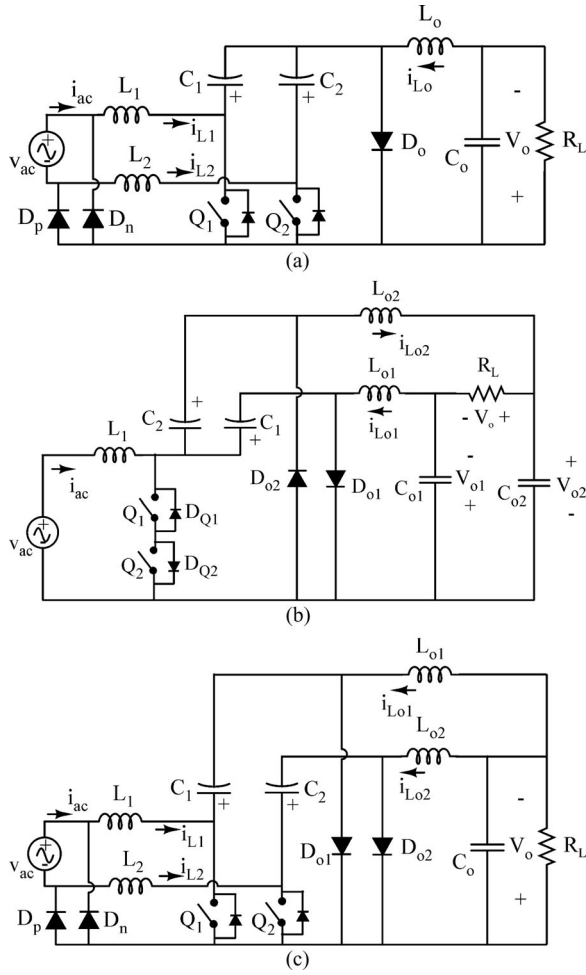


Fig. 2. Proposed bridgeless Cuk PFC rectifiers. (a) Type 1. (b) Type 2. (c) Type 3.

The Cuk converter offers several advantages in PFC applications, such as easy implementation of transformer isolation, natural protection against inrush current occurring at start-up or overload current, lower input current ripple, and less electromagnetic interference (EMI) associated with the discontinuous conduction mode (DCM) topology [26], [27]. Unlike the SEPIC converter, the Cuk converter has both continuous input and output currents with a low current ripple. Thus, for applications, which require a low current ripple at the input and output ports of the converter, the Cuk converter seems to be a potential candidate in the basic converter topologies.

In this paper, three topologies of bridgeless Cuk PFC rectifiers are proposed. The proposed rectifiers are compared based on efficiency, components count, harmonics, gain capability, and driver circuit.

II. PROPOSED BRIDGELESS CUK PFC RECTIFIERS

The three proposed bridgeless Cuk PFC rectifiers are shown in Fig. 2. The proposed topologies are formed by connecting two dc-dc Cuk converters, one for each half-line period ($T/2$) of the input voltage. It should be mentioned here that the topology

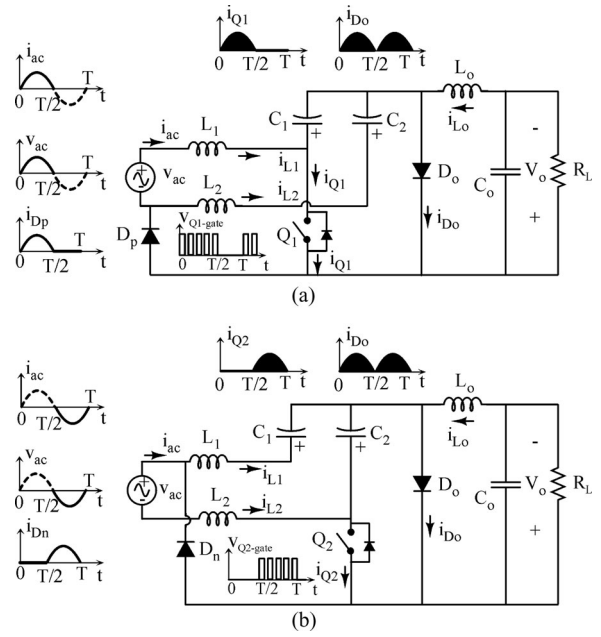


Fig. 3. Equivalent circuits for the type-1 rectifier. (a) During positive half-line period. (b) During negative half-line period of the input voltage.

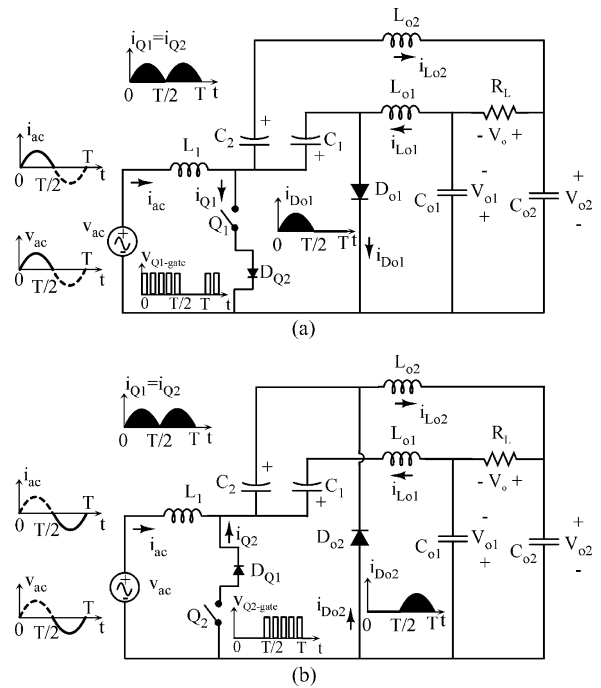


Fig. 4. Equivalent circuits for type-2 rectifier. (a) During positive half-line period. (b) During negative half-line period of the input voltage.

of Fig. 2(a) was listed in [20] as a new converter topology but not analyzed. The operational circuits during the positive and negative half-line period for the proposed bridgeless Cuk rectifiers of Fig. 2(a)–(c) are shown in Figs. 3–5, respectively. Note that by referring to Figs. 3–5, there are one or two semiconductor(s) in the current flowing path; hence, the current stresses in

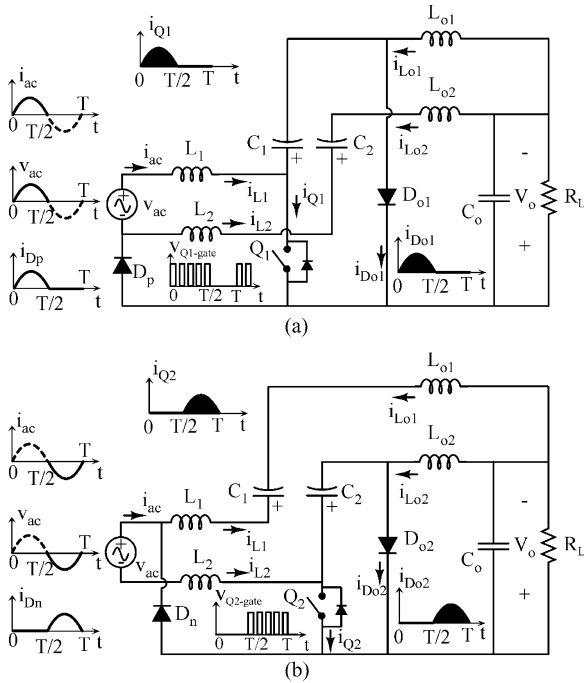


Fig. 5. Equivalent circuits for type-3 rectifier. (a) During positive half-line period. (b) During negative half-line period of the input voltage.

the active and passive switches are further reduced and the circuit efficiency is improved compared to the conventional Cuk rectifier. In addition, Fig. 2(a) and (c) shows that one rail of the output voltage bus is always connected to the input ac line through the slow-recovery diodes D_p and D_n or directly as in the case of the topology of Fig. 2(b). Thus, the proposed topologies do not suffer from the high common-mode EMI noise emission problem and have common-mode EMI performance similar to the conventional PFC topologies. Consequently, the proposed topologies appear to be promising candidates for commercial PFC products.

The proposed bridgeless rectifiers of Fig. 2 utilize two power switches (Q_1 and Q_2). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. Compared to the conventional Cuk topology, the structure of the proposed topologies utilizes one additional inductor, which is often described as a disadvantage in terms of size and cost. However, a better thermal performance can be achieved with the two inductors compared to a single inductor. It should be mentioned here that the three inductors in the proposed topologies can be coupled on the same magnetic core allowing considerable size and cost reduction. Additionally, the “near zero-ripple-current” condition at the input or output port of the rectifier can be achieved without compromising performance.

III. PRINCIPLE OF OPERATION AND THEORETICAL ANALYSIS

A. Principle of Operation

The proposed bridgeless type-3 Cuk rectifier of Fig. 2(c) will be considered in this study. Type 1 is similar to type 3, except for

the output stage stresses. The SEPIC version of type 2 has been analyzed in [19]. The analysis assumes that the converter is operating at a steady state in addition to the following assumptions: pure sinusoidal input voltage, ideal lossless components, and all capacitors are large enough such that their switching voltage ripples are negligible during the switching period T_s . Moreover, the output filter capacitor C_o (C_{o1} and C_{o2} for topology 2) has a large capacitance such that the voltage across it is constant over the entire line period. Referring to Fig. 5(a), during the positive half-line cycle, the first dc–dc Cuk circuit, L_1 – Q_1 – C_1 – L_{o1} – D_{o1} , is active through diode D_p , which connects the input ac source to the output. During the negative half-line cycle, as shown in Fig. 5(b), the second dc–dc Cuk circuit, L_2 – Q_2 – C_2 – L_{o2} – D_{o2} , is active through diode D_n , which connects the input ac source to the output. As a result, the average voltage across capacitor C_1 during the line cycle can be expressed as follows:

$$v_{C_1}(t) = \begin{cases} v_{ac}(t) + V_o, & 0 \leq t \leq \frac{T}{2} \\ V_o, & \frac{T}{2} \leq t \leq T \end{cases} \quad (1)$$

Due to the symmetry of the circuit, it is sufficient to analyze the circuit during the positive half cycle of the input voltage. Moreover, the operation of the proposed rectifiers of Fig. 2 will be described assuming that the three inductors are operating in DCM. By operating the rectifier in DCM, several advantages can be gained. These advantages include natural near-unity power factor, the power switches are turned ON at zero current, and the output diodes (D_{o1} and D_{o2}) are turned OFF at zero current. Thus, the losses due to the turn-ON switching and the reverse recovery of the output diodes are considerably reduced. Conversely, DCM operation significantly increases the conduction losses due to the increased current stress through circuit components. As a result, this leads to one disadvantage of the DCM operation, which limits its use to low-power applications (<300 W) [28].

Similar to the conventional Cuk converter, the circuit operation in DCM can be divided into three distinct operating stages during one switching period T_s . Equivalent circuits over a switching period T_s in the positive half-line period of Fig. 5(a) is shown in Fig. 6. Fig. 7 shows the theoretical DCM waveforms over one switching cycle during the positive half cycle of the input voltage. The topological stages of type 3 over a switching cycle can be briefly described as follows.

Stage 1 [t_0, t_1], [Fig. 6(a)]: This stage starts when the switch Q_1 is turned ON. Diode D_p is forward biased by the inductor current i_{L1} . As a result, the diode D_n is reverse biased by the input voltage. The output diode D_{o1} is reverse biased by the reverse voltage ($v_{ac} + V_o$), while D_{o2} is reverse biased by the output voltage V_o . In this stage, the currents through inductors L_1 and L_{o1} increase linearly with the input voltage, while the current through L_{o2} is zero due to the constant voltage across C_2 . The inductor currents of L_1 and L_{o1} during this stage are given by

$$\frac{di_{L_n}}{dt} = \frac{v_{ac}}{L_n}, \quad n = 1, o1. \quad (2)$$

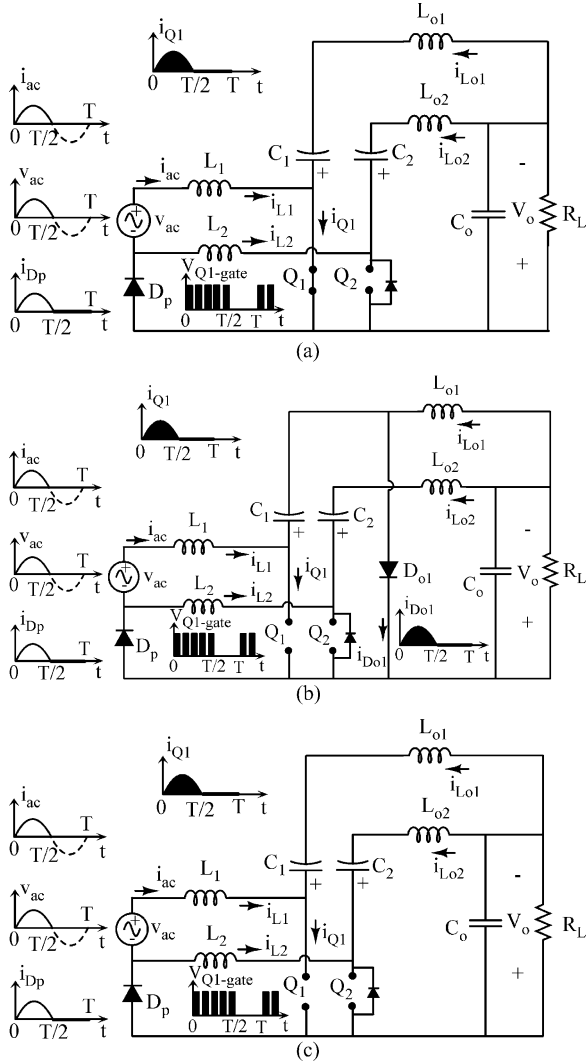


Fig. 6. Topological stages over one switching period T_s for the converter of Fig. 5(a). (a) Switch Q_1 is ON. (b) Switch Q_1 is OFF. (c) DCM.

Accordingly, the peak current through the active switch Q_1 is given by

$$I_{Q1,pk} = \frac{V_m}{L_e} D_1 T_s \quad (3)$$

where V_m is the peak amplitude of the input voltage v_{ac} , D_1 is the switch duty cycle, and L_e is the parallel combination of inductors L_1 and L_{o1} .

Stage 2 [t_1, t_2] [Fig. 6(b)]: This stage starts when the switch Q_1 is turned OFF and the diode D_{o1} is turned ON simultaneously providing a path for the inductor currents i_{L1} and $i_{L_{o1}}$. The diode D_p remains conducting to provide a path for i_{L1} . Diode D_{o2} remains reverse biased during this interval. This interval ends when $i_{D_{o1}}$ reaches zero and D_{o1} becomes reverse biased. Note that the diode D_{o1} is switched OFF at zero current. Similarly, the inductor currents of L_1 and L_{o1} during this stage can be represented as follows:

$$\frac{di_{Ln}}{dt} = -\frac{V_o}{L_n}, \quad n = 1, o1. \quad (4)$$

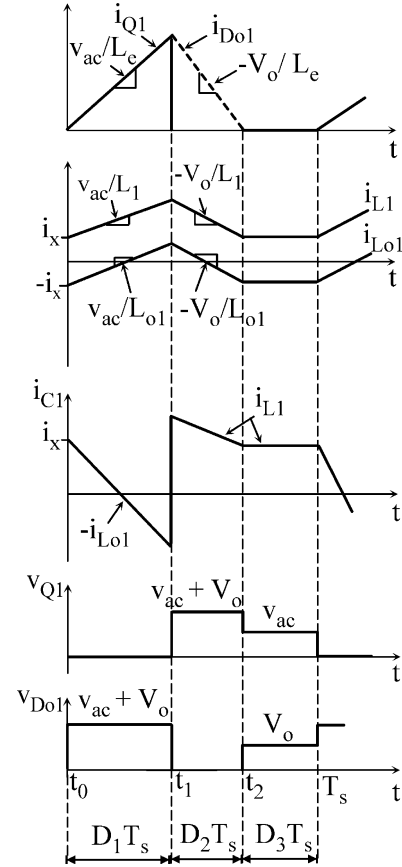


Fig. 7. Theoretical DCM waveforms during one switching period T_s for the converter of Fig. 5(a).

Stage 3 [t_2, t_3] [Fig. 6(c)]: During this interval, only the diode D_p conducts to provide a path for i_{L1} . Accordingly, the inductors in this interval behave as constant current sources. Hence, the voltage across the three inductors is zero. The capacitor C_1 is being charged by the inductor current i_{L1} . This period ends when Q_1 is turned ON.

By applying inductor volt-second across L_1 and L_{o1} , the normalized length of the second stage period can be expressed as follows:

$$D_2 = \frac{D_1}{M} \sin \omega t \quad (5)$$

where ω is the line angular frequency, and M is the voltage conversion ratio ($M = V_o/V_m$).

Since the diode D_p continuously conducts throughout the entire switching period, the average voltage across C_2 is equal to the output voltage V_o . As a result, a negligible ac current will flow through C_2 and L_{o2} . Therefore, the current through L_2 during the positive half cycle of the input voltage is equal to the negative current through the body diode of Q_2 . It should be noted that the body diode of the inactive switch Q_2 is always conducting current during the positive half cycle of the input voltage. This is due to the low impedance of the input inductors (L_1 and L_2) at the line frequency. Therefore, the input diode D_p and body diode of Q_2 appear in parallel configuration to share the return current. A large portion of the return current

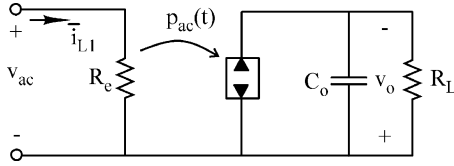


Fig. 8. Large signal model of the topology in Fig. 5.

will pass through the diode that has a lower voltage drop. The efficiency of the converter can be slightly improved by using synchronous rectification to turn ON the switch Q_2 during the positive half cycle of the input voltage, which eliminates its body-diode conduction.

B. Voltage Conversion Ratio M

The voltage conversion ratio M in terms of the converter parameters can be obtained by applying the power balance principle. The average input power can be expressed as follows:

$$\langle P_{in}(t) \rangle_{T/2} = \frac{2}{T} \int_0^{T/2} v_{ac}(t) \langle i_{ac}(t) \rangle_{T_s} dt \quad (6)$$

where the notation $\langle \bullet \rangle_x$ represents the average value over the interval x . Note that the input current in the positive half of the line cycle is the same as the inductor current L_1 . From Fig. 7, it can be shown that the average input current over a switching cycle is given by

$$\langle i_{ac}(t) \rangle_{T_s} = \langle i_{L_1}(t) \rangle_{T_s} = \frac{v_{ac}(t)}{R_e} \quad (7)$$

where the quantity R_e is defined as the emulated input resistance of the converter, and is given by

$$R_e = \frac{2 L_e}{D_1^2 T_s}. \quad (8)$$

Similar to the conventional Cuk PFC rectifier, (7) shows that the input port of the proposed rectifier obeys Ohm's law. Thus, the input current is sinusoidal and in phase with the input voltage. Hence, the power stage circuit of the converter of Fig. 5 can be represented by its large signal averaged model shown in Fig. 8. This model can be implemented in a simulation program to predict the steady state and large signal dynamic characteristics of the real circuit. Furthermore, the averaged model can greatly reduce the long computation time when it is implemented in simulation software.

Evaluating (6) by using (7) and applying the power balance between the input and output ports, the desired voltage conversion ratio is

$$M = \frac{V_o}{V_m} = \sqrt{\frac{R_L}{2R_e}}. \quad (9)$$

It should be noted that the voltage gain in (9) is also valid for the other two proposed topologies. However, the effective inductance (L_e) varies from one topology to another.

C. Boundaries Between Continuous Conduction Mode and DCM

Referring to the diode D_{o1} current waveform in Fig. 7, the DCM operation mode requires that the sum of the switch duty cycle and the normalized switch-OFF time length be less than one, i.e.,

$$D_2 \leq 1 - D_1. \quad (10)$$

Substituting (5) into (10) and using (8) and (9), the following condition for DCM is obtained:

$$K_e < K_{e-crit} = \frac{1}{2(M + \sin(\omega t))^2} \quad (11)$$

where the dimensionless conduction parameter K_e is defined as follows:

$$K_e = \frac{2 L_e}{R_L T_s}. \quad (12)$$

It is clear from (11) that the value of K_{e-crit} depends on the line angle (ωt). Hence, the minimum and maximum values of K_{e-crit} is given by

$$K_{e-crit_min} = \frac{1}{2(M+1)^2} \quad \text{and} \quad K_{e-crit_max} = \frac{1}{2M^2} \quad (13)$$

respectively. Therefore, for values of $K_e < K_{e-crit_min}$, the converter always operates in DCM, and it operates in the continuous conduction mode (CCM) for values of $K_e > K_{e-crit_max}$. However, for values of $K_{e-crit_min} < K_e < K_{e-crit_max}$, the converter operates in both modes: CCM near the peak value of the input line voltage and DCM near the zero crossing of the input line voltage.

D. Capacitor Selection

The energy transfer capacitors C_1 and C_2 are important elements in the proposed Cuk topologies since their values greatly influence the quality of input line current. Capacitors C_1 and C_2 must be chosen such that their steady-state voltages follow the shape of the rectified input ac line voltage waveform plus the output voltage with minimum switching voltage ripple as possible. Also, the values of C_1 and C_2 should not cause low-frequency oscillations with the converter inductors. In a practical design, the energy transfer capacitors C_1 and C_2 are determined based on inductors L_1, L_o values (assuming $L_1 = L_2$ and $L_{o1} = L_{o2} = L_o$) such that the resonant frequency (f_r) during DCM stage is higher than the line frequency (f_i) and well below the switching frequency (f_s). Thus,

$$f_1 < f_r < f_s \quad (14)$$

where

$$f_r = \frac{1}{2\pi\sqrt{C_1(L_1 + L_o)}}. \quad (15)$$

On the other hand, the output capacitor C_o needs to be sufficiently large to store minimum energy required for balancing the difference between the time varying input power and constant load power. The low-frequency peak-peak output voltage

TABLE I
COMPONENTS USED IN SIMULATION

Input inductor(s) L_1 and L_2	1 mH
Output inductor(s) L_{o1} and L_{o2}	22 μ H
Energy transfer capacitor(s) C_1 and C_2	1 μ F
Filter capacitors C_o	12000 μ F
Active switch(es) Q_1 and Q_2	IRFB4332PBF: 250 V, 60 A with $R_{DS-ON} = 29$ m Ω
Output diodes D_o , D_{o1} , and D_{o2} (For Type-1, this type of diode is inserted in series with Q_1 and Q_2)	STTH1003SB: 300 V, 10 A, with $V_F = 0.9$ V
Input diodes D_p and D_n	STTH2R02Q: 200 V, 2 A, with $V_F = 0.7$ V

ripple is given by

$$\Delta v_o = \frac{1}{C_o} \int_{T_L/8}^{3T_L/8} [\bar{i}_{L_{o1}} - I_o] dt \quad (16)$$

where I_o is the output load current, and $\bar{i}_{L_{o1}}$ represent the average output inductor current over one switching cycle and it is given by

$$\bar{i}_{L_{o1}} = \frac{v_{ac}^2}{R_e V_o}. \quad (17)$$

Substituting (17) into (16) and evaluating (16), the capacitor ripple equation is obtained as follows:

$$\Delta v_o = \frac{V_o}{\omega R_L C_o}. \quad (18)$$

IV. COMPARISON STUDY BETWEEN THE PROPOSED AND CONVENTIONAL CUK CONVERTERS

The proposed topologies are compared with respect to their components count, efficiency, driver circuitry complexity, THD, and voltage gain range.

To ensure a fair comparison, the inductance values in all topologies are selected such that $K_e = 0.9 K_{crit}$ at an operating point of an output power of 300 W. Moreover, an equivalent series resistor (ESR) of 20 m Ω and 12 m Ω is placed in series with all the inductors and capacitors, respectively. Furthermore, PSPICE actual semiconductor models have been used to simulate the switches. Table I shows the details of the components used in the simulation. The converters were simulated for an output voltage of 48 V under a minimum nominal input voltage of 120 V_{rms} condition.

The simulated efficiency presented in Fig. 9, includes conduction and switching losses of the semiconductor devices, inductors' copper losses, capacitors' ESR losses, as well as gate drive losses. Table II presents a comparison between topologies of interest. It should be noted that type 2 has the lowest number of semiconductor devices in the current conduction path. However, it has two disadvantages: floating switch and a step-up voltage gain greater than 2. The floating switch requires a more complex driver circuitry and typically causes higher electro-

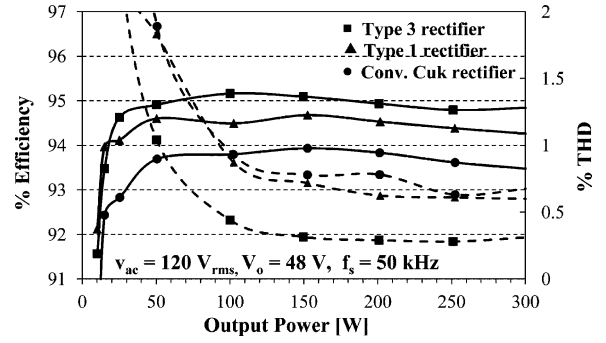


Fig. 9. Simulated efficiency (solid lines) and THD (dashed lines) of conventional PFC Cuk, type-1 rectifier, and type-3 rectifier operating in DCM.

TABLE II
COMPARISON BETWEEN CONVENTIONAL AND BRIDGELESS CUK RECTIFIERS IN DCM MODE

Item	Conv. Cuk	Type-1	Type-2	Type-3
Diode	4 slow + 1 fast	2 slow + 3 fast	2 fast	2 slow + 2 fast
Switch	1	2 (with unidirectional current capabilities)	2	2
Current conduction path when SW on	2 slow diodes and 1 switch	1 slow diode, and 1 switch with series diode	1 body diode and 1 switch	1 slow diode and 1 switch
Current conduction path when SW off	3 diodes (2 slow and 1 fast)	2 diodes (1 slow and 1 fast)	1 fast diode	2 diodes (1 slow and 1 fast)
Current conduction path in DCM	2 slow diodes	1 slow diode	—	1 slow diode
Component count	10	11	11	13
Number of capacitors	2	3	4	3
Equivalent inductance, L_e	$L_1 // L_o$	$L_1 // L_2 // L_o$	$L_1 // L_{o1} // L_{o2}$	$L_1 // L_{o1}$
Minimum conduction parameter, K_{e-crit_min}	$\frac{1}{2(M+1)^2}$	$\frac{1}{2(M+1)^2}$	$\frac{1}{2(M+2)^2}$	$\frac{1}{2(M+1)^2}$
Switch duty-cycle, D_1	$M \times \sqrt{2K_e}$			
Gain range	Step-up/down	Step-up/down	Only step-up ($M > 2$)	Step-up/down
Integrated magnetic core	One core for 2 inductors	One core for 3 inductors	One core for 3 inductors	2 cores for 4 inductors
Driver circuit complexity	1 non-floating	2 non-floating	1 floating + 1 non-floating	2 non-floating

magnetic emissions. The gain range is limited by the blocking voltage of D_{o2} during the positive half cycle of the input line signal similar to the topology discussed in [19]. This disadvantage can be minimized by implementing input/output galvanic isolation; however, components with higher blocking voltage capability are needed. Type 1 also has the advantage of a lower component count, but a higher current peak. Whereas, type 3 has a higher component count, but lower stresses. In conclusion, the converter of choice is an application dependent.

It is evident from Fig. 9 that the efficiency of type-3 topology is higher than that of the conventional PFC Cuk rectifier for the provided output power levels. It should be mentioned here that the discrepancies in efficiencies between type 3 and the conventional Cuk PFC rectifiers become more pronounced as

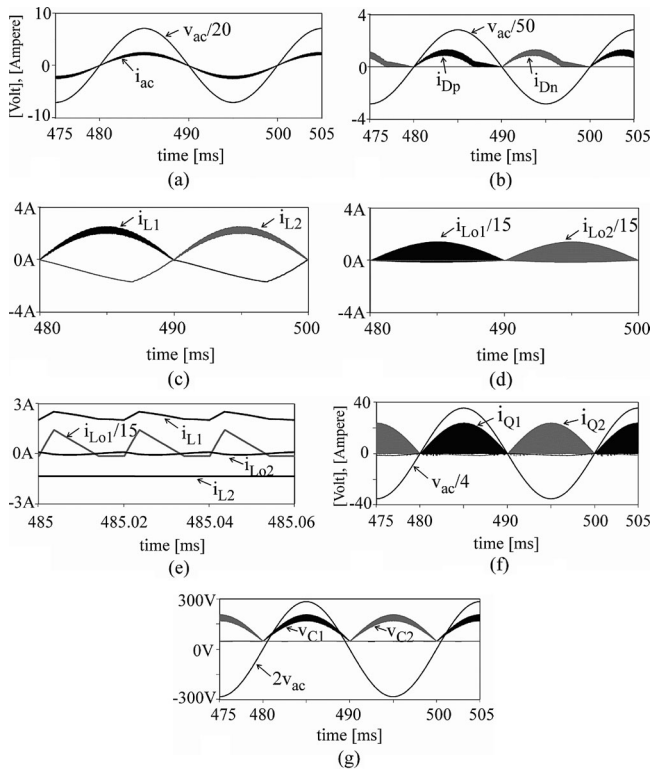


Fig. 10. Simulated waveforms for type-3 rectifier of Fig. 2(c) in DCM. ($v_{ac} = 100 V_{rms}$, $V_o = 48 V$, $P_{out} = 150 W$).

the power level increases. In this case, it is preferred to operate the converter in CCM region instead of DCM. Fig. 9 also shows input current THD as a function of output power. It is evident from Fig. 9 that both the proposed and the conventional Cuk rectifier exhibit extremely low THD ($<1\%$ for $P_{out} > 100 W$) when they are designed to operate in DCM. Note that, by referring to Fig. 9, the THD of the converters under study becomes independent of the output power for a power level greater than 100 W.

V. SIMULATION AND EXPERIMENTAL RESULTS

The type-3 converter of Fig. 2(c) has been simulated using PSPICE for the following input and output data specifications: $v_{ac} = 100 V_{rms}$, $V_o = 48 V$, $P_{out} = 150 W$, and $f_s = 50 kHz$. The circuit components used in the simulation are the same as those in Table I. Fig. 10 shows the simulated voltage and current waveforms at full-load condition. It can be observed from Fig. 10(a) that the input line current is in phase with the input voltage. Fig. 10(b) shows the current through the slow diodes D_p and D_n . Fig. 10(c) shows the inductors' currents waveforms over one line period. Fig. 10(d) shows the simulated output inductor currents over one line period, whereas the switching waveforms of the inductors' currents at peak input voltage are illustrated in Fig. 10(e), which correctly demonstrate the DCM operating mode. The active switches' currents and the intermediate capacitors' voltages waveforms are depicted in Fig. 10(f) and (g), respectively.

A prototype of type-3 converter has been built to validate the theoretical results as well as the simulation previously described. The circuit parameters were all the same as those for the simulation. The input voltage and current are shown in Fig. 11(a). Fig. 11(b) presents the currents through diodes D_p and D_n . Note that the current through D_p enters into DCM before the end of the positive cycle of the line. This occurs because the body diode of Q_2 provides an additional path to the current. Fig. 11(c) illustrates the switching waveforms of the inductors' currents near peak input voltage, which correctly demonstrates the DCM operating mode. Fig. 11(d) shows the voltage across the intermediate capacitors C_1 and C_2 along with the input voltage v_{ac} . It is clear from Fig. 11(d) that (1) is fully fulfilled. Finally, Fig. 11(e) and (f) presents the switches (Q_1 and Q_2) as well as output stage diodes' (D_{o1} and D_{o2}) currents over the line period, respectively. It is evident from Fig. 11(e) and (f) that the switches (Q_1, D_{o1}) and (Q_2, D_{o2}) conduct in alternate half-line cycles, as predicted by the analysis in this study. A very good agreement can be seen between simulation and experimental results. The measured efficiency is about 93.2% at full rated load.

In order to compare the differences between type-1 and type-3 topologies, a prototype of type-1 has also been built and tested with the same specifications and circuit parameters as for type 3. It should be mentioned here that type-1 topology requires two switches with unidirectional current capabilities. Accordingly, a low voltage drop with very low reverse leakage current Schottky barrier diode (type MBR40250 with $V_F = 0.75 V$ at 10 A) is connected in series with the power MOSFETs to prevent any current from flowing through the MOSFET body diode. Fig. 12(a) shows the measured input phase voltage and the input current of the proposed type-1 converter at full load. The low-frequency current envelopes of the three inductors are shown in Fig. 12(b). It is evident that the current envelope of L_1 during positive half line cycle (L_2 during negative half line cycle) follows a perfect sinusoidal envelope. Fig. 12(c) illustrates switching waveforms of the inductors' currents near peak input voltage, which correctly demonstrates the DCM operating mode. Fig. 12(d) illustrates the switching current waveforms of the switch Q_1 and the input diode D_p . Note that the peak switch current fulfills the theoretical predicted results shown in Table II. The low-frequency current envelopes of the three diodes D_p , D_n , and D_o over a few line cycles are depicted in Fig. 12(e). It is evident from Fig. 12(e) that the two input diodes (D_p and D_n) conduct in alternate half line cycles as expected. Likewise, Fig. 12(f) shows the voltage across the intermediate capacitors C_1 and C_2 . It is clear from Fig. 12(f) that during positive half line cycle, v_{C1} closely tracks the positive portion of the input ac voltage (v_{ac}) plus the output voltage (V_o), while the voltage across C_2 remains nearly constant and it is equal to V_o . The measured efficiency for type-1 topology came close to 92% at full rated load. Compared to type 3, the reduction in efficiency in type-1 topology is mainly due to the increased conduction losses introduced by the extra diodes connected in series with Q_1 and Q_2 . It is worth mentioning here that using the newly available reverse-blocking isolated gate bipolar transistor instead of using a power MOSFET with series-connected diode

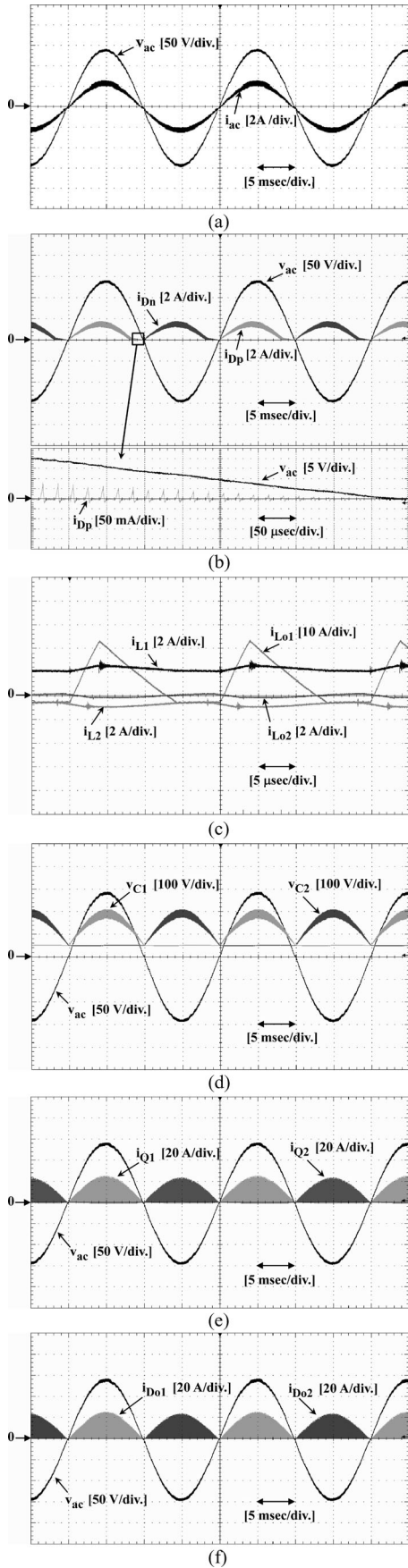


Fig. 11. Experimental waveforms for type-3 rectifier of Fig. 2(c) in DCM. ($v_{ac} = 100 V_{rms}$, $V_o = 48 V$, $P_{out} = 150 W$).

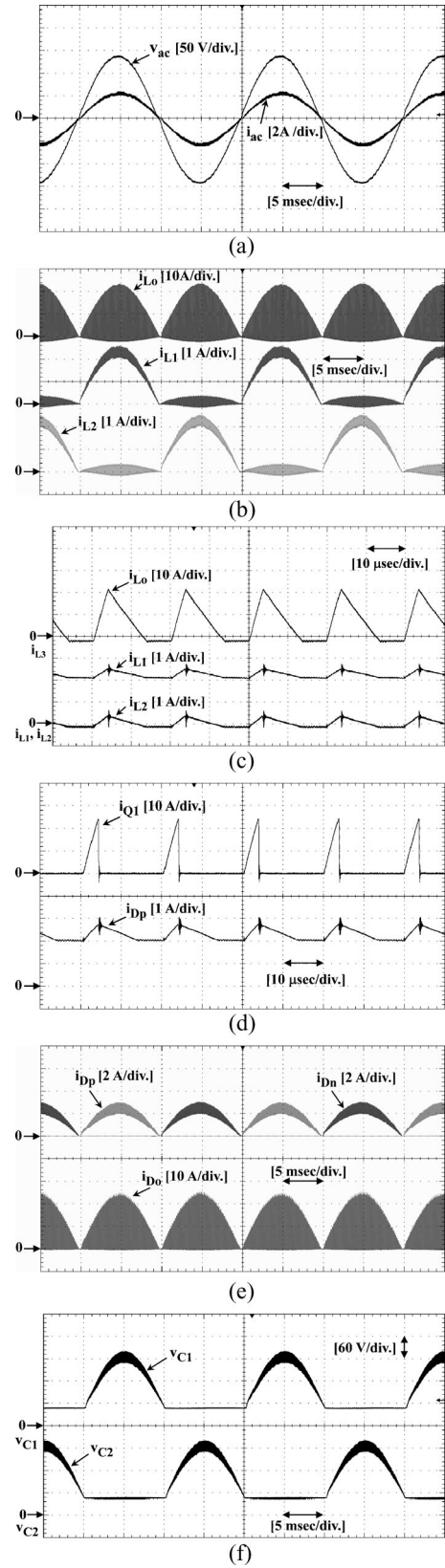


Fig. 12. Experimental waveforms for type-1 rectifier of Fig. 2(a) in DCM. ($v_{ac} = 100 V_{rms}$, $V_o = 48 V$, $P_{out} = 150 W$).

presents very low ON-state characteristics, which lead to low conduction losses in a converter that requires reverse-blocking voltage switches.

Finally, though the input voltage is not a pure sinusoidal waveform and contains about 1% THD, the measured THD of the input line current waveform illustrated in Figs. 11(a) and 12(a) is below 2%.

VI. CONCLUSION

Three single-phase ac–dc bridgeless rectifiers based on Cuk topology are presented and discussed in this paper. The validity and performance of the proposed topologies are verified by simulation and experimental results. Due to the lower conduction and switching losses, the proposed topologies can further improve the conversion efficiency when compared with the conventional Cuk PFC rectifier. Namely, to maintain the same efficiency, the proposed circuits can operate with a higher switching frequency. Thus, additional reduction in the size of the PFC inductor and EMI filter could be achieved. The proposed bridgeless topologies can improve the efficiency by approximately 1.4% compared to the conventional PFC Cuk rectifier. The performance of two types of the proposed topologies was verified on a 150 W experimental prototype. The measured efficiency of the prototype rectifier at 100 V_{rms} line and full load is above 93% with THD below 2%. Experimental results are observed to be in good agreement with simulation results.

REFERENCES

- [1] W. Choi, J. Kwon, E. Kim, J. Lee, and B. Kwon, "Bridgeless boost rectifier with low conduction losses and reduced diode reverse-recovery problems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 769–780, Apr. 2007.
- [2] G. Moschopoulos and P. Kain, "A novel single-phase soft-switched rectifier with unity power factor and minimal component count," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 566–575, Jun. 2004.
- [3] R.-L. Lin and H.-M. Shih, "Piezoelectric transformer based current-source charge-pump power-factor-correction electronic ballast," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1391–1400, May 2008.
- [4] S. Dwari and L. Parsa, "An efficient AC–DC step-up converter for low-voltage energy harvesting," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2188–2199, Aug. 2010.
- [5] Y. Jang and M. Jovanovic, "A bridgeless PFC boost rectifier with optimized magnetic utilization," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 85–93, Jan. 2009.
- [6] L. Huber, Y. Jang, and M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.
- [7] B. Su and Z. Lu, "An interleaved totem-pole boost bridgeless rectifier with reduced reverse-recovery problems for power factor correction," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1406–1415, Jun. 2010.
- [8] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.
- [9] H.-Y. Tsai, T.-H. Hsia, and D. Chen, "A family of zero-voltage-transition bridgeless power-factor-correction circuits with a zero-current-switching auxiliary switch," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1848–1855, May 2011.
- [10] H. Ye, Z. Yang, J. Dai, C. Yan, X. Xin, and J. Ying, "Common mode noise modeling and analysis of dual boost PFC circuit," in *Proc. Int. Telecommun. Energy Conf.*, Sep. 2004, pp. 575–582.
- [11] B. Lu, R. Brown, and M. Soldano, "Bridgeless PFC implementation using one cycle control technique," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2005, pp. 812–817.
- [12] P. Kong, S. Wang, and F. C. Lee, "Common mode EMI noise suppression for bridgeless PFC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 291–297, Jan. 2008.
- [13] W.-Y. Choi, J.-M. Kwon, E.-H. Kim, J.-J. Lee, and B.-H. Kwon, "Bridgeless boost rectifier with low conduction losses and reduced diode reverse-recovery problems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 769–780, Apr. 2007.
- [14] C.-M. Wang, "A novel single-stage high-power-factor electronic ballast with symmetrical half-bridge topology," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 969–972, Feb. 2008.
- [15] B. Su, J. Zhang, and Z. Lu, "Single inductor three-level boost bridgeless PFC rectifier with nature voltage clamp," *IEEE Int. Power Electron. Conf.*, pp. 2092–2097, Jun. 2010.
- [16] M. Mahdavi and H. Farzanehfard, "Zero-current-transition bridgeless PFC without extra voltage and current stress," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2540–2547, Jul. 2009.
- [17] W.-Y. Choi and J.-S. Yoo, "A bridgeless single-stage half-bridge AC/DC converter," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3884–3895, Dec. 2011.
- [18] W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo, "A novel bridgeless buck-boost PFC converter," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 1304–1308.
- [19] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1147–1157, Apr. 2009.
- [20] A. Sabzali, E. H. Ismail, M. Al-Saffar, and A. Fardoun, "New bridgeless DCM sepic and Cuk PFC rectifiers with low conduction and switching losses," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 873–881, Mar./Apr. 2011.
- [21] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.
- [22] M. R. Sahid, A. H. M. Yatim, and T. Taufik, "A new AC-DC converter using bridgeless SEPIC," in *Proc. IEEE Annu. Conf. Ind. Electron. Soc.*, Nov. 2010, pp. 286–290.
- [23] L. Huber, L. Gang, and M. M. Jovanovic, "Design-oriented analysis and performance evaluation of buck PFC front-end," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 85–94, Jan. 2010.
- [24] Y. Jang and M. M. Jovanović, "Bridgeless high-power-factor buck converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011.
- [25] J. M. Alonso, M. A. Dalla Costa, and C. Ordizl, "Integrated buck-flyback converter as a high-power-factor off-line power supply," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1090–110, Mar. 2008.
- [26] M. Brkovic and S. Cuk, "Input current shaper using Cuk converter," in *Proc. Int. Telecommun. Energy Conf.*, 1992, pp. 532–539.
- [27] D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode Sepic and Cuk power factor preregulators: Analysis and design," *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 630–637, Oct. 1997.
- [28] Y.-S. Roh, Y.-J. Moon, J.-C. Gong, and C. Yoo, "Active power factor correction (PFC) circuit with resistor-free zero-current detection," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 630–637, Feb. 2011.



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