On the Limit of the Output Capacitor Reduction in Power-Factor Correctors by Distorting the Line Input Current

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***Abstract*—Active power-factor correctors (PFCs) are needed to design ac–dc power supplies with universal input voltage range and sinusoidal input current. The classical method to control PFCs consists in two feedback loops and an analog multiplier. Hence, the input current is sinusoidal and it is in-phase with the input voltage. However, a bulk capacitor is needed to balance the input and the output power. Due to its high capacitance, an electrolytic capacitor is traditionally used as a bulk capacitor in PFCs. As a consequence, the lifetime of the ac–dc power supply is limited by the electrolytic capacitor's, which becomes insufficient to some applications (e.g., high-brightness LEDs). This paper proposes a reduction of the output voltage ripple (which allows reduction of the output capacitance) by distorting the input current, but maintaining the harmonic continent compatible with EN 61000-3-2 regulations. The limits of this output capacitor reductions are deduced. Also, a control strategy based on a low-cost microcontroller is developed to put the proposed study into practice. Finally, the theoretical results are validated in a 500-W prototype.**

***Index Terms*—Capacitor, harmonic, power factor correction, switched-mode power supplies.**

I. Introduction

In order to limit the harmonic content on the line current of mains-connected equipment, the use of an active power-factor corrector (PFC) as a first stage of the two-stage solution [1]–[6] is almost mandatory. Fig. 1(a) shows a general scheme of an active PFC controlled by two feedback loops, which is the most popular circuitry to control this type of power converters. In Fig. 1, the inner feedback loop is an input-current feedback loop and the outer one is an output-voltage feedback loop. The current loop makes the line current follow a reference signal, in-phase with the input voltage, which is obtained by multiplying a rectified sinusoidal waveform (obtained from the line voltage) by $v_A(t)$. The output voltage of the voltage loop ($v_A(t)$) is a dc voltage due to the low-pass filter placed in the voltage loop in order to obtain a sinusoidal line input current. Therefore, the pulsating input power is a square cosine function. In this case, a storage capacitor with large capacitance is required to balance the instantaneous power difference between the pulsating input power and the constant output power. A large capacitance is needed, and therefore, an electrolytic capacitor is often used as the storage capacitor. However, it is known that due to its liquid electrolyte, the lifetime of electrolytic capacitor is very limited. At this point, the output capacitor can be an obstacle to design an ac–dc power supply for long-lifetime loads, for example, ac–dc drivers for high-brightness LEDs (HB-LEDs) [7]–[12] or long-lifetime power supplies, for example, nonaccessible or remote equipment. Therefore, the power supply manufacturers are looking for reducing this capacitance in order to avoid the use of an electronic capacitor. According to this idea, nowadays, many of them offer lifetime warranty in the range of 5 to 10 years of lifetime.

The objective of this paper is to propose a method to reduce the storage capacitance, thus other capacitor technologies could be adopted instead of electrolytic capacitor to achieve long lifetime [13], [14]. Taking into account the energy transfer process of the PFC defined by its main waveforms [see Fig. 1(b)], if the pulsating output current waveform (which is equal to the pulsating input power) was adequately modified, then the amplitude of the output voltage ripple can be modified. The question is how the pulsating input power can be reduced. A possible solution consists on distorting the line input current. Following this idea, the second section of this paper presents a study that analyzes the tradeoff between the line input current distortion and the output voltage ripple reduction in PFC. However, if the input current is distorted, then the compliance with EN 61000-3-2 regulations is not assured. To solve this problem, the limits of the output ripple reduction compatible with international regulations are presented in the Section III of this paper. A simple control strategy based on a low-cost microcontroller that distorts the input current is presented in the Section IV of this paper. This control strategy allows the output voltage ripple reduction distorting the line input current. Finally, all the theoretical results presented in this paper are validated in a 500-W boost PFC prototype.

II. Reviewing the Static Modeling of PFCs With Fast-Output-Voltage Feedback Loop

The objective of this section is to determinate the evolution of the output voltage ripple when the line input current of the

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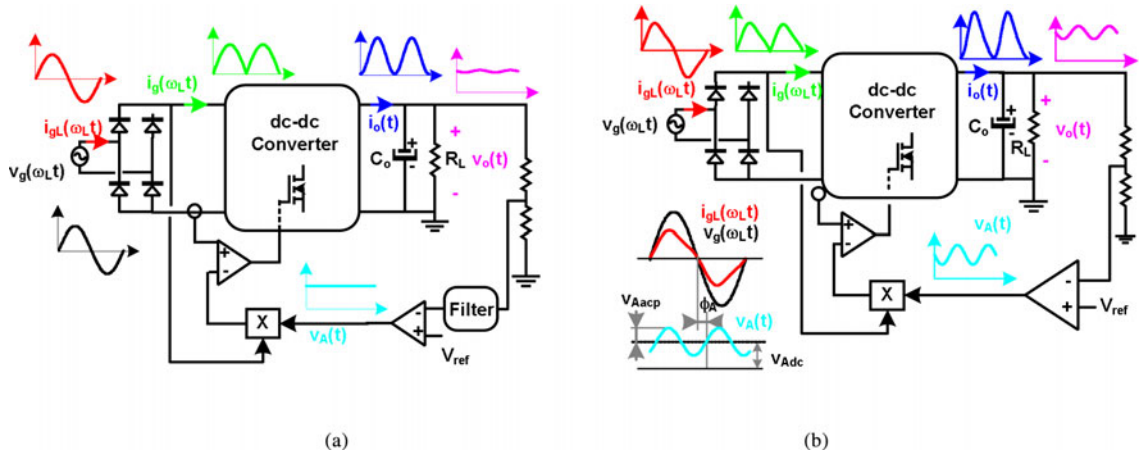

Fig. 1. PFC with (a) slow-output-voltage feedback loop and (b) fast-output-voltage feedback loop.

PFC is distorted. The static model of PFC with fast-output-voltage feedback loop presented in [18] can be useful for this study because it considers distortion in the line input current. This model describes the static behavior of the PFCs when the bandwidth of the output-voltage feedback loop is increased and, therefore, considerable voltage ripple appears in the control signal $v_A(t)$, distorting the input current [see Fig. 1(b)]. In this case, the voltage and the current at the input of the power stage shown in Fig. 1(b) can be written as follows:

$$v_g(\omega_L t) = v_{gp}\,|\sin(\omega_L t)| \tag{1}$$

$$i_g(\omega_L t) = \frac{v_{gp}\,|\sin(\omega_L t)|\,v_A(t)}{K_M} \tag{2}$$

where v_{gp} is the peak value of $v_g(\omega_L t)$, ω_L is the line angular frequency, $v_A(t)$ is the output voltage of the error amplifier, and K_M is a constant.

The voltage $v_A(t)$ can be rewritten as follows [see Fig. 1(b)]:

$$v_A(t) = v_{A\mathrm{dc}} + v_{A\mathrm{ac}}(t) \tag{3}$$

$$v_{A\mathrm{ac}}(t) = v_{A\mathrm{acp}}\sin(2\omega_L t - \phi_L) \tag{4}$$

where $v_{A\mathrm{dc}}$ is the dc component of $v_A(t)$, $v_{A\mathrm{ac}}(t)$ is its ac component, $v_{A\mathrm{acp}}$ is the peak value of $v_{A\mathrm{ac}}(t)$, and ϕ_L is its phase-lag angle. It should be noted that we have assumed that $v_A(t)$ only has an ac component of twice the line frequency because the rest of possible harmonics are strongly attenuated by the bulk capacitor C_B.

The pulsating input power $p_g(\omega_L t)$ can be obtained by multiplying the values of $v_g(\omega_L t)$ and $i_g(\omega_L t)$ obtained from (1) and (2)

$$p_g(\omega_L t) = v_g(\omega_L t) i_g(\omega_L t) \tag{5}$$

$$p_g(\omega_L t) = \frac{v_{gp}^2 v_{A\mathrm{dc}}}{K_M}\sin^2(\omega_L t)\cdot(1 + k\sin(2\omega_L t - \phi_L)) \tag{6}$$

where $k = v_{A\mathrm{acp}}/v_{A\mathrm{dc}}$ is the relative ripple of v_A. The pulsating output power [the power delivered by the power stage in Fig. 1(b)] can be obtained by multiplying the output voltage v_o by the current $i_o(t)$ injected by the power stage into the output cell made up of the bulk capacitor C_B and the load R_L

$$p_{oi}(\omega_L t) = v_o i_o(\omega_L t). \tag{7}$$

After establishing the balance between $p_g(\omega_L t)$ and $p_{oi}(\omega_L t)$, we obtain (i.e.,: $p_g(\omega_L t) = p_{oi}(\omega_L t)$)

$$i_o(\omega_L t) = \frac{v_{gp}^2 v_{A\mathrm{dc}}}{v_o K_M}\sin^2(\omega_L t)(1 + k\sin(2\omega_L t - \varphi_L)). \tag{8}$$

The average value of $p_g(\omega_L t)$ in half a line cycle will be as follows:

$$p_{g\mathrm{av}} = \frac{\omega_L}{\pi}\int_0^{\frac{\pi}{\omega_L}} p_g(\omega_L t)dt = \frac{v_{gp}^2 v_{A\mathrm{dc}}}{4K_M}(2 + k\sin\phi_L). \tag{9}$$

From (2)–(4) and (9), the value of the input line current $i_g(\omega_L t)$ will be as follows:

$$i_{gL}(\omega_L t) = \frac{4v_o^2}{v_{gp}R_L(2 + k\sin\phi_L)} \times \left[\sin(\omega_L t) + \frac{k}{2}\cos(\omega_L t - \phi_L) + \frac{k}{2}\cos(3\omega_L t - \phi_L)\right]. \tag{10}$$

Taking into account (2)–(5) and (9), the pulsating input power $p_g(t)$ will be as follows:

$$p_g(\omega_L t) = \frac{v_o^2}{R_L} + \frac{2v_o^2}{R_L(2 + k\sin\phi_L)} \times \left[k\sin(2\omega_L t - \phi_L) - \cos(2\omega_L t) - \frac{k}{2}\sin(4\omega_L t - \phi_L)\right]. \tag{11}$$

The harmonic content of $i_o(\omega_L t)$ is easily obtained from (7), (11), and the balance between input and output power, by applying basic trigonometric relationships

$$i_{o\mathrm{dc}} = \frac{v_o}{R_L} \tag{12}$$

$$i_{o2}(\omega_L t) = \frac{2v_o\left[k\sin(2\omega_L t - \phi_L) - \cos(2\omega_L t)\right]}{R_L(2 + k\sin\phi_L)} \tag{13}$$

$$i_{o4}(\omega_L t) = \frac{-v_o k}{R_L(2 + k\sin\phi_L)}\sin(4\omega_L t - \phi_L) \tag{14}$$

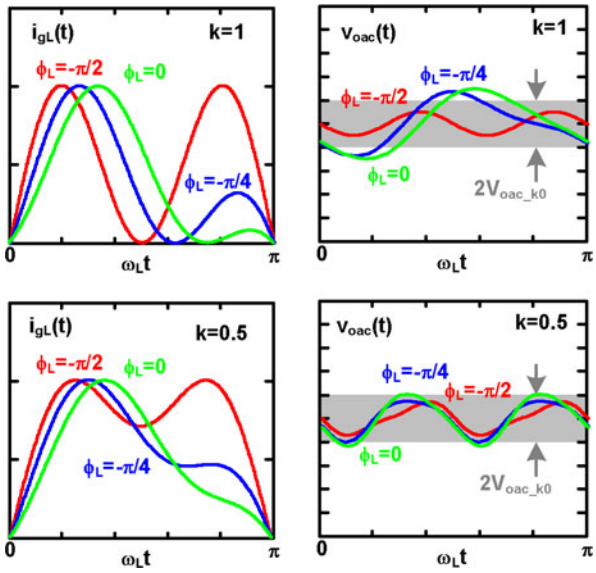

Fig. 2. Line current (left) and output voltage ripple (right) for the same output power and different values of k and ϕ_L.

where $i_{odc}, i_{o2}(\omega_L t)$, and $i_{o4}(\omega_L t)$ are the dc component, the second and the fourth harmonic of $i_o(\omega_L t)$, respectively.

The value of the output voltage ripple can be calculated by multiplying the value of $i_{o2}(\omega_L t)$ and $i_{o4}(\omega_L t)$ by the impedance constituted by C_B and R_L connected in parallel. However, the impedance of C_B at twice and at fourth, the line frequency must be much lower than R_L in order to maintain the output voltage ripple in a reasonable value and, hence, the parallel impedance of C_B and R_L can be approximated by the impedance of C_B. Thus, we obtain from (13) and (14)

$$v_o(t) = v_o + v_{oac}(t) = v_o + \frac{2v_o}{2\omega_L C_B R_L (2 + k\sin\phi_L)} \times \left[-k\cos(2\omega_L t - \phi_L) - \sin(2\omega_L t) + \frac{k}{2}\cos(4\omega_L t - \phi_L)\right]. \quad (15)$$

The expression of the output voltage ripple without distorting the input current (i.e., $k = 0$) can be easily calculated as follows:

$$v_{oac\_k0} = \frac{v_o}{2\omega_L C_B R_L}. \quad (16)$$

Fig. 2 shows the line current waveforms normalized at its peak value and the output voltage ripple compared to v_{oac_k0} (gray area), in both cases for the same output power and different values of k and ϕ_L. As can be seen, the output voltage ripple can be reduced distorting adequately the input current.

III. Limits of the Output Voltage Ripple Reduction and Compliance With EN 61000-3-2 and Energy Star Program Requirements for Solid-State Lighting Regulations

From (15), the peak-to-peak amplitude of the output voltage ripple can be calculated as a function of ϕ_L and k. Also, this amplitude can be normalized to the amplitude of the output voltage ripple of a PFC without distortion in the line current (14)

$$rv_{o\_pp} = \frac{\max\{v_{oac}(t)\} - \min\{v_{oac}(t)\}}{2v_{oac\_k0}}. \quad (17)$$

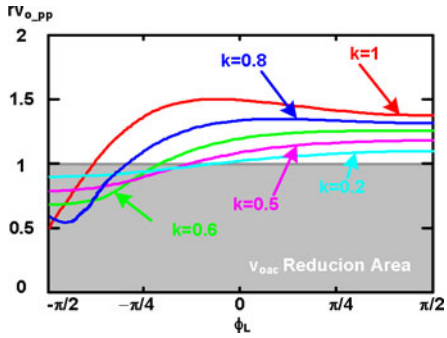

Fig. 3. Normalized peak-to-peak amplitude of the output voltage ripple in PFCs for different values of k and ϕ_L.

Fig. 3 shows rv_{o_pp} for different designs of the PFC with input current distortion. As Fig. 3 shows the reduction of the output voltage ripple (gray area) is obtained for negative ϕ_L values. When ϕ_L is close to –90°, the highest reduction in the output voltage ripple is obtained for a given k value. However, the proposed study is still not finished. This is because the line-current harmonic content corresponding to the values of k and ϕ_L obtained in Fig. 3 have not been checked yet. In fact, this harmonic content should be low enough to guarantee the compliance with EN 61000–3-2 regulations. As it is very well known, any piece of equipment can be classified into four classes according to EN 61000-3-2 regulations [15], [16].

A. Classes A and B

In these classes, the limits of $i_{gL}(t)$ are absolute values. Hence, the PFC will comply with the regulations up to a maximum input power for each class and for each set of values of ϕ_L and k. This maximum power for Classes A and B can be calculated by using (9)

$$\text{Class A}: p_{g\max} = \frac{529(2 + k\sin\phi_L)}{k} \quad (18)$$

$$\text{Class B}: p_{g\max} = \frac{793.5(2 + k\sin\phi_L)}{k}. \quad (19)$$

As an example, Fig. 4(a) shows the area (in gray color) of compliance with regulations in Class A for a 1500-W PFC. Fig. 4(b) shows rv_{o_pp} values that comply with regulations for different designs at the same input power. As can be seen, the maximum output voltage ripple reduction compatible with Class A regulations (i.e., 27.7%) is obtained for $k = 0.525$ and $\phi_L = -\pi/2$. In fact, the maximum output voltage ripple reduction at any output power always occurs at $\phi_L = -\pi/2$. Therefore, the maximum output voltage ripple reduction versus the output power can be easily calculated in Classes A and B (see Fig. 5). As Fig. 5 shows a 50% output voltage ripple reduction can be obtained for output power levels above 600 W in Class A and above 800 W in Class B.

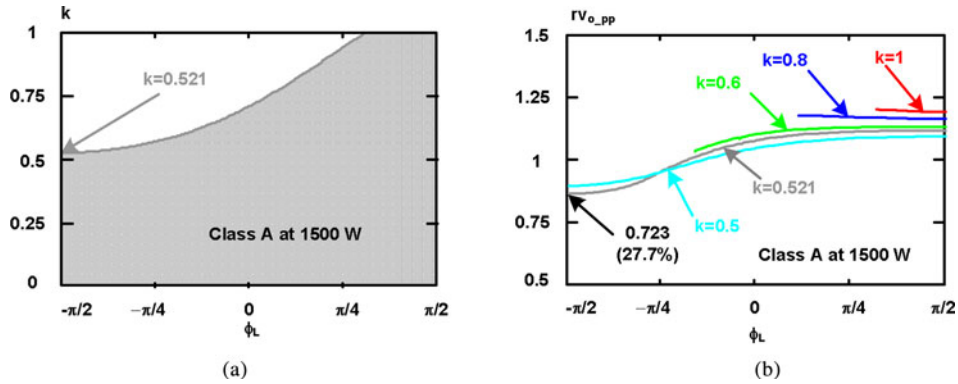

Fig. 4. (a) Combinations of k and ϕ_L for compliance in Class A at 1500 W. (b) rv_{o_pp} compatible with regulations in Class A at 1500 W for different k and ϕ_L values.

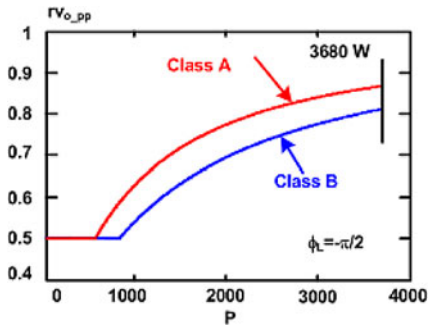

Fig. 5. rv_{o_pp} for $\phi_L = -\pi/2$ compatible with regulations in Classes A and B as a function of the output power.

B. Class C

In this class, the limit imposed on the third harmonic depends on the PF and on the rms value of the first harmonic of the line current. The expression of the inequality that defines the compliance with regulations in this class can be calculated by using (10)

$$0.212 \geq \frac{k\sqrt{2+k^2+2k\sin\phi_L}}{(2+k\sin\phi_L)\sqrt{4+k^2+4k\sin\phi_L}}. \tag{20}$$

This inequality defines the area of compliance shown in Fig. 6(a). As given in Fig. 6, the PFC always complies with the regulations in for Class C equipment if k is lower than 0.448, whereas it never complies with them if k is higher than 0.82. For values of k between 0.448 and 0.82, the compliance depends on the value of ϕ_L. Fig. 6(b) shows rv_{o_pp} values versus k and ϕ_L for PFC designs that comply with Class C regulations. The values of rv_{o_pp} given in Fig. 6(b) shows that reductions of 23.8% can be obtained for PFCs classified in Class C.

C. Class D

In this class of equipment, the limit imposed on each harmonic by the regulations is proportional to the power handled by the PFC. In other words, the quotient between the rms value of any harmonic divided by the input power must be below the limit specified by the regulations. For the third harmonic, this limit is 3.4 mA/W (rms value). Thus, applying this condition, we obtain the expression of compliance with regulations in Class D

$$\frac{\sqrt{2}}{v_{gp}}\frac{k}{(2+k\sin\phi_L)} \leq 3.4\times10^{-3}. \tag{21}$$

This inequality defines the area of compliance plotted in Fig. 7(a). As Fig. 7(a) shows the relative value of the third harmonic is below the limit imposed by EN 61000-3-2 for almost any design condition. In fact, the converter fails to comply with the regulations only if ϕ_L is between –90° and –45° and, at the same time, k is higher than 0.878. Also, Fig. 7(b) shows the rv_{o_pp} values complying with international regulations in Class D versus k and ϕ_L PFC designs. Maximum reductions of 37.8% can be obtained for PFCs classified in this class.

Also, as it is known that the input PF can be an important requirement in commercials products as ac–dc HB-LEDs. In fact, Energy Star program requirements for solid-state lighting (SSL) regulations specify certain PF in order to qualify certain equipment into Category A or B.

D. Energy Star Program Requirements for SSL Luminaries

PF must be higher than 0.9 for ac–dc power supplies of commercial luminaries as [17] specifies. The expression of the inequality that defines the compliance with regulations in this class can be calculated by using (10), too

$$\frac{\sqrt{2}(1+0.5k\sin\phi_L)}{\sqrt{2+k^2+2k\sin\phi_L}} \leq 0.9. \tag{22}$$

In this case, the aforementioned inequality defines the area of compliance plotted in Fig. 8(a). As you can see, all PFCs designs with a k value lower than 0.657 comply with regulations. Also, the maximum output voltage ripple reduction compatible with regulations is 34.3% [see Fig. 8(b)]. Maximum output voltage ripple reduction compatible Energy Star program SSL regulations (i.e., 34.3%) is obtained for $k = 0.653$ and $\phi_L = -\pi/2$.

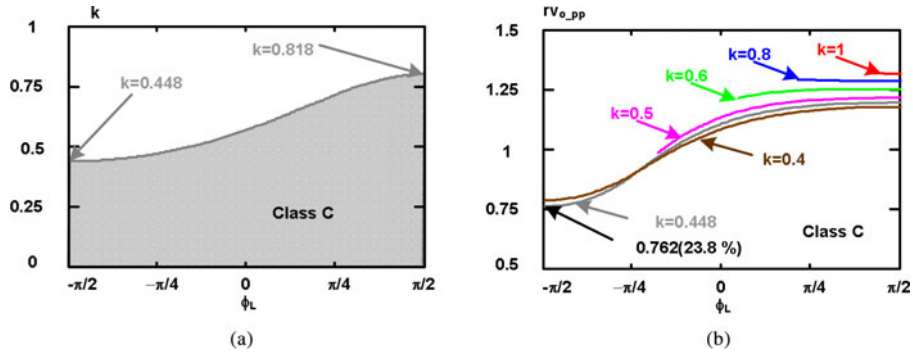

Fig. 6. (a) Area of compliance in Class C. (b) rv_{o_pp} compatible with regulations in Class C for different values of k and ϕ_L.

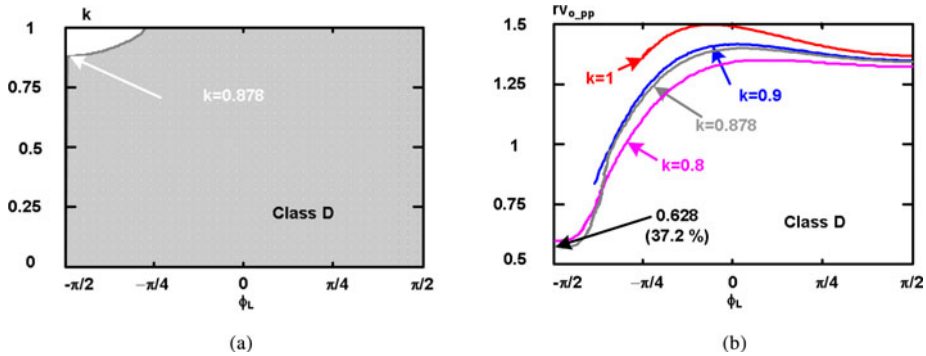

Fig. 7. (a) Area of compliance in Class D. (b) rv_{o_pp} compatible with regulations in Class D for different values of k and ϕ_L.

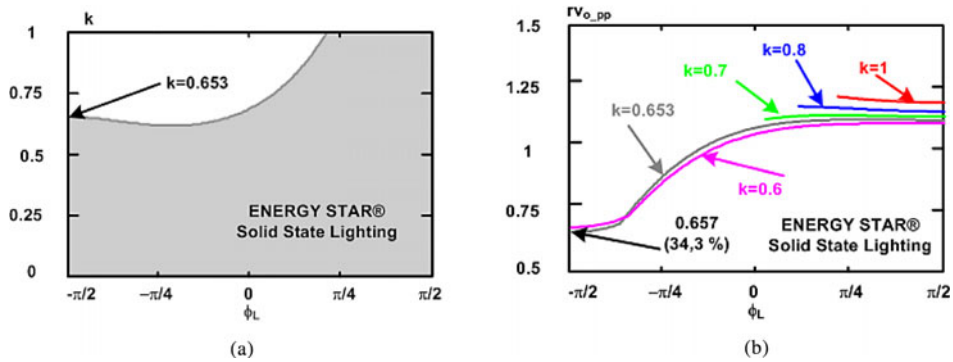

Fig. 8. (a) Area of compliance in Energy Star program requirements for SSL luminaries. (b) rv_{o_pp} compatible with regulations in Class D for different values of k and ϕ_L.

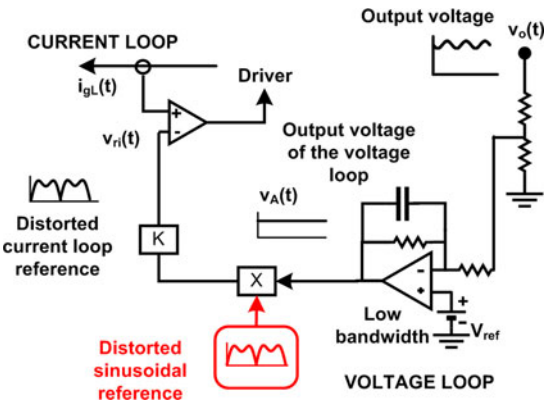

Fig. 9. New control strategy based on a distorted sinusoidal reference in PFC.

IV. Control Strategy Based on a Distorted Sinusoidal Fixed Reference Generated by a Low-Cost Microcontroller

A. Principle of Operation

In order to obtain the highest output voltage ripple reduction, the value of ϕ_L must be –90° and the k value varies with the classification of the piece of equipment [between 0.448 and 1, Figs. 4(b), 6(b), and 7(b)]. The ϕ_L value [which is the phase lag of $v_A(t)$] depends on the bandwidth of the output voltage regulator [18]. However, the standard regulator design of a PFC with fast-output-voltage feedback loop does not allow a ϕ_L value of –90° in $v_A(t)$ (i.e., lead angle of +90°). Therefore, a new control strategy must be adopted to distort adequately

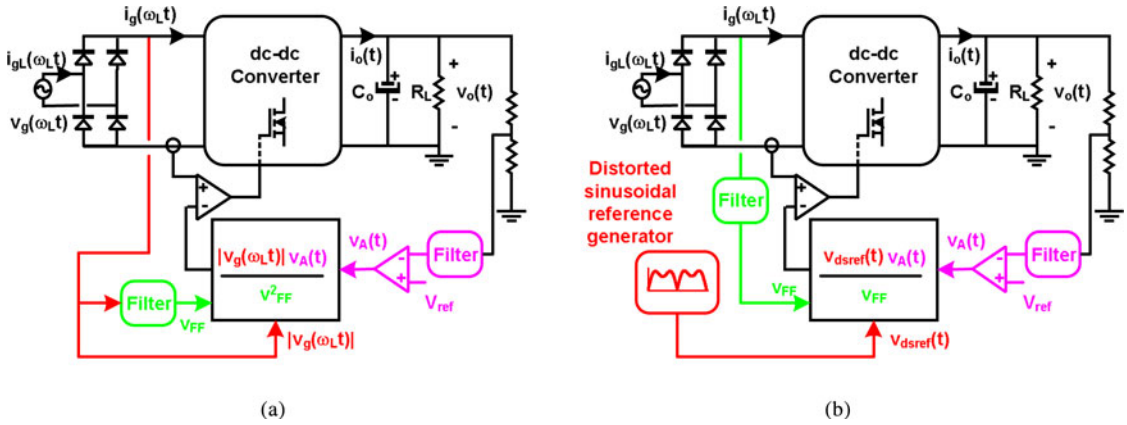

Fig. 10. Line voltage feedforward in PFCs controlled by (a) analog multiplier technique and (b) proposed control strategy.

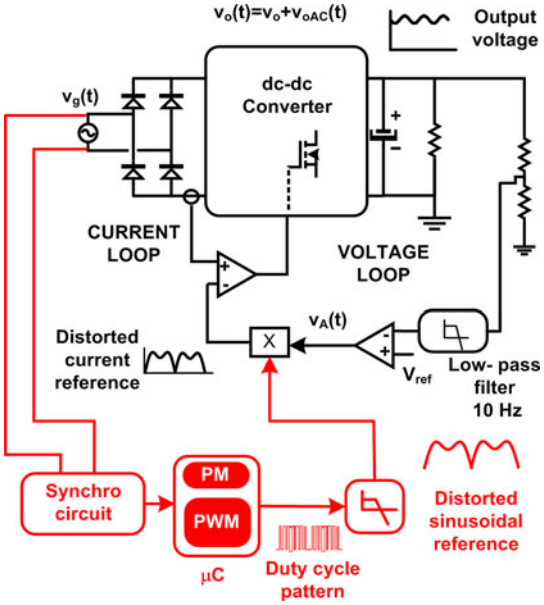

Fig. 11. Control strategy based on a distorted sinusoidal fixed reference generated by a low-cost microcontroller.

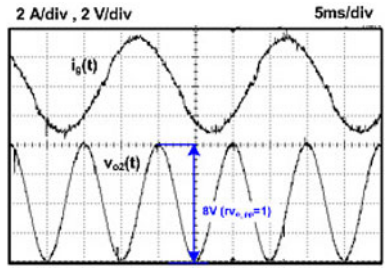

Fig. 12. Input current and the output voltage ripple for a traditional PFC design.

the line current in order to obtain the maximum output voltage ripple reduction.

If a distorted sinusoidal reference is introduced as a fixed pattern in the PFC multiplier [instead of the traditional sinusoidal reference sensed from the rectifier input voltage (see Fig. 9)], then the input current will follow the distorted sinusoidal reference. This distorted reference must be calculated in order to obtain the desired distortion in the input current. Therefore, the maximum possible output voltage reduction can be obtained. In this case, the output voltage of the voltage loop must be a constant value (i.e., $v_A(t) = V_{A\mathrm{dc}}$). Therefore, the classical low-pass filter is placed in the output-voltage feedback loop.

B. Line Voltage Feedforward

Equation (9) shows that the value of $V_{A\mathrm{dc}}$ depends on the square value of V_{gp} for a given average input power. Due to this, the gain of the transfer function between the control (v_A) and the output voltage (V_o) will vary when the line changes. As it is known [2], this problem can be overcome adding an additional loop, which is a feedforward loop [see Fig. 10(a)], allowing this control technique for universal input voltage. In this case, the input current becomes [19]

$$i_g(\omega_L t) = \frac{v_{gp}\,|\sin(\omega_L t)|\,v_A(t)}{K'_M\,v_{\mathrm{FF}}^2} \tag{23}$$

where K'_M is a new constant and v_{FF} is the feedforward voltage, which is the average value of the rectified input voltage (i.e., $V_{FF} = 2V_{gp}/\pi$). Assuming that the feedforward voltage is constant during each half line cycle, now the gain of the transfer function between the control and the output voltage will not vary when the line changes.

In the case of the proposed control strategy, the analysis is quite different. Now the input current expression is as follows:

$$i_g(\omega_L t) = \frac{v_{\mathrm{dsref}}(t)V_{A\mathrm{dc}}}{v_{\mathrm{dsref\_max}}K_{M\,\mathrm{dsref}}} \tag{24}$$

where $K_{M\,\mathrm{dsref}}$ is a new constant, $v_{\mathrm{dsref}}(t)$ is the distorted sinusoidal reference, and $v_{\mathrm{dsref\_max}}$ is the maximum value of the distorted sinusoidal reference. The expression of the distorted sinusoidal reference can be easily calculated

$$V_{\mathrm{dsref}}(\omega_L t) = \sin(\omega_L t)(1 + K\sin(2\omega_L t - \Phi_L)) \tag{25}$$

where now K and Φ_L are constant values in order to obtain the desired shape of the fixed distorted sinusoidal reference to obtain the maximum possible output voltage reduction. By using (24)

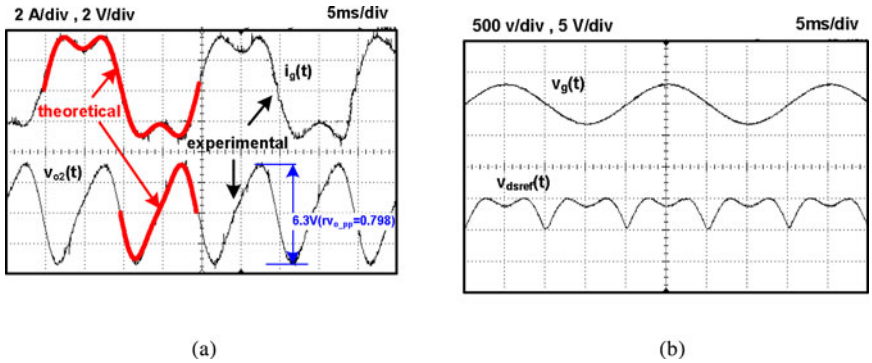

Fig. 13. (a) Input current and output voltage ripple for a Class C design. (b) Distorted sinusoidal reference synchronized with the input voltage.

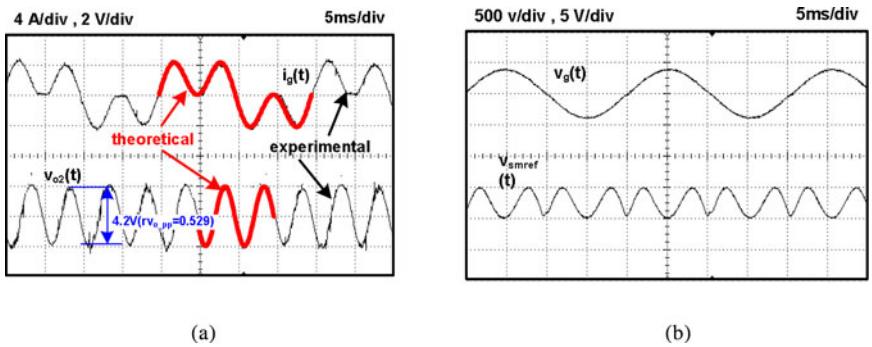

Fig. 14. (a) Input current and the output voltage ripple for a Class A design. (b) Distorted sinusoidal reference synchronized with the input voltage.

and (25), the input current can be rewritten as follows:

$$i_g(\omega_L t) = \frac{V_{A\mathrm{dc}}}{v_{\mathrm{dsref\_max}} K_{M\,\mathrm{dsref}}} \times \left[\sin(\omega_L t) + \frac{K}{2}\cos(\omega_L t - \Phi_L) + \frac{K}{2}\cos(3\omega_L t - \Phi_L)\right]. \tag{26}$$

In this case, pulsating input power can be obtained by using (5), and therefore, the expression of its the average value in half a line cycle will be as follows:

$$p_{g\mathrm{av}} = \frac{\omega_L}{\pi}\int_0^{\frac{\pi}{\omega_L}} p_g(\omega_L t)dt = \frac{V_{gp}V_{A\mathrm{dc}}}{4v_{\mathrm{dsref\_max}}K_{M\,\mathrm{dsref}}}(2 + K\sin\Phi_L). \tag{27}$$

Now the following equation shows that the value of $V_{A\mathrm{dc}}$ depends on the value of V_{gp} for a given average input power. Therefore, the feedforward loop in the proposed control strategy changes in order to allow this control technique for universal input voltage. In this case, current becomes

$$i_g(\omega_L t) = \frac{v_{\mathrm{dsref}}(t)\cdot V_{A\mathrm{dc}}}{v_{\mathrm{dsref\_max}}\cdot K'_{M\,\mathrm{dsref}}\cdot v_{\mathrm{FF}}} \tag{28}$$

where $K'_{M\,\mathrm{dsref}}$ is a new constant. As you can see now the current reference must be divided by the value of feedforward voltage instead of the square value of the feedforward voltage [see Fig. 10(b)].

C. Low-Cost Microcontroller Implementation

This pattern can be generated by a pulsewidth modulation (PWM) module of a low-cost microcontroller (μC), as can be seen in Fig. 11. The microcontroller reference is smaller than the traditional reference took from the rectifier input voltage. Nevertheless, these multiplier control chips (i.e., UC3854B) sense the $|v_g(t)|$ reference as a current reference. Therefore, if the value of current limit resistance [20] used in the traditional control is substituted by the adequate value, then the chip levels are maintained.

On the other hand, the fixed and $2f_L$ repetitive pattern has to be synchronized with the line. The distorted sinusoidal reference and the rectifier input voltage have to be "in-phase." Then, a synchronization circuit has to be implemented. Normally, this kind of circuits detects significant points of the input voltage. In this case, zero voltage points of $|v_g(t)|$ have been detected. When these points are detected, the microcontroller launches the fixed reference. Therefore, the reference signal is synchronized every 10 ms (European line).

Regarding the algorithm, it is based on a look-up table with normalized values of the duty cycle. With this system, the program goes through the table from top to bottom when the synchronized point is detected. Apart from the PWM generation, the microcontroller can also perform another systems: protection system, supervision system, soft start of the converter, etc.

V. Experimental Results

A 500-W PFC prototype, based on a boost topology, was developed in order to verify the proposed study. The main specifications of the PFC boost converter are the following:

TABLE I
EXPERIMENTAL HARMONIC CONTENT VERSUS THEORETICAL HARMONIC CONTENT

	Class C		Class A	
	Experimental results	**Theoretical results**	**Experimental results**	**Theoretical results**
Input current 1st harmonic (A_{rms})	2.23	2.261	2.31	2.261
Input current 3rd harmonic (A_{rms})	0.637	0.651	2.295	2.261
PF	0.967	0.961	0.718	0.707

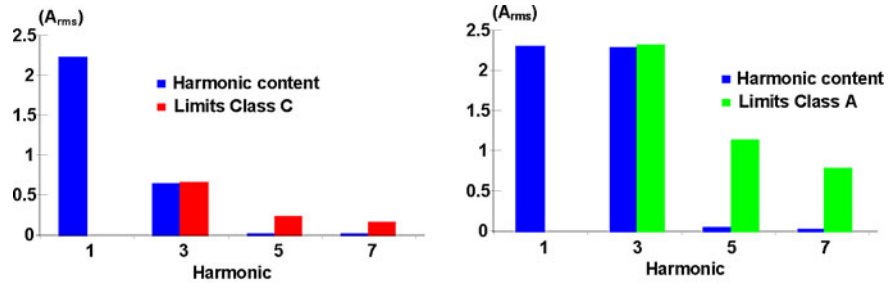

Fig. 15. Experimental harmonic content of the PFC versus EN 61000-3-2 regulations in (a) Class C and (b) Class A.

85–265 V input voltage, 400 V output voltage; output capacitor is of 500 μF (to obtain a 1% of output voltage ripple in traditional design, $k = 0$) and 10 kHz switching frequency. In this case, a low-cost microcontroller (PIC 16F627) working at 20 MHz has been used. Its cost is about 1 € .

First, the PFC experimental prototype was built with a traditional design. As can be seen in Fig. 12, the input current is sinusoidal and the output voltage ripple is 1% in amplitude (8 V peak-to-peak voltage). Therefore, the experimental output voltage ripple complies with aforementioned specifications.

Then, two PFC designs were implemented to maximize the output voltage ripple reduction in Classes C and A. Figs. 13 and 14 show the experimental results of the input current, the output voltage ripple, and the distorted sinusoidal reference synchronized with the input voltage. As can be deduced from Fig 13(a), a 20.2% of output voltage ripple reduction is obtained in Class C (from 8 to 6.3 V). Also, in Fig. 14(a), a 47.5% of output voltage ripple reduction is obtained in Class A (from 8 to 4.2 V). These reduction results match with the study presented in this paper in Class C [see Fig. 6(a)] and Class D (see Fig. 5). The experimental waveforms of the line current and the output voltage match with theoretical ones too. Table I shows the experimental harmonic content of these designs versus the theoretical one.

Finally, Fig. 15 shows the harmonic content of both designs versus the limits of Class C [see Fig. 15(a)] and Class A [see Fig. 15(b)]. As can be seen, the input current is distorted into the limits imposed by EN 61000-3-2 regulations. Therefore, the distorted sinusoidal reference used in both designs generates the desired input current in the edge of the regulation limits.

VI. CONCLUSION

The study of the output voltage ripple reduction distorting the input current in PFCs has been carried out in this paper. Also the limits of maximum reduction of the output voltage ripple compatible with EN 61000–3-2 regulations have been defined. In order to apply this study, a new control strategy for PFCs has been presented: if a properly distorted sinusoidal reference (based on the static analysis presented) is employed as a fixed pattern instead of the traditional reference, then the input current will be distorted allowing the maximum output voltage ripple reduction. The fixed pattern can be generated in a low-cost microcontroller. A 500-W prototype has been built and tested, and the experimental results are presented to verify the validity of the proposed method.

In summary, this paper proposes a method to reduce the storage capacitance in PFCs. The results show that reductions of 50% in Class A and B, 23% in Class C, 38% in Class D, and 34% in Energy Star program requirements for SSL luminaries can be achieved.

Taking into account these output capacitor reductions, it is difficult to remove the electrolytic capacitor only by distorting the line input current. A possible solution is to distort the input current and to allow a significant ripple in the output voltage in order to remove the electrolytic capacitor. In this case, a second stage is needed in order to eliminate the low-frequency ripple.

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