Practical Design and Implementation Procedure of an Interleaved Boost Converter Using SiC Diodes for PV Applications

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***Abstract*—The implementation of an interleaved boost converter (IBC) using SiC diodes for photovoltaic (PV) applications is presented in this paper. The converter consists of two switching cells sharing the PV panel output current. Their switching patterns are synchronized with 180° phase shift. Each switching cell has a SiC Schottky diode and a CoolMOS switching device. The SiC diodes provide zero reverse-recovery current ideally, which reduces the commutation losses of the switches. Such an advantage from the SiC diodes enables higher efficiency and higher power density of the converter system by reducing the requirement of the cooling system. This paper presents also an optimization study of the size and efficiency of the IBC. Based on 1) the steady-state characteristic of the topology; 2) the static and dynamic characteristics of the switching cells; 3) the loss model of the magnetic components; and 4) the cooling system design, the paper provides a set of design criteria, procedures, and experimental results for a 2.5 kW IBC prototype using SiC diodes.**

***Index Terms*—Diode, interleaved boost converter (IBC), MOSFET, power semiconductor, photovoltaic (PV), silicon carbide (SiC).**

I. Introduction

SILICON carbide (SiC) represents a breakthrough in silicon technology because it allows a larger energy gap. SiC is classified as a wide-band-gap (WBG) material, and it is becoming the mainstream material for power semiconductors [1], [2]. Among the different types of power semiconductors, the power diode was the first device to adopt SiC technology, which was commercialized years ago. The main advantages are the high-breakdown voltage and the small reverse-recovery current. Some research has proven that SiC Schottky diodes are superior to Si-based diodes in device characteristics [3]–[5]. As a result, higher efficiency and higher power density can be brought to power electronic systems in different applications [6]–[8].

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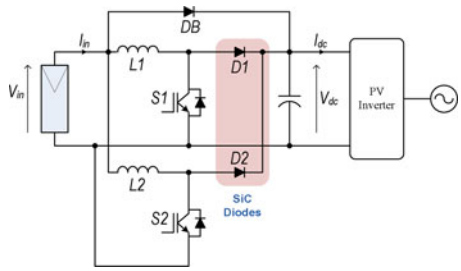

Fig. 1. Dual-stage topology for PV inverter using IBC.

The market for residential photovoltaic (PV) inverters is becoming highly competitive. PV manufacturers are competing to increase the efficiency for every 0.1%. From the maximum power point tracking (MPPT) algorithm point of view, the existing methods, such as perturbation and observation (P&O) and incremental conductance (IncCond), can track the maximum power point properly and the dynamic response is good enough to deal with changes in temperature and irradiation [9], [10]. From the hardware point of view, there are 2 DoFs in an inverter design used to improve the efficiency, namely semiconductor and topology. As the topology is limited by the issue of common mode voltage, the options of transformerless topologies are limited [11]. With regard to the semiconductor, high voltage and low current ratings for residential PV inverters are required. The commercialized SiC diodes are acceptable in this particular application from the electrical performance point of view. However, it is well known that SiC increases the overall cost of components. Moreover, a single diode replacement without any optimization cannot effectively improve the system efficiency. Instead it may prolong the payback time from electricity savings to compensate for the cost of the PV inverter. Thus, the right selection of topology and peripheral devices, such as switches, passive devices, and cooling systems, is important in order to maximize the benefits of using SiC diodes in a power electronics system.

Fig. 1 shows a typical dual power stage single-phase transformerless PV inverter [11]–[14]. It is formed by two converters: 1) a dc–dc converter for MPP tracking and dc-link voltage stabilizing (referred to as a preregulator) and 2) a dc–ac inverter for injecting ac power into the grid. It is a well known fact that the *I–V* characteristics of PV panel vary with the environment, such as temperature and irradiation. For general purpose single-phase inverter for low-power residential PV

TABLE I
SPECIFICATIONS OF A BOOST CONVERTER FOR SINGLE-PHASE PV INVERTERS PREREGULATION

Parameter	Value	Parameter	Value
Nominal Input Voltage Range of MPPT	125V – 650V	Max. Input voltage	800V
Nominal Output Voltage	400V	Rated Output Power	2.5kW
Operating Frequency	≥ 16kHz	Input Current Ripple	10% of $I_{\text{in, max}}$
Max. Ambient Temp.	50ºC	Max. Junction Temp.	125ºC

installation, the variation range of panel MPP voltage is typically from 125 to 650 V. And the absolute open-circuit voltage can be as high as 800 V. Although the inverter does not convert energy at this voltage, the breakdown voltage of semiconductors and capacitors has to deal with the voltage level. Besides, the dc-link voltage V_{dc} has to be higher than the peak of the grid voltage, e.g., 400 V. Thus, there are two operating modes in the energy converting process to reduce the losses in the PV inverter. They are as follows:

Mode 1: The PV panel output voltage is from 125 to 400 V, the dc–dc converter boosts up the dc-link voltage to 400 V and it handles the MPPT function.

Mode 2: The PV panel output voltage is from 400 to 650 V, the dc–dc converter bypasses by the diode, DB. The PV panel is directly connected to the inverter and the inverter takes over the MPPT function.

Moreover, both power stages have to operate at/or higher than 16-kHz switching frequency for residential PV inverters, in order to avoid acoustic noise generated by the inductors. Another limitation of the converter design is that the input current variation cannot be too large, otherwise the operating point is not stable at the MPP of PV. Table I summarizes the typical operating conditions of residential PV inverters.

This paper presents a practical design and implementation procedure for an interleaved boost converter (IBC) using SiC Schottky diodes in a residential PV preregulator application. It must be noted that this represents an example of the use of the method and procedure. It can be extended to optimize the dc–ac inverter. The design goal is to maximize the efficiency in the system and the design criteria are in agreement with the typical specification of single-phase PV inverters in Table I. The design procedure is based on the basic analysis of the steady-state characteristics of the topology and the semiconductor switching behavior. The further optimization for the passive devices and cooling system can be obtained based on the previously analyzed results. Fig. 2 shows the flow chart of the design steps. Experimental results in a 2.5 kW IBC prototype using SiC diodes are provided to show the performance of the optimized prototype.

II. REVIEW OF STEADY-STATE CHARACTERISTICS OF IBC

IBC consists of "*n*" single boost converters connected in parallel, i.e., *n*-phase, to share the handled power. In this paper, the two-phase IBC, shown in Fig. 1, is considered. Notice that the results can be easily extended to *n*-phases. In the case of

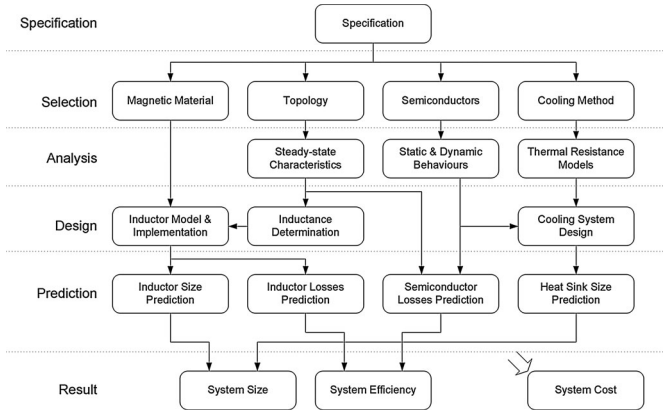

Fig. 2. Design procedure for prototyping the optimized IBC.

the two-phase IBC, the two switches $S1$ and $S2$ are controlled with 180° phase shift. By using this circuit structure and modulation scheme, the advantage of antiphase ripple cancellation of both inductors can be achieved. The amplitude of the input current ripple is smaller compared to a single boost converter. This makes the topology very attractive for PV preregulator applications. However, as the voltage of the PV string can reach 800 V, then in a purely silicon (Si) design, the converter suffers from reverse-recovery losses and commutation losses. SiC diodes are used to solve this problem because they have practically negligible reverse recovery and have a high-breakdown voltage.

In principle, the IBC is formed by two independent boost switching units. For each boost switch unit, there are two switching states.

1) Switch is ON. The current in the inductor starts to rise, while the diode is blocking.
2) Switch is OFF. The inductor starts to discharge and transfer the current via the diode to the load.

The following are the most important parameters used to study the steady-state characteristic of the IBC.

1) Boost Ratio: The boosting ratio of the converter is a function of the duty ratio. It is the same as in a conventional boost converters. It is defined by the duty ratio

$$\frac{V_{\text{dc}}}{V_{\text{in}}} = \frac{1}{1-D} \tag{1}$$

where V_{dc} is the output voltage, V_{in} is the input voltage, and D is the duty ratio.

2) Input Current: The input current can be calculated by the input power and the input voltage

$$I_{\text{in}} = \frac{P_{\text{in}}}{V_{\text{in}}}. \tag{2}$$

3) Inductor Current Ripple Peak-to-Peak Amplitude: The inductor current ripple peak-to-peak amplitude can be

determined by

$$\Delta I_{L1,L2} = \frac{V_{\rm in} \cdot D}{f_{\rm sw} \cdot L} \tag{3}$$

where $f_{\rm sw}$ is the switching frequency and L is the inductance.

4) Relationship Between Input Current Ripple Peak-to-Peak Amplitude and Inductor Current Ripple Peak-to-Peak Amplitude: As with most interleaved converters, the minimum input ripple occurs at a duty cycle of 0.5. This is due to the 180° phase difference between the two boost cells [15], [16]. There are two operating modes which can be defined by the inductor current behaviors.

1) Mode 1 ($D > 0.5$): Over a specific period of time the current in both inductors rises.
2) Mode 2 ($D < 0.5$): Over a specific period of time both inductors discharge.

Consequently, the input current ripple peak-to-peak amplitude is given by

$$\Delta I_{\rm in} = \frac{V_{\rm dc} - 2 \cdot V_{\rm in}}{f_{\rm sw} \cdot L} \cdot \begin{cases} -D, & \text{if } D \le 0.5 \\ 1 - D, & \text{if } D > 0.5. \end{cases} \tag{4}$$

5) Operating Currents in Semiconductors: Fig. 3 shows the typical waveforms of one leg of the IBC and the semiconductor loss distribution in one switching cycle. Ideally, the input current is evenly shared by the two switching cells. It means that half of the input current is flowing in each leg, i.e., $I_{\rm in}/2$. Thus

$$i_{D,\rm off} = i_{F,\rm on} = \frac{I_{\rm in} + \Delta I_{L1,L2}}{2} \tag{5}$$

$$i_{D,\rm on} = i_{F,\rm off} = \frac{I_{\rm in} - \Delta I_{L1,L2}}{2} \tag{6}$$

where $i_{D,\rm off}$ and $i_{D,\rm on}$ are drain currents of the MOSFETs at turn-off and turn-on transients, respectively. $i_{F,\rm off}$ and $i_{F,\rm on}$ are operating currents of the diodes at turn-off and turn-on transients, respectively.

The RMS values of the current flowing through the semiconductors are given by

$$I_{D,\rm RMS} = \sqrt{\left(i_{D,\rm on}^2 + \frac{i_{D,\rm on} \cdot \Delta I_{L1,L2}}{2} + \frac{\Delta I_{L1,L2}^2}{3}\right) \cdot D} \tag{7}$$

$$I_{F,\rm RMS} = \sqrt{\left(i_{F,\rm off}^2 + \frac{i_{F,\rm off} \cdot \Delta I_{L1,L2}}{2} + \frac{\Delta I_{L1,L2}^2}{3}\right) \cdot (1-D)}. \tag{8}$$

Based on (1)–(8), the inductance, the inductor losses, and the semiconductors losses can be determined.

III. Inductors

In modern power electronics systems, magnetic components play a very important role with regard to storage and filtering. In the operating principle of a boost converter, the inductor is used to transform the energy from the input voltage to the inductor current and to convert it back from the inductor current to the output voltage. Fig. 1 shows that there are two independent inductors in an IBC. In principle, the two inductors are identical in order to balance the current in the two boost cells. In this section, the design and implementation of the inductors are presented as well as the loss model of the inductors provided for the overall system loss estimation.

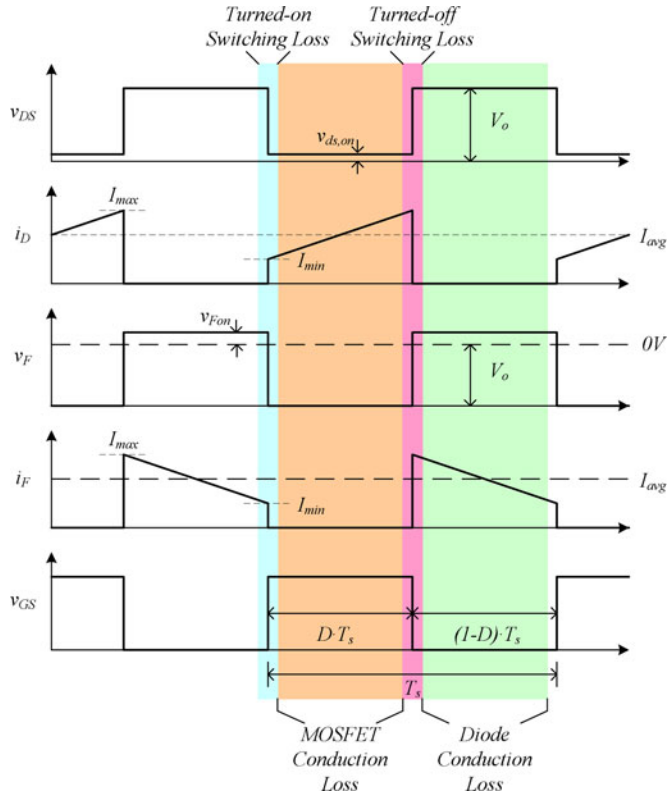

Fig. 3. Typical waveform of one leg of the IBC at rated power.

A. Determination of Inductor Value

According to the specifications in Table I, the boost converter operates when the input voltage is in the range from 125 to 400 V. Based on (1), the corresponding duty ratio range is 0 to 0.69. Fig. 4 shows a typical profile of the input ripple peak-to-peak amplitude against the duty ratio in an IBC, which can be determined using (4). It shows that the maximum amplitude of the input current ripple occurs at 0.25 duty ratio in the specified operating range. Thus, based on Table I and from (1) to (4), the inductor value can be determined by

$$L = \left[\frac{V_{\rm in} \cdot D \cdot \left(2 - (1-D)^{-1}\right)}{f_{\rm sw} \cdot 0.1 \cdot (P_{\rm in,\,max}/V_{\rm in,min})}\right]_{D=0.25}. \tag{9}$$

Finally, the resulting inductance per inductor is 1.5 mH and two inductors are used in the IBC.

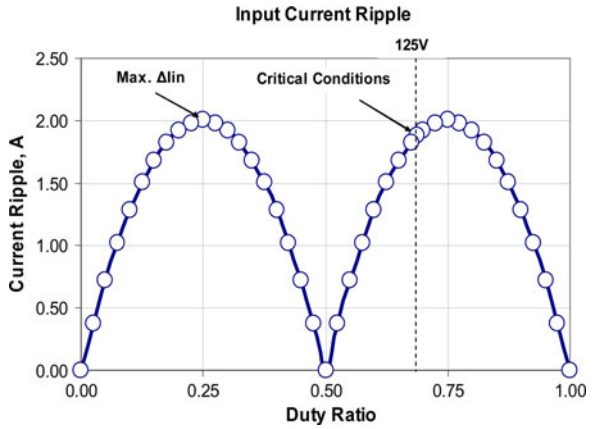

Fig. 4. Input current ripple current versus duty cycle.

TABLE II
SUMMARY OF INDUCTOR DESIGN

Symbol	Description	Value	Unit
	Input Parameters		
$I_{L1,L2\_max}$	Peak current per leg:	12.2	A
$I_{L1,L2}$	Average current per leg	10.4	A
	Data Sheet Parameters		
f_W	Window fill factor	0.4	
J_{max}	Maximum current density	5	A/mm^2
B_{max}	Maximum peak flux density	1.4	T
A_C	Core cross section of AMCC-20	270	mm^2
W_A	Window Area of AMCC-20	650	mm^2
n	Number of turns	50	
μ_0	Vacuum permeability	4π x 10^{-7}	H/m
	Output Parameters		
l_g	Air gap	0.053	cm
A_W	Cross section of wire	2.5	mm^2

B. Implementation

The main assembling components of an inductor are core and wire. The material of the core for the operating frequency can be ferrite, iron powder, and Metglas. Among the materials, Metglas provides a very high saturation flux density due to the iron-based amorphous alloy 2605SA1 [17]. Thus, the size and core loss can be minimized compared to the other materials. In the paper, the Metglas C-Core AMCC-20 and Litz wire (25 mm $\times$ 0.355 mm) have been selected based on the loss and size consideration. Two inductors have been implemented based on the design procedures in [18]. The practical design consideration will be discussed in Section VII. The summary of the inductor design and implementation is shown in Table II.

C. Inductor Loss Model

The losses in practical inductors can be divided in two main categories: copper loss and core loss. The copper loss depends on the length, thickness, and material of the wire. The core loss mainly appears in the air gap of the magnetic components. The loss model and equations are based on [18]. Please refer to Table III where all symbols used in the following equations are defined.

TABLE III
PARAMETERS OF INDUCTOR LOSSES

Symbol	Description	Unit	value
T_a	Maximum ambient temperature	50	°C
ΔT	Rise of temperature	30	°C
T_{max}	Maximum temperature $T_a + \Delta T$	80	°C
a,b,c,d	Geometrical values for core	11, 13, 50, 30	mm
ρ_{20}	Resistivity @ T=20°C	17.24x10^{-6}	Ωmm
α_{20}	Resistance temperature coefficient @ T=20°C	0.0042	1/K
R_{unit}	Resistance per unit length	5.36	μΩ/mm
MTL	Mean Turn Length	134	mm
Ω_{tot}	Total resistance of copper windings	35	mΩ
$\Delta I_{L1,L2}$	Current ripple per leg @125V, 2500W	3.58	A
B_{ac}	AC flux in air gap @125V, 2500W	210	mT
wt	Weight of the core	0.337	kg
f	Frequency in kHz	16	kHz

1) Copper Loss: The resistance per unit length R_{unit}, of conductor is given by

$$R_{\mathrm{unit}} = \frac{\rho_{20}\left[1+\alpha_{20}(T_{\max}-20)\right]\cdot n}{b\cdot c\cdot f_w}. \tag{10}$$

Notice that a, b, c, and d are the geometrical values for the core. "a" is the width of the core leg, "b" and "c" are the width and height of the window, respectively, the "c" is the thickness of the core. The detail geometry is given in [18]. Besides, the maximum operation temperature $T_{\max}$, has been taken into account in (10). Consequently, the result for the copper loss considers the temperature at 80 °C in the whole operating range. This is the worst case of the inductor temperature.

For the calculation of the total resistance, the mean turn length, MTL, is approximated as follows:

$$\mathrm{MTL} = 2\cdot(a+2b+d). \tag{11}$$

Therefore, the total resistance Ω_{tot}, is given by

$$\Omega_{\mathrm{tot}} = R_{\mathrm{unit}}\cdot \mathrm{MTL}\cdot n. \tag{12}$$

Furthermore, a Litz wire was applied to decrease skin and proximity effects. The copper loss can be calculated with the current per leg as follows:

$$P_{\mathrm{cu}} = I_{1,2}^2\cdot\Omega_{\mathrm{tot}}. \tag{13}$$

2) Core Loss: The ac flux in the air gap B_{ac}, is given by the following equation:

$$B_{\mathrm{ac}} = \frac{0.4\cdot\pi\cdot n\cdot\Delta I_L}{2\cdot l_g}. \tag{14}$$

Consequently, the core loss P_{core}, can be calculated using the "Steinmetz" equation, which is provided by the manufacturer's application note [18], and is given by

$$P_{\mathrm{core}} = 6.5\cdot f^{1.51}\cdot B_{\mathrm{ac}}^{1.74}\cdot wt. \tag{15}$$

According to the data sheet, the temperature condition for (15) is 25 °C. It also shows that the core loss variation is lower

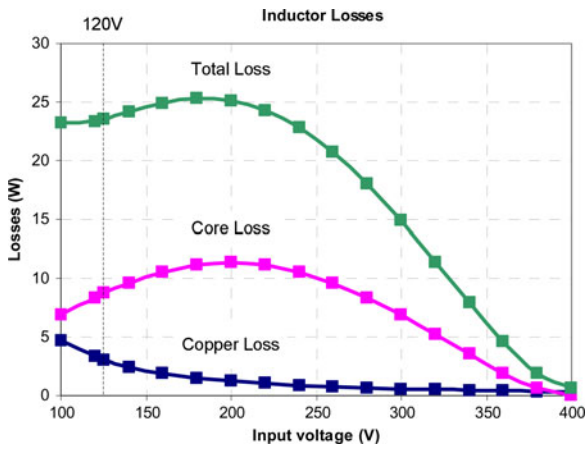

Fig. 5. Inductor losses at 80 °C.

than 5% when the temperature changes from 25 to 100 °C. Thus, the assumption that power loss is independent of temperature can be made.

With this result of copper loss, the total loss of two inductors $P_{\rm tot}$, can be estimated as

$$P_{\rm tot} = 2 \cdot (P_{\rm cu} + P_{\rm core}). \tag{16}$$

The results of the losses are shown in Fig. 5, which are based on the parameters in Table III. The copper loss, core loss, and total loss of the inductors at the thermal design point are 3, 8.7, and 23.5 W, respectively. The graph also shows that the core loss is the dominant part of the total losses and could be reduced by using less turns, smaller current ripple, or longer air gap. However, this has not been done in the present design. This is because the specification of the input ripple leads to a fixed inductance value, which causes fixed current ripple per leg. Also the number of turns cannot be decreased because of the saturation issue of the core. A tradeoff thus arises. If lower losses are to be achieved, then a bigger core has to be used to reduce the number of turns, but consequently the size of the core will increase as well.

IV. Semiconductors Evaluation

Semiconductor characterization is the first step in prototyping a power electronic system. Based on the data extracted from the semiconductors, the conduction losses and switching losses of a switching cell operating in a system can be estimated [19], [20]. Moreover, it is important to optimize the system by selecting the most suitable semiconductor devices and gate drive circuits. In this paper, CoolMOS and SiC Schottky diodes were selected as the active switch and diode, respectively. Table IV shows the part numbers and parameters of these devices. The advantages of the CoolMOS are low on-state resistance at low-junction temperature and no "tail" current during the turn-off transients. These result in relatively lower conduction loss and turn-off switching loss compared to IGBTs. Moreover, the SiC diodes bring low reverse-recovery losses and low commutation losses in the switching cell [21], [22], which is advantageous for systems with high-efficiency requirements.

TABLE IV
Parameters of the Evaluated Devices

Parameters	Symbol	Devices		Unit
		CoolMOS	SiC Diode	
Manufacturer		Infineon	Cree	
Part No.		IPW90R120C3	C2D20120D	
Type		CoolMOS	Schottky	
Breakdown Voltage	V_{BD}	900	1200	V
Rated Current	I_D	23 (@100°C)	22 (@125°C)	A
Max. Junction Temp.	$T_{J,max}$	150	175	°C
J-C Thermal Resistance	R_{thJC}	0.3	0.48	K/W
Package		TO-247	TO-247	

This section demonstrates the experimental results of the device characterization. It includes the output characteristics of the CoolMOS, the forward characteristic of the SiC diode, and the switching loss chart of one switching cell. An estimated loss breakdown for the semiconductors is included as well.

A. Static Characteristics of Semiconductors

The aim of the static characteristics measurements is to determine the conduction loss of the semiconductors, which will be used in the power electronics system. The Tektronix 371 A Curve Tracer was used to extract the parameters from the semiconductor devices.

Fig. 6 shows the output characteristics of the CoolMOS at different junction temperatures. The on-state resistances are 108, 156, and 250 mΩ at 25, 75, and 125 °C, respectively. This implies that the conduction loss of the CoolMOS dramatically increases at high-junction temperature. Fig. 7 shows the forward characteristics of the SiC Schottky diode as well as the CoolMOS, the diode forward characteristics are temperature dependent with positive coefficient. According to the static characteristics of the devices, 75 °C is a suitable junction temperature for both devices due to the low conduction loss in the semiconductors. In addition, the results show that the static characteristics of the components are close to the given results in the device data sheets.

B. Dynamic Characteristics of Semiconductors

Energy loss information in a switching cell can be extracted by double pulse test setup [23]. It simulates the switching actions of the switching cells in a power electronics system. Generally, the turn-on and turn-off switching loss of the switch and the turn-off switching loss of the diode are considered in the loss measurements as they dominate the loss during transients in the devices. Generally, the inductive switching loss information is not given by the semiconductor data sheet. This is because different combinations of active device and diode will result in different dynamic behaviors. It is hard to provide information by calculation, to estimate the switching losses in the semiconductors. Double pulse test is the usual way to obtain the accurate switching loss information before designing a converter.

Fig. 8 shows the experimental switching loss chart for the switching cell which is listed in Table IV. The testing

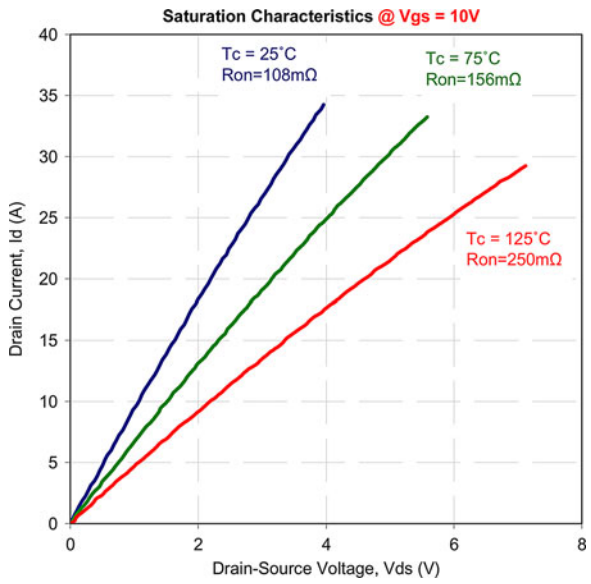

Fig. 6. CoolMOS output characteristic with different junction temperatures.

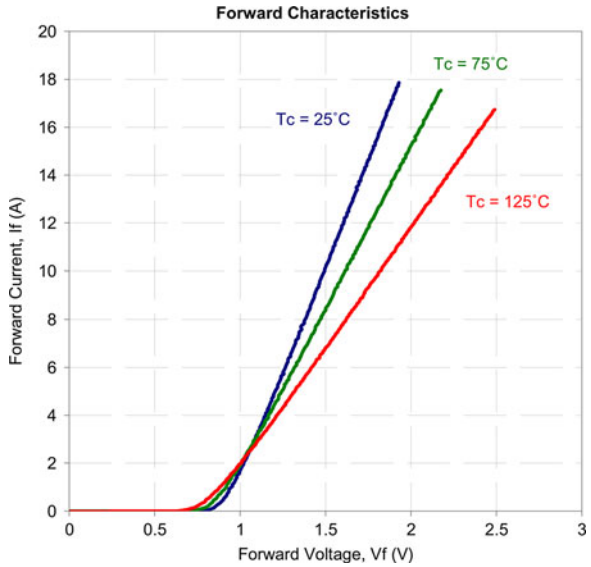

Fig. 7. SiC diode forward characteristic with different junction temperatures.

environment is simulated with an IBC operating, at 400 V dc-link voltage and 75 °C juncture temperature. The switching action time intervals are illustrated in Fig. 3. The chart shows that the reverse-recovery loss in the diode is very low, around 40 μJ at 10 A operation. The reason for this is the use of the SiC Schotkky barrier diodes that brings down the reverse recovery. Meanwhile, it reduces the turn-on transition time of the CoolMOS. Thus, the turn-on switching loss is low as well. Besides, the short turn-off transient time is a significant advantage of CoolMOS. It is proven in the measurements that, the turn-off loss of the CoolMOS is very low compared to IGBTs [21], [22].

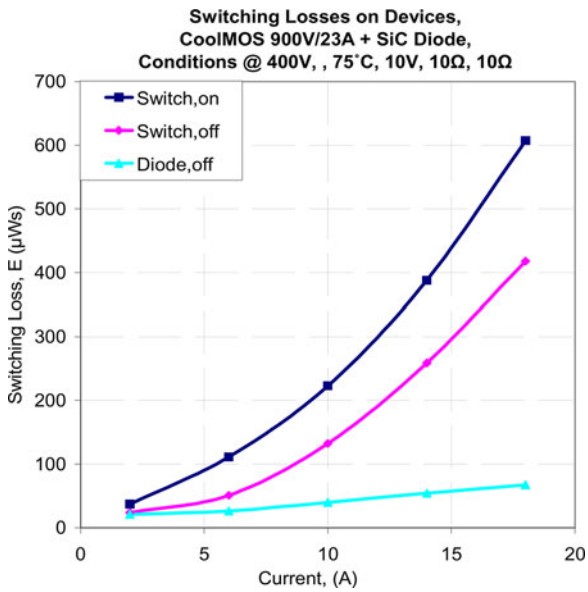

Fig. 8. Switching loss chart.

C. Semiconductor Loss Breakdown at Thermal Design Point

As previously mentioned, the main purpose of having the static and dynamic characteristics of the semiconductors is to use this information to predict the semiconductor loss in a power electronics system. Then, an appropriate cooling system can be designed based on the losses breakdown at the thermal design point, i.e., $P_{\rm in} = 2.5$ kW, $V_{\rm in} = 125$ V, and $D = 0.6875$. Notice that the semiconductors produce the highest loss at this point.

1) Conduction Losses: L, $\Delta I_{L1,L2}$, and $i_{D,\rm on}$ are determined in (9), (3), and (6), respectively. Out of these, $I_{D,\rm RMS}$ is obtained by (7). The conduction loss of the CoolMOS is determined by

$$P_{M\_\rm con} = I_{D,\rm RMS} \cdot V_{\rm DS} \tag{17}$$

where $V_{\rm DS}$ can be determined using Fig. 6 for the corresponding $I_{D,\rm RMS}$.

Similarly, $I_{F,\rm RMS}$ is obtained by (8). The conduction loss of the diode is determined by

$$P_{D\_\rm con} = I_{F,\rm RMS} \cdot V_F. \tag{18}$$

where V_F can be determined using Fig. 7 for the corresponding $I_{D,\rm RMS}$.

2) Switching Losses: The switching energy losses in the devices are simply determined using Fig. 8 for the corresponding currents. The equations are

$$P_{M\_\rm on} = E_{M,\rm on}(i_{D,\rm on}) \cdot f_{\rm sw} \tag{19}$$

$$P_{M\_\rm off} = E_{M,\rm off}(i_{D,\rm off}) \cdot f_{\rm sw} \tag{20}$$

$$P_{D\_\rm rr} = E_{D,\rm rr}(i_{F,\rm off}) \cdot f_{\rm sw}. \tag{21}$$

Table V shows the estimated loss breakdown of the switching cell operating in the IBC at 16-kHz switching frequency. It is observed that the reverse-recovery loss ($P_{D\_\rm rr}$) in the SiC diode is not significant, and the switching losses in the CoolMOS are quite low.

TABLE V
LOSS BREAKDOWN OF SEMICONDUCTORS IN IBC

CoolMOS				SiC Diode			Loss
P_{M_con}	P_{M_on}	P_{M_off}	P_{M_t}	P_{D_con}	P_{D_rr}	P_{D_t}	
W	W	W	W	W	W	W	W
11.3	2.88	2.4	16.58	5.14	0.64	5.78	44.7

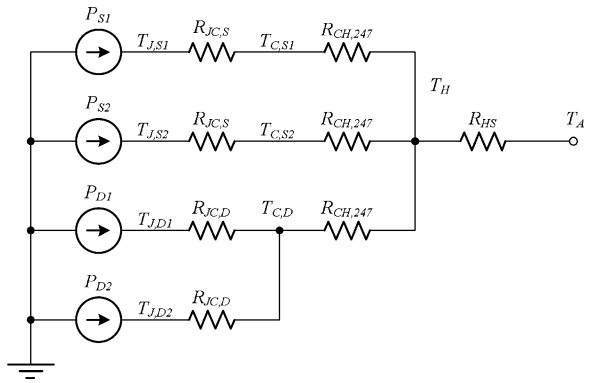

Fig. 9. Simplified thermal resistance network.

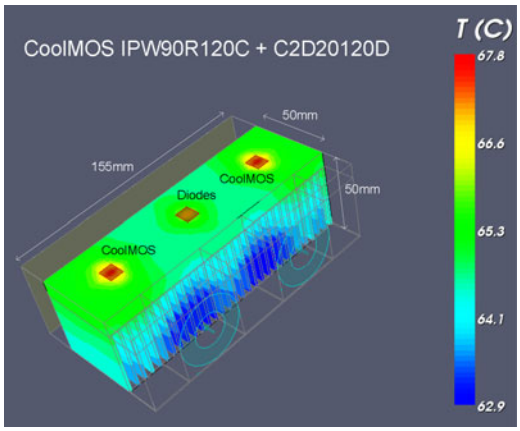

Fig. 10. Thermal simulation of designed cooling system.

V. COOLING SYSTEM

There are generally two main components in a cooling system for air-force convection, namely a heat sink and a fan. An aluminum 42-fin heat sink and two cooling fans, SUNON KDE1204PKV2, are used in the system. The thermal model of the cooling system has been created using "Qfin4" software. Based on the semiconductors J-C thermal resistances shown in Table IV and the loss of each device in Table V, the heat sink length can be determined. Fig. 9 shows the simplified thermal resistance network. The graphical simulated results are shown in Fig. 10. The figure shows the placement of the semiconductors, the dimensions of the heat sink and cooling fans, and the heat distribution. According to the simulated results, the maximum junction temperature of the CoolMOS in the system operating in the critical conditions is 76.2 °C. Notice that it is approximately the same as the designed junction temperature of the CoolMOS in Section IV.

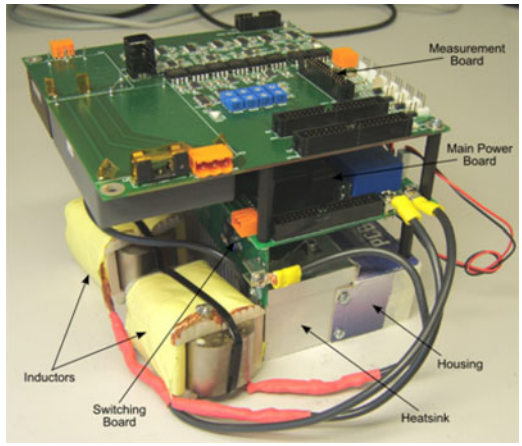

Fig. 11. Photograph of the optimized IBC prototype.

TABLE VI
TEMPERATURES IN IBC

	T_A	$T_{H,Diode}$	$T_{H,Switch}$	$T_{J,Diode}$	$T_{J,Switch}$	Unit
Simulated	50	60	68	69	76	°C
Measured	27	42	46	48*	55*	°C

**The value is estimated.*

VI. EXPERIMENTAL VERIFICATIONS

A laboratory prototype has been built based on the design procedures presented in the paper. The prototype is shown in Fig. 11. It shows all boards and components in the converter. The dimensions of the prototype are L150 × W170 × H150 mm.

The loss prediction in Sections III and IV for the inductors and the semiconductors in the critical conditions, 125-V input voltage and 2.5-kW output power, are 23.5 and 44.7 W, respectively. As a result, the measured system loss was 69 W. It is 0.8 W higher than the prediction, which is not significant. The reasons for this difference are as follows. First, the ambient temperature was not at 50 °C, thus the semiconductors were not working at the desired junction temperature of 75 °C. As a result, the loss of MOSFET is slightly different from the calculated values. Second, the losses of sensors, relays, and other passive devices have not been taken into account in the simulation. Nevertheless, the measured temperatures are shown in Table VI. The temperature information shows that the cooling system is designed properly. The measured case temperature of the CoolMOS has around 22 °C of difference with respect to the simulated result in Fig. 9, while the ambient temperatures have 23 °C of difference.

Fig. 12 shows the switching waveforms when the system is working in the critical conditions. It shows that the current waveforms of i_{L1} and i_{L2} are 180° out of phase, and they are almost in the even sharing mode. In fact, the distribution of the currents in the two switching cells is highly dependent on the parameters of the inductors and semiconductors. Besides, the input current is the sum of the two inductor currents. The current ripple amplitude is around 3.2 A, which matches (3). Fig. 13 shows the waveforms when the system is operating

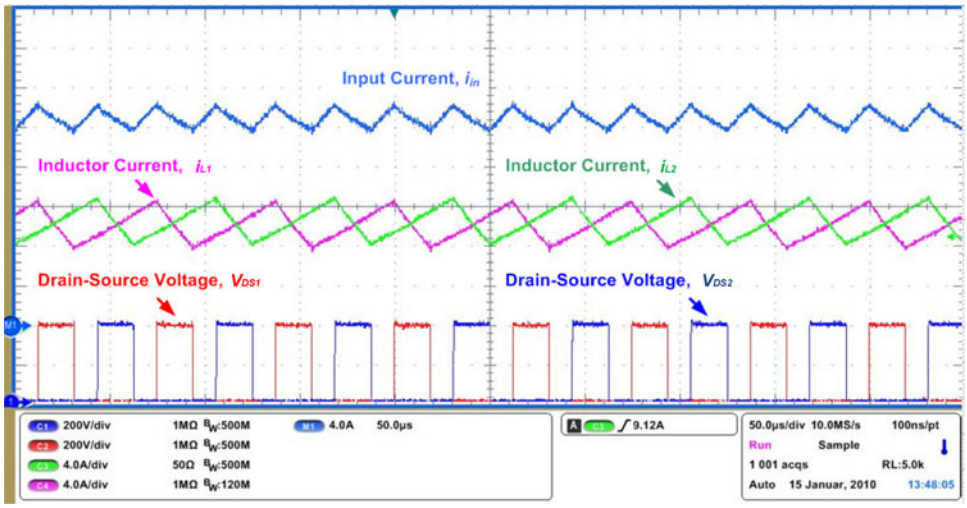

Fig. 12. Measured current waveforms of IBC at 2.5 kW, 125 V and $D = 0.6875$.

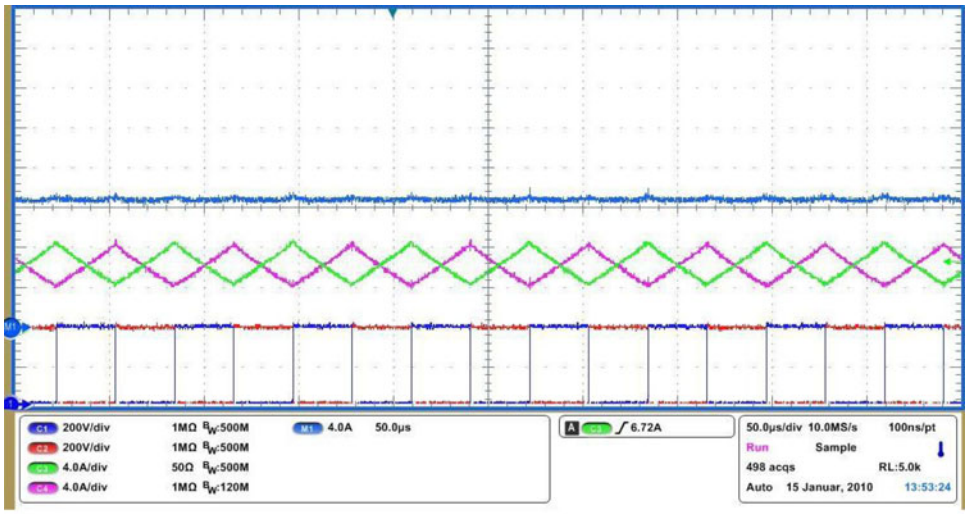

Fig. 13. Measured current waveforms of IBC at 2.5 kW, 200 V and $D = 0.5$.

at full load and the duty ratio is 0.5. The input current ripple amplitude is zero because of the ripple cancellation between the two inductor currents.

In order to verify the simulated result in the optimizing process, Fig. 14 shows the simulated and measured efficiencies in the completed PV operating range. In the simulation, the semiconductor losses are based on the experimental results shown in Figs. 6–8. The loss estimating program simulates the IBC operating at different input voltages and output powers. The charts show that the results are very similar in most regions, only the efficiency at low power and high-input voltage region are higher than 0.5% difference. The reasons for the difference are that when the output power is very low, the measuring error becomes significant in the efficiency calculation. Moreover, the input parameters of the simulation are in constant temperature condition, however, in practice, the temperature is changing simultaneously with the output power. Although the simulation results are slightly different with respect to the experimental results, they provide a very good overview for the system behaviors before the experiment is carried out.

Fig. 15 shows the European efficiency of the IBC operating in a PV system. The solid line is the optimized IBC using CoolMOS devices and SiC diodes. In contrast, another optimized IBC using commercial IGBTs and SiC diodes has been implemented and measured. The dash line shows the result of this latter system. It can be seen that the CoolMOS device provides 1% efficiency improvement compared to the IGBT, when SiC diodes are applied to the IBC. This illustrates the importance of an appropriate semiconductor selection.

VII. Discussions

A. Optimal Inductor Design

Loss, size, and cost of an inductor are always a tradeoff in the inductor design. There are no restricting criteria to guide engineers to design inductors to achieve an optimum design. The design should depend on the available physical dimensions and the loss optimization. Typically, there are two degrees of freedom in an inductor design to fit into the system, namely

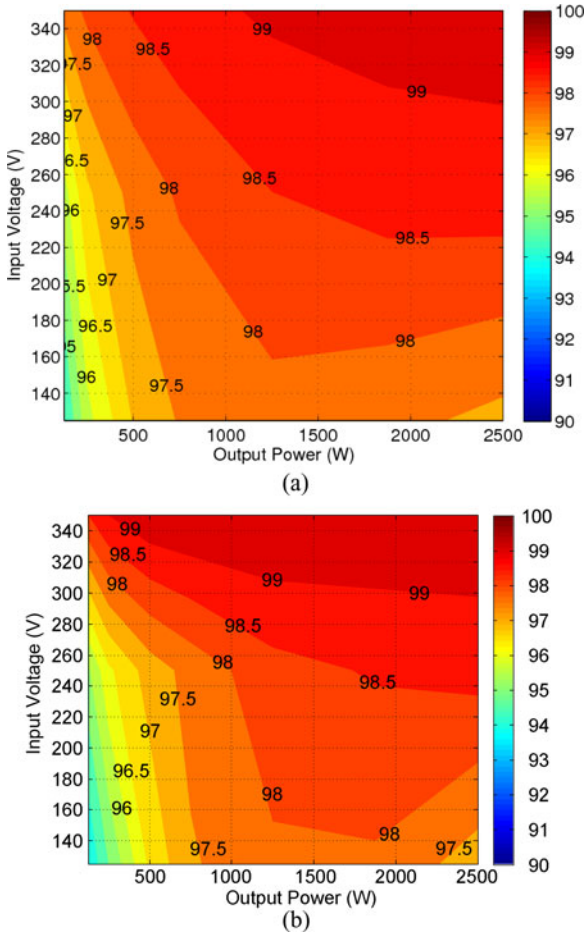

Fig. 14. Efficiencies in the whole PV system operating range. (a) Simulated. (b) Measured.

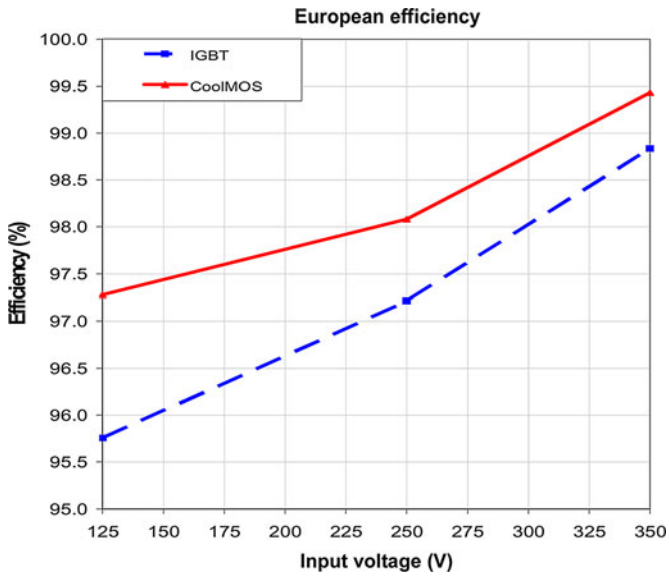

Fig. 15. European efficiency of the IBC.

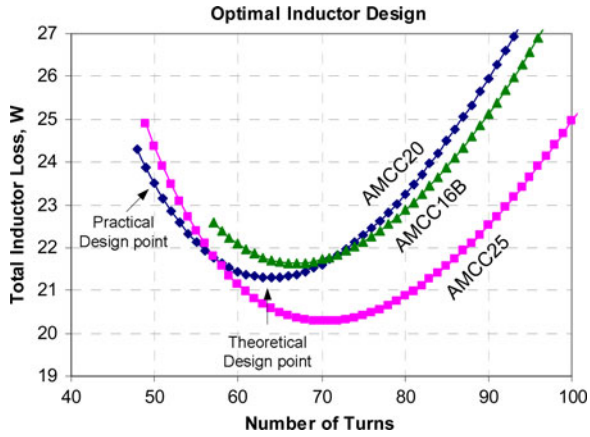

Fig. 16. Inductor design curves.

turns optimization and core selection. Fig. 16 shows the loss response of different inductor designs which can be used in the PV preregulator in the paper. All design points in the chart were calculated from (10) to (16). The optimal number of turns of the AMCC16B, AMCC20, and AMCC25 cores is 68, 63, and 70 turns, respectively. Based on the analysis, AMCC25 is the most suitable core due to the lowest loss. However, actual physical dimensions need to be considered in the practical design. As the inductors were to be located at the air flow output of the heat sink, which is shown in Fig. 11, then the total length of two cores could not be longer than the length of the heat sink (155 mm). Unfortunately, the total length of two AMCC25 is longer than the heat sink length. Therefore, AMCC20 core has been selected in this design, since the length of each core is 72 mm according to the data sheet [18]. With the local optimization, AMCC20 core with 63 turns is the theoretical design point of the inductor. However, the air gap should be minimized in the inductor, since a large air gap generates extra power losses and a rise in the conductor temperature, which is caused by the air gap fringing flux [24]. Therefore, a minimum numbers of turns and the shortest air gap were designed in the inductor. Finally, the loss difference between practical and theoretical inductor design point was 2 W based on (16). This difference is, however, not significant from the full system efficiency point of view.

B. Optimal Switching Frequency Selection

It is well known that the switching losses in the system can be reduced by using SiC semiconductors. Therefore, high efficiency can be achieved with high-switching frequency in converters. The switching frequency optimization of the IBC is shown in Fig. 17. It illustrates that the optimal switching frequency is 11 kHz. However, it has been mentioned that the minimum switching frequency of the application must be 16 kHz to avoid acoustic noise. Thus, the optimal switching frequency was fixed at 16 kHz due to the lowest total loss in the system within the usable frequency bandwidth.

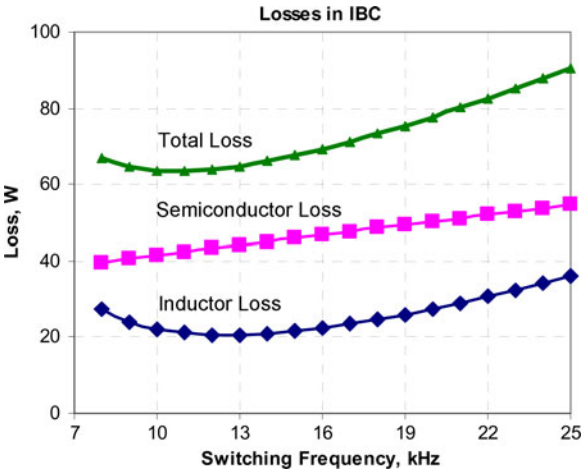

Fig. 17. Losses in IBC with switching frequency variation.

VIII. Conclusion

This paper has presented a complete design and implementation procedure for the IBC prototype using SiC diodes. The design criteria were based on four aspects: topology, semiconductors, magnetic devices, and cooling system. The steady-state characteristics of the IBC have been studied and the semiconductor losses have been experimentally obtained. Based on this, the optimized cooling system was designed to dissipate effectively the semiconductor losses. Moreover, the loss model of the magnetic devices was determined, thus the overall system's size and efficiency could be further optimized. The experimental results were similar to the simulated results in terms of junction temperature and efficiency. In conclusion, the converter with CoolMOS devices and SiC diodes is very suitable for PV preregulator applications because of the minimized system loss and size reductions.

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