

Reducing Storage Capacitor of a DCM Boost PFC Converter

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Abstract—The discontinuous current mode boost power factor correction (PFC) converter automatically achieves PFC when the duty cycle is kept constant in a line cycle; however, there is large third harmonic in the input current, and the third harmonic has the initial phase of π in respect of the fundamental component. Therefore, the input power factor is low, and a large storage capacitor is needed. Injecting appropriate third harmonic with initial phase of zero into the input current could reduce the storage capacitor. This paper proposes the variable duty cycle control to inject the required third harmonic into the input current to meet the requirement of IEC 61000-3-2 Class D or Energy Star. A method of fitting the duty cycle is further proposed for simplifying the circuit implementation. The experimental results from a 120-W universal input prototype are given to verify the effectiveness of the proposed method.

Index Terms—Discontinuous current mode (DCM), harmonic injection, power factor correction (PFC), storage capacitor.

I. INTRODUCTION

POWER factor correction (PFC) converters have been widely used in ac–dc power conversions to achieve high power factor (PF) and low harmonic distortion. The methods of achieving PFC can be classified into active and passive types. Generally, compared with passive PFC converters, active PFC converters can achieve a higher PF and a smaller size, especially at high power levels with input voltage of very low frequency (e.g., 50 Hz or 60 Hz) [1].

In a PFC converter, the input power is pulsating while the output power is constant. So, a storage capacitor with large capacitance is required for balancing the instantaneous power difference. The storage capacitor could be reduced by distorting the input current to some extent, and the “optimal input current” corresponding to different PF was given, which is complex for

precise implementation [2]. An approximate circuit realization method was proposed in [3]. Injecting the third harmonics into the input current could also reduce the storage capacitor [4]. Lamar *et al.* [5] defined a precise method to distort the input current in order to obtain a certain PF. Actually, the approaches proposed in [3]–[5] are that the reference signal of the input current is adjusted from the sinusoidal shape to the nonsinusoidal one, which is suitable for PFC converters with both voltage and current loop control.

Discontinuous current mode (DCM) boost PFC converter features zero-current turn-on for the switch and no reverse recovery of diode, and it operates in constant switching frequency, which is benefit for designing the inductor and electromagnetic interference filter. Meanwhile, the control is simple and the cost is low. A simplified design approach and the conduction boundary for DCM boost PFC converter were analyzed in [6] and [7], and the analysis of the interleaved DCM boost PFC converter was presented in [8] and [9]. The main drawback is that the PF is not so high, especially at high input voltage [10]. The input current of a DCM boost PFC converter mainly contains the third harmonic that has the initial phase of π in respect of the fundamental component. Therefore, compared to the PFC converter with unity PF, DCM boost PFC converter not only has lower PF, but also needs larger output storage capacitor. Some techniques for PF improvement of DCM boost PFC converter have been proposed in [11]–[22]. In [22], it showed that the control not only improves the PF to near unity, but also reduces the input power pulsation to some extent. This paper presents the further work of [22].

The objective of this paper is to propose a method of reducing the storage capacitor for the DCM boost PFC converter with input voltage range of 90–264 V_{ac}. Section II analyzes the input current harmonics of a DCM boost PFC converter and its effect on the input power pulsation. In Section III, the concept of the variable duty cycle control is presented to inject the third harmonic with initial phase of 0 in respect of the fundamental component. The normalized amplitudes of the third harmonic with the base of the fundamental component can be controlled to any value between 0 and 1, depending on the requirements of the regulation standards such as IEC 61000-3-2 Class D or Energy Star. The proposed method can achieve storage capacitor reduction of 63% over the constant duty cycle control, when the harmonic specification of IEC 61000-3-2 Class D is met. A method of fitting the duty cycle is further proposed for simplifying the circuit implementation. In Section IV, the comparison between the proposed fitting variable duty cycle control and the traditional constant duty cycle control is made in terms of the input current harmonics, output voltage ripple, and inductor

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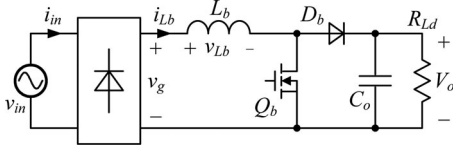


Fig. 1. Main circuit of the boost PFC converter.

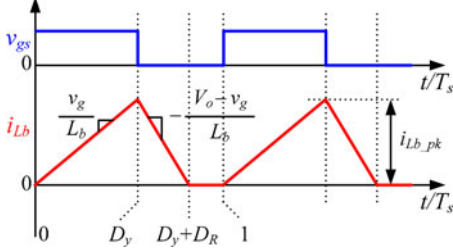


Fig. 2. Inductor current waveform in a switching cycle.

design. A 120-W prototype has been built and tested, and the experimental results are presented in Section V.

II. INPUT CURRENT HARMONICS OF A DCM BOOST PFC CONVERTER

Fig. 1 shows the main circuit of the boost PFC converter. Fig. 2 shows the inductor current waveform in a switching cycle when the converter operates at DCM.

The input voltage is defined as

$$v_{in}(t) = V_m \sin \omega t \quad (1)$$

where V_m is the amplitude of the input voltage and ω is the angular frequency of the input voltage.

During a line cycle, when the duty cycle is constant, assuming the efficiency of the converter is 100%, the average input current i_{in} , the duty cycle D_y , and the PF are expressed as [22]

$$i_{in}(t) = \frac{V_m D_y^2}{2L_b f_s} \frac{\sin \omega t}{1 - V_m |\sin \omega t| / V_o} \quad (2)$$

$$D_y = \frac{1}{V_m} \sqrt{\frac{2\pi L_b f_s P_o}{\int_0^\pi (\sin^2 \omega t / (1 - V_m |\sin \omega t| / V_o)) d(\omega t)}} \quad (3)$$

$$PF = \frac{\sqrt{2/\pi} \int_0^\pi (\sin^2 \omega t / (1 - V_m |\sin \omega t| / V_o)) d(\omega t)}{\sqrt{\int_0^\pi (\sin \omega t / (1 - V_m |\sin \omega t| / V_o))^2 d(\omega t)}} \quad (4)$$

where V_o is the output voltage, P_o is the output power, and f_s is the switching frequency.

For the simplicity of analysis, the average input current $i_{in}(t)$ is normalized with the base of $(V_m D_y^2 / 2L_b f_s)(1 / (1 - (V_m / V_o)))$, and the normalized input current $i_{in}^*(t)$ is plotted in Fig. 3. As seen, the shape of the average input current is only dependent on V_m / V_o , and the smaller the V_m / V_o , the closer to sinusoidal the current shape, which has been clearly explained in [22].

According to (4), when the output voltage is set to 400 V, the input PF can be plotted as the solid line shown in Fig. 4. It can

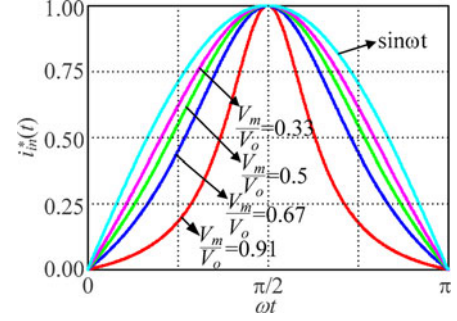


Fig. 3. Normalized input current waveform in a half line cycle.

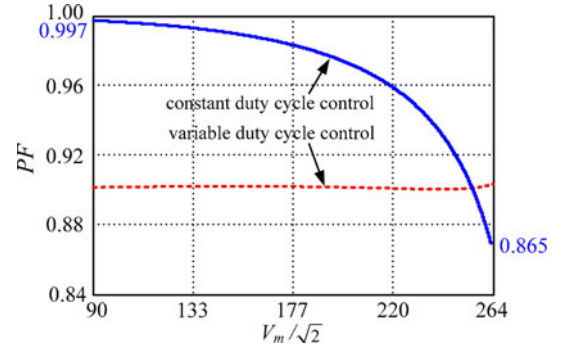


Fig. 4. PF comparison between constant and variable duty cycle control.

be seen that PF reduces when the input voltage increases. The PF is only 0.865 at the highest voltage of 264 V_{ac}.

By Fourier analysis, the harmonics of the input current can be obtained as

$$i_{in}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)] \quad (5)$$

where

$$a_n = \frac{2}{T_{line}} \int_0^{T_{line}} i_{in}(t) \cos(n\omega t) d(\omega t) \quad (n = 0, 1, 2, \dots)$$

$$b_n = \frac{2}{T_{line}} \int_0^{T_{line}} i_{in}(t) \sin(n\omega t) d(\omega t) \quad (n = 1, 2, 3, \dots) \quad (6)$$

where T_{line} is the period of the input voltage.

Substituting (2) into (5), the harmonics of the input current can be figured out, in which the cosine part and even the sinusoidal part are zero. The normalized amplitudes of the third, fifth, and seventh harmonics to the base of the fundamental component are plotted as the curves 6, 2, and 5 shown in Fig. 5. It should be noted that the negative amplitude means that the corresponding harmonic has an initial phase of π in respect of the fundamental component. As can be seen, the input current mainly contains the third harmonic with such a phase of π . The higher the input voltage, the higher the third harmonic.

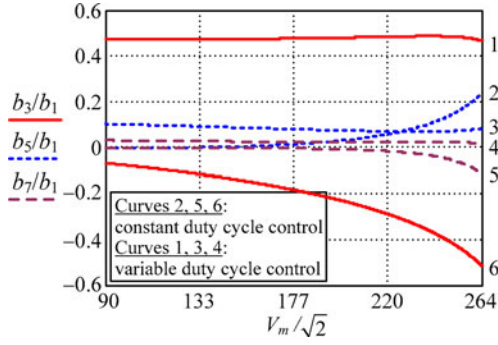


Fig. 5. Normalized amplitudes of the third, fifth, and seventh harmonics.

III. EFFECT OF THE THIRD HARMONIC CURRENT ON INPUT POWER PULSATION

When PFC is achieved, the fundamental input current i_{in1} is in phase with the input voltage v_{in} , i.e.,

$$i_{in1} = I_1 \sin \omega t \quad (7)$$

where I_1 is the amplitude of the fundamental component.

The instantaneous input power of the fundamental component is

$$p_{in1} = v_{in} i_{in1} = V_m I_1 \sin^2 \omega t. \quad (8)$$

If the input current contains the third harmonic with the initial phase of 0 in respect of the fundamental component, this third harmonic current can be expressed as

$$i_{in3} = I_3 \sin 3\omega t \quad (9)$$

where I_3 is the amplitude of the third harmonic current.

The instantaneous input power resulted by this third harmonic current is

$$p_{in3} = v_{in} i_{in3} = V_m I_3 \sin \omega t \sin 3\omega t. \quad (10)$$

If the third harmonic current has the initial phase of π in respect of the fundamental component, this third harmonic and its instantaneous input power can be expressed as

$$i_{in3-\pi} = I_3 \sin(\omega t - \pi) \quad (11)$$

$$p_{in3-\pi} = v_{in} i_{in3-\pi} = -V_m I_3 \sin \omega t \sin 3\omega t. \quad (12)$$

Fig. 6 shows the waveforms of v_{in} , i_{in1} , p_{in1} , i_{in3} , p_{in3} , $i_{in3-\pi}$, $p_{in3-\pi}$. The dashed area in the waveform of p_{in1} represents the energy the storage capacitor needs to charge or discharge when the input PF is unity. During the interval of $[T_{line}/8, 3T_{line}/8]$, the third harmonic with initial phase of π increases the pulsation of the input power. On the contrary, the third harmonic with initial phase of 0 could reduce the input power pulsation, and as a consequence, the storage capacitor can be reduced. Whatever the phase of the third harmonic is, it will reduce the PF. The input current harmonics of IEC 61000-3-2 is the absolute value, regardless of the initial phase. Therefore, the third harmonic with initial phase of 0 could be injected into the input current to reduce the storage capacitor.

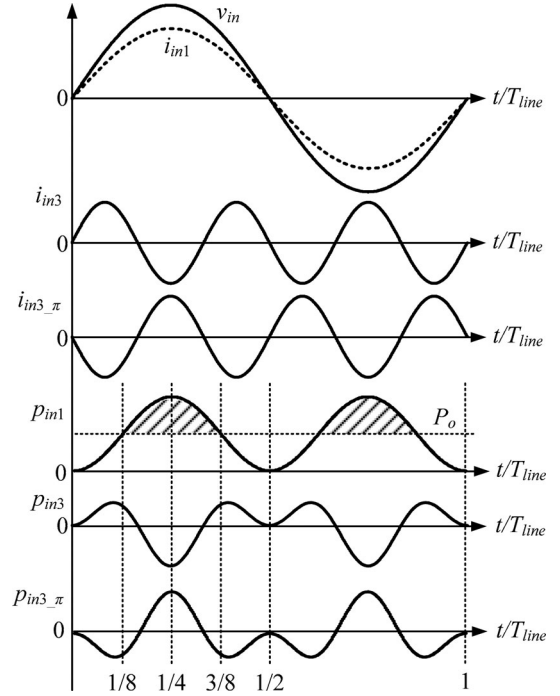


Fig. 6. Waveforms of the input voltage, fundamental input current and its power, third harmonic and its power.

While the third harmonic with initial phase of 0 is injected into the input current, the input current can be expressed as

$$i_{in}(t) = I_1 \sin \omega t + I_3 \sin 3\omega t = I_1 (\sin \omega t + I_3^* \sin 3\omega t) \quad (13)$$

where I_3^* is the normalized amplitude of the third harmonic with the base of fundamental component.

Meanwhile, the PF is

$$\text{PF} = \frac{1}{\sqrt{1 + I_3^{*2}}}. \quad (14)$$

The injected third harmonic should meet some regulation standards. For instance, according to IEC 61000-3-2 Class D, for 230-V_{ac} and 120-V_{ac} grid, the rate of third harmonic to the input power should meet the following equations, respectively:

$$\frac{I_3}{P_{in}} = \frac{I_3^* I_1}{230 I_1} \leq 3.4 \times 10^{-3}. \quad (15a)$$

$$\frac{I_3}{P_{in}} = \frac{I_3^* I_1}{120 I_1} \leq 1.76 \times 3.4 \times 10^{-3}. \quad (15b)$$

From (15), $I_{3-\max}^* = 0.718$ is obtained.

For Energy Star, the PF should be higher than 0.9; then $I_{3-\max}^* = 0.484$ [23].

Assuming the efficiency of the converter is 100%, i.e., the average input power equals the output power, then

$$\begin{aligned} P_{in} &= P_o = \frac{1}{\pi} \int_0^\pi v_{in}(t) i_{in}(t) d(\omega t) \\ &= \frac{1}{\pi} \int_0^\pi V_m \sin \omega t \cdot I_1 (\sin \omega t + I_3^* \sin 3\omega t) d\omega t = \frac{V_m I_1}{2}. \end{aligned} \quad (16)$$

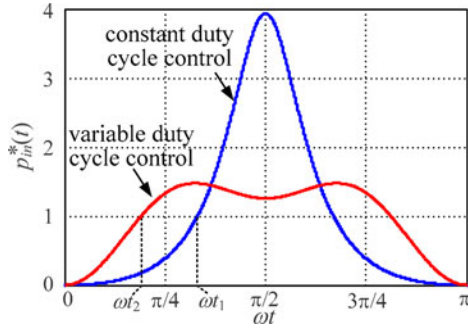


Fig. 7. Normalized instantaneous input power in a half line cycle with constant duty cycle control and variable duty cycle control.

From (1), (13), and (16), the normalized instantaneous input power is derived as

$$p_{in-2}^*(t) = \frac{v_{in}(t)i_{in}(t)}{P_o} = 2 \sin \omega t (\sin \omega t + I_3^* \sin 3\omega t). \quad (17)$$

When the DCM boost PFC converter is operated with constant duty cycle control, from (1)–(3), the normalized instantaneous input power is derived as

$$p_{in-1}^*(t) = \frac{v_{in}(t)i_{in}(t)}{P_o} = \frac{\sin^2 \omega t / (1 - a |\sin \omega t|)}{(1/\pi) \int_0^\pi (\sin^2 \omega t / (1 - a |\sin \omega t|)) d(\omega t)}. \quad (18)$$

where $a = V_m/V_o$.

According to (17) and (18), the normalized instantaneous input powers with constant and variable duty cycle control in a half line cycle are depicted in Fig. 7. When $p_{in}^*(t) > 1$, the storage capacitor C_o is charged, and when $p_{in}^*(t) < 1$, C_o is discharged. The energy discharging C_o (which equals the charged energy) in a half line cycle with constant duty cycle control and variable duty cycle control are

$$\Delta E_1^* = \frac{2 \int_0^{t_1} [1 - p_{in-1}^*(t)] dt}{(T_{line}/2)} \quad (19a)$$

$$\Delta E_2^* = \frac{2 \int_0^{t_2} [1 - p_{in-2}^*(t)] dt}{(T_{line}/2)} \quad (19b)$$

respectively, where t_1 and t_2 are the time instants when $p_{in}^*(t)$ crosses 1 with constant duty cycle control and variable duty cycle control, respectively.

ΔE_1^* and ΔE_2^* can be also expressed as

$$\begin{aligned} \Delta E_1^* &\approx \frac{(1/2)C_o(V_o + (\Delta V_{o1}/2))^2 - (1/2)C_o(V_o - (\Delta V_{o1}/2))^2}{P_o T_{line}/2} \\ &= \frac{2C_o V_o \cdot \Delta V_{o1}}{P_o T_{line}} \end{aligned} \quad (20a)$$

$$\begin{aligned} \Delta E_2^* &\approx \frac{(1/2)C_o(V_o + (\Delta V_{o2}/2))^2 - (1/2)C_o(V_o - (\Delta V_{o2}/2))^2}{P_o T_{line}/2} \\ &= \frac{2C_o V_o \cdot \Delta V_{o2}}{P_o T_{line}} \end{aligned} \quad (20b)$$

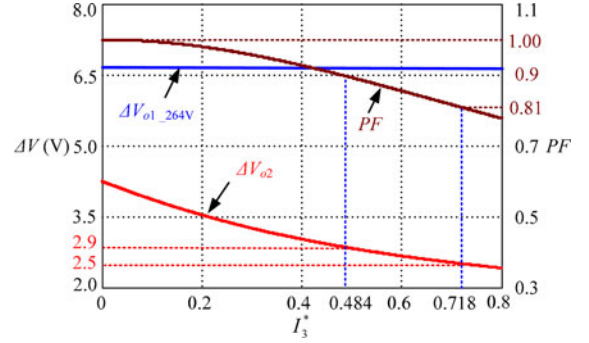


Fig. 8. Relationship of PF, ΔV_{o1} , and ΔV_{o2} with I_3^* .

where ΔV_{o1} and ΔV_{o2} are the output voltage ripple with constant duty cycle control and variable duty cycle control, respectively.

From (19) and (20), ΔV_{o1} and ΔV_{o2} are derived as

$$\Delta V_{o1} = \frac{2P_o \int_0^{t_1} [1 - p_{in-1}^*(t)] dt}{C_o V_o} \quad (21a)$$

$$\Delta V_{o2} = \frac{2P_o \int_0^{t_2} [1 - p_{in-2}^*(t)] dt}{C_o V_o}. \quad (21b)$$

According to (14) and (21), and the specifications of the converter which will be given in Section VI, the curves of PF and output voltage ripple can be plotted in Fig. 8. As seen, with constant duty cycle control, the output voltage ripple is 6.7 V when the input voltage is 264 V_{ac}. In compliance with IEC 61000-3-2 Class D, the maximum injected third harmonic is $I_3^* = 0.718$, and thus PF = 0.81, and the output voltage ripple is 2.5 V, which is 37% of that with constant duty cycle control. In other words, if the maximum output voltage ripple is the same, the storage capacitor can be reduced to 37% of that with constant duty cycle control. As for Energy Star specification of PF = 0.9, $I_3^* = 0.484$, and the output voltage ripple is 2.9 V. That is to say, the storage capacitor can be reduced to 43% while obtaining the same output voltage ripple.

IV. INJECTING THIRD HARMONIC WITH INITIAL PHASE OF ZERO

A. Ideal Duty Cycle

According to (13) and (16), the input current injected with the third harmonic with initial phase of 0 can be expressed as

$$i_{in}(t) = \frac{2P_o}{V_m} (\sin \omega t + I_3^* \sin 3\omega t). \quad (22)$$

From (2) and (22), in order to inject such a third harmonic into the input current, the duty cycle is

$$D_y = D_0 \sqrt{(1 - a |\sin \omega t|) (1 + 3I_3^* - 4I_3^* \sin^2 \omega t)} \quad (23)$$

where $a = V_m/V_o$, $D_0 = 2\sqrt{L_b f_s P_o}/V_m$.

B. Fitting Duty Cycle

The duty cycle expressed in (23) is very complicated to be implemented because several multipliers, divider, and square root extractor are needed. It is necessary to seek a function that fits (23), and it is more easily implemented.

Defining $y = |\sin \omega t|$, (23) can be rewritten as

$$D_y = D_0 \sqrt{(1 - ay)(1 + 3I_3^* - 4I_3^* y^2)}. \quad (24)$$

Based on Taylor's series, a function can be expanded around a point in the domain. So (24) can be expressed as

$$D_y = D_0 \left[\frac{\sqrt{(1 - ay_0)(1 + 3I_3^* - 4I_3^* y_0^2)}}{1} + \frac{12I_3^* a y_0^2 - 8I_3^* y_0 - a(1 + 3I_3^*)}{2\sqrt{(1 - ay_0)(1 + 3I_3^* - 4I_3^* y_0^2)}}(y - y_0) + \dots \right] \quad (25)$$

where y_0 is the expanded point.

Reserving only the constant and the first derivative item, (25) is approximated as

$$D_{y_fit} = D_1 \left[1 - \frac{a(1 + 3I_3^*) + 8I_3^* y_0 - 12I_3^* a y_0^2}{2(1 + 3I_3^*) - a(1 + 3I_3^*) y_0 - 4I_3^* a y_0^3} y \right] \quad (26)$$

where

$$D_1 = D_0 \frac{2(1 + 3I_3^*) - a(1 + 3I_3^*) y_0 - 4I_3^* a y_0^3}{2\sqrt{(1 - ay_0)(1 + 3I_3^* - 4I_3^* y_0^2)}}.$$

The selection of y_0 is very important to make the fitting duty cycle be accurate to the original duty cycle. Taking PF = 0.9 as an example and $I_3^* = 0.484$, then (26) is

$$D_{y_fit} = D_1 \left(1 - \frac{2.45a + 3.87y_0 - 5.81a y_0^2}{4.90 - 2.45a y_0 - 1.94a y_0^3} y \right). \quad (27)$$

Substituting (27) into (2) leads to, as shown (28), at the bottom of this page.

And the average input power is, as shown (29), at the bottom of this page.

$$i_{in}(t) = \frac{V_m D_1^2 \sin \omega t (1 - ((2.45a + 3.87y_0 - 5.81a y_0^2)/(4.90 - 2.45a y_0 - 1.94a y_0^3)) |\sin \omega t|)^2}{2L_b f_s (1 - a |\sin \omega t|)}. \quad (28)$$

$$\begin{aligned} P_{in} &= P_o = \frac{1}{T_{line}/2} \int_0^{T_{line}/2} v_{in}(t) i_{in}(t) dt \\ &= \frac{V_m^2 D_1^2}{2\pi L_b f_s} \int_0^\pi \frac{(\sin^2 \omega t) (1 - ((2.45a + 3.87y_0 - 5.81a y_0^2)/(4.90 - 2.45a y_0 - 1.94a y_0^3)) |\sin \omega t|)^2}{1 - a |\sin \omega t|} d(\omega t). \end{aligned} \quad (29)$$

$$\begin{aligned} PF &= \frac{P_{in}}{V_{in_rms} I_{in_rms}} = \frac{P_{in}}{(1/\sqrt{2}) V_m \sqrt{(1/(T_{line}/2)) \int_0^{T_{line}/2} (i_{in}(t))^2 dt}} \\ &= \frac{\sqrt{2/\pi} \int_0^\pi ((\sin^2 \omega t (1 - ((2.45a + 3.87y_0 - 5.81a y_0^2)/(4.90 - 2.45a y_0 - 1.94a y_0^3)) |\sin \omega t|)^2) / (1 - a |\sin \omega t|) d(\omega t)}{\sqrt{\int_0^\pi ((\sin^2 \omega t (1 - ((2.45a + 3.87y_0 - 5.81a y_0^2)/(4.90 - 2.45a y_0 - 1.94a y_0^3)) |\sin \omega t|)^4) / (1 - a |\sin \omega t|)^2) d(\omega t)}}. \end{aligned} \quad (30)$$

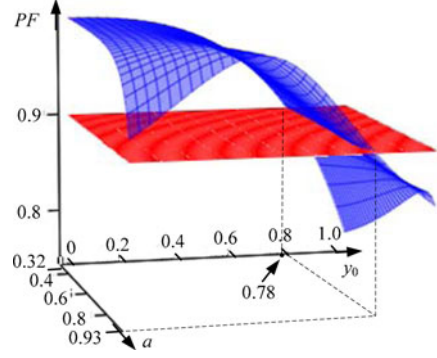


Fig. 9. Surface of the input PF as the functions of a and y_0 .

From (28) and (29), the PF is calculated, as shown (30), at the bottom of this page.

The PF is depicted in Fig. 9 according to (30). It can be seen that the surface of PF and the surface of "0.9" have an intersection line. As the input voltage ranges from 90 to 264 V_{ac}, the corresponding a ranges from 0.32 to 0.93. For $a = 0.32$ and $a = 0.93$ in the line, the value of y_0 is 0.78 and 0.8, respectively. Substituting $y_0 = 0.78$ into (30), the PF is higher than 0.9 over the whole input voltage range, which will be given in Section V-A. If y_0 is selected as 0.8, then PF = 0.891 with $a = 0.32$ can be obtained through calculation. So y_0 is selected to be 0.78.

Substituting $y_0 = 0.78$ into (27), the fitting duty cycle is expressed as

$$\begin{aligned} D_{y_fit} &= D_1 \left(1 - \frac{3 - 1.1a}{4.9 - 2.8a} |\sin \omega t| \right) \\ &= D_1 \left(1 - \frac{3V_o - 1.1V_m}{4.9V_o - 2.8V_m} |\sin \omega t| \right). \end{aligned} \quad (31)$$

C. Implementation of the Control Circuit

The control circuit can be implemented as shown in Fig. 10. The rectified input voltage is sensed through a voltage divider

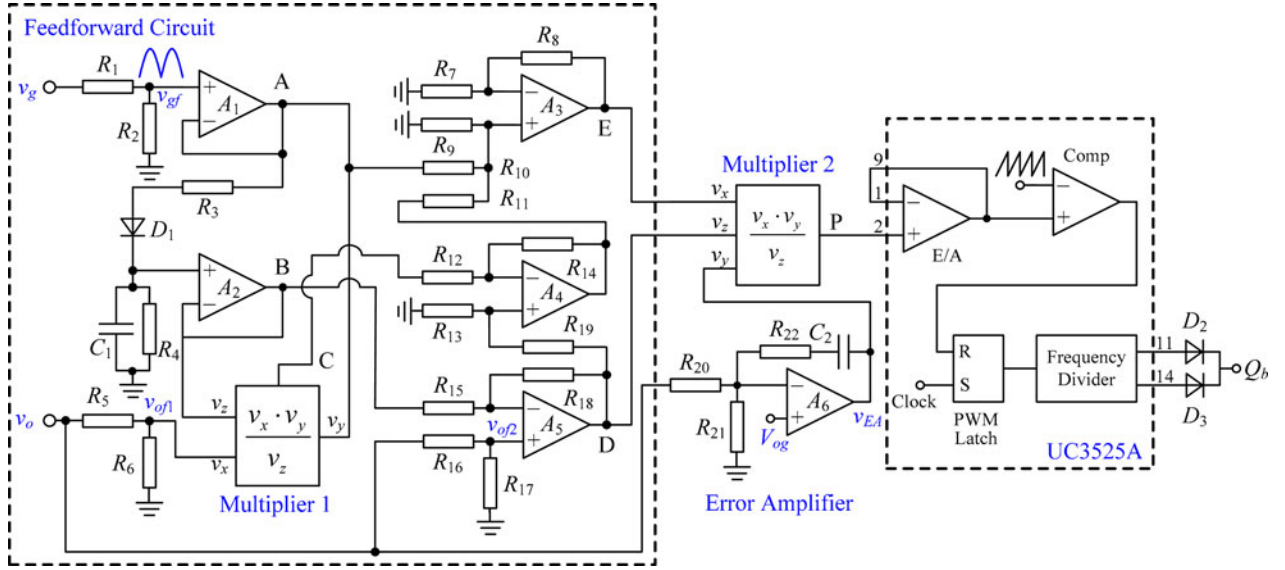


Fig. 10. Control circuit of the storage capacitor-less DCM boost PFC converter.

composed of R_1 and R_2 , and $v_A = k_{vg} V_m |\sin \omega t|$, where k_{vg} is the voltage sensor gain. R_3 , D_1 , C_1 , and R_4 are the circuit to obtain the peak value of the rectified input voltage, i.e., $v_B = k_{vg} \cdot V_m$. Please note that here R_3 is used to limit the charging current of C_1 , and it is very small compared to R_4 . The output voltage is sensed through a voltage divider composed of R_5 and R_6 , and the voltage sensor gain is purposely set to $1.94k_{vg}$; thus, $v_{of1} = 1.94k_{vg} V_o$. So the output of the Multiplier 1 is $v_c = 1.94k_{vg} V_o |\sin \omega t|$. The output voltage is sensed through a voltage divider composed of R_{16} and R_{17} , and the voltage sensor gain is purposely set to $1.29k_{vg}$, so $v_{of2} = 1.29k_{vg} V_o$.

Letting $R_{18} = 2.8R_{15}$, $R_{13} = R_{19}$, $R_{14} = 3.44R_{12}$, $R_9 = R_{11}$, $R_{10} = 0.41R_9$, and $R_7 = R_8$, then $v_z = k_{vg}(4.9V_o - 2.8V_m)$, $v_x = k_{vg}[4.9V_o - 2.8V_m - (3V_o - 1.1V_m)|\sin \omega t|]$. The output voltage is regulated through the error amplifier, and the sensed output voltage through a voltage divider composed of R_{20} and R_{21} compares with the reference voltage V_{og} . Here, V_{og} is set at 5.1 V, and the output voltage sense gain is set at $1/78.43$, i.e., $R_{20} = 77.43R_{21}$. R_{22} and C_2 form the compensation network and $v_y = v_{EA}$. v_x , v_y and v_z are sent to the multiplier, and $v_P = v_{EA}(1 - ((3V_o - 1.1V_m)/(4.9V_o - 2.8V_m))|\sin \omega t|)$. v_P is sent to the pulse width modulation (PWM) comparator and compared with the saw-tooth carrier, and the output of the PWM comparator determines the duty cycle, which varies as expressed in (31), where v_{EA} and the amplitude of the saw-tooth determine the coefficient D_1 . The components' values are listed in

Table I, where the no-nominal resistance is replaced by series or parallel resistors in practice.

V. PERFORMANCE COMPARISON

A. PF and the Input Current Harmonics

Substitution of $y_0 = 0.78$ into (30), the input PF with the fitting duty cycle control is plotted as the dashed line shown in Fig. 4. According to (5) and (28), the normalized amplitudes of the third, fifth, and seventh harmonics to the base of the fundamental component are plotted as the curves 1, 3, and 4 shown in Fig. 5. From the two figures, it can be seen that the PF is almost 0.9 over the whole input voltage range. The input current also contains a little fifth and seventh harmonics because the fitting duty cycle is adopted instead of the ideal one.

B. Reduction of the Output Voltage Ripple

When the fitting variable duty cycle control is employed, from (1), (28), and (29), the normalized instantaneous input power is, as shown (32), at the bottom of this page.

According to the specifications of the converter, which will be given in Section VI, ΔV_{o1} and ΔV_{o2} can be figured out according to (18), (21), and (32), as shown in Fig. 11. It can be seen that when the input voltage is 264 V_{ac}, the output voltage ripple is 6.7 V with the constant duty cycle and 2.75 V with the

$$\begin{aligned}
 p_{in-2}^*(t) &= \frac{v_{in}(t)i_{in}(t)}{P_o} \\
 &= \frac{(\sin^2 \omega t / (1 - a |\sin \omega t|)) (1 - ((3V_o |\sin \omega t| - 1.1V_m |\sin \omega t|) / (4.9V_o - 2.8V_m)))^2}{\frac{1}{\pi} \int_0^\pi ((\sin^2 \omega t (1 - ((3V_o |\sin \omega t| - 1.1V_m |\sin \omega t|) / (4.9V_o - 2.8V_m)))^2) / (1 - a \sin \omega t)) d(\omega t)}. \quad (32)
 \end{aligned}$$

TABLE I
COMPONENTS VALUE OF THE CONTROL CIRCUIT

R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}
10 k Ω	490 k Ω	1 k Ω	1 M Ω	490 k Ω	20 k Ω	10 k Ω	10 k Ω	15 k Ω	6.2 k Ω	15 k Ω	2.4 k Ω
R_{13}	R_{14}	R_{15}	R_{16}	R_{17}	R_{18}	R_{19}	R_{20}	R_{21}	R_{22}	C_1	C_2
10 k Ω	8.2 k Ω	3.9 k Ω	490 k Ω	13 k Ω	11 k Ω	10 k Ω	820 k Ω	10.6 k Ω	10 k Ω	1 μ F	1 μ F

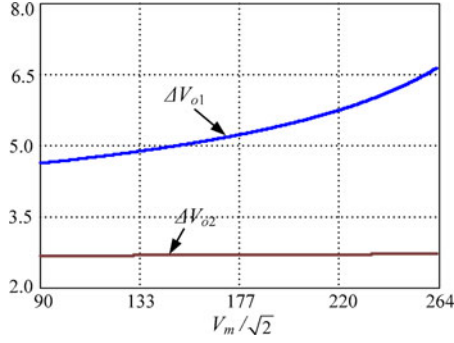


Fig. 11. Output voltage ripple with constant duty cycle control and variable duty cycle control.

fitting duty cycle control. If the maximum output voltage ripple is the same, the storage capacitor can be reduced to 41% of that with constant duty cycle control.

C. Design of the Inductor

In order to ensure the converter operates in DCM, the following condition should be met [22]:

$$D_y V_o / (V_o - V_m |\sin \omega t|) \leq 1. \quad (33)$$

Substituting (3) into (33), the critical boost inductor with constant duty cycle control is obtained as

$$L_{b1} \leq \frac{(1-a)^2 V_m^2}{2\pi P_o f_s} \int_0^\pi \frac{\sin^2 \omega t}{1-a|\sin \omega t|} d(\omega t). \quad (34)$$

Equation (29) can be rewritten, as shown (35), at the bottom of this page.

Substituting (35) into (31) leads to, as shown (36), at the bottom of this page.

Substituting (36) into (33), the critical boost inductor with variable duty cycle control is derived, as shown (37), at the bottom of this page.

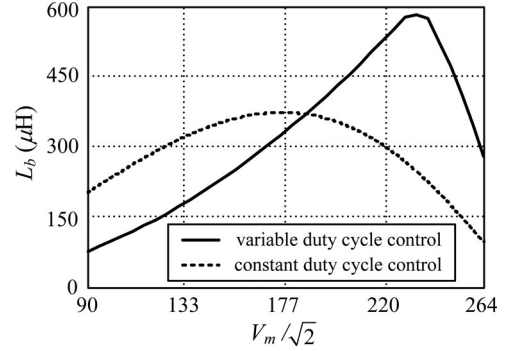


Fig. 12. Critical inductors over the input voltage range.

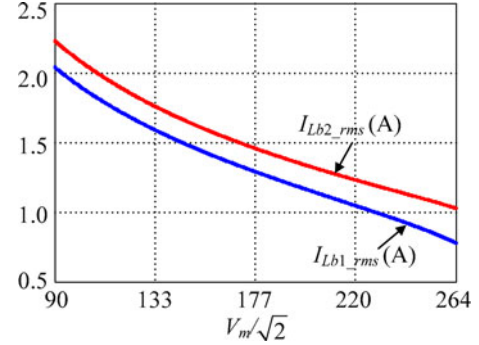


Fig. 13. RMS value of the inductor current with constant duty cycle and variable duty cycle control.

If $0.32 \leq a \leq 0.795$, then $(3 - 1.1a)/(4.9 - 2.8a) \geq a$, the minimum value of (37) occurs at $|\sin \omega t| = 0$, and the critical inductance is, as shown (38a), at the bottom of the next page.

If $0.795 \leq a \leq 0.93$, then $(3 - 1.1a)/(4.9 - 2.8a) \leq a$, the minimum value of (37) occurs at $|\sin \omega t| = 1$, and the critical inductance is, as shown (38b), at the bottom of the next page.

$$D_1 = \frac{1}{V_m} \sqrt{\frac{2\pi L_b f_s P_o}{\int_0^\pi ((\sin^2 \omega t)(1 - ((3 - 1.1a)/(4.9 - 2.8a)) |\sin \omega t|)^2 / (1 - a |\sin \omega t|)) d(\omega t)}}. \quad (35)$$

$$D_{y_fit} = \frac{(\sqrt{2\pi L_b f_s P_o} / V_m) (1 - ((3 - 1.1a)/(4.9 - 2.8a)) |\sin \omega t|)}{\sqrt{\int_0^\pi ((\sin^2 \omega t)(1 - ((3 - 1.1a)/(4.9 - 2.8a)) |\sin \omega t|)^2 / (1 - a |\sin \omega t|)) d(\omega t)}}. \quad (36)$$

$$L_{b2} \leq \frac{(V_m^2 / 2\pi P_o f_s) \int_0^\pi ((\sin \omega t)^2 (1 - ((3 - 1.1a)/(4.9 - 2.8a)) |\sin \omega t|)^2 / (1 - a |\sin \omega t|)) d(\omega t)}{(1 - ((3 - 1.1a)/(4.9 - 2.8a)) |\sin \omega t|)^2 (1 / (1 - a |\sin \omega t|))}. \quad (37)$$

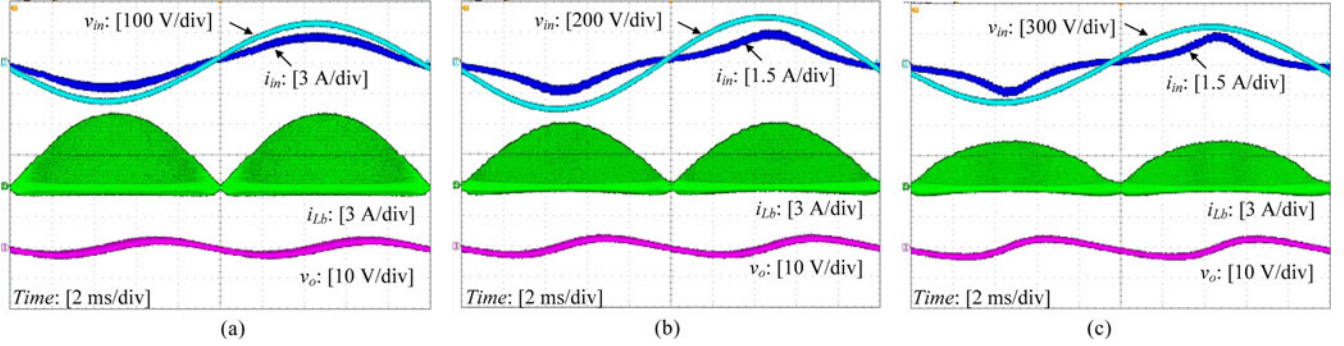


Fig. 14. Experimental waveforms of input voltage, input current, inductor current, and output voltage with constant duty cycle control: (a) 176 V; (b) 220 V; (c) 264 V.

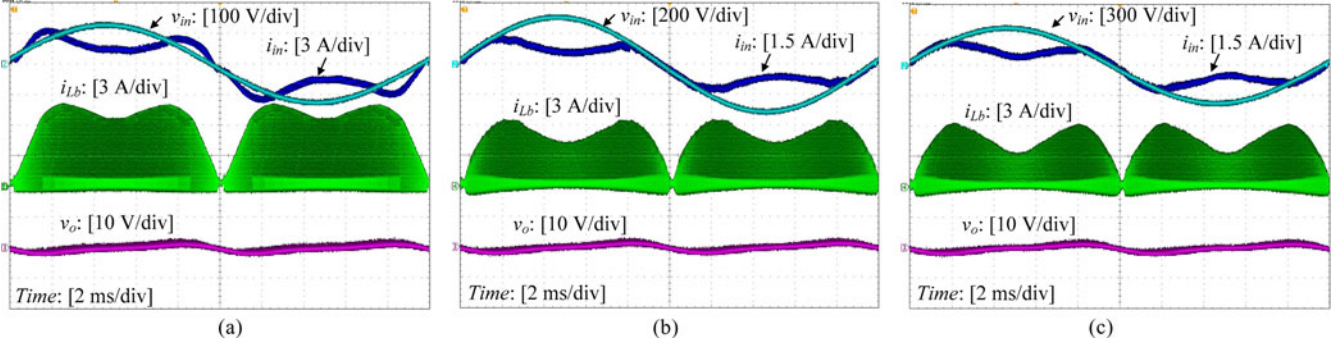


Fig. 15. Experimental waveforms of input voltage, input current, inductor current, and output voltage with variable duty cycle control: (a) 176 V; (b) 220 V; (c) 264 V.

According to the specifications of the converter, which will be given in Section VI, the critical boost inductor over the input voltage range with constant duty cycle control and fitting duty cycle control are depicted in Fig. 12, from which we choose $L_{b1} = 80 \mu\text{H}$ and $L_{b2} = 70 \mu\text{H}$.

The rms value of the inductor current in a line cycle is [22]

$$I_{Lb_rms} = \frac{V_m T_s}{L_b} \sqrt{\frac{2}{T_{line}} \int_0^{T_{line}} \frac{V_o D_y^3 \sin^2 \omega t}{3(V_o - V_m |\sin \omega t|)} dt}. \quad (39)$$

Substituting (3) and $L_{b1} = 80 \mu\text{H}$ into (39), and substituting (36) and $L_{b2} = 70 \mu\text{H}$ into (39), the rms value of the inductor current I_{Lb1_rms} with constant duty cycle control and I_{Lb2_rms} with variable duty cycle control can be obtained. The curves of I_{Lb1_rms} and I_{Lb2_rms} are plotted in Fig. 13. As seen, I_{Lb2_rms} is little higher than I_{Lb1_rms} . The increased rms current is due to the decrement of the inductor and increment of current ripple accordingly. Thus, the conduction loss of the switch and diode is little increased, leading to a slightly lower efficiency.

VI. EXPERIMENTAL VERIFICATION

In order to verify the validity of the proposed variable duty cycle control, a prototype has been built and tested in the laboratory. The specifications of the prototype are as follows:

- 1) input voltage $v_{in} = 90\text{--}264 \text{ V}_{ac}/50 \text{ Hz}$;
- 2) output voltage $V_o = 400 \text{ VDC}$;
- 3) output power $P_o = 120 \text{ W}$;
- 4) switching frequency $f_s = 100 \text{ kHz}$.

The power stage consists of the following devices and components:

- 1) input rectifier bridge RB: GBU406 (600 V, 4 A);
- 2) power switch Q_b : FCI11N60 (600 V, 11 A);
- 3) boost diode D_b : STTH8L06D (600 V, 8 A);
- 4) boost inductor: $80 \mu\text{H}$ (constant duty cycle control), $70 \mu\text{H}$ (variable duty cycle control);
- 5) output filter capacitor: $C_o = 220 \mu\text{F}$;
- 6) control IC: UC3525 A.

A small LC filter is added at the input side to attenuate the high-frequency current ripple, and the parameters of the LC filter are as follows:

$$L_{b2} = \frac{V_m^2}{2\pi P_o f_s} \int_0^\pi \frac{(\sin \omega t)^2 (1 - ((3 - 1.1a)/(4.9 - 2.8a)) |\sin \omega t|)^2}{1 - a |\sin \omega t|} d(\omega t). \quad (38a)$$

$$L_{b2} = \frac{(V_m^2/2\pi P_o f_s) \int_0^\pi ((\sin \omega t)^2 (1 - ((3 - 1.1a)/(4.9 - 2.8a)) |\sin \omega t|)^2 / (1 - a |\sin \omega t|) d(\omega t)}{((1 - ((3 - 1.1a)/(4.9 - 2.8a)))/(1 - a))^2}. \quad (38b)$$

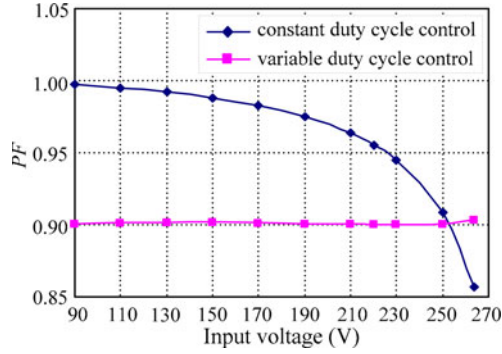


Fig. 16. Measured PF.

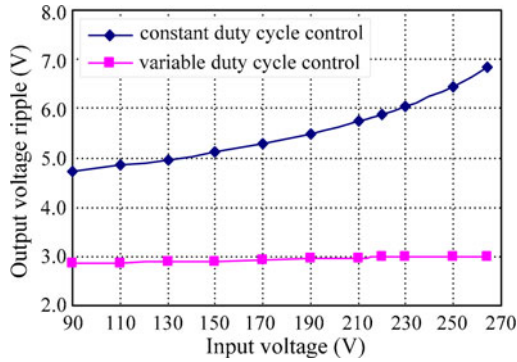


Fig. 17. Measured output voltage ripple.

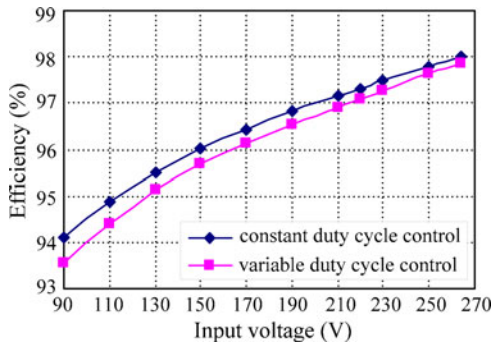


Fig. 18. Measured efficiency.

- 1) input filter inductor: $L_{in} = 230 \mu\text{H}$;
- 2) input filter capacitor: $C_{in} = 0.22 \mu\text{F}$.

Figs. 14 and 15 show the experimental waveforms of the input voltage, input current, boost inductor current, and output voltage with constant duty cycle and variable duty cycle control at $90 V_{ac}$, $220 V_{ac}$, and $264 V_{ac}$ input, respectively.

Figs. 16 and 17 show the measured input PF and output voltage ripple curve over the input voltage range, respectively, from which it can be seen that PF is almost 0.9 in the whole input voltage range and the output voltage ripple is greatly reduced. Fig. 18 shows the efficiency comparison; as seen, the efficiency is little decreased with variable duty cycle control. The experimental results agree well with the analysis.

VII. CONCLUSION

When the duty cycle is constant in a line cycle, the input current of DCM boost PFC converter contains the third harmonic with the initial phase of π in respect of the fundamental component. Consequently, the input PF is low, and a large storage capacitor is needed. A variable duty cycle control is proposed in this paper to make the input current contain only the third harmonic with the initial phase of zero. The proposed method greatly reduces the storage capacitor over the constant duty cycle control, while complying the regulation standards such as IEC 61000-3-2 Class D and Energy Star. A method of fitting the duty cycle is further proposed for simplifying the circuit implementation. The experimental results from a 120-W universal input prototype are given to verify the effectiveness of the proposed method. The proposed method is a tradeoff between the PF and the capacitor size. It is also a try so that the long lifetime capacitors such as film capacitor could be adopted in place of electrolytic capacitor.

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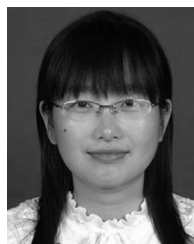


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