Single-Switch High Step-Up Converters With Built-In Transformer Voltage Multiplier Cell

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***Abstract*—In this paper, a built-in voltage gain extension cell is proposed to give a universal topology derivation on next-generation high step-up converters for large voltage gain conversion systems. Several improved single-switch high step-up converters with built-in transformer voltage multiplier cell are derived with some advantageous performance, which includes extremely large voltage conversion ratio, minimized power device voltage stress, effective diode reverse-recovery alleviation, and soft-switching operation. The turns ratio of the built-in transformer can be employed as another design freedom to extend the voltage gain, which shows great design flexibility. Compared with their active clamp counterpart, only one MOSFET is required to simplify the circuit configuration and improve the system reliability. The over resonance frequency and the below resonance frequency operation modes are studied to explore the circuit performance, and the key parameter design criterion is provided to show a valuable guidance for future industrial applications. Finally, the experimental results from a 500 W 36–380 V prototype are provided to validate the effectiveness of the main contributions in this paper.**

***Index Terms*—Built-in transformer, high step-up, voltage gain extension cell, voltage multiplier cell.**

I. Introduction

THE conventional single-switch boost converter, as shown in Fig. 1(a), is widely employed in the distributed front-end power factor correction applications, such as the server power systems due to its advantages of simple structure, low cost, and easy implementation [1], [2]. At ideal continuous current mode (CCM) operation, the voltage gain of the conventional boost converter is only determined by the switch duty cycle, which means only one control freedom is available to regulate the output voltage. Therefore, its optimal voltage conversion ratio is limited to approximately four times with a relatively high efficiency. However, nearly or even over 10 times of voltage gain is expected in some high step-up applications. For example, the automobile high-intensity-discharge headlamps usually need to convert 12 V onboard battery up to 100 V at steady operation, even to 400 V during the start-up stage [3]. The 48 V standard battery is required to be boosted to nearly 400 V for back-up uninterruptable power systems. Furthermore, the output voltage of the individual photovoltaic (PV) cell is generally lower than 60 V [4], [5]. However, the grid-connected ac voltage is 220 V for single-phase local utility in most countries, which also calls for high step-up and high-efficiency converters to realize the integrated PV modules. In these high step-up and high output voltage applications, the extremely large duty cycle is inevitable with the conventional boost converter, which increases the switch peak current, deteriorates the switching condition, and expands the conduction and switching losses. Furthermore, from the small-signal model analysis, once the duty cycle is close to 1, the dynamic response of the boost converters is limited because there is only a small duty cycle regulation range during the transient operation. How to realize high step-up dc/dc converters without extreme duty cycle to improve the system performance is becoming one of the most emergent technologies for power electrics researchers.

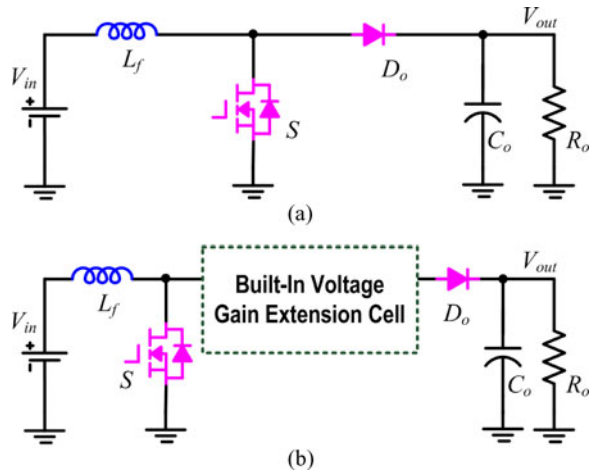

Fig. 1. Single-switch boost converters: (a) conventional boost converter and (b) conceptual high step-up converter.

A new class of single-switch high step-up dc/dc converters is proposed by introducing some passive voltage lift components in [6] and [7]. A voltage doubler cell is proposed to achieve nonisolated high step-up dc/dc converters by connecting many voltage doubler cells in cascaded structure [8]. The voltage gain of the singe-switch transformerless dc/dc topologies is twice of that of the conventional boost converter, where two similar inductors are charged in parallel and discharged in series [9]. However, the aforementioned converters operate at hard

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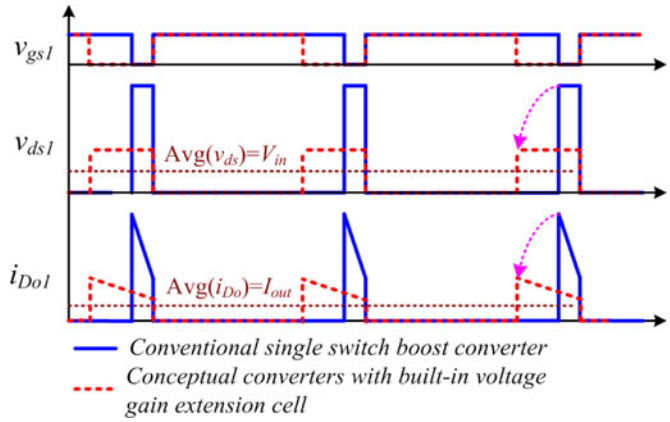

Fig. 2. Performance improvements of proposed conceptual converter with built-in voltage gain extension cell in high step-up applications.

switching condition and the diode reverse-recovery losses are considerable in the high output voltage applications. A zero voltage switching (ZVS) boost converter with voltage doubler cell is derived to reduce the switching losses [10]. One of the major limitations of the converters published in [6]–[10] is that these topologies cannot provide another controllable and flexible freedom except the duty cycle to obtain the large and wide voltage conversion.

In order to extend the voltage gain, avoid the extreme duty cycle operation, and reduce the switch voltage stress, a built-in voltage gain extension cell can be inserted into the conventional boost converter, which is plotted in Fig. 1(b). With the proposed built-in voltage gain extension cell, another control variable can be provided to achieve extremely high step-up conversion. The circuit performance improvements of the proposed conceptual converter in the large voltage conversion systems are depicted in Fig. 2, where v_{gs} and v_{ds} are the switch gate signal and drain-source voltage, respectively, i_{Do} is the output diode current. The solid line shows the steady-state waveforms for the conventional boost converter and the dashed line demonstrates the key waveforms for the conceptual high step-up boost converter. By inserting the built-in voltage gain extension cell, the switch voltage stress is reduced, the switch peak current is minimized, and the dynamic response may be enhanced because the turn-OFF period is greatly extended. A clear and advantageous circuit performance can be achieved in the high step-up applications. Therefore, how to realize the built-in voltage gain extension cell with simple but effective circuit components is an innovative and valuable solution to derive novel high step-up and high-efficiency converters.

The diode-capacitor voltage multiplier can be inserted into the conventional boost, Ćuk, Zeta, and Sepic converters to serve as the built-in voltage gain extension cell [11]–[14]. The voltage gain can be extended by making many diode-capacitor voltage multipliers in series. However, the circuit may be a little complex. A flexible and controllable variable is expected to appear on the voltage gain expression except the duty cycle to regulate the voltage conversion ratio. Generally, the turns ratio of the coupled inductor is one of the selectable control freedom to implement the built-in voltage gain extension cell. Recently, some single-phase coupled-inductor-based converters have been published in literatures to offer another design freedom rather than the switch duty cycle to satisfy the stringently high step-up requirements [15]–[23]. Some of them can be derived from the isolated flyback converters [15]. Some of them come from the composition of the conventional boost and flyback converter [16], and others can be taken as the integration of the coupled inductor and switched capacitor [17]–[19]. Furthermore, some voltage doubler, tripler, and quadrupler are integrated with the conventional single-switch boost converter to achieve an extremely large voltage conversion ratio [20]–[23]. Unfortunately, the input current ripple of most coupled-inductor-based converters is a little large because the input current is equal to the continuous magnetizing inductor current plus the reflected discontinuous secondary winding current. This makes the electrolytic capacitors in the input side indispensable. This has passive impact on the power density and circuit reliability improvements.

The transformer existed in the isolated converters is a pretty good component to regulate the circuit voltage conversion ratio and optimize the switch duty cycle. The built-in transformer concept can be also employed in the nonisolated converters to conduct as the voltage gain extension cell and achieve large and wide voltage conversion. Some single-phase built-in transformer based high step-up converters are proposed to achieve high step-up conversion, ZVS soft-switching operation, diode reverse-recovery alleviation, and low input current ripple [24], [25]. In these built-in transformer based converters, two active switches are required and both of them operate in the asymmetrical complementary manner.

In this paper, the active clamp switch in the single-phase high step-up built-in transformer based converter presented in [24] is replaced by a passive diode by exploring its detailed operation analysis. Furthermore, some other improved topologies are generated to better satisfy the extremely high step-up applications by introducing some topology derivation law. These proposed single-switch high step-up converters have quite simple circuit configuration and can reduce the system cost. Furthermore, zero current switching (ZCS) turn-ON condition is provided for the switch, and the diode reverse-recovery problem that existed in the conventional boost converters can be alleviated effectively by the inherent leakage inductance of the built-in transformer. In addition, the turns ratio of the transformer and the switch duty cycle can be both employed to achieve extremely large voltage conversion ratio with optimized circuit performance.

II. Topology Derivation and Circuit Operational Analysis

The published ZVS high step-up built-in transformer based converter in [24] is shown in Fig. 3(a). The built-in voltage multiplier cell is composed of a transformer, an active clamp switch S_c, a clamp capacitor C_c, a dc block capacitor C_b, a switched capacitor C_m, and a regenerative diode D_r. The turns ratio of the built-in transformer is another design freedom for the voltage gain extension. The switches S and S_c work with the asymmetrical complementary operation to regulate the voltage on the

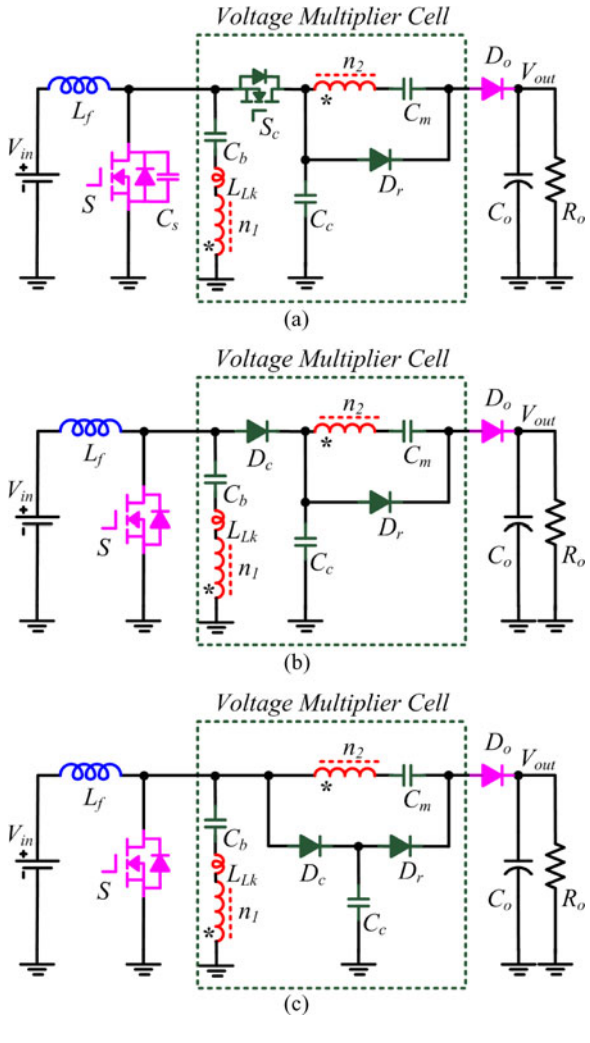

Fig. 3. High step-up built-in transformer based converter derivation: (a) ZVS high step-up converter with voltage multiplier cell; (b) derived single-switch high step-up converter; and (c) another improved single-switch high step-up converter.

capacitor C_c. ZVS soft-switching performance is achieved for the switches S and S_c due to the additional parallel capacitor C_s. The input current ripple is small due to its CCM operation to remove the large input electrolytic capacitors. As a result, this built-in transformer based converter is a good candidate for the high step-up and high-efficiency conversion systems.

However, from the detailed steady operation analysis of the ZVS high step-up converter in Fig. 3(a), during the active clamp switch S_c turn-ON stage, the clamp capacitor C_c is charged by the input inductor L_f through the clamp switch S_c, and the energy stored in the clamp capacitor is discharged to the load through the output diode D_o. It can be concluded that the discharging current of the clamp capacitor comes from the output current, and the clamp capacitor energy-charging path is not the same as the energy-discharging path. This means there is an existing discharging path for the clamp capacitor. The bidirectional power flow for the active clamp switch is not mandatory, which indicts that the auxiliary switch S_c can be replaced by a passive diode D_c. The derived single-switch high step-up converter is plotted in Fig. 3(b). The voltage gain of the converters in Fig. 3(a) and (b) are the same. Also, the clamp diode D_c can be shifted from the main power branch to the minor one to further enhance the circuit performance. The improved single-switch high step-up converter is introduced in Fig. 3(c). This improved version has some other clearly advantageous performance, which will be discussed in detail in the following sections. In the dashed block, a voltage multiplier cell is inserted to extend the voltage gain and reduce the switch voltage stress. The primary winding of the transformer has n_1 turns and its secondary winding has n_2 turns. $L_{\rm Lk}$ represents the leakage inductance of the transformer. N is defined as the turns ratio of n_2/n_1.

Based on the relationship between the switch turn-ON time and the resonance period caused by the leakage inductance $L_{\rm Lk}$ and the block capacitor C_b, there are two typical operation modes. The first one is named as the over resonance frequency (ORF) operation and the other one is the below resonance frequency (BRF) operation. In ORF mode, the switch turn-ON time DT_s is longer than the resonance period T_r caused by leakage inductance and block capacitor. The leakage current $i_{\rm Lk}$ is discontinuous and its key steady-state waveforms are shown in Fig. 4(a). On the contrary, in BRF mode, the switch turn-ON time DT_s is shorter than the resonance period T_r. The leakage current $i_{\rm Lk}$ keeps continuous and its corresponding key waveforms are described in Fig. 4(b). Each operation stages are analyzed briefly as follows. The equivalent circuits are demonstrated in Fig. 5.

A. ORF Operation ($T_r = \pi\sqrt{L_{\rm Lk}C_b} < DT_s$)

Stage 1 [t_0, t_1]: Before t_1, the switch S is in the turn-ON state and the voltage across the filter inductor L_f is the input voltage $V_{\rm in}$. The clamp diode D_c and the output rectifier D_o are reverse biased. And the energy stored in the clamp capacitor C_c is transferred to the switched capacitor C_m through the regenerative diode D_r and the secondary winding of the built-in transformer. The current of the switch is the summation of that of the filter inductor, leakage inductance, and secondary winding of the built-in transformer. The block capacitor C_b and the leakage inductance $L_{\rm Lk}$ begin to resonant

$$V_{T_s} = V_{C_m} - V_{C_c} \tag{1}$$

$$L_{\rm Lk}\frac{di_{\rm Lk}(t)}{dt} = V_{T_p} - V_{C_b}(t) \tag{2}$$

$$i_S(t) = i_{L_f}(t) + i_{\rm Lk}(t) + \frac{i_{\rm Lk}(t)}{N}. \tag{3}$$

Stage 2 [t_1, t_2]: At t_1, the current of the leakage inductance $L_{\rm Lk}$ resonates to zero and the regenerative diode D_r turns OFF naturally, which minimizes the regenerative diode reverse-recovery losses. The filter inductor current is still increased linearly due to the input voltage.

Stage 3 [t_2, t_3]: At t_2, the switch S turns OFF and then the clamp diode D_c and the output rectifier D_o turn ON to deliver the input energy to the output load. Part of another filter inductor energy transfers to the clamp capacitor C_c

$$i_{D_o}(t) = \frac{i_{\rm Lk}(t)}{N} \tag{4}$$

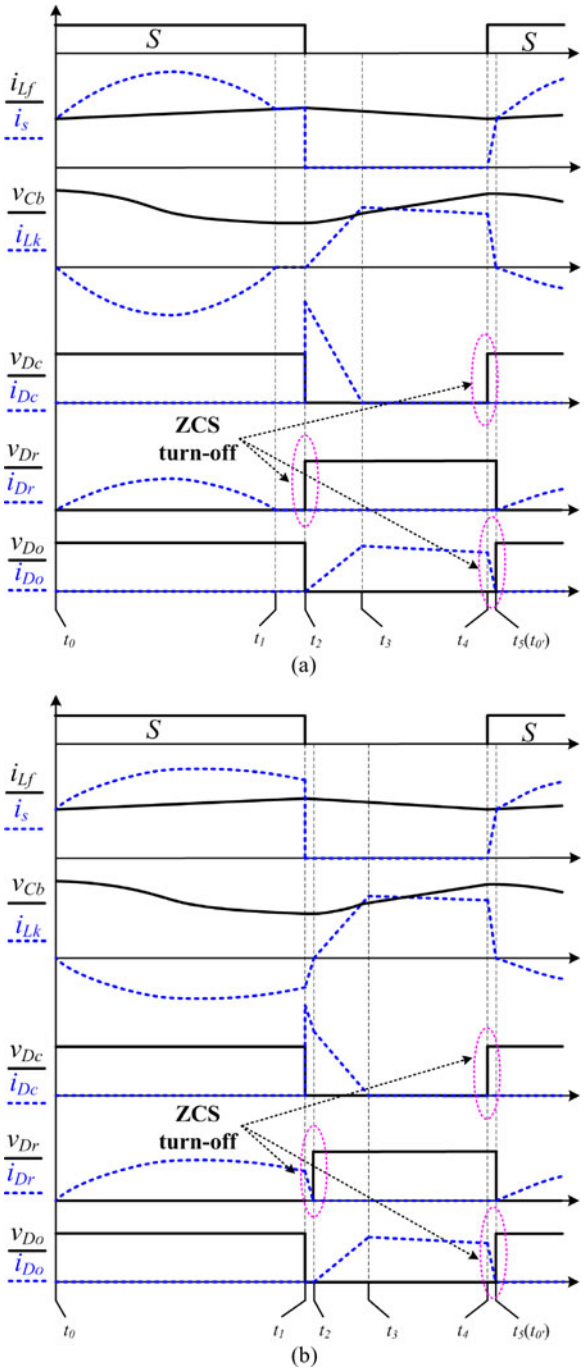

Fig. 4. Key steady-state waveforms of improved converter in Fig. 3(c): (a) ORF operation. (b) BRF operation.

$$i_{C_c}(t) = i_{L_f}(t) - i_{D_o}(t) - i_{\mathrm{Lk}}(t) \tag{5}$$

$$V_{T_s} = -V_{\mathrm{out}} + V_{C_c} + V_{C_m}. \tag{6}$$

Stage 4 [t_3, t_4]: At t_3, the clamp diode D_c turns OFF naturally, which alleviates the diode reverse-recovery problem. The filter inductor current is the summation of the leakage current and output diode current

$$i_{L_f}(t) = i_{D_o}(t) + i_{\mathrm{Lk}}(t). \tag{7}$$

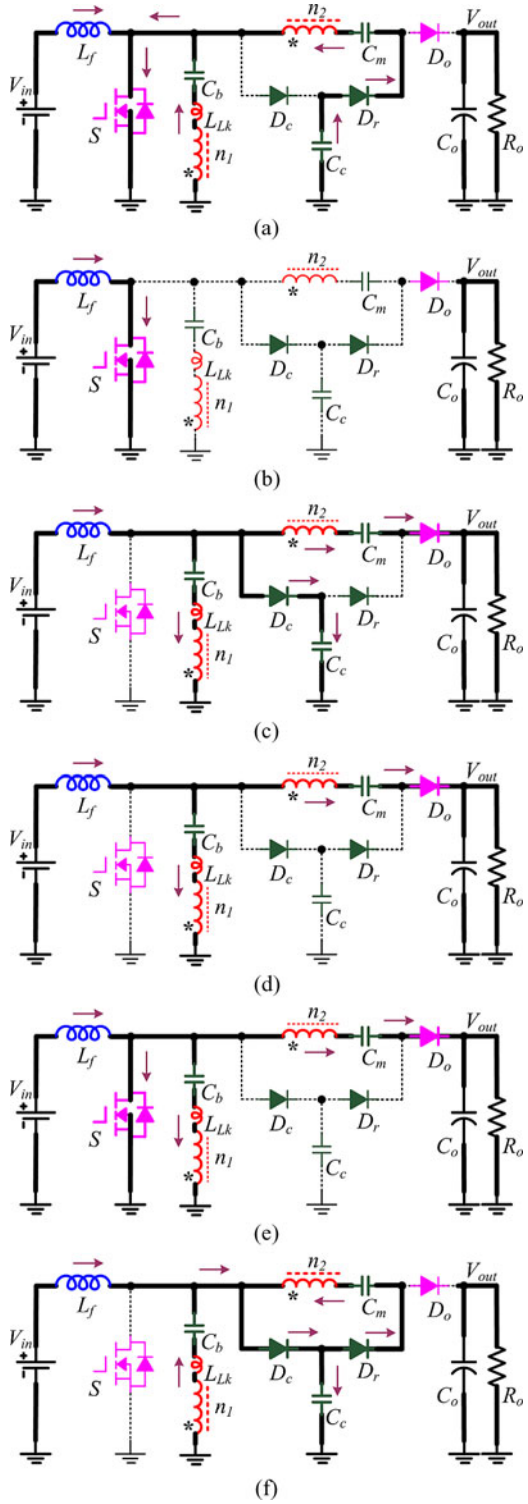

Fig. 5. Operational stages of proposed converter in ORF and BRF modes: (a) ORF stage 1 [t_0–t_1]; (b) ORF stage 2 [t_1–t_2]; (c) ORF stage 3 [t_2–t_3]; (d) ORF stage 4 [t_3–t_4]; (e) ORF stage 5 [t_4–t_5]; and (f) BRF stage 2 [t_1–t_2].

Stage 5 [t_4, t_5]: At t_4, the switch S turns ON with the ZCS soft-switching performance because its turn-ON current is increased linearly from zero. The filter inductor current starts to increase again, and the current of the leakage inductance L_{Lk} and that of

the output diode D_o decreases to zero at the end of this stage

$$V_{T_s} = -V_{\rm out} + V_{C_m} \tag{8}$$

$$L_{\rm Lk}\frac{di_{\rm Lk}}{dt} = V_{T_p} - V_{C_b}. \tag{9}$$

B. BRF Operation ($T_r = \pi\sqrt{L_{\rm Lk}C_b} > DT_s$)

During BRF operation, the leakage current $i_{\rm Lk}$ is still higher than zero when the switch S turns OFF. In this case, the operation of stage 2 has a small difference compared with the ORF operation whose equivalent circuit is plotted in Fig. 5(f). Once the switch S turns OFF, the clamp diode D_c starts to conduct to make the voltage on the secondary winding equal to that of the switched capacitor C_m. The leakage current $i_{\rm Lk}$ decreases quickly in an approximately linear way. The other stages in the BRF operation are the same as those of the ORF operation

$$V_{T_s} = -V_{C_m} \tag{10}$$

$$L_{\rm Lk}\frac{di_{\rm Lk}}{dt} = -V_{C_c} + V_{C_b} + V_{T_p}. \tag{11}$$

III. Circuit Performance Analysis and Discussion

A. Voltage Gain Expression

In order to simplify the derivation of the voltage gain of the improved high step-up converter with voltage multiplier cell, it is reasonable to taken the voltage ripple on the block capacitor C_b, the clamp capacitor C_c, and the switched capacitor C_m as zero. As a result, the voltage on C_c can be derived by employing the voltage-second balance principle on the input inductor L_f, which is given by

$$V_{C_c} = \frac{1}{1-D}V_{\rm in}. \tag{12}$$

The voltage on the block capacitor C_b is the average dc voltage of the switch S, which is obtained by

$$V_{C_b} = V_{C_c}(1-D) = V_{\rm in}. \tag{13}$$

When the switch S turns ON, the voltage on the primary winding of the built-in transformer V_{Tp} is the voltage on the block capacitor C_b. Its secondary winding voltage V_{Ts} is equal to the voltage on the switched capacitor C_m minus that on the clamp capacitor C_c. They are calculated by

$$V_{T_p} = V_{C_b} = \frac{V_{Ts}}{N} = \frac{V_{Cm} - V_{Cc}}{N}. \tag{14}$$

When the switch S is in the turn-OFF state, the output voltage is derived by

$$V_{\rm out} = V_{C_m} + V_{C_c} - V_{T_s}. \tag{15}$$

From (12) to (15), the voltage gain of the improved converter can be derived as follows:

$$M = \frac{V_{\rm out}}{V_{\rm in}} = \frac{N+2}{1-D}. \tag{16}$$

From (16), it can be seen that the turns ratio of the built-in transformer can serve as another control freedom to extend the voltage gain compared with the conventional boost converter. Furthermore, the voltage gain of the improved version is a little higher than that of ZVS high step-up built-in transformer based converter published in [24]. Even the turns ratio of the built-in transformer is zero, which means the transformer is removed from the proposed converter, the voltage gain of the simplified topology is doubled compared with the conventional boost converter. Great design flexibility is provided to achieve large and wide voltage conversion by regulating the built-in transformer turns ratio and the switch duty cycle alternatively.

B. Power Device Voltage and Current Stress Analysis

The voltage stresses of the switch S and the clamp diode D_c are equal to the voltage on the clamp capacitor C_c, which are given by

$$V_S = V_{\rm dc} = V_{C_c} = \frac{V_{\rm in}}{1-D} = \frac{V_{\rm out}}{N+2}. \tag{17}$$

From (17), it can be drawn that the switch voltage stress is decreased greatly as the turns ratio increases, which makes high-performance MOSFETs with low $R_{\rm DS\_ON}$ available to improve the circuit performance. The maximum switch voltage is only half of the high output voltage.

The voltage stress of the regenerative diode D_r is the same as that of the output diode D_o, which is equal to the output voltage minus the clamp capacitor voltage

$$V_{D_o} = V_{D_r} = V_{\rm out} - V_{C_c} = \frac{N+1}{1-D}V_{\rm in} = \frac{N+1}{N+2}V_{\rm out}. \tag{18}$$

From (18), it can be seen that the voltage stress of the output and regenerative diodes is lower than the output voltage. If the turns ratio of the built-in transformer is zero, the voltage stress of the output diode and the regenerative diode is only half of the output voltage.

For the current stress analysis, the clamp capacitor C_c is charged by the current across the clamp diode D_c. The switched capacitor C_m is charged by the current across the regenerative diode D_r and the discharging current of the switched capacitor C_m is equal to the output diode current i_{Do}. As a result, the average current of the diodes D_c, D_r, and D_o is the same. In order to simplify the analysis, the switch turn-ON period is assumed to be half of the resonant period, which is given as $DT_s \approx T_r/2$. In this case, the improved converter operates in critical mode, where the regenerative diode current is just decreased to zero when the switch turns ON. This assumption is reasonable to give an approximate result for the power device selection. The peak current of the diodes D_c, D_r, and D_o can be derived by

$$I_{\rm dc\_peak} \approx I_{\rm in} \approx \frac{(N+2)}{(1-D)}I_{\rm out} \tag{19}$$

$$I_{Dr\_peak} \approx \frac{\pi T_s}{T_r}I_{\rm out} \approx \frac{\pi}{2D}I_{\rm out} \tag{20}$$

$$I_{Do\_peak} \approx \frac{I_{Lf}}{N+1} \approx \frac{I_{\rm in}}{N+1} \approx \frac{(N+2)}{(N+1)(1-D)}I_{\rm out}. \tag{21}$$

and the switch peak current and rms current are calculated by

$$I_{S\_\text{peak}} \approx I_{\text{in}} + \frac{\pi T_s}{T_r} I_{\text{out}} \approx \frac{(N+2-\pi)D+\pi}{2(1-D)D} I_{\text{out}} \tag{22}$$

$$\begin{aligned} I_{\text{rms\_}S} &\approx \sqrt{\frac{1}{T_S}\int_0^{T_r/2}\left[\frac{(N+1)\pi T_s I_{\text{out}}}{T_r}\sin(\omega_r t) + I_{\text{in}}\right]^2 dt} \\ &\approx I_{\text{out}}\sqrt{\frac{1}{D}\left[\frac{(N+1)^2\pi^2}{8D^2} + \frac{(N+2)^2}{(1-D)^2} + \frac{2(N+2)(N+1)}{(1-D)D}\right]}. \end{aligned} \tag{23}$$

C. Diode Reverse-Recovery Alleviation

From the steady-state operation, it can be drawn that the clamp diode current is reduced to zero before it turns OFF, which means that is no reverse-recovery problem for the clamp diode. For the output diode, its turn-OFF current falling rate is controlled by the leakage inductance of the built-in transformer, which is derived by

$$\frac{di_{Do}(t)}{dt} = \frac{(N+1)V_{\text{out}}}{N(N+2)L_{\text{Lk}}}. \tag{24}$$

For the regenerative diode, there are two different cases based on the operation modes. In ORF operation, the current across the regenerative diode is resonated to zero before it turns OFF without any reverse-recovery problem. In BRF mode, its turn-OFF current falling rate is given by

$$\frac{di_{Dr}(t)}{dt} = \frac{V_{\text{out}}}{(N+2)L_{\text{Lk}}}. \tag{25}$$

From (24) and (25), it can be seen that the reverse-recovery problem can be alleviated effectively by employing a small leakage inductance as the turns ratio increases, which can reduce the electromagnetic interference noise and improve the circuit efficiency.

D. Circuit Performance Comparison and Evaluation

In summary, there are two fundamental schemes to provide another controllable freedom rather than the duty cycle to extend the voltage gain greatly without extremely large duty cycle. The first one is to employ the coupled inductor. In this case, the turns ratio of the coupled inductor can serve as another control variable to regulate the voltage gain. The other solution is to adopt the built-in transformer, where its turns ratio is used to control the output voltage. Furthermore, the switched capacitor technique can be combined with the coupled inductor or built-in transformer to derive advanced high step-up converters, which can further extend the voltage gain and reduce the switch voltage stress. Most of the recent published coupled-inductor-based high step-up converters can be regarded as the integration of the coupled inductor and switched capacitor techniques [17]–[23], which can achieve the voltage doubler, tripler, and quadrupler, and even higher voltage conversion ratio with several coupled inductor doubler cells in series. Meanwhile, the switch voltage stress can be reduced correspondingly. Moreover, the leakage energy can be recycled by employing active or passive clamp schemes, which cannot only suppress the possible turn-OFF voltage spikes on the power MOSFETs, but also provide ZVS or ZCS soft-switching operation. However, generally speaking, the topologies with higher voltage gain under the same duty cycle and turns ratio need more power diodes and switched capacitors, which may increase the circuit complexity and system cost. Consequently, a tradeoff should be made to optimize the converter performance based on the application specifications. In fact, the built-in transformer based converter can be also integrated with the switched capacitor technique to realize the voltage doubler, tripler, and quadrupler. These derived converters have quite similar circuit performance with the coupled-inductor-based converters, including the voltage gain, the power device voltage/current stress, leakage energy recycle solution, and regulation capability. One of the main differences is that an individual filter inductor is adopted in the input side to reduce the current ripple, which can benefit the input source, especially for the PV, fuel cells, and battery sources. The limitation of the built-in transformer based converters is that two magnetic components are required, which impact the power density improvement.

IV. Key Parameter Design Guidance

A. Turns Ratio of Built-In Transformer Selection

The turns ratio of the built-in transformer is the most significant parameter for the proposed converter because it determines the switch duty cycle, the power device voltage, and current stress, which is obtained by

$$N = \frac{V_{\text{out}}}{V_{\text{in}}}(1-D) - 2. \tag{26}$$

Once the switch duty cycle is selected, the turns ratio of the built-in transformer can be calculated and the power device voltage/current stress can be easily carried out.

B. Leakage Inductance of Built-In Transformer Design

The leakage inductance can be employed to control the output diode current falling rate and to alleviate the diode reverse-recovery problem. The relationship between the leakage inductance and the diode current falling rate is derived by

$$\frac{di_{Do}(t)}{dt} = \frac{(N+1)V_{\text{out}}}{N(N+2)L_{\text{Lk}}}. \tag{27}$$

It can be seen that the diode current falling rate is determined by the turns ratio, the output voltage, and the leakage inductance. As the turns ratio increases, a small leakage inductance is sufficient to alleviate the diode reverse-recovery problem.

C. Input Filter Inductor Selection

The input filter inductor L_f is designed to make that the input current ripple is approximately 20% of the average input current,

which is derived by

$$L_f = \frac{V_{\rm in} D}{\Delta I_{L_f} f_s}. \tag{28}$$

Due to the built-in voltage multiplier cell of the proposed converter, the switch duty cycle can be optimized to reduce the input current ripple, which can prolong the usage life of the PV arrays or the fuel cells.

D. Power Device Selection

Once the turns ratio of the built-in transformer is designed, the voltage and current stress of the switch and diodes can be derived. As a result, the power devices can be selected by considering some acceptable voltage and current margins.

E. Capacitor Design

How to suppress the voltage ripple on the clamp capacitor C_c and the switched capacitor C_m to a tolerant range is the main consideration for the capacitor design. The relationship between the voltage ripple and the output power can be derived by

$$C \geq \frac{P_{\rm out}}{V_{\rm out} \Delta V_c f_s} \tag{29}$$

where ΔV_c is the maximum tolerant voltage ripple on the capacitor C_c or C_m.

The design of the block capacitor is a little complex based on the operation modes. From the operation analysis, the required block capacitor can be obtained considering the proposed converter working in critical mode

$$C_b \approx \frac{D^2}{\pi^2 L_{\rm Lk} f_s^2}. \tag{30}$$

If the block capacitor is larger than the critical value, the proposed converter operates in BRF mode. However, a smaller block capacitor makes the proposed circuit in ORF mode. Generally speaking, a large block capacitor can minimize its voltage ripple, but it is bulky and costly. As a result, a compromise should be made to optimize the circuit performance.

V. Experimental Verification

In order to verify the effectiveness of the proposed converters, a 500 W prototype with the topology shown in Fig. 3(c) is built and tested. The main components and parameters are summarized in Table I.

For the magnetic components, the toroidal sendust core CS572125 from Magnetics is employed for the input filter inductor, and the input inductance is about 100 μH with 26 turns. The PQ3230 magnetic core is used for the built-in transformer with turns ratio of 17/7. The magnetizing inductance is about 260 μH and the leakage inductance is as 1.6 μH. For the power devices, IRFP4227 is selected as the switch. MUR820 is used for the clamp diode. Both the regenerative and output diodes are MUR1560. For the capacitors, the clamp capacitor is 2.2 μF and the switched capacitor is 1 μF. The output capacitor is 470 μF. The block capacitor has three choices, which can make the proposed converter operate in ORF, BRF, and critical modes with

TABLE I
Utilized Components and Parameters of Prototype

Components	Parameters
V_{in} (Input voltage)	*36V*
V_{out} (Output voltage)	*380 V*
P_{out} (Maximum output power)	*500 W*
f_s (Switching frequency)	*100 kHz*
L_f (Input filter inductor)	*100 μH*
N (Turns ratio n_2/n_1 of transformer)	*17/7*
L_m (Magnetizing inductor)	*260 μH*
L_{Lk} (Leakage inductance)	*1.6 μH*
S (Power MOSFET)	IRFP4227
D_c (Clamp diode)	MUR820
D_r and D_o (Diodes)	MUR1560
C_c (Clamp capacitor)	*2.2 μF*
C_b (Block capacitor)	*3.7, 6.9 or16.3 μF*
C_m (Switched capacitor)	*1 μF*
C_o (Output capacitor)	*470 μF*

$V_{\rm in} = 36$ V at 500 W full loads. In ORF operation, the block capacitor is 3.7 μF. In BRF operation, the block capacitor is about 16.3 μF. When the block capacitor is 6.9 μF, the proposed converter can operate in critical mode. The following experimental results are given with $P_{\rm out} \approx 500$ W and $V_{\rm in} = 36$ V. The key waveforms with different block capacitors are demonstrated in Figs. 6–8.

The gate signal/drain–source voltage of the switch S and the voltage/current waveforms of the clamp diode D_c are given in Fig. 6(a). The switch duty cycle is about 0.6 because the built-in transformer voltage multiplier cell provides another design freedom for the voltage gain extension. This is optimal for the input current ripple cancellation, dynamic response improvement, and power device peak current reduction. Moreover, the switch voltage stress is only about 90 V, which is far lower than the 380 V output voltage. As a result, the low-voltage-rated power MOSFETs with low $R_{\rm ds\_ON}$ can be used to improve the circuit performance. Furthermore, the clamp diode current decreases to zero before it turns OFF, which means there is no reverse-recovery problem for the clamp diode.

The voltage waveforms on the clamp capacitor C_c, block capacitor C_b, and switched capacitor C_m are shown in Fig. 6(b). The voltage on the clamp capacitor is about 90 V, which is equivalent to the switch voltage stress. The voltage on the block capacitor is nearly 40 V, which is the input voltage, and the voltage on the switched capacitor is almost 190 V.

The voltage and current waveforms of the regenerative and output diodes are plotted in Fig. 6(c). Both the regenerative and output diodes have the voltage stress of approximate 300 V, which is also lower than the output voltage. The turn-OFF current falling rate of the output diode is controlled by the leakage inductance of the built-in transformer, which effectively alleviates the output diode reverse-recovery problem.

The key current waveforms, including the input inductor current, the switch current, the clamp capacitor current, and the current across the second winding of the built-in transformer, are demonstrated in Fig. 6(d). Due to the input inductor and the

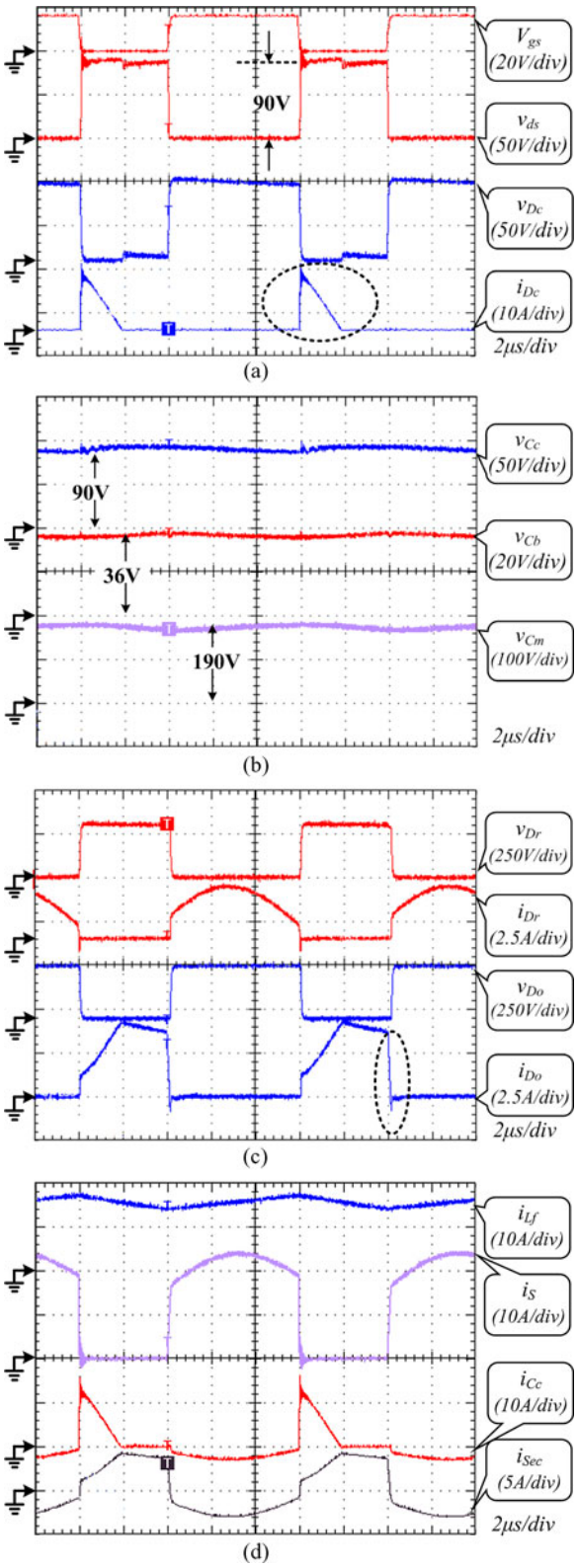

Fig. 6. Experimental results with $C_b = 16.3\ \mu$F: (a) waveforms of switch S and clamp diode D_c; (b) voltage waveforms of clamp capacitor C_c, block capacitor C_b, and switched capacitor C_m; (c) waveforms of regenerative diode D_r and output diode D_o; and (d) key current waveforms.

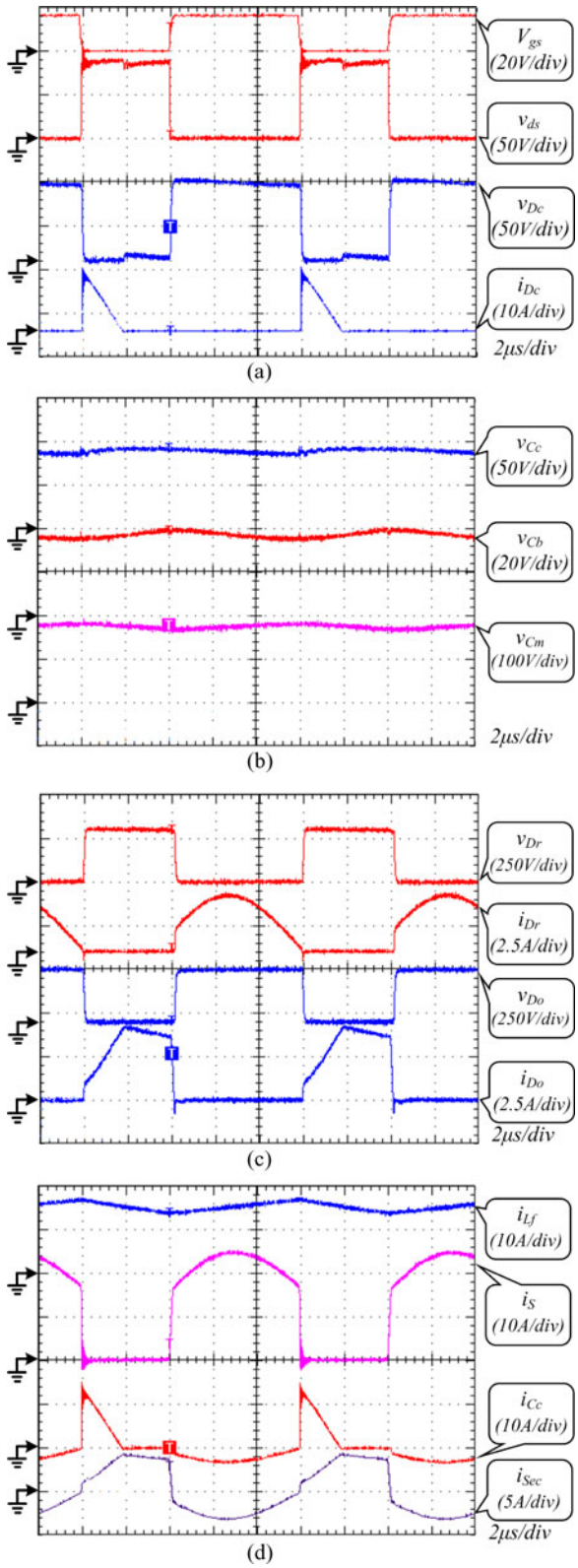

Fig. 7. Experimental results with $C_b = 6.9\ \mu$F: (a) waveforms of switch S and clamp diode D_c; (b) voltage waveforms of clamp capacitor C_c, block capacitor C_b, and switched capacitor C_m; (c) waveforms of regenerative diode D_r and output diode D_o; and (d) key current waveforms.

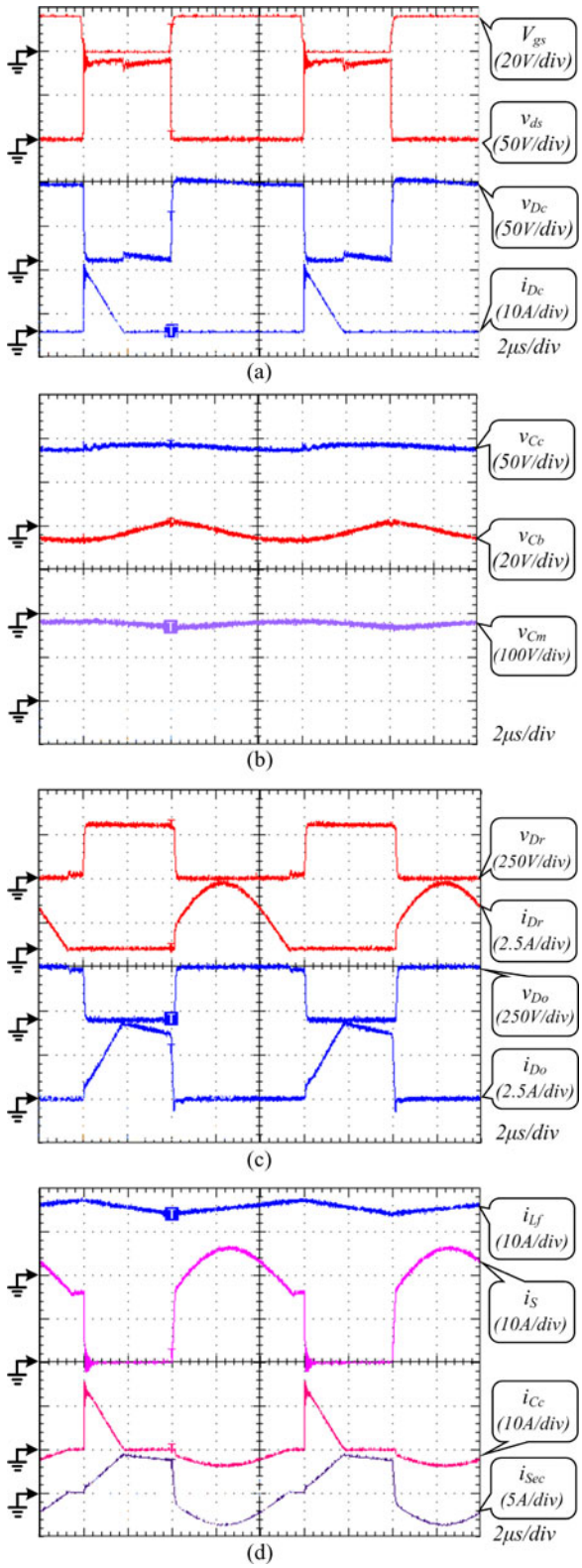

Fig. 8. Experimental results with $C_b = 3.7\ \mu$F: (a) waveforms of switch S and clamp diode D_c; (b) voltage waveforms of clamp capacitor C_c, block capacitor C_b, and switched capacitor C_m; (c) waveforms of regenerative diode D_r and output diode D_o; and (d) key current waveforms.

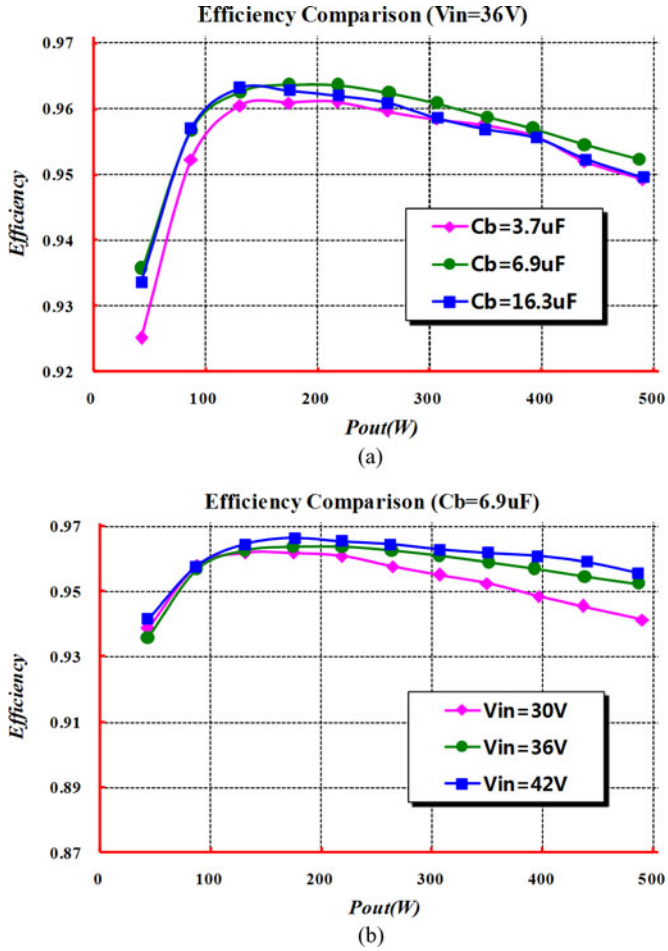

Fig. 9. Measured efficiency curves: (a) $V_{\rm in} = 36$ V with different block capacitors. (b) $C_b = 6.9\ \mu$F with different input voltages.

optimal operation without extreme duty cycle, the input current ripple is small, which can minimize the input capacitor and prolong the usage life of the input source. Furthermore, the switch current is flat, which can reduce the conduction losses.

The influence of different block capacitors on the circuit performance can be also found in Figs. 6–8. When the block capacitor is 16.3 μF, the proposed converter operates in BRF mode, where the current across the regenerative diode is still higher than zero when the switch turns ON, as shown in Fig. 6(c). This may increase the reverse-recovery losses a little although its turn-OFF current falling rate is controlled by the leakage inductance. When the block capacitor is 3.7 μF, the proposed converter works in ORF mode. The regenerative diode turns OFF naturally without reverse-recovery problem, which is shown in Fig. 8(c). However, in this case, the switch peak current increases a little, which is given in Fig. 8(d). When the block capacitor is changed to 6.9 μF, the proposed converter operates in critical mode, where the regenerative diode current is just decreased to zero when the switch turns ON. The corresponding waveforms are given in Fig. 7. In addition, the voltage ripple on the block capacitor is different with different values. The higher the block capacitor, the smaller the voltage ripple.

The measured efficiency of the proposed converter is plotted in Fig. 9. Fig. 9(a) shows the efficiency comparison with different block capacitors and $V_{\rm in} = 36$ V. The measured efficiency in the three cases is very close and the critical operation has the highest efficiency. The maximum efficiency of 96.6% and the efficiency of 95.6% at 500 W full loads are achieved with $C_b = 6.9$ μF. From the efficiency point of view, the critical operation mode can provide the optimal efficiency.

The tested efficiency comparison with different input voltages and $C_b = 6.9$ μF is given in Fig. 9(b). It can be seen that even the input voltages have a large variations; the conversion efficiency can be kept up to a high level within a large load range. Even though the input voltage is reduced to 30 V, the maximum efficiency is still over 96%.

VI. Conclusion

In this paper, the inherent limitation of the conventional boost converter in the high step-up applications is summarized and a voltage gain extension cell is proposed to provide a conceptual solution for high step-up, low cost, and high-efficiency conversion. Some improved single-switch high step-up converters with built-in transformer voltage multiplier cell are derived from their active clamp counterpart to simplify the circuit structure. These improved converters contain the following clear advantages: 1) The switch duty cycle and the turns ratio of the built-in transformer can be employed as two controllable variables to extend the voltage gain; 2) The power device voltage stress is far lower than the high output voltage; and 3) The diode reserve-recovery problem can be fully or partly solved based on the operation modes due to the leakage inductance. Experimental results have demonstrated that the proposed converters are excellent topology candidates for high future high step-up conversion systems.

References

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York: Kluwer, 2001.

[2] W. Li and X. He, "Review of non-isolated high step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[3] Q. Zhao and F. C. Lee, "High-efficiency, high step-up DC-DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.

[4] B. Yang, W. Li, Y. Zhao, and X. He, "Design and analysis of a grid-connected PV power system," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 992–1000, Apr. 2010.

[5] Q. Rong, W. Li, J. Shi, D. Yan, and X. He, "Performance analysis of a single stage single phase high step-up soft switching boost converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2011, pp. 859–863.

[6] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, "A family of single-switch PWM converters with high step-up conversion ratio," *IEEE Trans. Circuits Syst. I Regular Papers.*, vol. 55, no. 4, pp. 1159–1171, May 2008.

[7] E. H. Ismail, M. A. Al-Saffar, and A. J. Sabzali, "High conversion ratio DC–DC converters with reduced switch stress," *IEEE Trans. Circuits Syst. I Regular Papers.*, vol. 55, no. 7, pp. 2139–2151, Aug. 2008.

[8] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.

[9] L. S. Yang, T. J. Liang, and J. F. Chen, "Transformerless DC–DC converters with high step-up voltage gain," *IEEE Trans. Power Electron.*, vol. 56, no. 8, pp. 3144–3152, Aug. 2010.

[10] S. Park and S. Choi, "Soft-switched CCM boost converters with high voltage gain for high-power applications," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1211–1216, May 2010.

[11] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Hybrid switched-capacitor-Cuk/Zeta/Sepic converters in step-up mode," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2005, pp. 1310–1313.

[12] B. Axelrod, Y. Berkovich, S. Tapuchi, and A. Ioinovici, "Steep conversion ration Ćuk, Zeta, and sepic converters based on a switched coupled-inductor cell," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 3009–3014.

[13] Y. Berkovich, A. Shenkman, B. Axelrod, and G. Golan, "Structures of transformerless step-up and step-down controlled rectifiers," *IET Power Electron.*, vol. 1, no. 2, pp. 245–254, 2008.

[14] A. Shenkman, Y. Berkovich, and B. Axelrod, "Novel AC-DC and DC-DC converters with a diode-capacitor multiplier," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 40, no. 4, pp. 1286–1293, Oct. 2004.

[15] T. F. Wu, Y. S. Lai, J. C. Hung, and Y. M. Chen, "Boost converter with coupled inductors and buck–boost type of active clamp," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 154–162, Jan. 2008.

[16] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *Proc. IEE-Elect. Power Appl.*, vol. 151, no. 2, pp. 182–190, Mar. 2004.

[17] R. J. Wai and R. Y. Duan, "High step-up converter with coupled-inductor," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1025–1035, Sep. 2005.

[18] R. J. Wai and R. Y. Duan, "High-efficiency power conversion for low power fuel cell generation system," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 847–856, Jul. 2005.

[19] Y. Zhao, W. Li, Y. Deng, X. He, S. Lambert, and V. Pickert, "High step-up boost converter with coupled inductor and switched capacitor," in *Proc. IET Int. Conf. Power Electron. Mach. Drives*, 2010, pp. 1–6.

[20] Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "A novel high step-up DC–DC converter for a microgrid system," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1127–113, Apr. 2011.

[21] S. K. Changchien, T. J. Liang, J. F. Chen, and L. S. Yang, "Novel high step-up DC–DC converter for fuel cell energy conversion system," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2007–2017, Jun. 2010.

[22] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-up DC–DC converter with coupled-inductor and voltage-doubler circuits," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4196–4206, Sep. 2011.

[23] Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "Novel high step-up DC–DC converter with coupled-inductor and switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 998–1007, Feb. 2012.

[24] W. Li, W. Li, Y. Deng, and X. He, "Single-stage single-phase high-step-up ZVT boost converter for fuel-cell microgrid system," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3057–3065, Dec. 2010.

[25] H. L. Do, "A soft-switching DC/DC converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1193–1200, May 2010.

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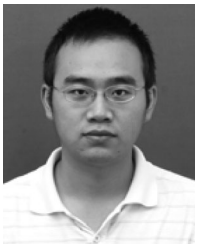

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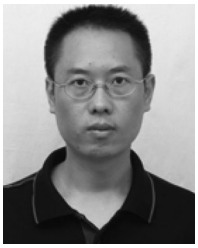

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