Soft-Switching SEPIC Converter With Ripple-Free Input Current

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***Abstract*—A soft-switching single-ended primary inductor converter (SEPIC) is presented in this paper. An auxiliary switch and a clamp capacitor are connected. A coupled inductor and an auxiliary inductor are utilized to obtain ripple-free input current and achieve zero-voltage-switching (ZVS) operation of the main and auxiliary switches. The voltage multiplier technique and active clamp technique are applied to the conventional SEPIC converter to increase the voltage gain, reduce the voltage stresses of the power switches and diode. Moreover, by utilizing the resonance between the resonant inductor and the capacitor in the voltage multiplier circuit, the zero-current-switching operation of the output diode is achieved and its reverse-recovery loss is significantly reduced. The proposed converter achieves high efficiency due to soft-switching commutations of the power semiconductor devices. The presented theoretical analysis is verified by a prototype of 100 kHz and 80 W converter. Also, the measured efficiency of the proposed converter has reached a value of 94.8% at the maximum output power.**

***Index Terms*—SEPIC converter, voltage multiplier, zero-current-switching (ZCS), zero-voltage-switching (ZVS).**

I. Introduction

SEPIC converters have been adopted for many applications such as power factor correction [1]–[5], photovoltaic system [6], [7], and LED lighting [8]–[11]. However, it has several drawbacks. Its two major drawbacks are high voltage stresses of power semiconductor devices and low efficiency due to hard-switching operation of the power switches. Especially in high-voltage applications, higher voltage rated power semiconductor devices should be used. When the voltage rating is higher, the $R_{\mathrm{ds(on)}}$ of power MOSFETs is higher. So, it causes higher conduction loss at the same level current. Therefore, if the voltage stress is reduced at the same level current, the overall efficiency can be improved. To reduce the voltage stress and increase the voltage gain, voltage multiplier techniques are proposed in [1], [12]–[15].

In order to reduce the volume and weight of the converter, soft-switching techniques such as zero-voltage-switching (ZVS) and zero-current-switching (ZCS) are necessary. High-frequency operation of dc–dc converters allows reduction of the volume and weight of their magnetic components. However, switching losses and electromagnetic interference noises are significant in high-frequency operation. Therefore, various soft-switching techniques have been introduced. Among them, the active clamp technique is often used to limit the voltage spike effectively, achieve soft-switching operation, and increase the system efficiency [16]–[21].

SEPIC converters can have a low input current ripple, which is one of the advantages of SEPIC converters. However, a bulk inductor should be used to minimize the current ripple. Input current ripple becomes one of important requirements due to the wide use of low voltage sources such as batteries, super capacitors, and fuel cells. It is because large ripple current may shorten the lifetimes of those input sources [22]–[24].

In [25], a ZCS PWM SEPIC Converter was proposed. Two switches can operate with soft switching. However, three power diodes and three separate inductors are utilized. The voltage stress of the power switches is the sum of the input voltage and the output voltage which is equal to that in the conventional SEPIC converter. In [26], a resonant step up/down converter was proposed. Sort-switching operation is achieved. Two power switches and two magnetic components are required. However, it has a pulsating input current and an additional filter stage is required in the input stage to suppress the input current ripple. Therefore, the number of magnetic components can be increased. In [27], a bidirectional ZVS PWM SEPIC/ZETA converter was proposed. Two main switches can operate with soft switching. However, a bidirectional switch consisting of two power MOSFETs is required. Many switches are required and also complex driving circuits for them are required. Moreover, the voltage stress of the switches is equal to that in the conventional SEPIC converter. In addition, a snubber circuit is required to suppress the parasitic voltage ringings across the bidirectional switches.

A soft-switching SEPIC converter with ripple-free input current is proposed. An auxiliary switch and a clamp capacitor are added to the conventional SEPIC converter. A coupled inductor and an auxiliary inductor are utilized to obtain ripple-free input current and achieve ZVS operation of the main and auxiliary switches. The voltage stresses of the power switches and diode are reduced by half by utilizing the voltage multiplier technique. Moreover, the reverse-recovery loss of the output diode is significantly reduced due to the resonance between the resonant inductor and the capacitor in the multiplier circuit. The proposed converter achieves high efficiency due to soft-switching characteristics of power semiconductor devices. The theoretical analysis is verified by an 80-W experimental prototype with 48–200 V conversion.

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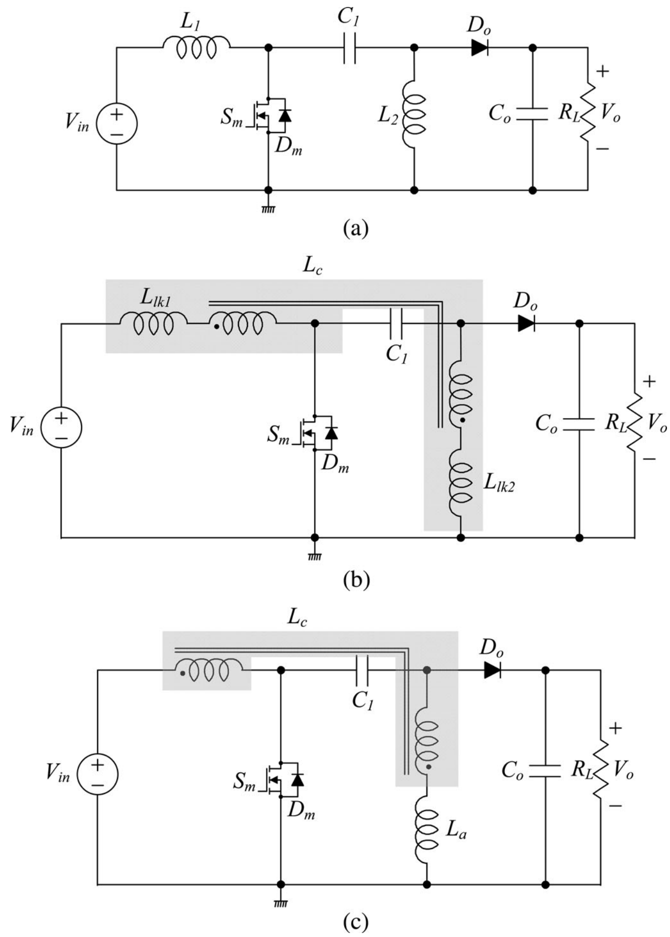

Fig. 1. SEPIC converters. (a) Conventional SEPIC converter. (b) Ripple-free SEPIC converter with a loosely coupled inductor. (c) Ripple-free SEPIC converter with a tightly coupled inductor.

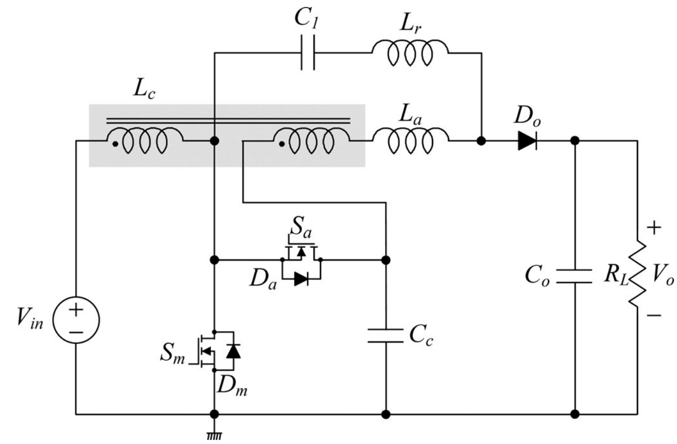

Fig. 2. Proposed soft-switching ripple-free SEPIC converter.

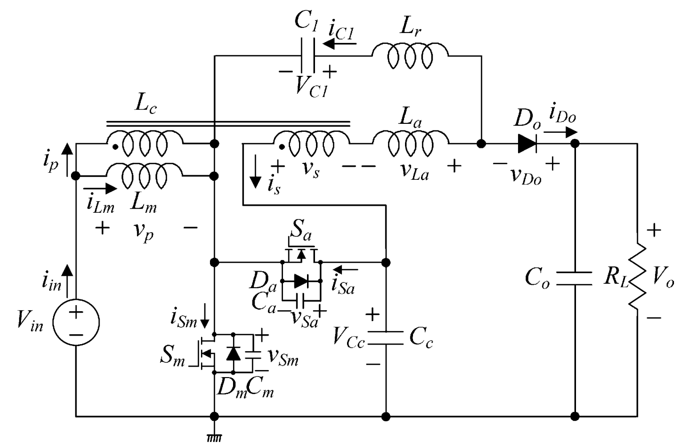

Fig. 3. Equivalent circuit of the proposed converter.

II. Analysis of the Proposed ZVS Resonant SEPIC Converter

The conventional SEPIC converters are shown in Fig. 1. The separate inductor version is shown in Fig. 1(a) and the coupled inductor version is shown in Fig. 1(b). In the coupled inductor version, a loosely coupled inductor L_c is used instead of two separate inductors L_1 and L_2. L_{lk1} and L_{lk2} imply the leakage inductances of the coupled inductor. The coupled inductor version has advantages such as single magnetic component and a ripple-free input current. The ripple-free condition is related with the magnetizing inductance, the turn ratio, and the leakage inductance L_{k2} of the coupled inductor. However, the leakage inductance is hard to control in mass production. Fortunately, the leakage inductance L_{k1} is not related with the ripple-free condition. Therefore, a tightly coupled inductor can be used with an additional inductor L_a instead of L_{k2} as shown in Fig. 1(c).

The circuit diagram of the proposed soft-switching SEPIC converter with a ripple-free input current is shown in Fig. 2. In the proposed converter, the resonant inductor L_r and the active clamp cell consisting of the auxiliary switch S_a and the clamp capacitor C_c are added to the conventional SEPIC converter shown in Fig. 1(c). The equivalent circuit of the proposed converter is shown in Fig. 3. The coupled inductor L_c is modeled as the magnetizing inductance L_m and an ideal transformer with a turn ratio of 1:n. The diodes D_a and D_m are the intrinsic body diodes of the auxiliary switch S_a and the main switch S_m. The capacitors C_a and C_m are their parasitic output capacitances. Key waveforms of the proposed converter are shown in Fig. 4. The switches S_a and S_m are operated asymmetrically and the duty ratio D is based on the main switch S_m. The operation of the proposed converter in one switching period T_s can be divided into five modes as shown in Fig. 5. To simplify the steady-state analysis, it is assumed that those capacitors C_1, C_c, and C_o have large values and the voltage ripples across them can be ignored.

Prior to mode 1, the auxiliary switch S_a is conducting. The magnetizing inductance current i_{Lm} is approaching to its minimum value I_{Lm2} and the auxiliary inductor current i_{La} is approaching to its maximum value I_{La1}. And the output diode is not conducting.

Mode 1 [t_0, t_1]: At t_0, the auxiliary switch S_a is turned OFF. Then, the energy stored in the magnetic components such as L_m, L_r, and L_a starts to charge C_a and discharge C_m. Therefore, the voltage v_{Sa} across the auxiliary switch S_a starts to rise from zero and the voltage v_{Sm} across the main switch S_m starts to fall from V_{Cc}. Since the capacitors C_a and C_m are very small, the

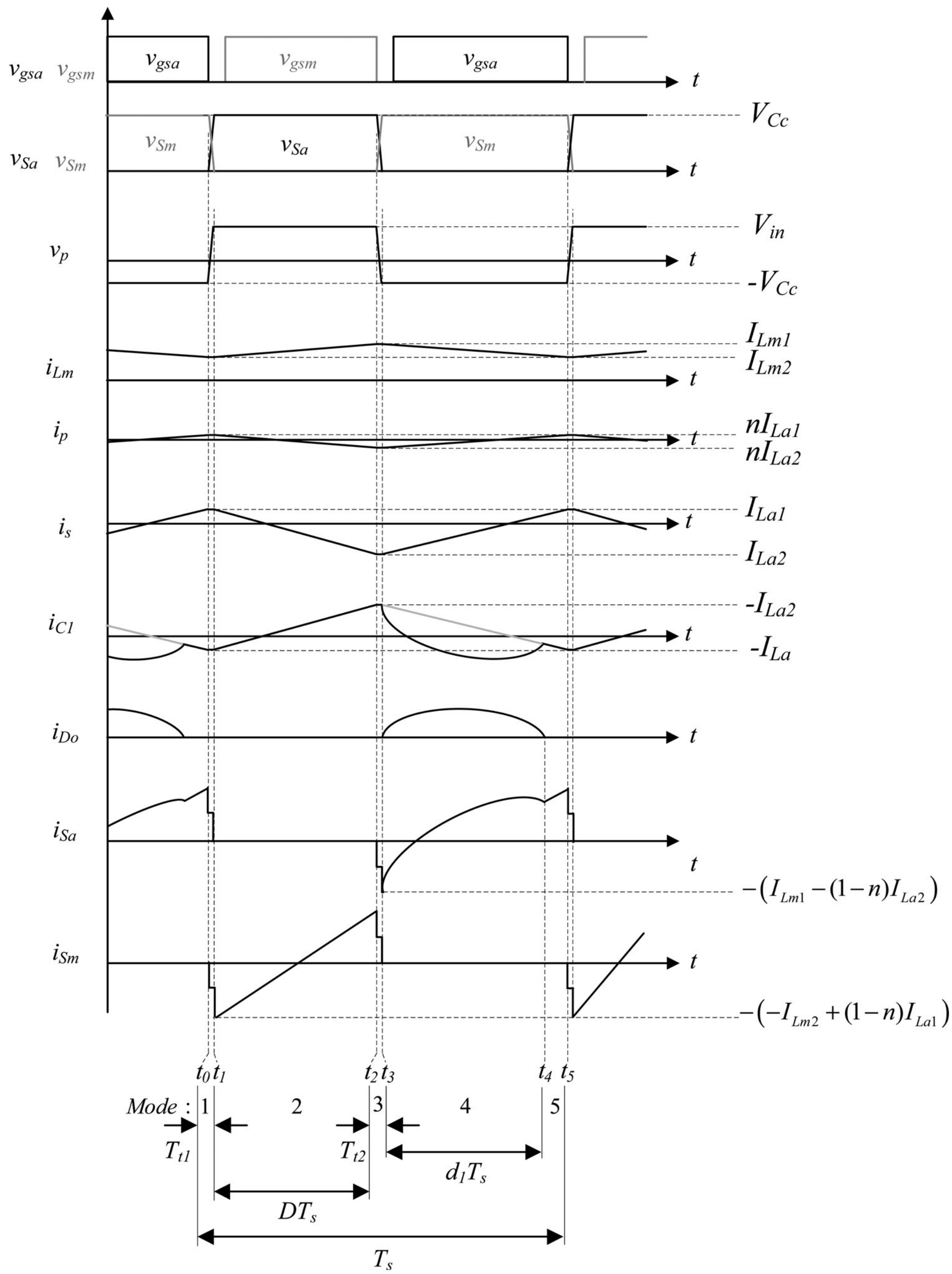

Fig. 4. Key waveforms of the proposed converter.

transition time interval T_{t1} is very short and it can be simplified as follows:

$$T_{t1} = \frac{(C_a + C_m)\, V_{Cc}}{(1-n) I_{La1} - I_{Lm2}}. \tag{1}$$

Since the transition interval T_{t1} is very short, all the currents flowing through the magnetic components are considered constant during this mode.

Mode 2 [t_1, t_2]: At t_1, the voltage v_{Sm} arrives at zero. Then, the body diode D_m is turned ON. After that, the gate signal is applied to the switch S_m and the channel of S_m takes over the current flowing through D_m. Since the voltage v_{Sm} is clamped as zero with turn-on of D_m before the switch S_m is turned ON, zero-voltage turn-on of S_m is achieved. In this mode, the input voltage V_{in} is applied to L_m and the current i_{Lm} increases linearly from its minimum value I_{Lm2} as follows:

$$i_{Lm}(t) = I_{Lm2} + \frac{V_{\text{in}}}{L_m}(t - t_1). \tag{2}$$

Since the voltage v_s at the secondary side of the coupled inductor L_c is nV_{in}, the voltage v_{La} across L_a is$-(V_{Cc}-nV_{\text{in}}-V_{C1})L_a/(L_a+L_r)$. Therefore, the secondary current i_s decreases linearly from its maximum value I_{La1} as follows:

$$i_s(t) = I_{La1} - \frac{V_{Cc} - nV_{\text{in}} - V_{C1}}{L_a + L_r}(t - t_1). \tag{3}$$

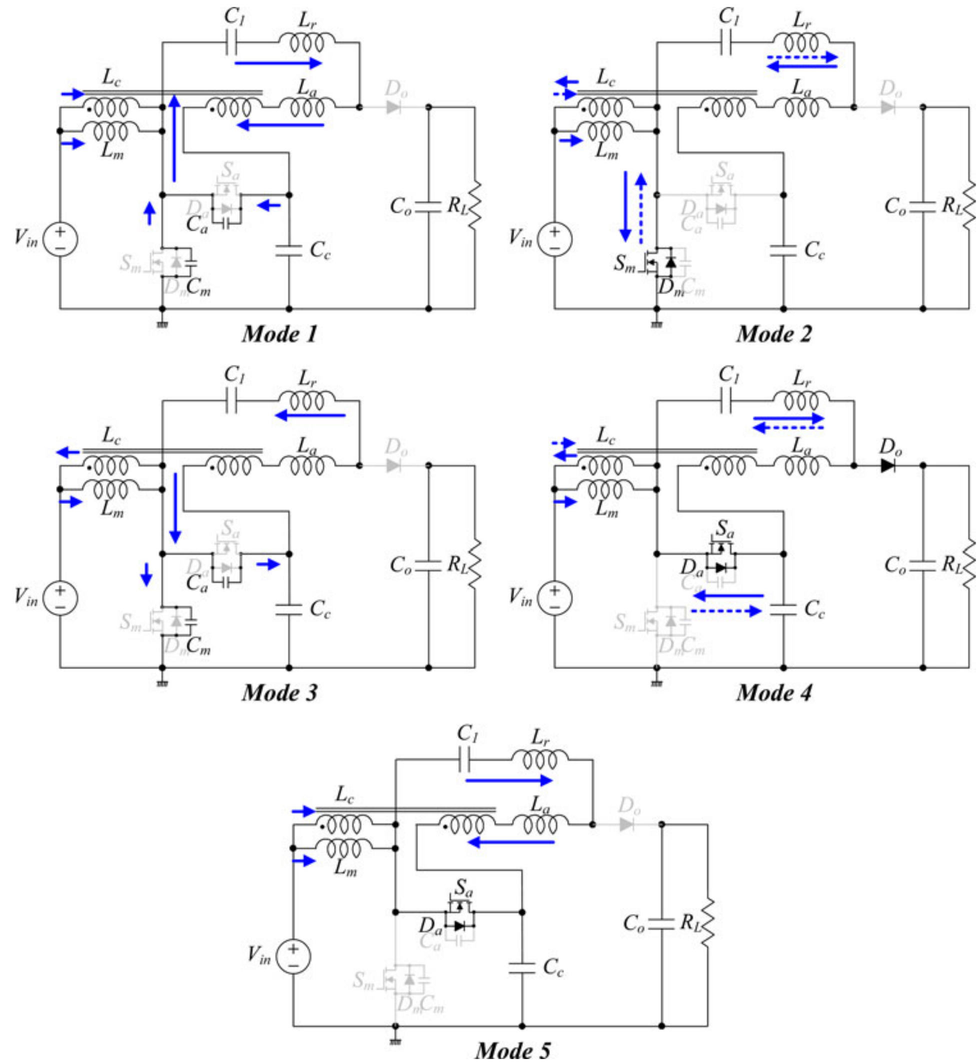

Fig. 5. Operating Modes.

The input current i_{in} is the sum of i_p and i_{Lm} and given by

$$i_{\text{in}}(t) = i_{Lm}(t) + i_p(t) = I_{Lm2} + nI_{La1} + \left[\frac{V_{\text{in}}}{L_m} - \frac{n\,(V_{Cc} - nV_{\text{in}} - V_{C1})}{L_a + L_r}\right](t - t_1). \quad (4)$$

The main switch current i_{Sm} in this mode can be derived by

$$i_{Sm}(t) = i_{Lm}(t) - (1-n)i_s(t) = -\left[(1-n)I_{La1} - I_{Lm2}\right] + \left[\frac{V_{\text{in}}}{L_m} + \frac{(1-n)\,(V_{Cc} - nV_{\text{in}} - V_{C1})}{L_a + L_r}\right](t - t_1). \quad (5)$$

At the end of this mode, the current i_{Lm} arrives at its maximum value I_{Lm1} and the minimum value I_{La2}.

Mode 3 [t_2, t_3]: The main switch S_m is turned OFF at t_2. Then, the voltage v_{Sm} increases from zero and the voltage v_{Sa} decreases from V_{Cc} at the same time due to the energy stored in the magnetic components. With the same assumption as in mode 1, the transition time interval T_{t2} can be simplified as follows:

$$T_{t2} = \frac{(C_a + C_m)\,V_{Cc}}{I_{Lm1} - (1-n)I_{La2}}. \quad (6)$$

T_{t2} is also negligible. All the currents are assumed constant during T_{t2}.

Mode 4 [t_3, t_4]: At t_3, the voltage v_{Sa} arrives at zero. Then, the body diode D_a is turned ON. After that, the gate signal is applied to the switch S_a and the channel of S_a takes over the current flowing through D_a. Since the voltage v_{Sa} is clamped as zero before the switch S_a is turned ON, zero-voltage turn-on of S_a is achieved. In this mode, the voltage v_p across L_m is$-(V_{Cc}-V_{\text{in}})$ and the current i_{Lm} decreases linearly from its maximum value I_{Lm1} as follows:

$$i_{Lm}(t) = I_{Lm1} - \frac{V_{Cc} - V_{\text{in}}}{L_m}(t - t_3). \quad (7)$$

With the turn-on of S_a, the output diode D_o starts to conduct. Then the resonance between the resonant inductor L_r and the capacitor C_1 occurs. Since the voltage across the inductor L_a is $V_o+nV_{\text{in}}-(1+n)V_{Cc}$, the current i_s increases linearly in this mode as follows:

$$i_s(t) = I_{La2} + \frac{V_o + nV_{\text{in}} - (1+n)V_{Cc}}{L_a}\,(t - t_3)\,. \tag{8}$$

The input current in this mode is given by

$$i_{\text{in}}(t) = I_{Lm1} + nI_{La2} - \left[\frac{V_{Cc} - V_{\text{in}}}{L_m} - \frac{n\,(V_o + nV_{\text{in}} - (1+n)V_{Cc})}{L_a}\right](t - t_3)\,. \tag{9}$$

The current i_{C1} is given by

$$i_{C1}(t) = \frac{V_o - V_{C1} - V_{Cc}}{Z_r}\sin\omega_r\,(t - t_3) - I_{La2}\cos\omega_r\,(t - t_3) \tag{10}$$

where the resonant frequency ω_r and the impedance Z of the resonant tank are

$$\omega_r = \frac{1}{\sqrt{L_r C_1}} \tag{11}$$

$$Z_r = \sqrt{\frac{L_r}{C_1}}. \tag{12}$$

In this mode, the output diode current i_{Do} and the switch current i_{S1} can be written by

$$i_{Do}(t) = -i_s(t) - i_{C1}(t) \tag{13}$$

$$i_{Sa}(t) = -i_{\text{in}}(t) - i_{C1}(t). \tag{14}$$

Mode 5 [t_4, t_5]: At t_4, the output diode current i_{Do} decreases to zero and the zero-current turn OFF of the diode D_o is achieved. Since the current changing rate of D_o is controlled by a resonant manner, its reverse-recovery problem is significantly alleviated. Since the voltage across the inductor L_a is $(V_{C1}-nV_{Cc}+nV_{\text{in}})L_a/(L_a+L_r)$, the current i_s increases linearly in this mode as follows:

$$i_s(t) = i_s(t_4) + \frac{V_{C1} - nV_{Cc} + nV_{\text{in}}}{L_a + L_r}\,(t - t_4)\,. \tag{15}$$

At the end of this mode, i_{Lm} arrives at its minimum values I_{Lm2} and maximum value I_{La1}.

III. Design Parameters

A. V_{Cc} and V_{C1}

Since the average voltage across L_m should be zero under a steady state, the clamp capacitor voltage V_{Cc} is obtained by

$$V_{Cc} = \frac{V_{\text{in}}}{1 - D}. \tag{16}$$

Also, the average voltages across the inductors L_r and L_a should be zero. Therefore, the voltage V_{C1} is obtained by

$$V_{C1} = V_{Cc} - V_{\text{in}} = \frac{D}{1 - D}V_{\text{in}}. \tag{17}$$

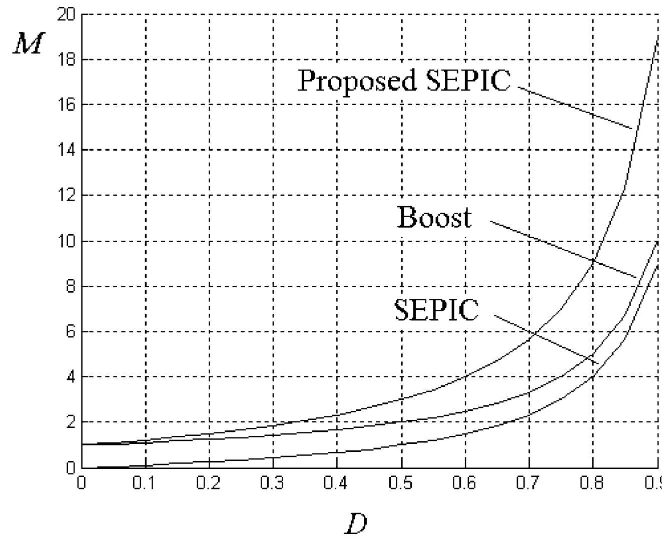

Fig. 6. Voltage gain.

B. Voltage Gain

By applying the volt-second balance law to the voltage across the inductor L_a, the following relation is obtained:

$$-\frac{L_a}{L_a + L_r}\,(V_{Cc} - nV_{\text{in}} - V_{C1})\,DT_s + (V_o - V_{Cc} - n(V_{Cc} - V_{\text{in}}))\,d_2T_s + \frac{L_a}{L_a + L_r}\,(V_{C1} - n(V_{Cc} - V_{\text{in}}))\,(1 - D - d_2)\,T_s = 0. \tag{18}$$

From (16) to (18), the voltage gain M of the proposed converter can be obtained by

$$M = \frac{V_o}{V_{\text{in}}} = \frac{1}{1 - D}\cdot\left(1 + nD + \frac{(1-n)DL_a}{L_a + L_r}\right) \approx \frac{1 + D}{1 - D}. \tag{19}$$

The voltage gain of (19) is plotted and compared with other converters in Fig. 6.

C. Input Current Ripple

In mode 2, the input current i_{in} is given by (4). From (16) and (17), the ripple component of i_{in} can be removed by satisfying the following condition:

$$L_a + L_r = n(1 - n)L_m. \tag{20}$$

Under the condition of (20), the input current i_{in} is constant as $I_{Lm2} + nI_{La1}$. In mode 4, the input current i_{in} is given by (9). Similarly, from (16), (17), and (19), its ripple component can be removed by satisfying the same condition of (20). In this mode, the input current i_{in} is constant as $I_{Lm1} + nI_{La2}$. From (19), it can be seen that the inductor current i_{La} has the same slope both in mode 4 and 5. Therefore, the input current i_{in} does not change in mode 5.

From (2), $I_{Lm1}-I_{Lm2}$ is obtained by

$$I_{Lm1} - I_{Lm2} = \frac{V_{\text{in}}}{L_m} DT_s. \tag{21}$$

Similarly, $I_{La1}-I_{La2}$ is obtained from (3) as follows:

$$I_{La1} - I_{La2} = \frac{V_{Cc} - nV_{\text{in}} - V_{C1}}{L_a + L_r} DT_s. \tag{22}$$

With the condition of (20), the following relation can be easily derived from (16), (17), (21), and (22):

$$I_{Lm2} + nI_{La1} = I_{Lm1} + nI_{La2}. \tag{23}$$

Therefore, the ripple component of the input current i_{in} can be removed under the condition of (20).

D. Minimum and Maximum Values of i_{Lm} and i_s

From Fig. 3, $i_s = i_{C1} + i_{Do}$. Since the average capacitor current should be zero under a steady state, the average value $i_{C1,\text{avg}}$ of the capacitor current i_{C1} is zero. And the average output diode current $i_{Do,\text{avg}}$ is equal to the average output current I_o. Therefore, the following relation can be obtained from the waveform of the secondary current i_s in Fig. 4:

$$I_{La1} + I_{La2} = -2I_o. \tag{24}$$

From (16), (17), (20), (22), and (24), the maximum and minimum values of i_s are derived by

$$I_{La1} = \frac{(1-n)\, V_{\text{in}} DT_s}{2\,(L_a + L_r)} - I_o \tag{25}$$

$$I_{La2} = -\frac{(1-n)\, V_{\text{in}} DT_s}{2\,(L_a + L_r)} - I_o. \tag{26}$$

Similarly, from Fig. 3, the input current i_{in} is the sum of i_p and i_{Lm}. Since the average current $i_{s,\text{avg}}$ is $-I_o$, the average primary current $i_{p,a}vg$ is equal to $-nI_o$. Therefore, the following relation can be obtained from the waveform of the magnetizing current i_{Lm} in Fig. 4:

$$I_{Lm1} + I_{Lm2} = 2\left(\frac{P_o}{\eta V_{\text{in}}} + nI_o\right) \tag{27}$$

where η is the efficiency and P_o is the output power. From (21) and (27), the maximum and minimum values of i_{Lm} are derived by

$$I_{Lm1} = \frac{P_o}{\eta V_{\text{in}}} + nI_o + \frac{V_{\text{in}} DT_s}{2L_m} \tag{28}$$

$$I_{Lm2} = \frac{P_o}{\eta V_{\text{in}}} + nI_o - \frac{V_{\text{in}} DT_s}{2L_m}. \tag{29}$$

E. ZVS Condition

From Fig. 4, the ZVS condition for S_a is given by

$$I_{Lm1} - (1-n)I_{La2} > 0. \tag{30}$$

Since I_{Lm1} is always positive from (28) and I_{La2} is always negative from (26) for $n < 1$, the condition of (30) is always satisfied for $n < 1$. Therefore, the ZVS of S_a is always achieved.

Similarly, for the ZVS of S_m, the following condition should be satisfied

$$-I_{Lm2} + (1-n)I_{La1} > 0. \tag{31}$$

From (19), (25), and (29), the inequality (31) is rewritten by

$$L_m < \frac{V_{\text{in}} DT_s}{2n\,(M/\eta + 1)\, I_o}. \tag{32}$$

F. ZCS Condition

From (8), (10), and (13), the output diode current reset timing ratio d_2 can be obtained by solving the following equation:

$$- I_{La2} - \frac{V_o + nV_{\text{in}} - (1+n)V_{Cc}}{L_a} d_2 T_s - \frac{V_o - V_{C1} - V_{Cc}}{Z_r} \sin\omega_r d_2 T_s + I_{La2}\cos\omega_r d_2 T_s = 0. \tag{33}$$

To obtain ZCS of the output diode, the following condition should be satisfied

$$d_2 < 1 - D. \tag{34}$$

G. Voltage Stresses of the Power Switches and Output Diode

From Fig. 2, it can be seen that the voltages across the main and auxiliary switches are confined to the clamp capacitor voltage V_{Cc}. By using (16) and (19), the voltage V_{Cc} can be rewritten as $(V_{\text{in}}+V_o)/2$. Since the voltage stress of the power semiconductor devices in the conventional SEPIC converters shown in Fig. 1 is $V_{\text{in}} + V_o$, the voltage stress in the proposed converter is reduced by half. In the proposed converter, the voltage stress of the output diode is also reduced by half. In mode 2, the voltage v_{La} is $-(V_{Cc}-nV_{\text{in}}-V_{C1})L_a/(L_a+L_r)$. Therefore, the maximum voltage $v_{Do,\max}$ across the output diode is given by

$$v_{Do,\max} = V_o + \frac{(1-n)V_{\text{in}} L_a}{L_a + L_r} + nV_{\text{in}} - V_{Cc}. \tag{35}$$

For $L_a >> L_r$, it can be easily seen that $v_{Do,\max}$ is $(V_{\text{in}}+V_o)/2$, which is half of that in the conventional SEPIC converters.

IV. Experimental Results

To verify the steady-state performance and the theoretical analysis of the proposed soft-switching SEPIC converter with ripple-free input current, a laboratory prototype is implemented and tested with the following specification.

1) Input voltage $V_{\text{in}} = 48$ V.
2) Output voltage $V_o = 200$ V.
3) Switching frequency $f_s = 100$ kHz.
4) Output power $P_o = 80$ W.

The control circuit was implemented with a constant-frequency pulse width modulation controller KA7552 from Fairchild. The required voltage gain M is 4.17. From (19), the duty cycle D is calculated as 0.613. The turn ratio n of the coupled inductor is selected as 0.25. The ZVS condition of (32)

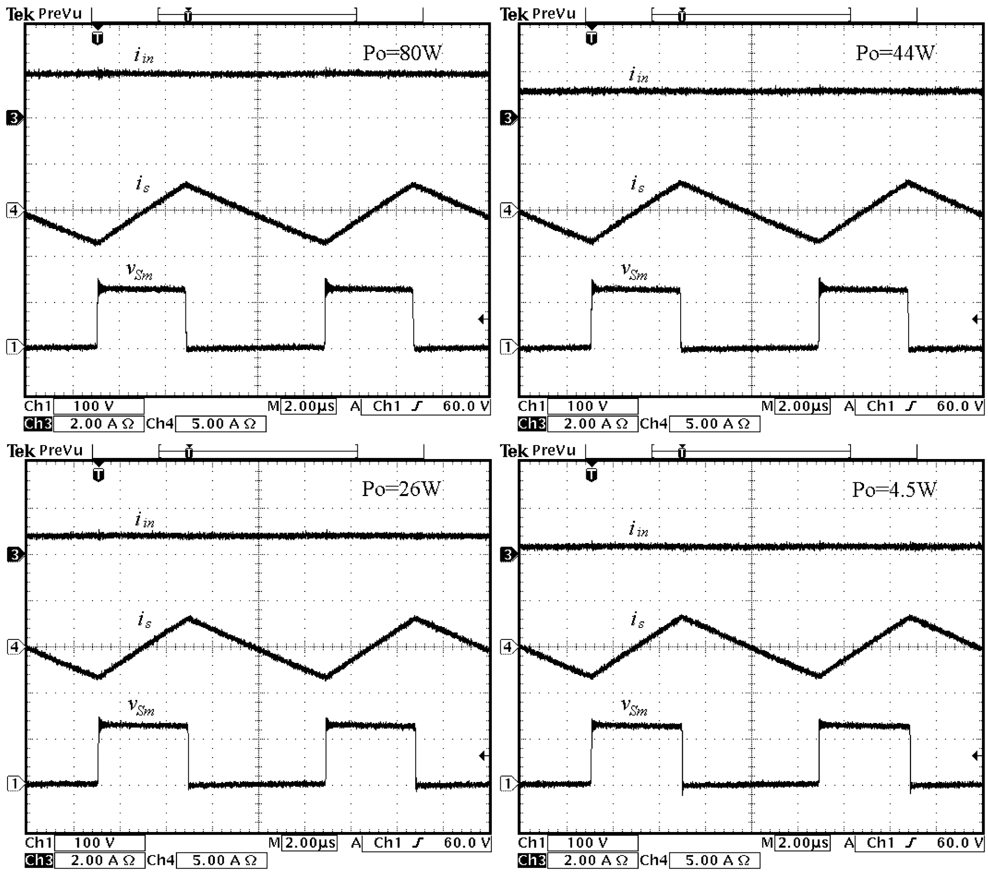

Fig. 7. Experimental waveforms of $i_{\rm in}$, i_s, and v_{Sm}.

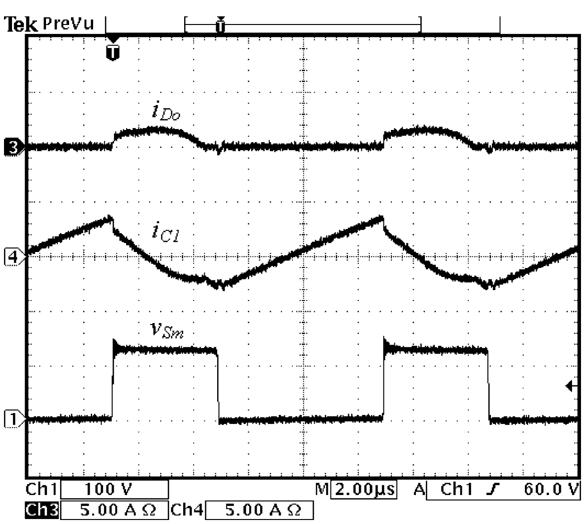

Fig. 8. Experimental waveforms of i_{Do}, i_{C1}, and v_{Sm}.

gives $L_m < 272\ \mu$H with an assumption of $h = 0.95$. The magnetizing inductance L_m is selected as 190 μH. Then, the condition for ripple-free input current of (20) gives $L_a + L_r = 35.6\ \mu$H. Then, the values of the inductors L_a and L_r are selected as 34.5 and 1.1 μH, respectively. The value of C_r is selected as 1 μF to meet the condition of (34). The values of the capacitors C_c and C_o are selected as 6.6 and 100 μF, respectively.

Fig. 7 shows the experimental waveforms of $i_{\rm in}$, i_s, and v_{Sm} under various load conditions. Regardless of load condition, the proposed converter shows almost ripple-free input current. In Fig. 7, the main switch voltage v_{Sm} is well clamped as around 124 V, which agrees with the theoretical analysis. Fig. 8 shows the experimental waveforms of i_{Do}, i_{C1}, and v_{Sm}. It can bee seen that the resonance between L_r and C_1 occurs and the resonant current flows through the output diode during turn-off of S_m. The experimental results are in good agreement with the theoretical analysis. Fig. 9 shows the soft-switching waveforms of D_o, S_m, and S_a. Fig. 9(a) shows the ZCS operation of D_o. The resonance between C_1 and L_r ends before the turn-on of S_m. Since the voltage v_{Do} is maintained as zero after the current i_{Do} arrives at zero, the turn-off loss of the output diode is seen to be almost zero and the ZCS operation of D_o is achieved. Also, the reverse recovery of the output diode is significantly alleviated. Fig. 9(b) shows the soft-switching waveforms of S_m. It is observed that the gate pulses are driving the main switch S_m, only after the switch voltage v_{Sm} has reached zero. It indicates the zero voltage turn-on of S_m. Similarly, the auxiliary switch S_a is turned ON at zero voltage as shown in Fig. 9(c). Fig. 10 shows the measured efficiency of the proposed converter and it is compared with that of the conventional SEPIC converter in Fig. 1(a). The proposed converter exhibits an efficiency of 94.8% at full load condition. The proposed converter shows higher efficiency than the conventional SEPIC converter due to its soft-switching characteristic of power switches S_m and S_a and the output diode

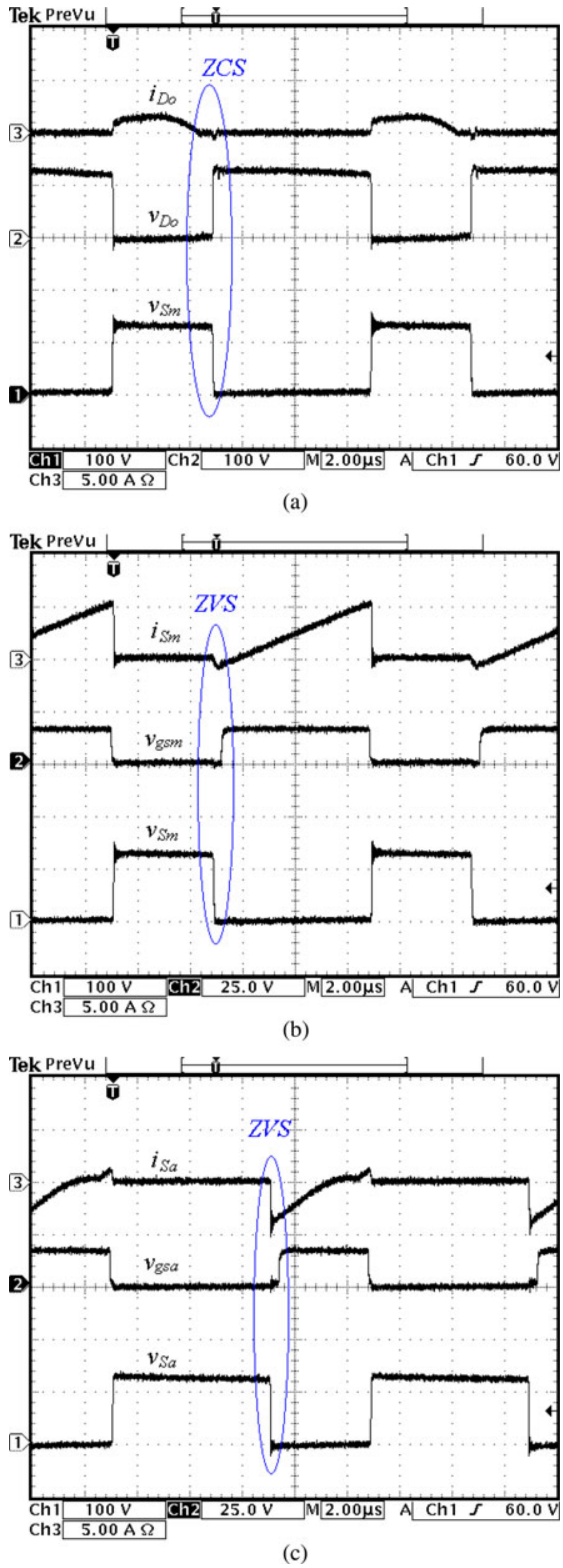

Fig. 9. Soft-switching waveforms D_o, S_m, and S_a.

D_o. At light load, the proposed converter shows lower efficiency. It is mainly because the secondary current i_s increases the conduction loss and it makes up a significant portion of the power

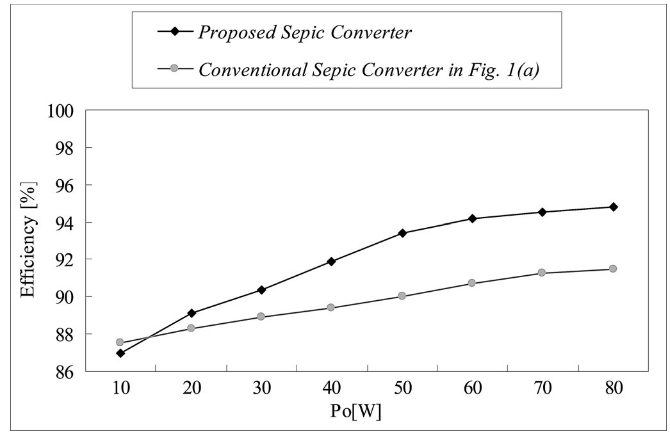

Fig. 10. Measured efficiency.

loss at light load. As shown in Fig. 7, the current i_s is large even at light load. It is one of the major drawbacks of the proposed converter.

V. Conclusion

The operation principle, theoretical analysis, and the implementation of a soft-switching SEPIC converter with ripple-free input current are presented in this paper. In the proposed converter, the coupled inductor with an auxiliary inductor is used to provide ripple-free input current and achieve ZVS operation of main and auxiliary switches. The advantages of the proposed converter are low voltage stresses, low switching losses, ripple-free input current, alleviated reverse-recovery problem of the output diode, and high efficiency. The design consideration of the proposed converter is included. The experimental results based on a prototype are presented for validation.

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