Study of Multisampled Multilevel Inverters to Improve Control Performance

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***Abstract*—A classic digitally controlled power converter usually uses the same sampling and switching frequency. The technique is known as uniform sampling. As the performance of digital signal processors is increasing dramatically and the price is decreasing, applying high sampling frequency becomes increasingly feasible. The multisampling technique is developed to reduce switching delay. However, the control gains are still limited by the switching frequency. To demonstrate an alternative way of improving the control performance without increasing the switching frequency, this paper discusses multisampled multilevel inverters. The example of a voltage controlled multilevel inverter with cascaded control loops is provided. The filter current ripple frequency is increased by the phase-shifted pulsewidth modulation. The multisampling is synchronized to the peaks of the phase-shifted carriers. The small-signal z-domain model is derived to analyze the multisampled multilevel inverter. Compared to the bipolar switched inverter, the multisampled multilevel inverter is characterized by the capability of achieving higher feedback control gains, which improves the control performance. An experimental prototype based on a 10-kHz switching frequency, 80-kHz sampling frequency five-level single-phase H-bridge inverter is tested to demonstrate the validity of the analysis.**

***Index Terms*—Control gain, digital control, multilevel inverters, multisampling, small-signal z-domain model.**

I. Introduction

As the price/performance ratio of digital signal processors (DSPs) decreases, there is an increasing trend of implementing the entire controller digitally for switching power supplies. In classic digital control methods, synchronized sampling and switching is a good solution to avoid noise and ripple in the vicinity of the switching instants [1], [2], with the uniformly sampled converter current representing the current value averaged in each switching cycle. The controller usually employs an internal converter current loop with a proportional (or plus integral) feedback controller [3], [4]. To guarantee a stable operation, the maximum proportional feedback gain in the current loop is limited by the sampling frequency and the converter side inductance [5]. As is reported in [6], if the current sampling frequency is halved, the control gain has to be reduced by the factor of 2, which results in a degraded control performance. Apparently, if both the sampling frequency and the switching frequency can be increased, larger control gains and better performance are achievable.

The rapid performance improvement of DSPs, or DSPs combined with additional field programable gate arrays (FPGAs) means that applying high sampling frequency of exact multiples of the switching frequency becomes feasible [7]–[9]. This new approach is known as multisampling and has the purpose of reducing the delay of the pulsewidth modulation (PWM) and improving the control bandwidth. However, this approach has a major drawback that the multisampling also samples the current ripple. If the samples are not acquired at the peaks of the triangle PWM carrier, an average current is not guaranteed for the digital controller. In the dc–ac or ac–dc converters with a multisampling factor N, current distortion may appear when the duty-ratio is equal to the integer multiples of $1/N$. Hence, a digital filter is required to remove the switching ripple from the sampled current [10]. Moveover, when multisampling is used without increasing the switching frequency, the control gains and performance are still limited by the switching frequency. Therefore, a high switching frequency [6] or a high converter current ripple frequency [5] is still necessary to improve the control performance.

Due to practical limitations of switching devices, the switching frequency cannot be easily increased. However, with the number of the switches increased by multilevel inverters [11]–[14], the filter current ripple frequency can be increased by the phase-shifted PWM strategy [15]–[19]. Without changing the switching frequency of each switch, the ripple frequency can be increased in respect to the number of inverter levels. The multisampling is performed according to the number of the phase-shifted carriers [20], [21]. A classic voltage controller with cascaded control loops for the multilevel inverter, behaving as a typical linear control system, is given as an example. In order to study the improved control performance of the multisampled multilevel inverter in contrast to the bipolar switched inverter, the small-signal z-domain model is derived for the analysis. The analysis reveals that higher feedback gains can be employed in the controller of the multisampled multilevel inverter, which improves the control performance. Experimental results obtained from a uniformly sampled bipolar switched inverter and a multisampled five-level inverter are provided to validate the analysis.

II. Uniformly Sampled Bipolar Switched Single-Phase H-Bridge Inverters

Fig. 1 shows the power circuit of a single-phase bipolar switched H-bridge inverter. An LC filter is connected to smooth

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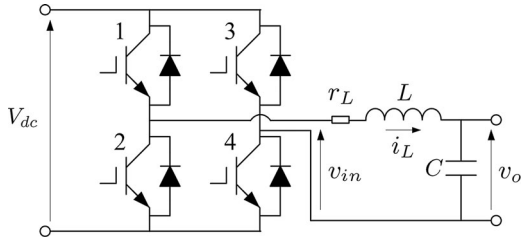

Fig. 1. Single-phase H-bridge inverter.

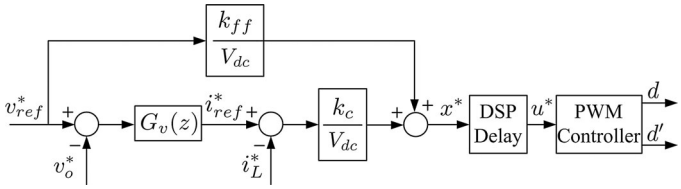

Fig. 2. Digital controller of the single-phase H-bridge inverter.

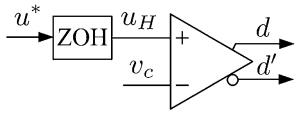

Fig. 3. Functional block diagram of the PWM controller.

the filter input voltage $v_{\rm in}$. The controller of the stand-alone inverter is a cascaded linear controller composed of an internal current control loop and an external voltage control loop with duty-ratio feedforward ($k_{\rm ff}=1$), as is shown in Fig. 2. The ideally sampled output voltage and inductor current are represented by v_o^* and i_L^*, respectively. A proportional feedback controller is used in the internal loop with the gain of k_c, while a proportional plus resonant controller is applied to the external voltage loop. The compensator of the voltage control loop is $G_v(z)=k_v+k_r\sum_{k=1}^{h}H_k(z)$, where $H_k(z)$ is the digitalized band-pass filter resonating at kth odd harmonic frequency. The ideally calculated (without delay) digital duty-ratio is x^*, which is updated into the PWM controller with a DSP delay period (analog-to-digital conversion delay and computation delay). The functional block diagram of the PWM controller is shown in Fig. 3. The PWM controller updates duty-ratio signal u^*, which is then converted to u_H by a zero-order-hold (ZOH). By comparing u_H to the triangle carrier v_c, the drive signals d and d' are generated. For a bipolar switched single-phase H-bridge inverter, the drive signal for insulated gate bipolar transistor (IGBT) 1 and 4 is d, whereas for IGBT 2 and 3 is d'. Signals d and d' are complementary but with a deadband.

In order to select the feedback control gains, the model describing the digital control loops is required. The key waveforms of the bipolar PWM inverter is shown in Fig. 4. The carrier is v_c with a switching frequency of $f_s=1/T_s$. The sampling is synchronized to the time when the PWM counter equals period value. Assuming the total time of analog-to-digital conversion and duty-ratio computation is less than half sampling period, then the calculated duty-ratio can be updated into the compare register at the time when the counter equals zero. Therefore,

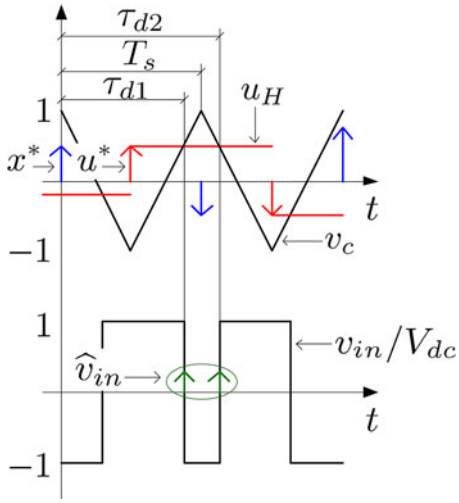

Fig. 4. Key waveforms of the bipolar switched inverter.

the DSP delay from x^* to u^* is a half sampling period. As u^* is converted to u_H by a ZOH and the drive signals are generated by comparing u_H with v_c, the PWM delays from u^* to the relevant drive signals in small signal are described by $e^{-s\frac{DT_s}{2}}$ and $e^{-s\frac{(2-D)T_s}{2}}$, where D is the average duty-ratio scaled in the range of $(0,1)$. Assuming there is no delay from the drive signals to the filter input voltage $v_{\rm in}$, the small-signal pulse-to-continuous transfer function describing $\widehat{v}_{\rm in}$ as a function of $\widehat{x}^*$ can be written as [22]

$$G_{v_{\rm in}x^*}(s)=\frac{V_{\rm dc}T_s}{2}(e^{-s\tau_{d1}}+e^{-s\tau_{d2}}) \tag{1}$$

with $\tau_{d1}=((1+D)T_s/2)$ and $\tau_{d2}=((3-D)T_s/2)$.

When the inverter has no load, the transfer functions describing the inductor current i_L and output voltage v_o as a function of the filter input voltage $v_{\rm in}$ are

$$G_{i_L v_{\rm in}}(s)=\frac{s/L}{s^2+sr_L/L+1/LC} \tag{2}$$

and

$$G_{v_o v_{\rm in}}(s)=\frac{1/LC}{s^2+sr_L/L+1/LC} \tag{3}$$

respectively. Hence, the pulse transfer functions from x^* to the sampled signals i_L^* and v_o^* in small signal are

$$G_{i_L^* x^*}(z)=\mathcal{Z}\{G_{v_{\rm in}x^*}(s)G_{i_L v_{\rm in}}(s)\} \tag{4}$$

and

$$G_{v_o^* x^*}(z)=\mathcal{Z}\{G_{v_{\rm in}x^*}(s)G_{v_o v_{\rm in}}(s)\} \tag{5}$$

respectively. The analytical expressions of (4) and (5) can be derived using the mathematical method in [22]. According to Fig. 2, the closed-loop transfer function from $i_{\rm ref}^*$ to x^* without feedforward can be written as

$$G_1(z)=\frac{\frac{k_c}{V_{\rm dc}}}{1+\frac{k_c}{V_{\rm dc}}G_{i_L^* x^*}(z)}. \tag{6}$$

TABLE I
PARAMETERS OF THE INVERTER

Symbol	Quantity	Value
V_{dc}	DC voltage amplitude	200 V
T_s	Switching and sampling period	100 μs
L	Inductor	1642 μH
C	Capacitor	10 μF
r_L	Inductor parasite resistance	0.4 Ω

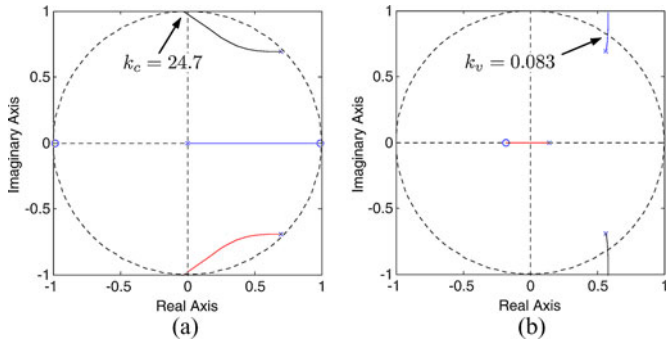

Fig. 5. Root loci of the uniformly sampled control loops. (a) Internal current loop. (b) External voltage loop with $k_c = 4$.

The closed-loop transfer function from $v^*_{\rm ref}$ to x^* without feedforward is

$$G_2(z) = \frac{G_v(z)G_1(z)}{1 + G_v(z)G_1(z)G_{v_o^* x^*}(z)}. \quad (7)$$

By using the parameters listed in Table I, the root loci of the internal current control loop and the external voltage control loop are shown in Fig. 5. To ensure stable operation in the experimental tests, the proportional gains are chosen as $k_c = 4$ and $k_v = 0.05$.

III. MULTISAMPLED MULTILEVEL INVERTERS

To demonstrate the improved control performance as a result of the multisampled multilevel inverter, this section provides a detailed analysis of the system's operation in contrast to the bipolar switched inverter. A system comprised of two cascaded H-bridges inverters and modulated by four phase-shifted triangle carriers with octuple-sampling frequency is modeled. The analysis is undertaken to assess the performance advantages of the multisampled multilevel inverter.

A. System Configuration

The power circuit of a multilevel inverter with two cascaded H-bridges is shown in Fig. 6. Compared to the single H-bridge inverter, the dc voltage for each bridge is halved. The drive signals for the upper and lower switches in each leg are complementary. Therefore, four independent drive signals are generated from the digital controller which block diagram is shown in Fig. 7.

B. Phase-Shifted PWM

Two typical modulations strategies are usually used for multilevel inverters [15], [17]. The level-shifted modulation method

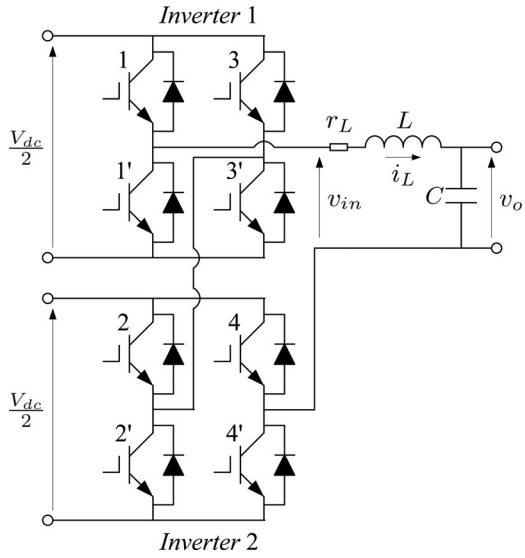

Fig. 6. Five-level H-bridge inverter.

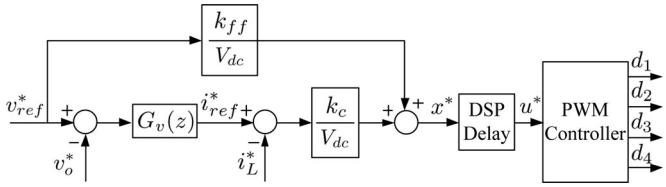

Fig. 7. Digital controller of the five-level H-bridge inverter.

requires the same switching frequency as the filter current ripple frequency [23]. To achieve higher ripple frequency than switching frequency, the phase-shifted PWM can be employed for the multilevel inverters. This modulation method is characterized by its capability of improving the control performance of the filter voltage and current [24]. Since the filter input voltage frequency is increased as multiples of the switching frequency, achieving an enhanced dynamic performance becomes feasible. However, a proper model for the digital PWM which can be used to design the controller has not been proposed to date.

If a vertical transition of the modulation signal u_H has an intersection with a carrier, a special phenomenon occurs which is called vertical crossing [9]. For the case when there is no vertical crossing between the modulation signals and the carriers, the time-domain diagram explaining the phase-shifted PWM is shown in Fig. 8. To generate the drive signals, two opposite duty-ratios are updated into PWM comparator as u_H and u'_H. The carriers v_{c1} and v_{c2} are used to compare with u_H to drive switches 1 and 2 in Fig. 6, respectively, with v_{c2} leading v_{c1} by a phase angle of 90°. The carriers v_{c3} and v_{c4} are used to compare with u'_H to drive switches 3 and 4, respectively, with v_{c4} leading v_{c3} by a phase angle of 90°. Moreover, v_{c1} and v_{c3} are synchronized. The sampling is synchronized to the peaks of the carriers with the sampling frequency being eight times of the switching frequency.

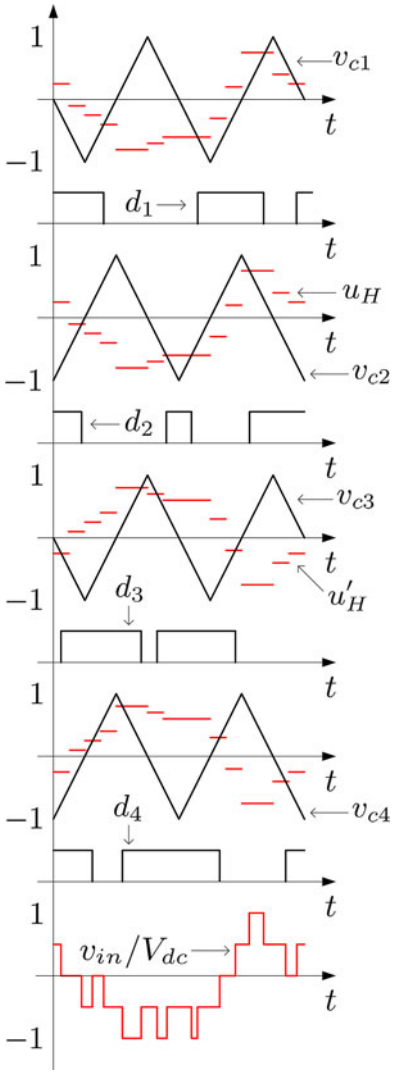

Fig. 8. Time-domain waveforms of the phase-shifted PWM.

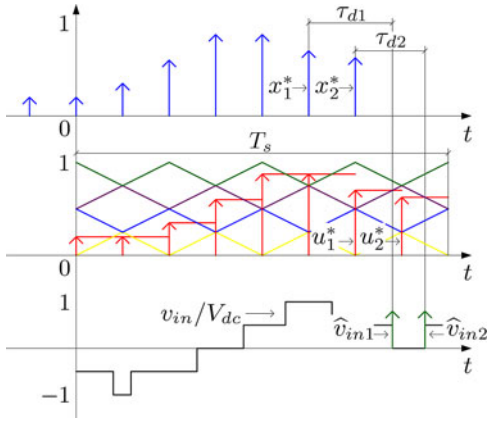

Fig. 9. Time-domain enlarged view of the equivalent waveforms in the phase-shifted PWM multilevel inverter.

C. Current Ripple Reduction

Multilevel inverters also provide an effective way of suppressing the filter current ripple [25]. For comparison, the ripple amplitude of the bipolar switched inverter is derived first. To simplify the analysis, we assume the inductor has no parasitic resistance and the capacitor voltage v_o exhibits a relative slow dynamic behavior. Then, the voltage on the filter inductor is

$$V_{\rm dc} - v_o = L\frac{\Delta i_L}{DT_s} \tag{8}$$

during the rising edge of the inductor current, with Δi_L the peak-to-peak amplitude of the current ripple. When the current is falling, the inductor voltage is written as

$$-V_{\rm dc} - v_o = L\frac{-\Delta i_L}{(1-D)T_s}. \tag{9}$$

Subtracting (9) from (8), it can be derived that

$$\Delta i_L = \frac{2V_{\rm dc}T_sD(1-D)}{L}. \tag{10}$$

Therefore, the maximum inductor current ripple $\Delta i_{L\max}$ of bipolar switched inverter is obtained when $D = 0.5$, i.e., $\Delta i_{L\max} = V_{\rm dc}T_s/2L$.

In the example of the five-level phase-shifted PWM multilevel inverter (see Fig. 9), the input voltage frequency is increased to $4f_s$ and the voltage amplitude variation is reduced to $V_{\rm dc}/2$. Hence, the amplitude of the current ripple in the multilevel inverter can be written as

$$\Delta i_L = \frac{V_{\rm dc}T_sD'(1-D')}{4L} \tag{11}$$

with $D' = 4D - \text{floor}(4D)$. The maximum value of the ripple amplitude can be derived as $\Delta i_{L\max} = V_{\rm dc}T_s/16L$. Compared to the bipolar switched inverter, the multilevel inverter have reduced the filter current ripple amplitude by a factor of eight. Usually an inductor with much smaller size can be used to suppress the ripple in multilevel inverters.

D. Small-Signal z-Domain Modeling for Switching Function

The waveforms in the last switching period in Fig. 8 are enlarged and shown in Fig. 9. The modulation model can be obtained by describing the small-signal filter input voltage $\widehat{v}_{\rm in}$ as a function of $\widehat{x}^*$. It is shown in Fig. 9 that when x^* is changing slowly compared to the carriers, the delay effect can be determined by the average duty-ratio D. If the drive signal is generated in the duration of the rising edge of the carriers (e.g. $\widehat{v}_{\rm in1}$), the delay effect is expressed as $e^{-s\tau_{d1}}$, where $\tau_{d1} = \frac{DT_s}{2} - \frac{\text{floor}(NDT_s)}{N} + \frac{T_s}{N}$ with the multisampling factor $N = 8$. On the other hand, when the drive signal is generated during the falling edge of the carriers (e.g. $\widehat{v}_{\rm in2}$), the delay effect is written as $e^{-s\tau_{d2}}$, with $\tau_{d2} = \frac{(1-D)T_s}{2} - \frac{\text{floor}(N(1-D)T_s}{N} + \frac{T_s}{N}$.

Since the exact double-update-mode PWM model cannot be obtained straightforwardly [22], an approximation can be derived by averaging the delay effects and the small-signal transfer function is written as

$$G_{v_{\rm in}x^*}(s) = \frac{V_{\rm dc}T_s}{2N}(e^{-s\tau_{d1}} + e^{-s\tau_{d2}}). \tag{12}$$

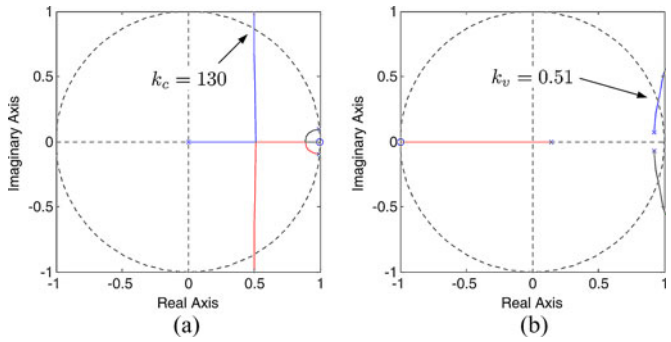

Fig. 10. Root loci of the multisampled control loops. (a) Internal current loop. (b) External voltage loop with $k_c = 16$.

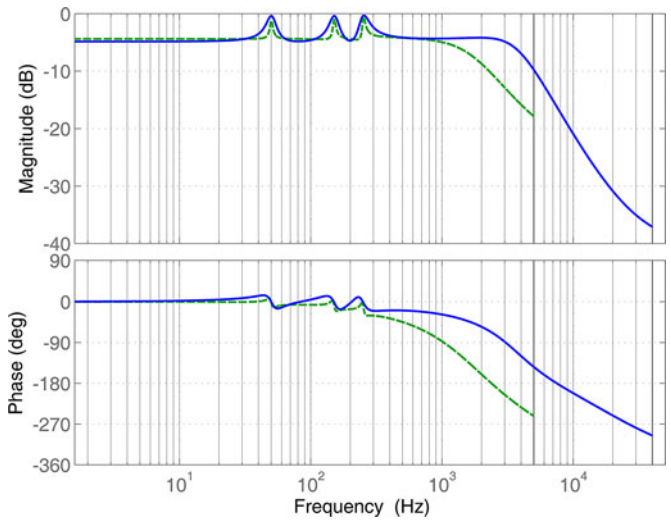

Fig. 11. Bode diagrams of closed-loop transfer functions (dashed line: bipolar switched inverter; full line: multisampled multilevel inverter).

The theoretical method similar to that in Section II can be applied to derive the small-signal transfer functions of $G_{i_L^* x^*}(z)$ and $G_{v_o^* x^*}(z)$ for the multisampled multilevel inverter, by using the z-transform with the sampling frequency Nf_s. Based on the z-domain transfer functions, the root loci of the internal current loop and the external voltage loop are shown in Fig. 10. As the sampling frequency is increased, the driving delay becomes significant, which may slightly affect the stability boundaries in the root loci. Hence, the proportional gains are chosen as $k_c = 16$ and $k_v = 0.2$ to ensure stable operation. Compared to the gains of the bipolar switched inverter in Section II, much higher gains are achieved in the multisampled multilevel inverter, resulting in better capability for voltage tracking. The closed-loop transfer functions describing v_o^* as a function of v_{ref}^* for the two systems are compared. With a heave resistive load ($R = 5\ \Omega$), the bode diagrams of the closed-loop transfer functions are shown in Fig. 11. It can be seen from Fig. 11 that the closed-loop gain of the multisampled multilevel inverter at selected frequencies is higher than that of the bipolar switched inverter. At the fundamental frequency, the gains of the multisampled multilevel inverter and the bipolar switched inverter are 0.956 and 0.869, respectively. Therefore, the control performance has been improved by the multisampled multilevel inverter. The experimental tests are implemented based on the previous analysis.

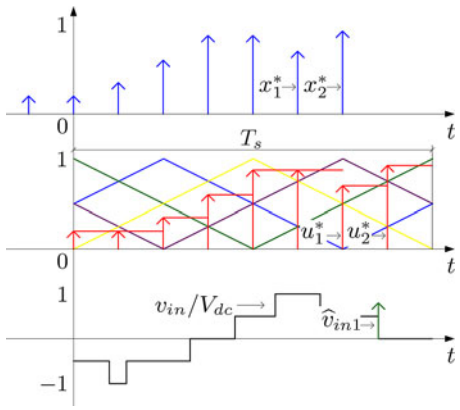

Fig. 12. Key waveforms of the phase-shifted PWM multilevel inverter when vertical crossing occurs.

E. Modulation Error

Note that the small-signal model (12) assumes that there is no vertical crossing, in which case the phase-shifted PWM strategy is equivalent to the alternative phase opposition level-shifted PWM strategy with quadruple-switching frequency. Since the frequency of level-shifted carriers is a half of the sampling frequency, no vertical crossing exists when using the level-shifted PWM. However, when the phase-shifted PWM is applied, the vertical crossing may occur when $D = 0.25$, $D = 0.5$, and $D = 0.75$ where the phase-shifted carriers have intersections. Fig. 12 shows the waveforms when vertical crossing occurs at $D = 0.75$. It can be seen that if the intersection of two carriers is between the levels of two adjacent duty-ratios, a vertical crossing appears on one carrier and a double horizonal crossing appears on the other. Therefore, a switching action is missing at that sampling period and the gain of the PWM in small signal becomes zero. As is addressed in [5] and [10], the vertical crossing results in a modulation nonlinearity which may affect regulating performance of the digital controller. The number of carriers intersections will significantly increase according to the number of inverters, where more vertical crossing may occur. Hence, the modulation error is a disadvantage existing in the multisampled multilevel inverters which limits the level of inverters.

IV. Experimental Results

The bipolar switched single-phase H-bridge inverter and the multilevel cascade H-bridge inverter were experimentally compared. Each digital controller was implemented using a TMS320F28335, floating-point 150-MHz DSP. For the bipolar switched inverter, only one PWM module has been used. The sampling instant is synchronized to the upper peak of the triangle carrier and both the sampling frequency and switching frequency are 10 kHz. On the other hand, for the multilevel inverter, four PWM modules with relevant phase offsets are used.

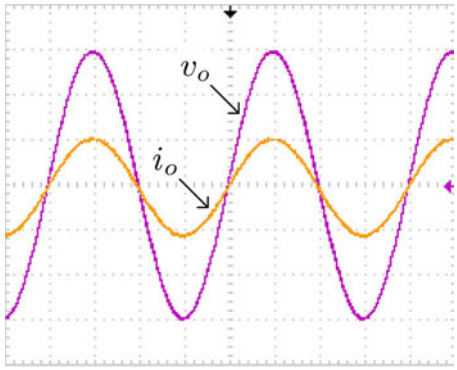

Fig. 13. Experimentally retrieved output voltage and output current waveforms of the conventional bipolar switched inverter with a resistive load (*X*-axis: time, 5 ms/div; *Y*-axis: magnitude of output voltage, 50 V/div; magnitude of output current, 5 A/div).

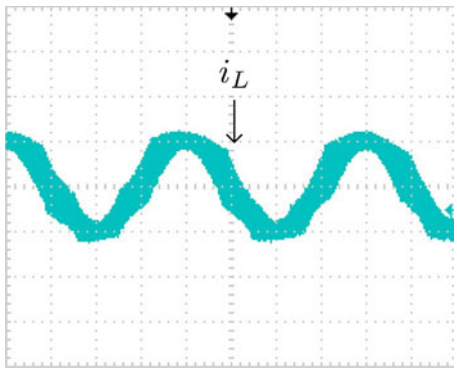

Fig. 14. Experimental inductor current waveform of the conventional bipolar switched inverter with a resistive load (*X*-axis: time, 5 ms/div; *Y*-axis: magnitude of inductor current, 5.33 A/div).

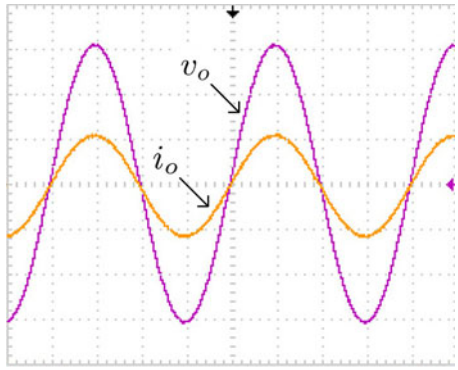

Fig. 15. Experimentally retrieved steady-state response of the multisampled multilevel inverter with a resistive load (*X*-axis: time, 5 ms/div; *Y*-axis: magnitude of output voltage, 50 V/div; magnitude of output current, 5 A/div).

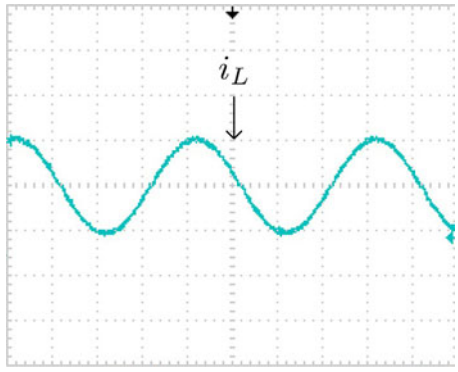

Fig. 16. Experimental inductor current waveform of the multisampled multilevel inverter with a resistive load (*X*-axis: time, 5 ms/div; *Y*-axis: magnitude of inductor current, 5.33 A/div).

The sampling frequency is 80 kHz and the switching frequency is 10 kHz. Intelligent power modules PM30CSJ060 are used as H-bridges with the deadband of 2.67 μs. The same circuit parameters in Table I are used and the control parameters are chosen according to the analysis in Section III, with the highest harmonic order of $h = 5$ and the resonant gain of $k_r = 20k_v$.

With a reference voltage of 110 V (RMS value), Fig. 13 shows the steady-state experimental waveforms of the output voltage and current of the bipolar switched inverter. As the control gains are limited by the sampling frequency, the measured output voltage is 106 V. The inductor current waveform is measured on the analog-to-digital converter's input channel, as is shown in Fig. 14. It can be seen from Fig. 14 that the current contains considerable switching noises with a frequency of 10 kHz. The maximum peak-to-peak value of the experimentally measured inductor current ripple is 7.5 A (when $D = 0.5$), where a well designed filter must be used to suppress the switching ripple.

Compared to the bipolar switched inverter, octuple-sampling frequency is used and quadruple filter input voltage frequency is achieved for the multilevel inverter. The feedback control gains are quadrupled. Fig. 15 shows the experimental waveforms of the output voltage and current of the multisampled multilevel inverter. As much higher control gains are guaranteed, the control accuracy has been improved and the measured RMS value of the output voltage is 109 V. The inductor current waveform is shown in Fig. 16, where the ripple is significantly suppressed. The inductor current contains a ripple with a frequency of 40 kHz and a peak-to-peak amplitude less than 1 A.

The dynamic responses of the bipolar switched inverter and the multisampled multilevel inverter are also compared. The experimental waveforms are retrieved during the transition of a load step. Figs. 17 and 18 show the dynamic responses when the load steps from 108 to 21.6 Ω. After the load step of the bipolar switched inverter, the output voltage drops significantly within the first line cycle. The lowest peak value of output voltage is close to 130 V. It takes at least seven line cycles for the output voltage to achieve the steady-state. In contrast, the output voltage drop of the multisampled multilevel inverter after the load step is smaller. The lowest peak value of the output voltage during the transition period is almost 140 V. Moveover, after the load step, the output voltage reaches the steady-state within five line cycles. Hence, a much better dynamic performance is achieved by the multisampled multilevel inverter.

However, there are also some disadvantages of the multisampled multilevel inverter. The deadband is usually mandatorily required by the H-bridges. When the number of the levels or the switching frequency increases, the phase-shift time reduces. In that case, the deadband time is no longer negligible and it may introduce considerable modulation error which leads to

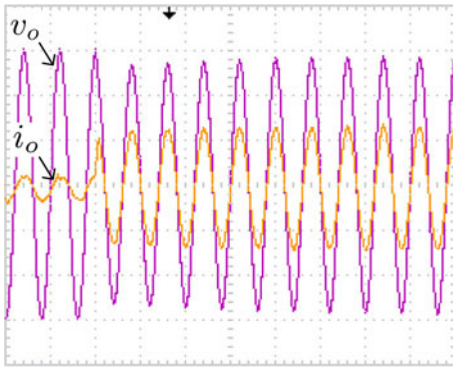

Fig. 17. Experimental dynamic response of the conventional bipolar switched inverter when the load steps (*X*-axis: time, 5 ms/div; *Y*-axis: magnitude of output voltage, 50 V/div; magnitude of output current, 5 A/div).

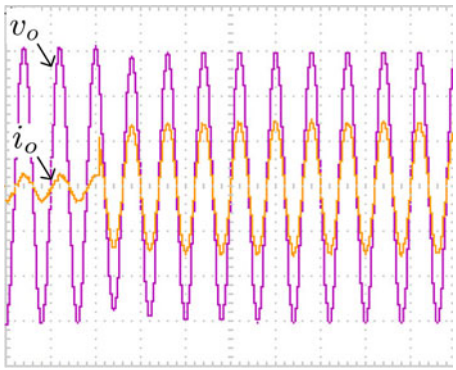

Fig. 18. Experimental dynamic response of the multisampled multilevel inverter when the load steps (*X*-axis: time, 5 ms/div; *Y*-axis: magnitude of output voltage, 50 V/div; magnitude of output current, 5 A/div).

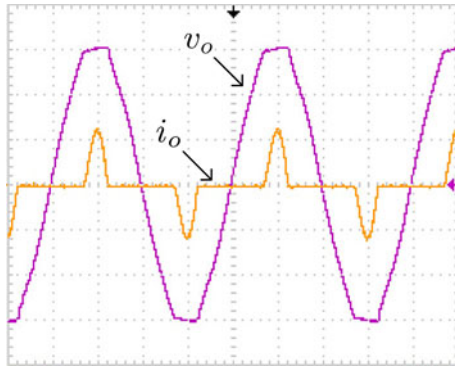

Fig. 19. Experimentally retrieved waveforms of the multisampled multilevel inverter with a nonlinear load (*X*-axis: time, 5 ms/div; *Y*-axis: magnitude of output voltage, 50 V/div; magnitude of output current, 5 A/div).

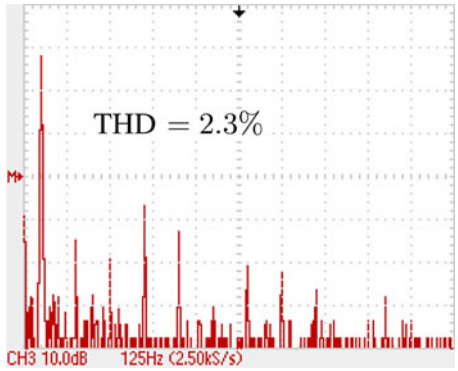

Fig. 20. Output voltage FFT result of the multisampled multilevel inverter with a nonlinear load.

waveforms distortion. Another drawback of the multisampled multilevel inverter is that the complexity of the control algorithm is limited by the capability of devices with high sampling frequency. As the computation load of the digital controller in our system is almost saturated, the highest harmonic order of the resonant compensator is $h = 5$. When a nonlinear load is connected, the output voltage distortion is obvious.

Fig. 19 shows the output voltage and current waveforms of the multisampled multilevel inverter with a nonlinear load connected. The relevant fast Fourier transform (FFT) result of the output voltage is shown in Fig. 20, where the total harmonic distortion (THD) is about 2.3%. The THD of the output voltage remains low as long as the current is low. Nevertheless, the current waveshape also differs when different distortion shapes exist on the output voltage. In an environment with a high current injected to the nonlinear load, guaranteeing low output voltage THD without sufficient harmonic compensators is difficult. To solve this problem, one method is to use different control algorithms such as repetitive or repetitive-based controllers under certain conditions. Another solution is to use FPGA to reduce the computation time, where many complicated control schemes can be implemented. The participation of additional FPGA will bring feasibilities to more complicated control algorithms, if the complexity and cost of hardware is not a big issue.

V. Conclusion

As increasing sampling and switching frequency of power converters is becoming more and more interesting, switching devices which can afford higher operating frequency are required. There are still practical limitations for switches running at high frequency. However, by using the phase-shifted PWM method in multilevel inverters, the filter current ripple frequency is increased, which allows the controller to achieve better performance. This paper discusses the digital control of a multisampled multilevel inverter with a comparison to the control of a uniformly sampled bipolar switched inverter. The uniform sampling is used for the bipolar switched inverter, while the octuple sampling is used for the five-level inverter. A standard digital controller with cascaded control loops is applied to the two inverters.

By developing the small-signal transfer function from the duty-ratio to the filter input voltage, the z-domain model for the multisampled multilevel inverter is theoretically derived. Based on the closed-loop transfer functions of the two systems, the root loci and closed-loop gains are obtained. The control parameters are chosen according to the root loci. It is shown that the control gains of the multisampled five-level inverter can be increased as quadruple as the gains of the conventional uniformly sampled bipolar switched inverter. Therefore, a better control accuracy and dynamic performance is achieved. Following on from the

theoretically obtained control parameters, the experimental systems are implemented. Experimental results have validated the analysis, showing the feasibility of employing higher gains to achieve better control performance in the multisampled multilevel inverter. Hence, compared to the classic uniformly sampled inverter, the multilevel inverter, which remains the same switching frequency, is an alternative way of effectively implementing higher sampling frequency.

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