Towards a 99% Efficient Three-Phase Buck-Type PFC Rectifier for 400-V DC Distribution Systems

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***Abstract*—In telecom applications, the vision for a total power conversion efficiency from the mains to the output of point-of-load (PoL) converters of 95% demands optimization of every conversion step, i.e., the power factor correction (PFC) rectifier front-end should show an outstanding efficiency in the range of 99%. For recently discussed 400-V dc distribution bus voltages, a buck-type PFC rectifier is a logical solution. In this paper, an efficiency-optimized, 98.8% efficient, 5-kW three-phase buck-type PFC rectifier with 400-V output is presented. Methods for calculating losses of all components are described and are used to optimize the converter design for efficiency at full load. Special attention is paid to semiconductor losses, which are shown to be dominant, with the parasitic device capacitance losses being a significant component. The calculation of these parasitic capacitance losses is treated in detail, and the charge-balance approach used is verified. A prototype of the proposed rectifier is constructed which verifies the accuracy of the models used for loss calculation and optimization.**

***Index Terms*—AC-DC power converters, energy efficiency, modeling, optimization, three-phase electric power.**

I. Introduction

THREE-PHASE power factor correction (PFC) rectifier systems are frequently employed as active front-ends in utility interfaced systems such as power supplies in telecommunications and process technology. Broadly, two approaches to the design of these rectifiers are possible: a boost-type topology (as considered in [1]–[4]), or a buck-type topology (as considered in [5]–[9]). Buck-boost-type topologies have also been investigated, as in [10]. Compared to the boost-type topologies, the three-phase buck-type rectifiers (3ph-BRs) provide a wide output-voltage control range down to low voltages while maintaining PFC capability at the input, and allow for current limitation in the case of an output short circuit [5]. Recent discussion on power distribution architectures for telecom and data centres has shown [11], [12] the advantages that facility-wide 400-V dc distribution systems would have over traditional 48–54 V dc distribution architectures, especially when dealing with loads that are tens to hundreds of kilowatts. The main advantage are lower load currents on the bus, meaning less cable is required for transmission, and/or the overall efficiency could be increased by 1%–2%. A challenging aspect of the design of such higher voltage dc distribution architectures is providing adequate overcurrent protection, as discussed, with a proposed solution, in [13].

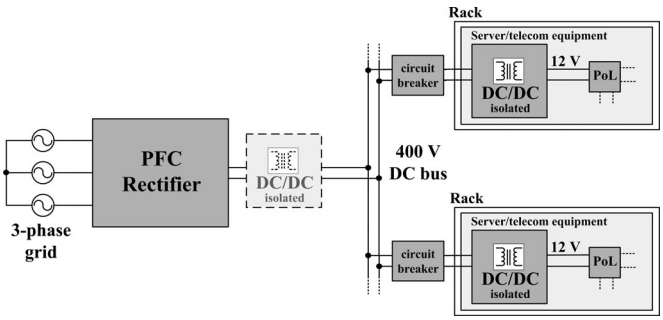

Fig. 1. Possible 400-V dc distribution architecture [11] for telecom and/or data center applications. The dc/dc converter shown in light gray can be omitted if the PFC rectifier is buck type with 400-V output and if no isolation is required.

A 400-V distribution architecture for telecom or data center applications is shown in Fig. 1. For such a system, a buck-type PFC rectifier is preferred since boost-type three-phase rectifiers produce an output voltage too high (typically 700–800 V) to directly feed a 400-V dc bus, necessitating a step-down dc/dc converter at their output. The usage of a buck-type PFC rectifier then allows potentially the removal of the dc/dc converter between the PFC and the distribution bus (see Fig. 1, if isolation at that point is not required), increasing efficiency and reducing costs. In order to achieve an overall efficiency from the mains to the chip (i.e., output of point-of-load converters) of 90%–95% (whereas today it is typically below 80% [11]), all converter stages in the distribution system must be realized with highest possible efficiency—starting with 99% at the PFC rectifier stage. Currently, commercially available three-phase rectifier systems with an isolated dc/dc output converter offer peak efficiencies ranging from 93% [14] for "true" three-phase systems to 97% [15] for systems built from three single-phase rectifier modules. Recent publications similarly report efficiencies of 94% for a "true" three-phase PFC rectifier [16], 95% for an unspecified design [17], and 97% for a modular three-phase PFC rectifier [18].

A different application of the buck-type PFC rectifier could be the charging of the battery of hybrid or electric vehicles (EVs), where 400-V dc is a good approach [19] for the voltage level of the connection among the battery, motor, and charger. Here again the use of a 3ph-BR operating from the 230 V mains would allow direct supply of the dc bus. If in either the telecom or EV application isolation of the PFC output from the bus is

Manuscript received March 4, 2011; revised May 31, 2011; accepted July 30, 2011. Date of current version February 20, 2012. Recommended for publication by Associate Editor U. K. Madawala.

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Digital Object Identifier 10.1109/TPEL.2011.2166406

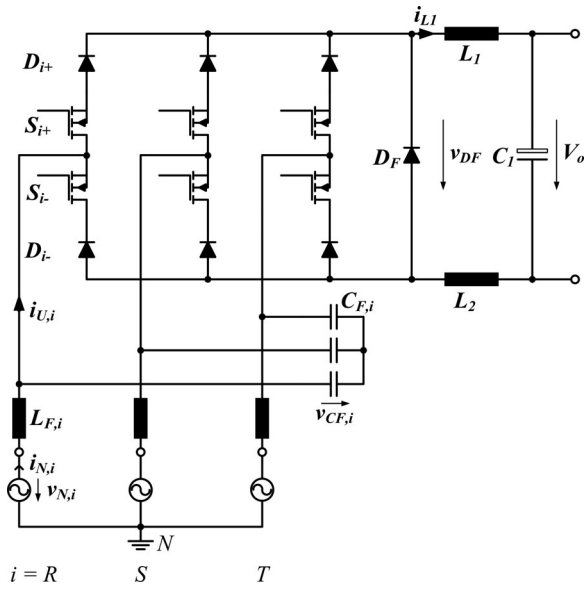

Fig. 2. Power circuit schematic of the 3ph-BR. The full electromagnetic interference (EMI) input filter structure is shown in Fig. 9.

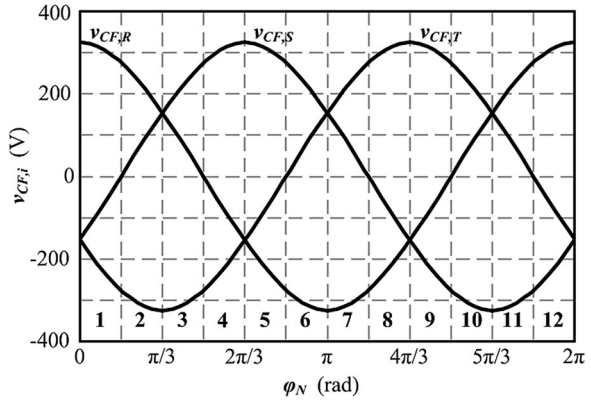

Fig. 3. Mains phase voltages and/or input capacitor voltages over one mains period, showing the division into 12 equal 30°-wide sectors for the purpose of the switching-loss optimized (SLO) modulation scheme (see Fig. 4).

TABLE I
APPLIED DUTY RATIOS BY INPUT VOLTAGE SECTOR

Sector	$\delta_{eff,R}$	$\delta_{eff,S}$	$\delta_{eff,T}$
1, 7	δ_R	$1-\delta_T+t_d$	δ_T
2, 8	δ_R	$1-\delta_R+t_d$	δ_T
3, 9	$1-\delta_S+t_d$	δ_S	δ_T
4, 10	$1-\delta_T+t_d$	δ_S	δ_T
5, 11	δ_R	δ_S	$1-\delta_R+t_d$
6, 12	δ_R	δ_S	$1-\delta_S+t_d$

desired due to safety reasons, this can be accomplished with an isolated 400 V/400 V dc/dc converter (e.g., [20]) with very narrow voltage control range, which could also be optimized for 99% efficiency using the approach presented in [21]. Other applications for the 3ph-BR, where isolation at the output is not required, include the power supplies of lamps or heaters [22] and inverters of variable speed ac drives [23].

In this paper, the design of an ultrahigh efficiency, i.e., 98.8% efficient, 5-kW, 400-V output, three-phase buck-type PFC rectifier (3ph-BR) is presented, optimized for nominal 230 V $\pm$ 10% ac input phase voltage at 50 Hz and peak efficiency at full load. The topology of this system is presented in Section II. In Section III, the methods for calculating the losses of all the components, semiconductors and passives, are given along with a detailed loss breakdown for the converter by component type. Special attention is paid to all types of semiconductor losses since many switches must be paralleled in order to achieve a high efficiency. Section IV presents the prototype with measurement results. An alternative implementation and conclusions are discussed in Sections V and VI, respectively.

II. CONVERTER TOPOLOGY

The converter topology of the 3ph-BR is given in Fig. 2. This topology, and its derivation and principle of operation have been described previously in detail in [5], and [24]–[26]. It is designed to provide the necessary 400-V dc output while guaranteeing sinusoidal input current and maintaining high efficiency. The topology presented here is slightly modified. Instead of insulated gate bipolar transistors (IGBTs) (see Fig. 1 in [26]), high-voltage MOSFETs are used as switches, due to their better switching performance and lower forward voltage when paralleled to increase efficiency. A line-to-line mains voltage amplitude of 566 V (for rated mains rms voltage, i.e., 400-V line-to-line) allows the realization of the converter with 900-V superjunction Si-MOSFETs and 1200-V silicon carbide (SiC) diodes. The electromagnetic interference (EMI) filter for the converter can be designed using the approach of [27]. Note also that the converter inductance is split evenly ($L = L_1 = L_2$) between the positive and negative output rail in order to provide symmetric attenuation impedances for conducted common-mode (CM) noise currents.

A. Modulation Scheme

Modulation schemes for the topology of Fig. 2 have been developed [24], [25], which guarantee minimum switching losses as well as minimum input filter capacitor voltage ripple and minimum dc current ripple. This was further improved in [5] and [26] to eliminate sliding intersections of the input capacitor voltages and the resulting distortions. This results in the switching-loss optimized (SLO) modulation scheme, which contains only a short interval t_d during which switch ON-times overlap, where the duty ratios for the three bridge legs are set according to [5], [25], and [26]

$$\delta_i = \frac{V_{o,\mathrm{ref}}}{\sum_{j=R,S,T} v_{CF,j}^2} \left| v_{CF,i} \right| . \tag{1}$$

where $V_{o,\mathrm{ref}}$ is the required rectifier output voltage and $i = R, S, T$. To apply (1), the input voltage mains period is divided into 12 equal 30°-wide sectors, as shown in Fig. 3. The effective duty ratio $\delta_{\mathrm{eff},i}$ applied to each bridge leg is then calculated according to the present sector, as shown in Table I. A switching

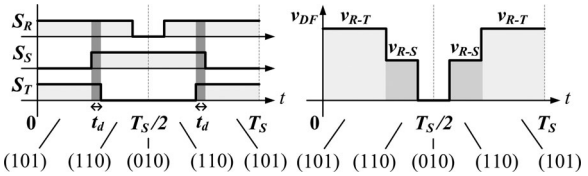

Fig. 4. SLO modulation scheme. (a) Switching actions during a switching period T_S in sector 1, showing overlapping time t_d and the switching states. (b) Freewheeling diode voltage v_{DF} during the switching states.

sequence in sector 1 is depicted in Fig. 4(a). The output voltage generation can be characterized by the modulation index *M* [26]

$$M = \frac{2}{3}\frac{V_o}{\hat{V}_N} = \frac{\sqrt{2}}{3}\frac{V_o}{V_{N,\mathrm{rms}}} \tag{2}$$

ranging from 0 to 1, where $\hat{V}_N$ is the input phase voltage amplitude and V_o the converter output voltage. The resulting waveform of the voltage across freewheeling diode D_F is depicted in Fig. 4(b), showing that the SLO modulation scheme results in the minimum possible and staircase-shaped voltage steps during state transitions for this circuit, therefore, minimizing the switching losses.

The same duty ratio is applied always to both the switches in a bridge leg, for example, a single gate signal is connected to the gate drives of, for instance, S_{R+} and S_{R-}. Accordingly, the half of the leg and the diode, which conducts, is determined by the input voltage conditions. Although this slightly decreases efficiency as the gates of all six MOSFETs are charged and discharged while only three are conducting current within one sector and pulse period, it allows the use of only three gating signals and a simple software implementation of the control algorithm on a DSP.

III. Converter Design and Loss Calculations

In order to achieve the highest possible efficiency, losses of all components must be calculated as precisely as possible and minimized during the design stage. The losses can be divided broadly into two categories: losses of the semiconductors and losses of the passive components.

A. Semiconductor Losses

As the topology employs a large number of semiconductor devices, their losses are considered first and are the main focus of the efficiency optimization for the converter. The rms and average values of the series diode current I_{DS}, MOSFET current I_S, and freewheeling diode current I_{DF} can be calculated by (3)–(6) [5] as follows:

$$I_{DS,\mathrm{avg}} = I_{S,\mathrm{avg}} = \frac{\hat{I}_N}{\pi} \tag{3}$$

$$I_{DS,\mathrm{rms}} = I_{S,\mathrm{rms}} = \frac{\hat{I}_N}{\sqrt{M\pi}} \tag{4}$$

$$I_{DF,\mathrm{rms}} = \left(\frac{1}{M} - \frac{3}{\pi}\right)\hat{I}_N \tag{5}$$

$$I_{DF,\mathrm{rms}} = \sqrt{\frac{1}{M^2} - \frac{3}{M\pi}}\hat{I}_N \tag{6}$$

where I_N is the input phase current. The total conduction losses in the converter $P_{c,S}$ and $P_{c,DS}$ of the MOSFETs and diodes, respectively, are then

$$P_{c,S} = 6I^2_{S,\mathrm{rms}}\frac{R_{DS,\mathrm{ON}}}{n_S} \tag{7}$$

$$P_{c,DS} = 6\left(I^2_{DS,\mathrm{rms}}\frac{R_D}{n_D} + I_{DS,\mathrm{avg}}V_D\right) \tag{8}$$

$$P_{c,DF} = \left(I^2_{DF,\mathrm{rms}}\frac{R_D}{n_{DF}} + I_{DF,\mathrm{avg}}V_D\right) \tag{9}$$

where $R_{DS,\mathrm{ON}}$ is the MOSFET ON-resistance, n_S the number of transistors paralleled for each switch S_i, R_D the diode ON-resistance, n_D the number of devices paralleled for each diode D_i, and V_D the diode forward voltage. To reduce conduction losses, each device (S_i, D_i, and D_F) is implemented with several MOSFETs or diodes in parallel. This, however, increases switching losses, especially that portion of switching losses occurring due to the parasitic output capacitances of the devices. Therefore, the transitions between the switching states in a pulse period (Fig. 4) must be analyzed for all sectors (Fig. 3) to determine where losses occur.

Fig. 5 shows the approximate switching behavior of the MOSFETs in the circuit. In each sector, there is always one MOSFET, which is always switched at zero voltage (e.g., S_{S-} in sector 1 since due to the SLO modulation, the voltage in the $S-$ branch is blocked by D_{S-} in sector 1). Fig. 5 refers to the switching behavior of the remaining two MOSFETs switched in a sector (e.g., S_{R+} and S_{T-} in sector 1).

The switching losses consist of two main portions. The first is due to the overlapping of voltage and current during MOSFET transitions, as shown with the overlapping of I_{ON} and $V_{DS,\mathrm{ON}}$ in Fig. 5. The second is due to the charging and discharging of the parasitic capacitances of the MOSFETs and diodes.

Consider the transitions in sector 1 (Figs. 4 and Fig. 6). The first transition is from state (101) to (110). There, first S_{S-} is turned on at zero voltage, causing no losses, then S_{T-} is turned off. As seen from Fig. 5, the MOSFET turn-OFF produces negligible losses since the overlapping of voltage and current is extremely small during this transition. It remains then to analyze losses due to the parasitic capacitances. Refer to Fig. 6 for the equivalent circuits of the two states. The input voltages are considered constant over one switching period and are therefore represented as voltage sources V_{R-S} and V_{S-T}. Conducting MOSFETs are represented by their ON-resistances, and blocking MOSFETs and diodes are represented by their parasitic output capacitances. Conducting diodes are neglected with a through connection since their forward voltage is very low compared to the input and blocking voltages in the circuit. The inductor current I_L is taken as constant and initially [i.e. in state (101)] flowing entirely through the $R+$ and $T-$ branches. The parasitic output capacitance (typically given in datasheets

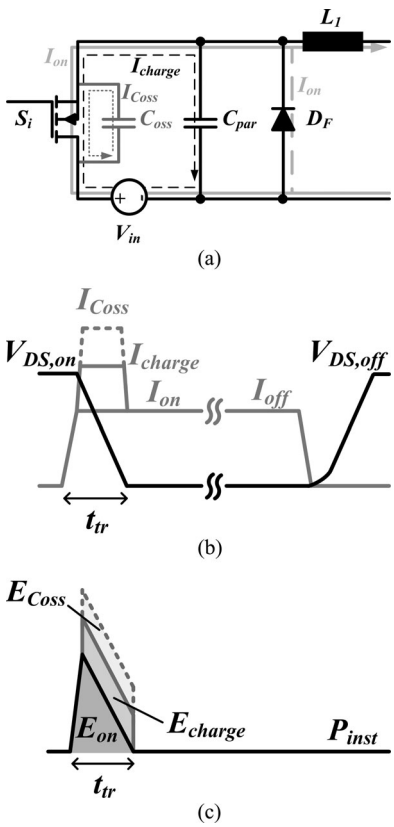

Fig. 5. (a) Simplified equivalent circuit depicting a MOSFET turn-ON transition. The current $I_{\rm ON}$ commutates from the freewheeling diode branch (dashed line) to the MOSFET branch (solid line) as the switch is turned on. Other branches, which are not switching, contain parasitic capacitances $C_{\rm par}$, which are charged during the transition as the voltage across them changes. $V_{\rm in}$ represents an input phase-to-phase voltage. (b) MOSFET switching behavior. For the turn-ON, also the current $I_{C\,\rm oss}$ occurring due to the discharge of the parasitic capacitance (here with an assumed constant capacitance at higher voltages) is shown, which is not measurable as it occurs internally within the MOSFET. There is also a current $I_{\rm charge}$ through the MOSFET due to the charging of the parasitic capacitors of other semiconductors (Fig. 6). For turn-OFF, as $C_{\rm oss}$ is very high at low voltage, I_L charges this parasitic output capacitor, therefore, different from the turn-ON transition, the overlapping of voltage and current is negligible. (c) Instantaneous power $P_{\rm inst}$ dissipated in the MOSFET during the transitions, with energy loss components shaded. $E_{\rm ON}$ results from the overlapping of $I_{\rm ON}$ and $V_{DS,\rm ON}$ and when multiplied by transition time $t_{\rm tr}$ gives the power $P_{\rm ON}$ dissipated due to this effect as given by (10). $E_{\rm charge}$ is only a portion of the energy losses due to the charging of other parasitic capacitors since losses due to this occur also in MOSFETs, which are already conducting (i.e., not switching during this transition). For this reason, $E_{\rm charge}$ and $E_{C\rm oss}$ are calculated together using a comprehensive circuit analysis, as in (16).

as $C_{\rm oss}$) is voltage dependent and nonlinear, with a relatively high value at low drain–source voltage V_{DS} and then decreasing sharply as V_{DS} increases (Fig. 17). As S_{T-} is turned off, its capacitance $C_{O,S_{T-}}$ must be charged as the blocking voltage builds up until diode D_{S-} is forward biased and takes over I_L. Therefore, simultaneous to the charging of $C_{O,S_{T-}}$, $C_{O,D_{S-}}$ is discharged. As $C_{O,S_{T-}}$ is uncharged and large when S_{T-} becomes high ohmic, I_L flows via $C_{O,S_{T-}}$ until it is charged and S_{T-} displays the behavior of the OFF-transition depicted in Fig. 5. Similarly, I_L flows via $C_{O,D_{S-}}$ until it is discharged. Note that also in this transition, the voltage across blocking diodes D_{R-} and D_{F-} decreases, meaning $C_{O,D_{R-}}$ and C_{O,D_F} must be partially discharged. To accomplish this, a portion of I_L flows through these capacitors as well. Therefore, for a brief duration, I_L splits between five branches: $R+$, $R-$, $S-$, $T-$, and the freewheeling diode branch. This continues until the capacitors are charged/discharged fully and finally all of I_L is flowing through the $S-$ and $R+$ branches. The switching interval is very short compared to the pulse period, and therefore, due to the splitting of I_L to four branches, the losses, which occur during this interval in the ON-resistances of the turned-ON switches $R_{\rm ON,S_{R-}}$, $R_{\rm ON,S_{R+}}$, $R_{\rm ON,S_{S-}}$ [and also the printed circuit board (PCB) trace resistances, etc.] are lower than already accounted by the conduction loss calculations, in which the current flow is always taken to be via two branches only and is assumed to commutate only from one branch to another (e.g., in this case immediately from $T-$ to $S-$). For this reason, the losses occurring during this transition are not counted in addition to the already calculated conduction losses.

Consider now the reverse transition, from state (110) to (101), the equivalent circuit of which is also shown in Fig. 6. In this transition, S_{T-} is turned on, then S_{S-} is turned off, and D_{S-} becomes reverse biased. Accordingly, S_{S-} is turned off at zero voltage and produces no switching losses. However, switching losses $P_{\rm ON}$ occur at the turn-ON of S_{T-} due to the gate–drain and gate–source capacitance causing a finite transition time $t_{\rm tr}$ at turn-ON, producing the behavior shown in the ON-transition in Fig. 5. Whereas the conduction loss is calculated using average currents assuming an ideal transition, here the MOSFET conducts a portion of the load current while still carrying a portion of the blocking voltage. Therefore, this must be accounted for and added into the total losses. Taking $V_{DS,\rm ON}$ as the drain–source voltage prior to turn-ON and $I_{\rm ON}$ as the drain–source current after turn-ON [Fig. 5(b)], this power loss can then be approximated by the following:

$$P_{\rm ON} = \frac{V_{DS,\rm ON} I_{\rm ON}}{2} t_{\rm tr} f_{\rm sw}. \tag{10}$$

Not captured by this equation are the losses occurring due to discharging the parasitic output capacitance switched to zero from blocking voltage V_{S-T}. This switching also forces the blocking voltage V_{S-T} to occur across D_{S-} and causes a charging of $C_{O,D_{S-}}$. Diode reverse recovery losses are avoided by using SiC diodes. Also note that while D_F and D_{R-} do not switch in this transition, the voltage across them changes from V_{R-S} to V_{R-T}, partially charging their parasitic capacitors. Voltages across the remaining switches and diodes do not change for this transition.

This hard-switched transition occurs too quickly to allow energy exchange with the converter output, and therefore, $C_{O,D_{S-}}$ is charged from source V_{S-T} causing an additional current to flow via $R_{\rm ON,S_{T-}}$, causing a loss. Similarly, $C_{O,D_{R-}}$ and C_{O,D_F} are charged from sources V_{R-S} and V_{S-T}, which are connected in series giving one source V_{R-T}. The charging of C_{O,D_F} causes an additional current to flow from V_{R-T} to it via $R_{\rm ON,S_{R+}}$ and $R_{\rm ON,S_{T-}}$, producing losses. For the charging of $C_{O,D_{R-}}$, an additional current flows from V_{R-T} to it via $R_{\rm ON,S_{R-}}$ and $R_{\rm ON,S_{T-}}$.

Solving the circuit for power losses by considering these currents would require solving differential equations and knowing

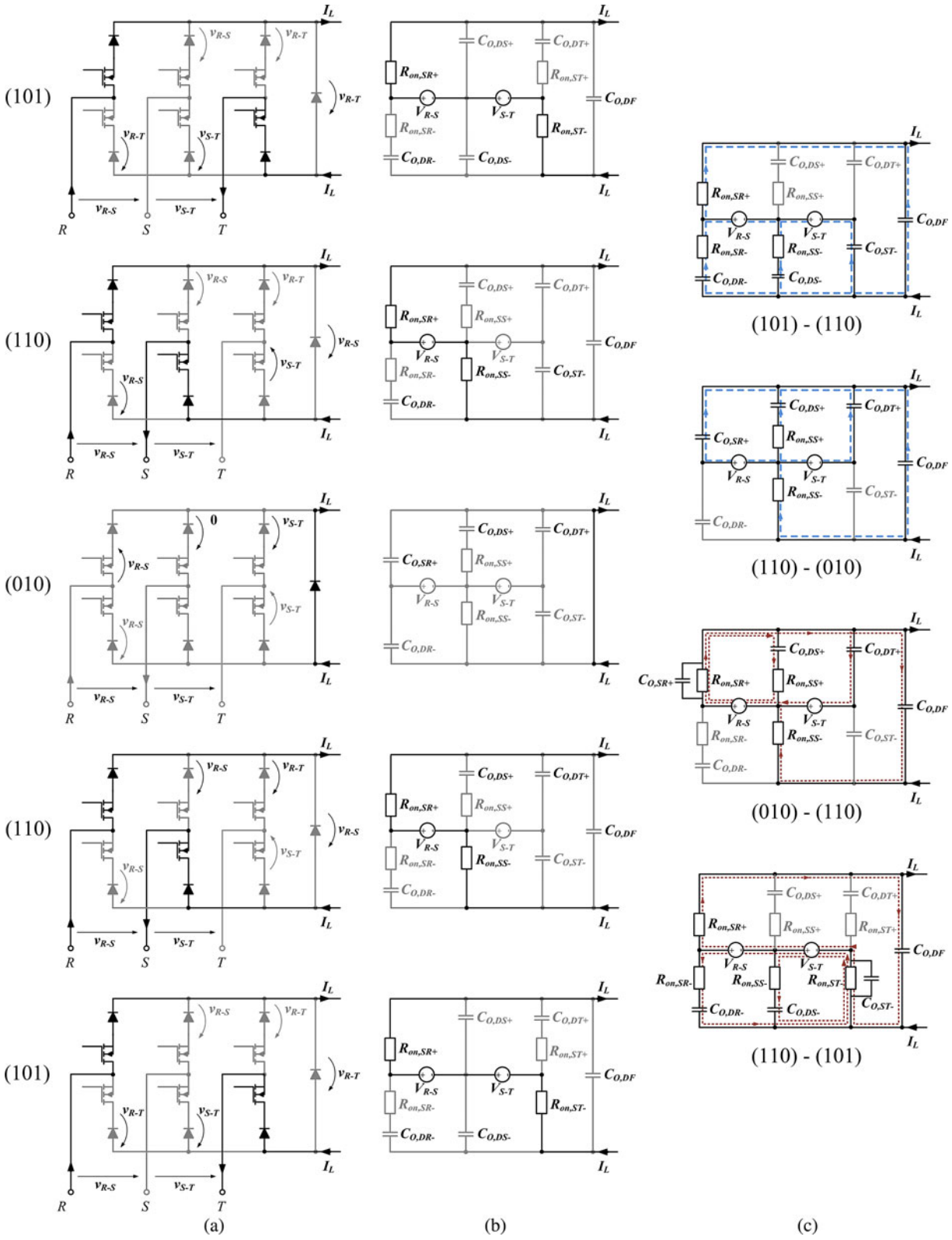

Fig. 6. Current paths (a) and equivalent circuits (b) for the switching states within a pulse period in sector 1 (Fig. 4). Current path in each state is shown in black. Voltages that change as that state is entered are also shown in black. (c) Equivalent circuits of the transitions between the states. For the transitions from state (101) to (110) and from (110) to (010), the blue dashed line shows the path of the inductor current I_L as it splits among the branches of the circuit to charge and discharge the parasitic capacitors during the transitions. For the transitions from state (010) to (110) and from (110) to (101), the red dotted lines show the paths of the currents drawn from the sources to charge the capacitors during the transitions. Losses occur along the current paths, mostly in the transistor initiating the transition.

quite precisely parasitics such as the PCB resistance. However, as in a first step the average power loss over a switching period, which is of constant duration for a particular switching frequency, is of interest, it suffices to find the total energy loss in a transition. The total energy loss due to capacitor charging and discharging in an *RC* circuit does not depend on the value of the resistance (for details, see the Appendix). Therefore, the energy balance in the circuit is considered.

For many switching devices, the $C_{\rm oss}(v)$ characteristic becomes flat or nearly flat above a certain V_{DS}. If the blocking voltage is always or most of the time above this value, the output capacitor of a device can be approximated by a constant value equal to the flat portion of its $C_{\rm oss}(v)$ curve. Hence, a constant capacitance is taken for the following analysis. In (11) and (12), the energy present in the circuit before and after the transition from (110) to (101) is given. There, only those capacitors, which change their voltage during the transition, are considered. The energy exchanged with the sources is determined considering the changes of the charging levels of the parasitic capacitors, as shown in (13) and (14). The charge flow is considered positive if it flows away from the source positive terminal. The total energy loss $\Delta E_{(110)-(101)}$ occurring in this transition is then calculated by (15).

$$E_{(110)} = \frac{1}{2}C_{O,D_{R-}}{V_{R-S}}^2 + \frac{1}{2}C_{O,S_{T-}}{V_{S-T}}^2 + \frac{1}{2}C_{O,D_F}{V_{R-S}}^2 \tag{11}$$

$$E_{(101)} = \frac{1}{2}C_{O,D_{R-}}{V_{R-T}}^2 + \frac{1}{2}C_{O,D_{S-}}{V_{S-T}}^2 + \frac{1}{2}C_{O,D_F}{V_{R-T}}^2 \tag{12}$$

$$\Delta E_{V_{S-T}} = \Delta Q_{O,D_{S-}}V_{S-T} = C_{O,D_{S-}}{V_{S-T}}^2 \tag{13}$$

$$\begin{aligned}\Delta E_{V_{R-T}} &= \Delta Q_{O,D_{R-}}V_{R-T} + \Delta Q_{O,D_F}V_{R-T}\\ &= C_{O,D_{R-}}(V_{R-T}-V_{R-S})V_{R-T}\\ &\quad + C_{O,D_F}(V_{R-T}-V_{R-S})V_{R-T}\end{aligned} \tag{14}$$

$$\begin{aligned}\Delta E_{(110)-(101)} &= E_{(110)} + \Delta E_{V_{S-T}} + \Delta E_{V_{R-T}} - E_{(101)}\\ &= \frac{1}{2}C_{O,S_{T-}}{V_{S-T}}^2 + \frac{1}{2}C_{O,D_{S-}}{V_{S-T}}^2\\ &\quad + \frac{1}{2}C_{O,D_F}(V_{R-T}-V_{R-S})^2\\ &\quad + \frac{1}{2}C_{O,D_{R-}}(V_{R-T}-V_{R-S})^2.\end{aligned} \tag{15}$$

The remaining transitions can be similarly analyzed: no switching losses are counted at the transition from (110) to (010), analogously to the transition from (101) to (110), while losses occur in the transition from (010) to (110) due to the discharging of $C_{O,S_{R+}}$ (turn-ON of S_{R+}), charging of C_{O,D_F} (due to building up the blocking voltage V_{R-S} across D_F), charging of $C_{O,D_{S+}}$ (blocking voltage changes from approximately 0 to V_{R-S}), and partial charging of $C_{O,D_{T+}}$ (blocking voltage changes from V_{S-T} to V_{R-T}). The total capacitive energy loss in one switching cycle in sector 1 is therefore given by

$$\begin{aligned}E_{\rm Sec1} &= \frac{1}{2}C_{O,S_{R+}}{V_{R-S}}^2 + \frac{1}{2}C_{O,S_{T-}}{V_{S-T}}^2\\ &\quad + \frac{1}{2}C_{O,D_F}{V_{R-S}}^2 + \frac{1}{2}C_{O,D_{S-}}{V_{S-T}}^2\\ &\quad + \frac{1}{2}C_{O,D_F}{V_{S-T}}^2 + \frac{1}{2}C_{O,D_{R-}}{V_{S-T}}^2\\ &\quad + \frac{1}{2}C_{O,D_{S+}}{V_{R-S}}^2 + \frac{1}{2}C_{O,D_{T+}}{V_{R-S}}^2.\end{aligned} \tag{16}$$

Over the entire sector, the voltages are not constant but a function of angle φ_N (Fig. 3). Inserting $v_{R-S}(\varphi_N)$ and $v_{S-T}(\varphi_N)$ for the appropriate voltage terms in (16) and averaging, i.e., integrating the total losses over sector 1, i.e., over 30°, gives the total power loss due to the parasitic device output capacitances since all 12 sectors are symmetric in terms of switching behavior and voltages. This total power loss $P_{Co,\rm tot}$ is then given by

$$P_{Co,\rm tot} \approx \frac{6}{\pi}\hat{V}_N^2\left(\frac{1}{2}n_S C_{O,S} + \frac{3}{2}n_D C_{O,D}\right)\left(\frac{14\pi - 9\sqrt{3}}{32}\right)f_{\rm sw}. \tag{17}$$

Note that this is an approximation since, as mentioned previously, the parasitic capacitances are approximated by constant capacitors for this analysis. For some semiconductor devices, the $C_{\rm oss}(v)$ characteristic is such that it cannot be well approximated by a constant value (Fig. 17). In this case, the energy and charge in the capacitors must be determined by integrating the nonlinear capacitance. This is shown in detail in the Appendix.

Taking into account as above the varying blocking voltages across MOSFETs S_{R+} and S_{T-} in sector 1, (10) must also be integrated to calculate the total MOSFET turn-ON power losses due to the overlapping of voltage and current. Knowing the voltages from the previous analysis and that in this case $I_{\rm ON} = I_L/n_S$, the total turn-ON losses due to overlapping of voltage and current $P_{\rm ON,tot}$ in the system can be calculated as follows:

$$P_{\rm ON,tot} = \frac{6}{\pi}\hat{V}_N\frac{\sqrt{3}}{4}I_L t_{\rm tr} f_{\rm sw} \tag{18}$$

where I_L is the dc inductor (output) current.

B. Optimization of the Number of Paralleled Semiconductors

With these loss components defined, it is possible to vary n_D and n_S to find an optimum number of devices to place in parallel for each switch and diode in Fig. 2. Superjunction power MOSFETs with 900-V blocking capability (IPW90R120C3 from Infineon) were chosen for the implementation, with an average $t_{\rm tr} = 20$ ns (estimated from previous measurements of the switch behavior) and a $C_{\rm oss}(v)$ characteristic requiring the use of integration approach shown in the Appendix to calculate losses. The diodes chosen were SiC 1200 V C2D10120A from Cree. A switching frequency of $f_{\rm sw} = 18$ kHz at the edge of audible range was chosen to keep switching losses low. Fig. 7 shows the resulting total losses for the MOSFETs and series diodes for different numbers of devices used in parallel for each switch and diode. The minimum losses occur with $n_S = 8$ and $n_D = 12$; however, as can be seen, the curves are nearly flat

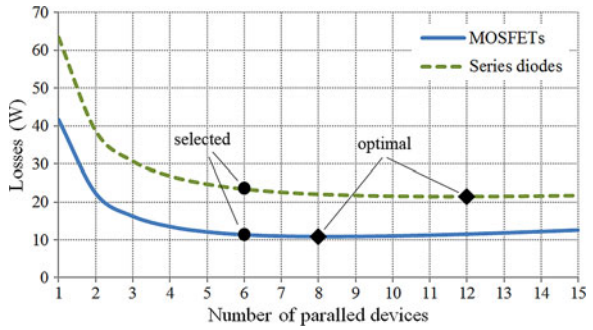

Fig. 7. Total losses of switches S_i and series diodes D_i depending on the number of devices in parallel to construct each. For example, $n_S = 7$, $n_D = 4$, total losses are 11 W + 26.8 W = 37.8 W. Marked on the curves are the optimal n_S and n_D according to the calculations, and the selected n_S and n_D for the prototype.

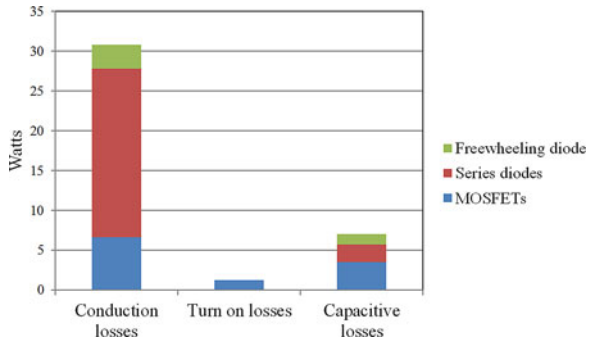

Fig. 8. Breakdown of total semiconductor losses by component and by loss type. Turn-ON losses shown in the figure are the losses resulting from the overlapping of voltage and current as calculated by (18). Capacitive losses are those occurring due to the charging and discharging of parasitic capacitances.

for $6 \leq n_S \leq 11$ and $7 \leq n_D \leq 15$. The losses saved by going from 6 MOSFETs in parallel to 8 are not even 1 W. Setting $n_D = 12$ would have resulted in an overly expensive prototype, and moreover, the difference between $n_D = 6$ and $n_D = 12$ is less than 2 W, which is less than the measuring error of the equipment that was available for measuring efficiency. Therefore, for the implementation, $n_S = n_D = 6$ was set in order to save costs. Fig. 8 gives a breakdown of the total semiconductor losses in the converter. Out of a total 39 W of losses, diode conduction losses are dominant with 21.2 W. Also note that the capacitive losses of the MOSFETs alone are larger than half the conduction losses and that for the MOSFETs the switching losses in total are almost equal to the conduction losses. This underlines the need to consider the switching, and in particular, the capacitive losses, carefully.

C. Losses of the Output Inductors

Inductor losses can be divided into three groups: losses due to dc winding resistance, core losses, and high-frequency (HF) losses due to skin and proximity effect. The configuration chosen for output inductors $L = L_1 = L_2$ consists of three pairs of ferrite E-cores wound with solid rectangular wire [Fig. 11(b)]. The inductor dc resistance $R_{L,\mathrm{dc}}$ is therefore

$$R_{L,\mathrm{dc}} = \frac{\rho N l_T}{A_w} \tag{19}$$

where N is the number of turns, l_T the average length of a turn, A_w the wire cross-sectional area, and ρ its resistivity. The core losses can be calculated using the modified Steinmetz equation [28]. The losses P_{core} for the triangular current (switching ripple) present in L_1 and L_2 are

$$P_{\mathrm{core}} = k f_{\mathrm{sw}} \left(\frac{2}{\pi^2} \cdot 4 f_{\mathrm{sw}} \right)^{\alpha - 1} \hat{B}^{\beta} V_{\mathrm{core}} \tag{20}$$

where k, α, and β are Steinmetz parameters, given or extractable from core material datasheets, V_{core} the total core volume, and $\hat{B}$ the peak magnetic flux density, which can be calculated by

$$\hat{B} = \frac{L(0.5 \Delta I_L)}{N A_e} \tag{21}$$

where I_L is the average inductor current, ΔI_L the inductor current ripple, and A_e the inductor core cross-sectional area. For the HF losses, the rectangular wire used can be approximated closely as a conductor with a square cross section, and the ac winding resistance $R_{L,\mathrm{ac},n}$ due to skin and proximity effect resulting from the nth harmonic of the inductor current ripple can be calculated using the Ferreira method [29]

$$R_{L,\mathrm{ac},n} = R_{L,\mathrm{dc}} \frac{\xi(\eta)}{2} \frac{\sinh \xi(\eta) + \sin \xi(\eta)}{\cosh \xi(\eta) - \cos \xi(\eta)} + \sum_{m=1}^{m_{\mathrm{tot}}} \frac{R_{L,\mathrm{dc}}}{m_{\mathrm{tot}}} \frac{\xi(\eta)}{2} \eta^2 (2m-1) \frac{\sinh \xi(\eta) - \sin \xi(\eta)}{\cosh \xi(\eta) + \cos \xi(\eta)} \tag{22}$$

for an inductor with m_{tot} layers of windings with porosity factor η and skin depth related term $\xi(\eta)$

$$\eta = \frac{a N_m}{b} \tag{23}$$

$$\xi(\eta) = \sqrt{A_w \pi \mu_0 \sigma n f_{\mathrm{sw}} \eta} \tag{24}$$

where a is the side length of the square conductor, b the width of a layer, N_m the number of turns in a layer, and σ the conductivity of the wire. Taking into account inductor current harmonics [21], the total losses $P_{L,\mathrm{tot}}$ for a dc choke with triangular current then are

$$P_{L,\mathrm{tot}} = {I_L}^2 R_{L,DC} + \sum_{n=1}^{n_{\mathrm{tot}}} \frac{{\Delta I_{L,n}}^2}{3} R_{L,\mathrm{ac},n} + P_{\mathrm{core}} \tag{25}$$

where $\Delta I_{L,n}$ is the amplitude of the nth harmonic. Knowing that at full load $I_L = 12.5$ A and selecting an inductor current peak-to-peak ripple of 25%, the inductance value $L_1 = L_2 = 650\ \mu$H is obtained (for details see [5]). Using Ferroxcube E64 3C91 cores with $N = 18$ ($N_m = 2$, $m_{\mathrm{tot}} = 9$), copper wire with $A_w = 4.1$ mm $\times$ 2.1 mm $= 8.6$ mm^2 and assuming an inductor temperature of 50 °C, the total dc losses for the chokes L_1 and L_2 given by (19) are 5.7 W, and the total HF losses given by (25) are approximately 0.9 W. Core losses calculated by (20) do not take into account dc magnetic bias, which has been shown

in [30] to have a nonnegligible influence. Therefore, for higher accuracy, the core losses were measured and confirmed to be approximately 0.5 W.

D. Losses of Output Capacitor

Losses in the capacitors are caused by their equivalent series resistance (ESR) and by leakage current. The ESR value is given in capacitor datasheets or can be calculated using the loss factor $\tan(\delta)$ also given in datasheets as [21]

$$\mathrm{ESR} = \frac{\tan(\delta)}{2\pi f_{\mathrm{sw}} C} \tag{26}$$

where C is the capacitance of the capacitor in question. The leakage current I_{leak} is determined using characteristic equations given in the capacitor datasheet. The total power losses P_C of a capacitor can then be calculated by

$$P_C = I_{C,\mathrm{rms}}^2 \mathrm{ESR} + I_{\mathrm{leak}} V_C \tag{27}$$

where $I_{C,\mathrm{rms}}$ is the rms current through the capacitor and V_C the average capacitor voltage. The output capacitor is selected to be $C_1 = 376\ \mu$F to keep output voltage ripple below 100 mV (for details see [5]) and implemented with 8 parallel 47 μF KXJ electrolytic capacitors from Nippon-Chemicon. As $V_C = V_O =$ 400 V, losses due to leakage current are about 1.3 W ($I_{\mathrm{leak}} =$ 3.3 mA). With the paralleling of these low-ESR capacitors and with $I_{C,\mathrm{rms}} = 0.9$ A, resistive losses of the output capacitors were found to be negligible.

E. Other Losses

In order to make the rectifier prototype compliant to existing EMI norms, the EMI input filter depicted in Fig. 9 is used. From circuit simulations of the rectifier system, the expected differential mode (DM) and CM noise are calculated, as well as the necessary attenuation based on the limits for Comité International Spécial des Perturbations Radioélectriques (CISPR) Class B. Following the approach of [27], the EMI filter is designed with $C_{\mathrm{return}} = 200$ nF, $C_{F,i} = 13.2\ \mu$F, $C_{CM,i} = C_{DM1,i} = 4.7$ nF, $C_{DM2,i} = 2\ \mu$F, $L_{F,i} = 50\ \mu$H, $L_{CM1} = 900\ \mu$H, and $L_{CM2} =$ 800 μH. EPCOS film capacitors having a negligible leakage current are used producing 0.7 W of losses due to ESR. Each $L_{F,i}$ is implemented with a pair of EPCOS ETD49 cores with 10 turns of solid copper wire, a Vacuumschmelze VAC6123X240 CM choke is used for L_{CM1}, and L_{CM2} is implemented with three 8-turn windings around a Vacuumschmelze 500F W423 core. This gives in total 2 W of losses due to the dc resistance, with HF and core losses in the milliwatt range.

An auxiliary power supply, a flyback converter, is used to power the TI TMS320F2808 DSP system used for the control and the gate drives. This supply was also analyzed and found to operate at an efficiency of 77.6% consuming a total of 3.1 W.

Finally, the FR-4 PCB material sandwiched between copper layers, i.e., the relatively wide tracks for the positive and negative rail of the converter, is considered, which creates essentially a plate capacitor in parallel to D_F, charged and discharged in the same manner as the capacitance of D_F. The PCB, being multilayered, basically creates several plate capacitors in series.

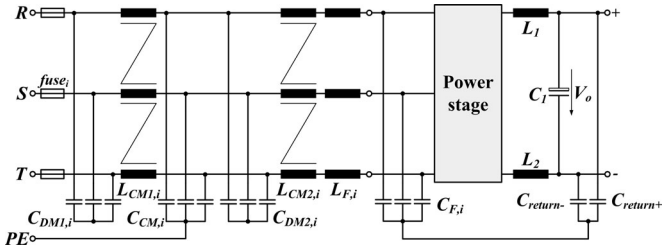

Fig. 9. EMI filtering concept and topology of the input filter.

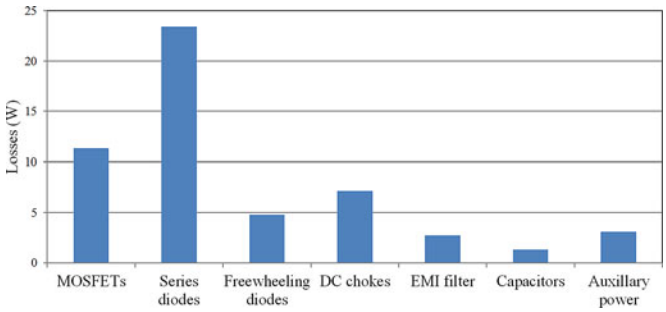

Fig. 10. Summary of loss components.

The FR-4 thickness is approximately 0.5 m, and considering a maximum trace area of 375 mm^2 and taking a relative permittivity of 4.7, this adds another 0.5 W of losses. As will be seen in Section IV, no heat sink or fan is needed to cool the system, and therefore any losses due to a cooling fan are avoided.

F. Total Losses

Total losses calculated for the converter were 53.7 W, giving an efficiency of 98.94%. A breakdown of the total losses is depicted in Fig. 10. As can be seen, semiconductor losses dominate and account for over 70% of the total. Clearly, for the 3ph-BR topology examined in this paper, semiconductor technology is the most significant barrier to achieving 99% efficiency. Therefore, not the optimization of inductors [21] and/or power passives, but the improvement of the properties of the semiconductors, either through decreased $R_{DS,\mathrm{ON}}$ or C_{oss}, i.e., an improved Figure of Merit—would be the only practical way to further significantly decrease losses.

IV. Experimental Results

A prototype of the proposed 3ph-BR was constructed with the EMI filter implemented on a separate board. The prototype is shown in Fig. 11. In total, 36 CoolMOS and 42 SiC diodes were mounted concentric on the top of the converter, minimizing commutation inductances. The dc choke and output capacitors were mounted on the bottom of the converter. Infrared camera measurements after 30 min of operation at full load showed a maximum temperature of 71.7 °C, which confirms that the operation without heat sink was unproblematic and temperature was uniformly distributed across the semiconductors. The inductors reached 51.5 °C. Fig. 12 shows the achieved sinusoidal input currents. EMI measurements were also performed (Fig. 13) confirming that the converter fulfills CISPR 22 Class B.

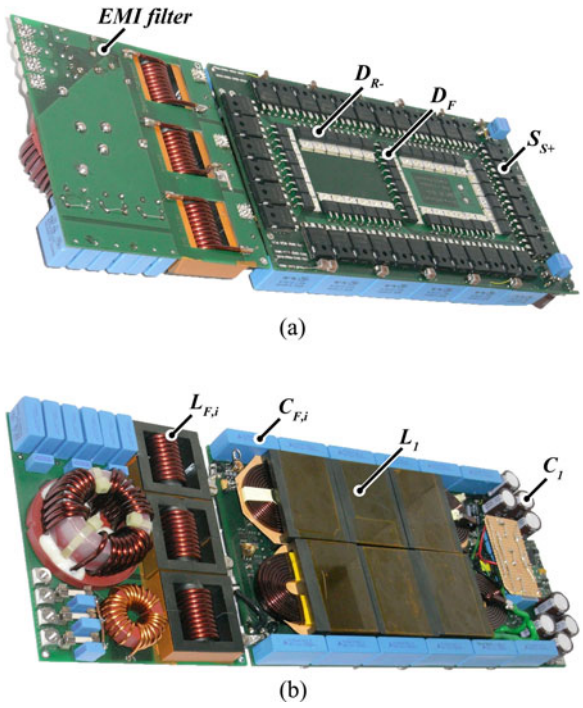

Fig. 11. Constructed prototype of the converter (right) and EMI filter on separate board (left). (a) Top view and (b) bottom view. The power stage measures $283 \times 155 \times 31$ mm^3 and the EMI filter board $135 \times 155 \times 42$ mm^3 resulting in a total power density of 2.2 kW/dm^3.

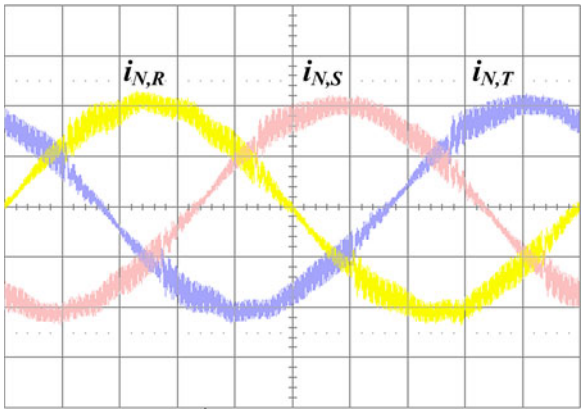

Fig. 12. Measurement of the input currents $i_{N,R}$, $i_{N,S}$, and $i_{N,T}$ of the rectifier for rated load ($P_O = 5$ kW) and for input voltage $V_{N,\mathrm{rms}} = 230$ V. Scale: 5 A/div. Timescale: 2 ms/div.

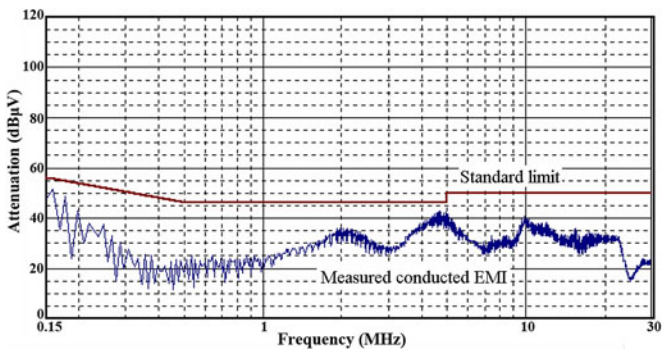

Fig. 13. EMI measurements of the converter using an average detector showing the CISPR Class B standard limit (red) and conducted EMI (blue).

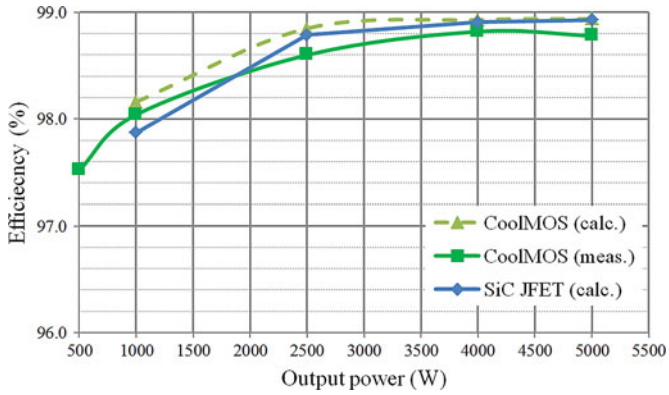

Fig. 14. Calculated efficiencies at different load levels for the 3ph-BR at 230-V AC input compared to calorimetric measurements of efficiency at different load points and the calculated efficiency for a 3ph-BR where the CoolMOS switches are replaced by SiC JFETs. Calculated efficiencies for the 10% load point are not shown as at this load the converter operates in discontinuous conduction mode, which is not modeled in this paper.

A. *Efficiency Measurements*

Results of calorimetric measurements of the converter prototype efficiency at different load points with a precision calorimeter with an accuracy of ± 2 W [31] are given in Fig. 14. As can be seen, with 230-V nominal input voltage and at full load, an efficiency of 98.8% was measured, giving good agreement with the calculations in Section III. The difference between the calculation according to the models in Section III and the calorimetric efficiency measurement (which gives 61.6 W of losses at full load) is about 8 W or 15%. Considering the full output power of 5000 W, this is an error of 0.16% of efficiency. Possible sources of error are the polynomial fits used for the parasitic capacitance characteristics, losses in the PCB tracks (not considered in this paper), and tolerances of the components, i.e., variation of the actual component characteristics from given datasheet values.

It should be noted that down to 10% rated load and across the rated input voltage range, a high efficiency of over 97% is always maintained. The lower efficiency at low loads can be partly explained by the significant voltage-dependent loss components, which are constant over the load range, i.e., the losses due to the parasitic capacitors.

V. Alternative Implementations

In order to achieve a higher blocking voltage of the switches, one possibility is to replace the MOSFETs in the converter with 1200-V IGBTs. A preliminary investigation was carried out where the losses of the CoolMOS calculated in Section III were replaced by the losses that 1200 V Infineon IGW40T120 IGBTs, available in the same package as the MOSFETs, would have under the same operating conditions. Conduction and switching losses of the IGBTs were estimated based on the output characteristic and switching energy curves given in the device datasheet. The optimum design yielded only one device for each switch, with total switch losses of approximately 80 W, giving a

total of approximately 122 W of losses for the entire converter, i.e., an efficiency of only 97.6% at full load. The optimized IGBT-based converter suffers from higher switching losses than the MOSFET-based converter due to much higher switching energies of the IGBTs compared to the Superjunction MOSFETs and also from higher conduction losses, as the ON-state voltage drop of the IGBTs does not scale down linearly as extra devices are added in parallel, as is the case with the MOSFETs. Therefore, an IGBT-based system appears not to be a viable solution for a converter targeting 99% efficiency.

Another possibility, which achieves a higher blocking voltage of the switches while maintaining high efficiency at full load, is to replace the MOSFETs with 1200-V SiC JFETs from SiCED ($R_{DS,\mathrm{ON}} = 80$ mΩ at a junction temperature of 25 °C). Again, the losses of the MOSFETs calculated in Section III were replaced by the losses that SiC JFETs would have under the same operating conditions. Four JFETs, the optimal configuration for efficiency, were used in parallel for each switch, with the rest of the circuit unchanged, i.e., $n_D = 6$, and the losses were calculated based on a characterization from earlier experimental conduction and switching loss measurements. The results are shown in Fig. 14. According to calculations an efficiency of 98.9% would be achieved at full load and $f_{\mathrm{sw}} = 18$ kHz making an all SiC 3ph-BR a viable design.

VI. Conclusion

A three-phase buck-type PFC rectifier was presented with measured 98.8% efficiency suitable for supplying 400-V dc distribution systems. Models for calculating losses of all components were discussed and verified by experimental measurement of the converter's efficiency. The dominance of semiconductor losses indicates that the achieved efficiency is a limit for the presented topology obtainable with currently commercially available power semiconductors, and that further improvements in semiconductor components are the key to reaching the 99% efficiency target. If a higher blocking voltage than is available with MOSFETs is to be targeted, IGBTs are not a suitable replacement as they suffer from significantly higher switching and conduction losses. On the other hand, replacing MOSFETs with higher blocking voltage SiC JFETs results in the same calculated efficiency of 98.9%.

Appendix

Calculating Energy Losses in *RC* Circuits

Here, the calculation of losses due to the charging and discharging of parasitic capacitors (Section III) are shown in more detail. Consider first the case of a constant capacitor, e.g., $C_{O,D_{S-}}$, charged from zero to a voltage V_{S-T} from a voltage source, as occurring during the transition from state (110) to (101) in sector 1, (Fig. 15). Considering the charge delivered to the capacitor, the loss $\Delta E_{(110)-(101),D_{S-}}$ is calculated, with (28) giving the energy in the capacitor before the transition, (29) the energy after, (30) the energy exchanged with the source, and (31) the energy loss due to charging

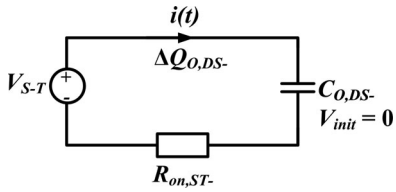

Fig. 15. Equivalent circuit for the charging of the parasitic capacitor of D_{S-} to voltage level V_{S-T} from zero.

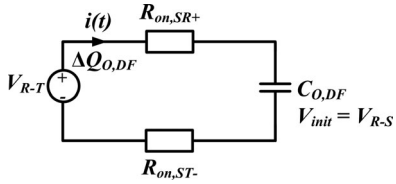

Fig. 16. Equivalent circuit for the charging of the parasitic capacitor of D_F to voltage level V_{R-T} from an initial voltage V_{R-S}.

$$E_{(110),D_{S-}} = 0 \tag{28}$$

$$E_{(101),D_{S-}} = \frac{1}{2} C_{O,D_{S-}} {V_{S-T}}^2 \tag{29}$$

$$\Delta E_{V_{S-T}} = \Delta Q_{O,D_{S-}} V_{S-T} = C_{O,D_{S-}} {V_{S-T}}^2 \tag{30}$$

$$\begin{aligned} \Delta E_{(110)-(101),D_{S-}} &= E_{(110),D_{S-}} + \Delta E_{V_{S-T}} - E_{(101),D_{S-}} \\ &= C_{O,D_{S-}} {V_{S-T}}^2 - \frac{1}{2} C_{O,D_{S-}} {V_{S-T}}^2 \\ &= \frac{1}{2} C_{O,D_{S-}} {V_{S-T}}^2 \end{aligned} \tag{31}$$

The energy loss in this circuit occurs in the resistor $R_{\mathrm{ON},S_{T-}}$. Note that (31) holds true whether $R_{\mathrm{ON},S_{T-}}$ is constant or whether it is varying with time (e.g., as the ON-resistance of a MOSFET varies during its transition from its OFF-state to its ON-state). Therefore, the above analysis is valid for any $R_{\mathrm{ON},S_{T-}}(t)$. The characteristics of $R_{\mathrm{ON},S_{T-}}$, e.g., its actual change from a high-ohmic OFF-state value to the ON-state does not influence the energy losses occurring due to charging of the capacitor.

The same analysis can be applied to a case where the capacitor is charged or discharged from one voltage level to another. Consider for example the change of voltage of C_{O,D_F} from V_{R-S} to V_{R-T} during the transition from state (110) to (101) in sector 1 (Fig. 16). The energy in C_{O,D_F} before the transition is given in (32), the energy after in (33), the energy exchanged with the source in (34), and the energy loss in (35)

$$E_{(110),D_F} = \frac{1}{2} C_{O,D_F} {V_{R-S}}^2 \tag{32}$$

$$E_{(101),D_F} = \frac{1}{2} C_{O,D_F} {V_{R-T}}^2 \tag{33}$$

$$\begin{aligned} \Delta E_{V_{S-T}} &= \Delta Q_{O,D_F} V_{R-T} \\ &= C_{O,D_F} \left(V_{R-T} - V_{R-S}\right) V_{S-T} \end{aligned} \tag{34}$$

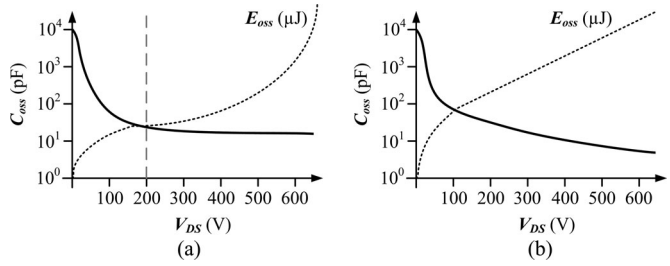

Fig. 17. Possible shapes of $C_{\rm oss}$ curves of semiconductor devices. (a) A case where the capacitance becomes constant or nearly constant after a certain voltage. In this case, for example, if the blocking voltage in the circuit is mainly above 200 V (marked by the dashed line), the $C_{\rm oss}$ value may be approximated by the flat portion of the curve and the equations [e.g., (17)] derived from the constant capacitor model may be used to calculate losses. (b) A case where $C_{\rm oss}$ cannot be approximated by a constant and the equations where the $C_{\rm oss}$ curve is integrated [e.g., (43)] must be used to calculate losses. For both cases, the resulting energy ($E_{\rm oss}$) curve is shown by the dotted lines.

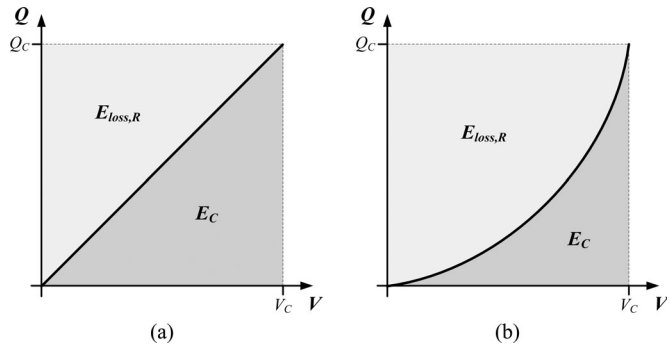

Fig. 18. Capacitor charge Q resulting from a capacitor voltage V for (a) a constant capacitor and (b) a nonlinear capacitor with varying voltage-dependent capacitance. Shown also is the resulting loss $E_{{\rm loss},R}$ (area shaded in light gray) in the circuit resistance as the capacitor is charged from zero to a voltage V_C and charge Q_C by a voltage source, as well as the resulting energy E_C (area shaded in dark gray) stored in the capacitor at voltage V_C. With the linear constant capacitor, when charging from zero, the energy loss due to charging is equal to the energy stored in the capacitor after the charging is completed, as shown, e.g., by (31). For the nonlinear capacitor, this is not the case and the energy loss must be determined via integration.

$$\begin{aligned}\Delta E_{(110)-(101),D_F} &= E_{110,D_F} + \Delta E_{V_{R-T}} - E_{101,D_F} \\ &= \frac{1}{2}C_{O,D_F}{V_{R-S}}^2 \\ &\quad + C_{O,D_F}\left(V_{R-T} - V_{R-S}\right)V_{R-T} \\ &\quad - \frac{1}{2}C_{O,D_F}{V_{R-T}}^2 \\ &= \frac{1}{2}C_{O,D_F}\left(V_{R-T} - V_{R-S}\right)^2. \end{aligned} \tag{35}$$

Again, the result is valid regardless of the varying resistance in the circuit.

For some semiconductors, the voltage-dependent parasitic output capacitor cannot be effectively approximated with a constant value (Fig. 17). For nonlinear capacitors, the energy loss due to charging cannot be calculated as shown previously, as it depends on the nonlinear capacitance characteristic, which varies with voltage (Fig. 18). In these cases, the charge and the energy must be determined by integrating the $C_{\rm oss}(v)$ curve given in device datasheets. $C_{\rm oss}(v)$ is a differential capacitance defined as follows:

$$C_{\rm oss}(v) = \frac{dq_{\rm oss}}{dv}. \tag{36}$$

In this case, the energy $E_{Co}(V)$ stored in the output capacitor of a device at a voltage V must be calculated by [32]

$$E_{Co}(V) = \int_0^Q v dq_{\rm oss} = \int_0^V v C_{\rm oss}(v) dv. \tag{37}$$

In some cases, an $E_{\rm oss}(v)$ curve is already given in the datasheet. The charge $Q_{Co}(V)$ stored in the output capacitor of a device at a voltage V is then determined by

$$Q_{Co}(V) = \int_0^Q dq_{\rm oss} = \int_0^V C_{\rm oss}(v) dv. \tag{38}$$

For the previously considered case, where the capacitor is charged from zero, this then allows (31) to be rewritten as follows:

$$\begin{aligned}\Delta E_{(110)-(101),D_{S-}} &= E_{110,D_{S-}} + \Delta E_{V_{S-T}} - E_{110,D_{S-}} \\ &= Q_{O,D_{S-}}(V_{S-T})V_{S-T} - E_{O,D_{S-}}(V_{S-T})\end{aligned} \tag{39}$$

where the charge and energy terms are calculated using (38) and (37), respectively. To then get the average power loss in a switching period due to this energy loss, the following integration is performed taking into account the dependence of V_{S-T} on angle φ_N

$$\begin{aligned}P_{Co,D_{S-}} = f_{\rm sw}\frac{6}{\pi}n_D\Bigg(&\int_0^{\pi/6} v_{S-T}(\varphi_N)Q_{Co,D}(v_{S-T}(\varphi_N))d\varphi_N \\ &- \int_0^{\pi/6} E_{Co,D}(v_{S-T}(\varphi_N))d\varphi_N\Bigg).\end{aligned} \tag{40}$$

Similarly, for the considered case, where a capacitor is charged from one voltage level to another, (35) can be rewritten as follows:

$$\begin{aligned}\Delta E_{(110)-(101),D_F} &= E_{110,D_F} + \Delta E_{V_{R-T}} - E_{110,D_F} \\ &= E_{O,D_F}(V_{R-S}) \\ &\quad + (Q_{O,D_F}(V_{R-T}) - Q_{O,D_F}(V_{R-S}))V_{R-T} \\ &\quad - E_{O,D_F}(V_{R-T})\end{aligned} \tag{41}$$

and then integrated as above to obtain the power loss.

$$\begin{aligned}P_{Co,D_F} = f_{\rm sw}\frac{6}{\pi}n_D\Bigg(&\int_0^{\pi/6} E_{Co,D}(v_{R-S}(\varphi_N))d\varphi_N \\ &+ \int_0^{\pi/6} v_{R-T}(\varphi_N)Q_{Co,D}(v_{R-T}(\varphi_N))d\varphi_N \\ &- \int_0^{\pi/6} v_{R-T}(\varphi_N)Q_{Co,D}(v_{R-S}(\varphi_N))d\varphi_N \\ &- \int_0^{\pi/6} E_{Co,D}(v_{R-T}(\varphi_N))d\varphi_N\Bigg).\end{aligned} \tag{42}$$

The MOSFET output capacitances are discharged always to zero from the blocking voltage by being effectively short circuited by the ON-resistance. Therefore, it is sufficient to calculate the energy present in the capacitors before MOSFET turn-ON, giving total power losses due to the discharging of the MOSFET $C_{\rm oss}$ (for all switches)

$$P_{Co,S,\rm tot} = f_{\rm sw}\frac{6}{\pi}n_S\left(\int_0^{\pi/6} E_{Co,S}(v_{R-S}(\varphi_N))d\varphi_N + \int_0^{\pi/6} E_{Co,S}(v_{S-T}(\varphi_N))d\varphi_N\right). \quad (43)$$

ACKNOWLEDGMENT

The authors would like to thank D. Christen for performing the calorimetric converter loss measurements and Dr. G. Deboy of Infineon Technologies for providing CoolMOS power transistor samples for research on ultrahigh efficiency converter systems.

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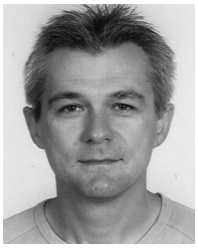

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